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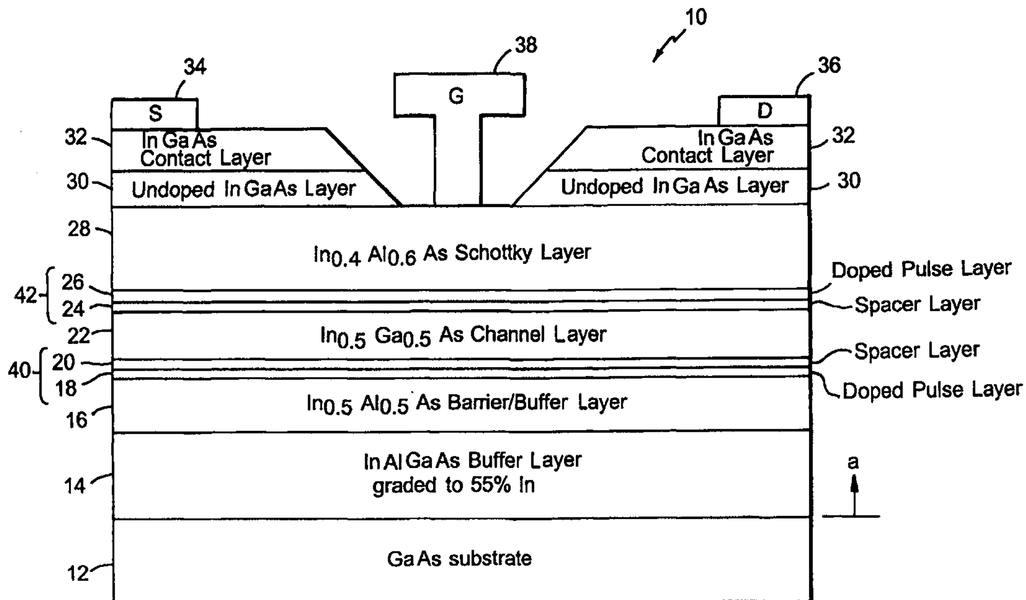

(57) Abstract

A high electron mobility transistor structure (10) is provided having an insulating substrate (12) having a substrate lattice constant. A buffer layer (14) is disposed over the substrate and has a graded lattice constant substantially equal to a first lattice constant near a bottom of the buffer layer and substantially equal to a second lattice constant near a top of the buffer layer larger than the substrate lattice constant and the first lattice constants. A channel layer (22) is disposed above the buffer layer and has a concentration of indium to provide a lattice constant of the channel layer that is larger than the substrate lattice constant.

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HIGH ELECTRON MOBILITY TRANSISTOR

Background of the Invention

5 This invention relates generally to field-effect transistors and more particularly to high electron mobility transistors (HEMTs).

As is known in the art, there are several types of active devices that can amplify radio frequency (RF) 10 signals. One such device is a HEMT. With HEMTs, a heterojunction is formed between a donor-spacer layer, including a doped pulse layer and an undoped spacer layer, and an undoped channel that has a smaller bandgap than the donor-spacer layer. The heterojunction provides 15 spatial separation of electrons injected from the pulse layer into the channel layer from the donor atoms in the pulse layer. Electrons move parallel to the heterojunction confined within the channel layer. Limiting conduction to the channel layer provides low 20 impurity scattering and good electron mobility.

Two types of HEMTs are gallium arsenide (GaAs) based HEMTs and Indium phosphide (InP) based HEMTs. GaAs HEMTs use GaAs wafers (i.e., substrates) and InP based HEMTs use InP wafers. The GaAs substrates are 25 inexpensive and durable compared to the InP substrates. For example, a 4 in. diameter GaAs wafer costs about $200 while a 2 in. InP wafer costs about $250, a 3 in. InP wafer costs about $800-1,000, and 4 in. InP wafers are currently unavailable, preventing 4 in. manufacturing 30 lines from using InP substrates. Channel layers in GaAs HEMTs typically are made of $In_xGa_{1-x}As$ with $0.15 \le x \le 0.25$. InP HEMTs, on the other hand, provide low noise figures and high gains, but the InP wafers are expensive and fragile compared to the GaAs wafers. InP HEMTs typically 35 use a channel layer of $In_xGa_{1-x}As$, where $0.5 \le x \le 0.6$. The increased indium in the channel of the InP HEMTs provides

improved conductivity in the channel layer. The indium concentration in the InGaAs channel is limited due to the lattice constant of the InP substrate. The channel is lattice matched to the InP substrate if the indium
5 concentration is about 53% (i.e., x=0.53). Indium concentrations above or below about 53% tend to cause dislocations in the material from strain if the channel layer is grown sufficiently thick, e.g., 400Å, to provide other desirable features such as a flat transconductance
10 response for improved linearity.

Summary of the Invention

In accordance with a feature of the invention, a high electron mobility transistor structure is provided having an insulating substrate having a substrate lattice
15 constant. A buffer layer is disposed over the substrate and has a graded lattice constant substantially equal to a first lattice constant near a bottom of the buffer layer and substantially equal to a second lattice constant near a top of the buffer layer larger than the
20 substrate lattice constant and the first lattice constant. A channel layer is disposed above the buffer layer and has a concentration of indium to provide a lattice constant of the channel layer that is larger than the substrate lattice constant.

25 With such a structure, a channel layer with a high indium concentration can be used to provide good noise figure, high mobility, and good gain using a substrate with a smaller lattice constant than the channel. Also, strain produced by different lattice constants is
30 relieved in the buffer layer, protecting against material dislocations in the channel layer affecting performance of the transistor.

In a preferred embodiment of the invention, a barrier/buffer layer is disposed over the buffer layer

and has a lattice constant smaller than the second lattice constant.

In another preferred embodiment of the invention, the lattice constant of a portion of the buffer layer varies with distance from the substrate.

In accordance with another feature of the invention, a method of forming a high electron mobility transistor structure is provided. The method includes providing an insulating substrate having a substrate lattice constant. A buffer layer is formed over the substrate, the buffer layer having a graded lattice constant substantially equal to a first lattice constant near a bottom of the buffer layer and substantially equal to a second lattice constant near a top of the buffer layer larger than the substrate lattice constant and the first lattice constant. A channel layer is formed above the buffer layer, the channel layer having a concentration of indium to provide a lattice constant of the channel layer larger than the substrate lattice constant.

In a preferred embodiment of the invention, forming the buffer layer includes growing a Group III-V buffer layer material at a first temperature in a first temperature range while increasing an indium concentration from a first indium concentration to an intermediate indium concentration, and growing the Group III-V buffer layer material at a temperature in a second temperature range while increasing the indium concentration from the intermediate indium concentration to a second indium concentration. A barrier/buffer layer is formed over the buffer layer by growing a Group III-V barrier/buffer layer material at a third temperature in a third temperature range. The second temperature range is lower than the first and the third temperature ranges.

With such an arrangement, the buffer layer can be grown with a planar top surface.

In accordance with another feature of the invention, a field-effect transistor structure is
5 provided having a gallium arsenide substrate. A buffer layer of a Group III-V material is disposed over the substrate and includes a Group III material having a graded indium concentration substantially equal to a first concentration near a bottom of the buffer layer and
10 substantially equal to a second concentration near a top of the buffer layer larger than the first concentration. A barrier/buffer layer of a Group III-V material is disposed over the buffer layer and includes a Group III material having a third indium concentration lower than
15 the second indium concentration. A channel layer of a Group III-V material is disposed above the buffer layer and includes a Group III material having an indium concentration substantially equal to the third concentration.

20 In accordance with another feature of the invention, a field-effect transistor structure is provided having a gallium arsenide substrate having a substrate lattice constant. A buffer layer is disposed over the substrate and has a graded lattice constant
25 substantially equal to a first lattice constant near a bottom of the buffer layer and substantially equal to a second lattice constant near a top of the buffer layer larger than the substrate lattice constant and the first lattice constant. A channel layer is disposed above the
30 buffer layer and has a concentration of indium to provide a lattice constant of the channel layer larger than the first substrate constant. A donor-spacer layer has a doped region and an undoped region and forms a heterojunction with the channel layer. A contact layer
35 is disposed above the channel layer.

With such an arrangement, a low-cost substrate can be used with a channel layer having enough indium to provide good noise figure, mobility, and gain, and a lattice constant for the channel layer that is larger than the lattice constant of the substrate.

In accordance with another feature of the invention, a high electron mobility transistor structure is provided having a gallium arsenide substrate. A buffer layer of $In_x(Al_yGa_{1-y})_{1-x}As$ is disposed over the substrate, with $0 \le x \le 1$. The buffer layer has a graded concentration of indium such that x is about 0.05 near the substrate and is equal to m at a position remote from the substrate. A barrier/buffer layer of $In_n(G3)_{1-n}As$ is disposed over the buffer layer, G3 being a Group III material and m being greater than n. A channel layer of $In_nGa_{1-n}As$ is disposed above the first buffer layer. A donor-spacer layer has a doped region and an undoped region and forms a heterojunction with the channel layer. A contact layer is disposed above the channel layer.

Embodiments of the invention may provide one or more of the following advantages. For example, an indium concentration in a channel layer is adjustable, allowing indium concentrations that produce a channel layer with a much different lattice constant than an associated substrate. A GaAs substrate can be used with a channel layer having a lattice constant that is larger than the substrate lattice constant without dislocations affecting device performance. High linearity, high gain, and low noise HEMT performance is possible at a much lower cost than InP based HEMTs.

Other advantages will become apparent from the following description and from the claims.

Brief Description of the Drawings

FIG. 1 is a cross-sectional diagrammatical view of a HEMT according to the invention;

FIG. 2 is a plot of indium concentration versus thickness and growth time of a buffer layer and of a barrier/buffer layer of the HEMT shown in FIG. 1;

FIG. 3 is a plot of temperature versus growth time of the buffer layer and the barrier/buffer layer shown in FIG. 1;

FIG. 4 is a flow diagram of a method of making the HEMT shown in FIG. 1; and

FIG. 5 is a cross-sectional diagrammatical view of another HEMT according to the invention.

Description of Preferred Embodiments

Referring to FIG. 1, a metamorphic high electron mobility transistor (MHEMT) 10 is shown. MHEMT 10 includes an insulating GaAs substrate 12, an undoped InAlGaAs buffer layer 14, an undoped $In_xAl_{1-x}As$ barrier/buffer layer 16 500-1,500Å, and preferably 1,000Å, thick, a doped pulse layer 18 with a silicon sheet concentration of about $1\times10^{12}cm^{-2}$, an undoped $In_xAl_{1-x}As$ spacer layer 20 about 50Å thick, an undoped InGaAs, here $In_{0.5}Ga_{0.5}As$, channel layer 22 about 100-400Å thick, an undoped $In_xAl_{1-x}As$ spacer layer 24 about 30Å thick, a doped pulse layer 26 with a silicon sheet concentration of about $2\times10^{12}cm^{-2}$ - $3\times10^{12}cm^{-2}$, an undoped $In_{x-0.1}Al_{1.1-x}As$ Schottky layer 28 about 200Å thick, an undoped InGaAs layer 30 about 100Å thick, an n+ doped InGaAs contact layer 32 about 100Å thick, a source electrode 34 and a drain electrode 36 in ohmic contact with contact layer 32, and a gate electrode 38 in Schottky contact with Schottky layer 28.

Pulse layer 18 and spacer layer 20 form a first donor-spacer layer 40 and spacer layer 24 and pulse layer

26 form a second donor-spacer layer 42. Donor-spacer layers 40 and 42 form heterojunctions with channel layer 22.

Although many values of x are possible, e.g., $0.2 \leq x \leq 1.0$, for MHEMT 10 x equals 0.5. Thus, barrier/buffer layer 16, spacer layer 20, and spacer layer 24 have equal indium concentrations. The indium concentration refers to the ratio (e.g., percentage) of indium atoms of the total atoms of Group III material (i.e., a material containing Group III elements, e.g., InAlGa), in a given material, here the Group III-V materials that make up barrier/buffer layer 16, spacer layer 20, and spacer layer 24. AlAs, GaAs, and AlGaAs have almost identical lattice constants. However, because indium to arsenic bonds are longer than gallium to arsenic and aluminum to arsenic bonds, alloying indium into AlAs, GaAs, or AlGaAs expands the lattice constant. Using different lattice constant materials in the same device introduces strain to the device. To reduce strain, channel layer 22 has an indium concentration substantially equal to that of layers 16, 20, and 24. For thick (e.g., 300-400Å) channel layers, the channel layer indium concentration is preferably substantially equal to (e.g., within ±2 percentage points of) the indium concentrations of layers 16, 20 and 24. For thin channel layers (e.g., 100Å), the channel layer indium concentration can differ up to about ±20 percentage points from that of layers 16, 20, and 24. The indium concentration of Schottky layer 28 is slightly less than for layers 16, 20, and 24 in order to increase the bandgap of Schottky layer 28 and help the breakdown voltage of MHEMT 10.

Buffer layer 14 is a Group III-V material having a graded, metamorphic indium concentration and a thickness depending on the indium concentration. As shown in FIG.

2, at the bottom of buffer layer 14 (a_0=0), the indium concentration is about 5%. The indium concentration linearly increases with the thickness of buffer layer 14 until a maximum concentration c_{max} is reached at thickness a_2 corresponding to the top of buffer layer 14 and corresponding to a maximum lattice constant. At a_2, the indium concentration is about 3-8 percentage points higher than a desired relaxed indium concentration c_{rel} (i.e., the indium concentration associated with a desired relaxed lattice constant). As shown, preferably the maximum indium concentration, here 55%, is about 5 percentage points more than the desired relaxed indium concentration, here 50%. The thickness of buffer layer 14 from a_0 to a_2 is about 0.5μm - 3.0μm. This thickness depends upon the desired relaxed indium concentration and the rate of increase of indium concentration in buffer layer 14.

The top of buffer layer 14 coincides with the bottom of barrier/buffer layer 16 at a_2. Between a_2 and the top a_3 of barrier/buffer layer 16, a thickness of about 1,000Å, the indium concentration is constant and equal to the desired relaxed indium concentration of 50%.

In MHEMT 10, the channel layer indium concentration substantially matches the desired relaxed indium concentration of about 50%. Thus, channel layer 22 can be made thick, e.g., 300-400Å, to improve linearity (i.e., to flatten the transconductance response). The 50% indium concentration in channel layer 22 provides MHEMT 10 with a low noise figure, high gain, good conductivity, and a conduction band discontinuity for the heterojunction between layers 40 and 42 and channel layer 22 of about 0.47 eV. This indium concentration also means that the lattice constant of channel layer 22 is larger than the lattice constant of substrate 12.

The graded indium concentration of buffer layer 14 provides a graded lattice constant from substantially equal to the lattice constant of substrate 12 to a larger lattice constant than that of barrier/buffer layer 16. The lattice constant of buffer layer 14 changes with distance (a) from the upper surface of substrate 12 in accordance with the indium concentration in buffer layer 14. With an indium concentration of less than about 15%, here 5%, the lattice constant at the bottom a_0 of buffer layer 14 is larger, but substantially equal to the lattice constant of substrate 12. The buffer layer lattice constant increases with buffer layer thickness (a) so that at the top a_2 of buffer layer 14 the lattice constant is larger than the lattice constant of barrier/buffer layer 16.

Increased lattice constants in buffer layer 14 cause strain that results in dislocations in buffer layer 14 that relieve or relax the strain. Most of the dislocations in buffer layer 14 occur near substrate 12. This helps ensure that the dislocations do not effect device performance by guarding against dislocations in channel layer 22. Exceeding (i.e., "overshooting") the desired relaxed indium concentration in buffer layer 14 produces dislocations that relieve or relax most, if not all, of the strain associated with the desired relaxed lattice constant, which is lower than the maximum lattice constant.

Barrier/buffer layer 16 has the desired relaxed lattice constant. Barrier/buffer layer 16 is therefore substantially free of strain, i.e., is relaxed. Thus, most, if not all, of the strain associated with using the high indium concentration, high lattice constant channel layer 22 with the low lattice constant substrate 12 is relieved.

Channel layer 22 has a lattice constant substantially equal to the desired relaxed lattice constant. With an indium concentration within ±2 percentage points, here 0 percentage points, of the barrier/buffer layer indium concentration, channel layer 22 has a lattice constant substantially equal to the desired relaxed lattice constant.

Referring to FIG. 4, a method 50 of making MHEMT 10 is shown. Method 50 uses molecular beam epitaxy (MBE) to deposit/grow materials on top of existing materials in a single wafer deposition chamber, e.g., a VG-80H made by VG Semicon, a division of Thermo Electron, Corp. Thus, a substrate 12 is provided and prepared (Step 54), graded, metamorphic buffer layer 14 is grown (Steps 56, 58, 60, 62), barrier/buffer layer 16 is grown (Steps 64 and 66), device layers, including channel layer 22, are grown (Step 68) and etched (Step 70), and ohmic contacts and Schottky contact are formed (Step 70).

More particularly, GaAs substrate 12 is prepared (Step 54) by desorbing oxide from substrate 12 and growing layers to smooth the surface of substrate 12. Oxide is desorbed from substrate 12 at about 640°C in an arsenic overpressure using conventional techniques. More GaAs is deposited at a temperature of about 560-600°C to a thickness of about 100-400Å, preferably about 100Å, to help provide a smooth top surface of GaAs. A 5-10 period superlattice is formed at about 560-600°C over the deposited GaAs. Each period includes about 20-40Å of GaAs and 20-40Å of $Al_yGa_{1-y}As$, where $0.2 \le y \le 1.0$. This superlattice helps prevent propagation of substrate defects (e.g., dislocations) into buffer layer 14. More GaAs is grown over the superlattice at about 560-600°C to a thickness of less than about 1,000Å, and preferably about 500Å.

Referring also to FIGS. 1-3, the temperature of the wafer is reduced (Step 56) and a portion of buffer layer 14 is grown (Step 58) from times t_0 to t_1. The wafer temperature is reduced to between about 480°C and about 520°C. Buffer layer 14 is grown (Step 58) starting with either $Al_{.95}In_{.05}As$ or $In_{.05}(Al_wGa_{1-w})_{.95}As$. The indium concentration is initially less than about 15% to guard against 3-dimensional (nonplanar) growth. As buffer layer 14 begins growing, more indium is introduced into the material being deposited so that the indium concentration linearly increases with time, t, and, correspondingly, with the thickness, a, of buffer layer 14. For $In_{.05}(Al_wGa_{1-w})_{.95}As$, as the indium concentration is increased, the aluminum and gallium concentrations are adjusted (aluminum being ramped up and gallium being ramped down) to help ensure that buffer layer 14 remains insulating and that the bandgap of buffer layer 14 remains greater than the bandgap of GaAs substrate 12. The indium concentration is linearly increased to an intermediate concentration c_{int} between 10-20%, and preferably about 15%, at time t_1 corresponding to thickness a_1.

When the indium concentration in buffer layer 14 reaches the intermediate concentration c_{int}, the temperature is reduced (Step 60) for more buffer layer growth (Step 62). The temperature is reduced (Step 60) to between about 380 and about 420°C. Buffer layer 14 may be grown during the time needed to reduce (Step 60) the temperature or, as indicated in FIGS. 2 and 3, a growth interrupt may occur during temperature reduction. With the temperature reduced (Step 60), buffer layer 14 is continued to be grown (Step 62). The reduced temperature helps reduce 3-dimensional growth, yielding substantially planar growth of buffer layer 14. The indium concentration is linearly increased between times

t_1 and t_2 while growing (Step 62) buffer layer 14 from thickness a_1 to a_2 until the indium concentration in buffer layer 14 reaches the predetermined maximum concentration c_{max} at the top a_2 of buffer layer 14.

5 When the maximum desired indium concentration c_{max} is reached, the temperature is increased (Step 64) for growing barrier/buffer layer 16 (Step 66). The temperature is increased (Step 64) to between about 470 and about 520°C. Barrier/buffer layer 16 may be grown 10 during the time needed to increase (Step 64) the temperature or, as indicated in FIGS. 2 and 3, a growth interrupt may occur during temperature increase (Step 64). With the temperature raised (Step 64), barrier/buffer layer 16 is grown (Step 66) with the 15 indium concentration adjusted to the desired relaxed indium concentration c_{rel}.

Device layers 18, 20, 22, 24, 26, 28, 30, and 32 are grown (Step 68) and etched (Step 70), and electrodes 34, 36, and 38 are formed (Step 70). The device layers 20 are grown (Step 68) at temperatures between about 480 and about 520°C using conventional techniques. A recess is formed (Step 70) through undoped layer 30 and contact layer 32 for gate electrode 38 using a selective succinic acid based etch based wet etch. Source and drain 25 electrodes 34 and 36 are formed (Step 70) using an AuGe-Au metallurgy alloyed in a tube furnace in an H_2 ambient. Gate electrode 38 is formed from Ti-Pt-Au as a 0.15μm - 0.25μm T-gate using conventional techniques to complete the device 10.

30 MHEMTs similar to MHEMT 10 were built with an $In_{0.65}Ga_{0.35}As$ channel layer and an $In_{0.53}Ga_{0.47}As$ channel layer, respectively. The 65% In MHEMT exhibited room temperature mobility of greater than 10,000 cm^2/Vs with a sheet density of $4 \times 10^{12} cm^{-2}$, and better transconductance 35 and gain than pseudomorphic HEMTs (PHEMTs). The 53%

MHEMT exhibited better transconductance than PHEMTs, at least 3 dB better gain, and better noise figure above 11 GHz than PHEMTs.

Referring to FIG. 5, a metamorphic high electron mobility transistor (MHEMT) 80 is shown. FIG. 5 illustrates that the invention is applicable to other compositions than that of MHEMT 10 shown in FIG. 1. MHEMT 80 is similar to MHEMT 10 except that x=0.35 in MHEMT 80 and barrier/buffer layer 16 and Schottky layer 28 are replaced by barrier/buffer layer 82 and Schottky layer 84. Barrier layer 82 is made of $In_x(Ga_zAl_{1-z})_{1-x}As$ and Schottky layer 84 is made of $In_{x-0.1}(Ga_zAl_{1-z})_{1.1-x}As$. Layers 82 and 84 are made using MBE with the appropriate ratios of elements.

Other embodiments are within the spirit and scope of the appended claims. For example, the indium concentration in channel layer 22 can be different than specifically mentioned above. The channel layer indium concentration is adjustable, and can be as low as 0% or as high as 100%. Thus, the relaxed lattice constant of buffer layer 14 can be, e.g., as low as about 5.653Å (GaAs) or as high as about 6.058Å (InAs). Also, undoped layer 30 and contact layer 32 may be formed as a single layer, either doped or undoped.

What is claimed is:

1. A high electron mobility transistor structure comprising:

an insulating substrate having a substrate lattice constant;

5 a buffer layer disposed over the substrate and having a graded lattice constant substantially equal to a first lattice constant near a bottom of the buffer layer and substantially equal to a second lattice constant near a top of the buffer layer larger than the substrate

10 lattice constant and the first lattice constant; and

a channel layer disposed above the buffer layer and having a concentration of indium to provide a lattice constant of the channel layer larger than the substrate lattice constant.

15 2. The structure recited in claim 1 further comprising a barrier/buffer layer disposed over the buffer layer.

3. The structure recited in claim 2 wherein the lattice constant near a top of the barrier/buffer layer

20 is substantially equal to the lattice constant of the channel layer.

4. The structure recited in claim 2 wherein the lattice constant of the barrier/buffer layer is different from the lattice constant of the channel layer.

25 5. The structure of claim 2 wherein the lattice constant of the barrier/buffer layer is smaller than the second lattice constant.

6. The structure recited in claim 2 wherein the lattice constant of a portion of the buffer layer varies

30 with distance from the substrate.

7. The structure recited in claim 2 wherein the buffer layer is a Group III-V material including a Group III material having a first concentration of indium at the bottom of the buffer layer lower than a second indium
5 concentration at the top of the buffer layer.

8. The structure recited in claim 7 wherein the first indium concentration is about 5%.

9. The structure recited in claim 7 wherein the barrier/buffer layer is a Group III-V material including
10 a Group III material having a lower indium concentration than the second indium concentration of the buffer layer.

10. The structure recited in claim 9 wherein a difference between the second indium concentration and the indium concentration of the barrier/buffer layer is
15 between about 3 percentage points and about 8 percentage points.

11. The structure recited in claim 9 wherein the channel layer is a Group III-V material including a Group III material having an indium concentration substantially
20 equal to an indium concentration of the barrier/buffer layer.

12. The structure recited in claim 7 wherein the channel layer is a Group III-V material including a Group III material having an indium concentration between about
25 25% and about 75%.

13. The structure recited in claim 7 wherein the indium concentration in the buffer layer varies with thickness of the buffer layer from the first indium concentration to the second indium concentration.

14. The structure of claim 13 wherein the indium concentration in the buffer layer varies linearly with thickness from the first concentration to the third concentration.

5 15. The structure recited in claim 1 wherein the substrate comprises gallium arsenide.

16. A method of forming a high electron mobility transistor structure, the method comprising:

providing an insulating substrate having a
10 substrate lattice constant;

forming a buffer layer over the substrate, the buffer layer having a graded lattice constant substantially equal to a first lattice constant near a bottom of the buffer layer and substantially equal to a
15 second lattice constant near a top of the buffer layer larger than the substrate lattice constant and the first lattice constant; and

forming a channel layer above the buffer layer, the channel layer having a concentration of indium to
20 provide a lattice constant of the channel layer larger than the substrate lattice constant.

17. The method recited in claim 16 further comprising forming a barrier/buffer layer over the buffer layer.

25 18. The method recited in claim 17 wherein the barrier/buffer layer has a lattice constant substantially equal to the lattice constant of the channel layer.

19. The method recited in claim 17 wherein the barrier/buffer layer has a lattice constant different
30 than the lattice constant of the channel layer.

20. The method recited in claim 17 wherein the lattice constant of the barrier/buffer layer is smaller than the second lattice constant.

21. The method recited in claim 17 wherein the buffer layer is a Group III-V buffer layer material including a Group III material having a first indium concentration near the bottom of the buffer layer and a second indium concentration, higher than the first indium concentration, disposed near the top of the buffer layer, and wherein the barrier/buffer layer is a Group III-V barrier/buffer layer material including a Group III material having an indium concentration lower than the second indium concentration.

22. The method recited in claim 21 wherein forming the buffer layer includes growing the Group III-V buffer layer material at a first temperature in a first temperature range while increasing the buffer layer indium concentration from the first indium concentration to an intermediate indium concentration, and growing the Group III-V buffer layer material at a second temperature in a second temperature range while increasing the buffer layer indium concentration from the intermediate indium concentration to the second indium concentration, and wherein forming the barrier/buffer layer includes growing the Group III-V barrier/buffer layer material at a third temperature in a third temperature range, and wherein the second temperature range is lower than the first and third temperature ranges.

23. The method recited in claim 22 wherein the first temperature range is about 480°C to about 520°C, the second temperature range is about 380°C to about

420°C, and the third temperature range is about 470°C to about 520°C.

24. A field-effect transistor structure comprising:

5 a gallium arsenide substrate;

a buffer layer of a Group III-V material disposed over the substrate and including a Group III material having a graded indium concentration substantially equal to a first concentration near a bottom of the buffer 10 layer and substantially equal to a second concentration near a top of the buffer layer larger than the first concentration;

a barrier/buffer layer of a Group III-V material disposed over the buffer layer and including a Group III 15 material having a third indium concentration lower than the second indium concentration; and

a channel layer of a Group III-V material disposed above the buffer layer and including a Group III material having an indium concentration substantially equal to the 20 third indium concentration.

25. A field-effect transistor structure comprising:

a gallium arsenide substrate having a substrate lattice constant;

25 a buffer layer disposed over the substrate and having a graded lattice constant substantially equal to a first lattice constant near a bottom of the buffer layer and substantially equal to a second lattice constant near a top of the buffer layer larger than the substrate 30 lattice constant and the first lattice constant;

a channel layer disposed above the buffer layer and having a concentration of indium to provide a lattice

constant of the channel layer larger than the substrate lattice constant;

a donor-spacer layer having a doped region and an undoped region forming a heterojunction with the channel
5 layer; and

a contact layer disposed above the channel layer.

26. A high electron mobility transistor structure comprising:

a gallium arsenide substrate;

10 a buffer layer of $In_x(Al_yGa_{1-y})_{1-x}As$ disposed over the substrate, where $0 \le x \le 1$, the buffer layer having a concentration of indium such that x is about 0.05 near the substrate and is equal to m at a position remote from the substrate;

15 a barrier/buffer layer of $In_n(G3)_{1-n}As$ disposed over the buffer layer, G3 being a Group III material and m being greater than n;

a channel layer of $In_nGa_{1-n}As$ disposed above the first buffer layer;

20 a donor-spacer layer having a doped region and an undoped region forming a heterojunction with the channel layer; and

a contact layer disposed above the channel layer.

27. The structure recited in claim 26 wherein m
25 is about 0.05 greater than n.

28. The structure recited in claim 26 wherein the indium concentration in the buffer layer increases substantially linearly with buffer layer thickness from the substrate to the position remote from the substrate.

30 29. The structure recited in claim 26 wherein the donor-spacer layer is a first donor-spacer layer disposed

between the buffer layer and the channel layer, the structure further comprising a second donor-spacer layer disposed over the channel layer and having a doped region and an undoped region forming a heterojunction with the
5 channel layer.

30. The structure recited in claim 29 wherein G3 is Ga_zAl_{1-z}, wherein the first donor-spacer layer comprises:

a first pulse layer disposed over the
10 barrier/buffer layer and including a high concentration of carriers; and

a first spacer layer of $In_n(Ga_zAl_{1-z})_{1-n}As$ disposed over the first pulse layer;

wherein the second donor-spacer layer comprises:

15 a second spacer layer of $In_n(Ga_zAl_{1-z})_{1-n}As$ disposed over the channel layer;

a second pulse layer disposed over the second spacer layer and including a high concentration of carriers; and

20 wherein the structure further comprises a Schottky layer of $In_{n-0.1}(Ga_zAl_{1-z}As)_{1.1-n}$ disposed over the second pulse layer.

31. The structure recited in claim 29 wherein G3 is Al, wherein the first donor-spacer layer comprises:

25 a first pulse layer disposed over the barrier/buffer layer and including a high concentration of carriers; and

a first spacer layer disposed over the first pulse layer;

30 wherein the second donor-spacer layer comprises:

a second spacer layer disposed over the channel layer;

a second pulse layer disposed over the second spacer layer and including a high concentration of carriers; and

wherein the structure further comprises a Schottky

5 layer of $In_{n-0.1}Al_{1.1-n}As$ disposed over the second pulse layer.

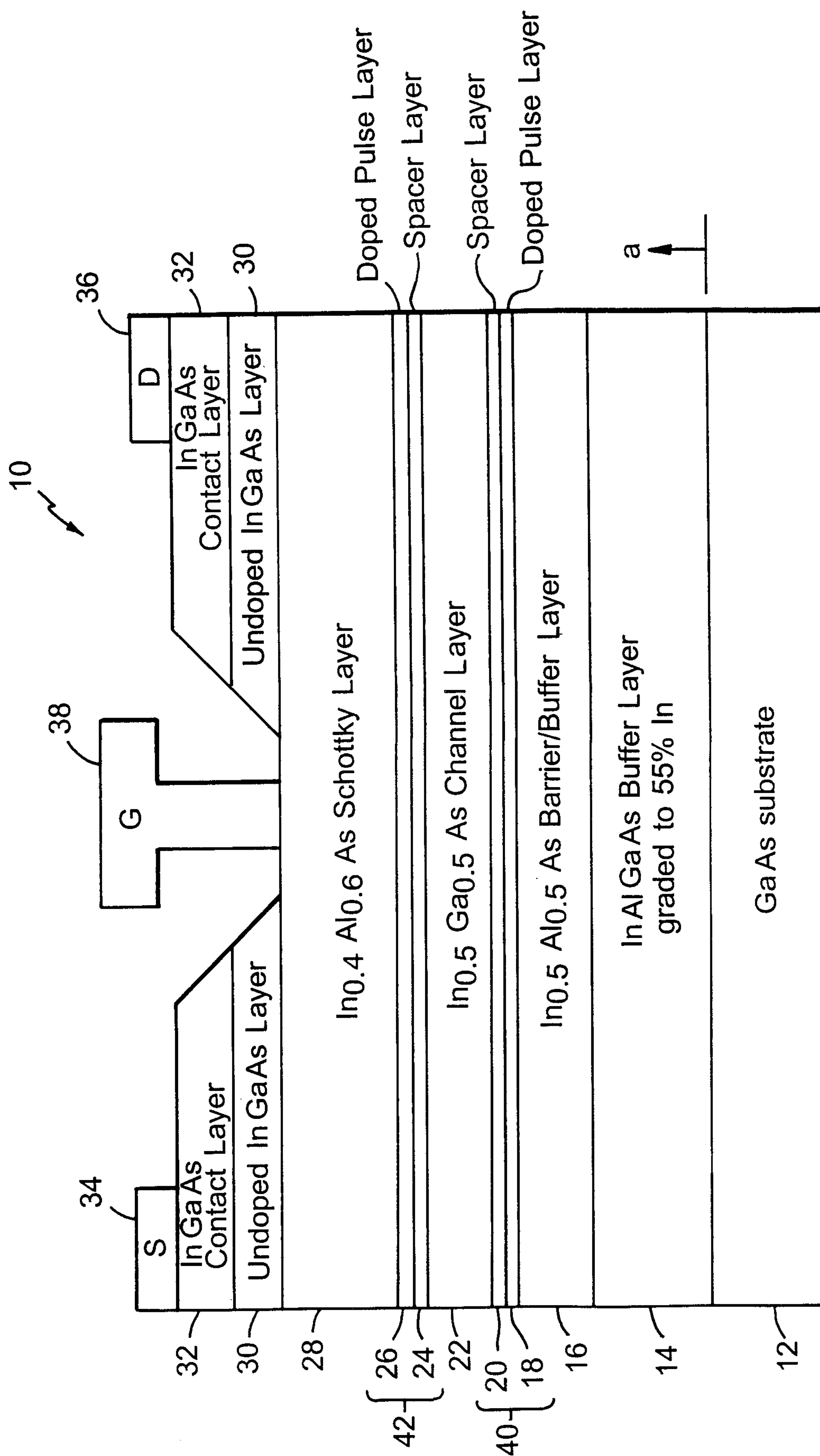

FIG. 1

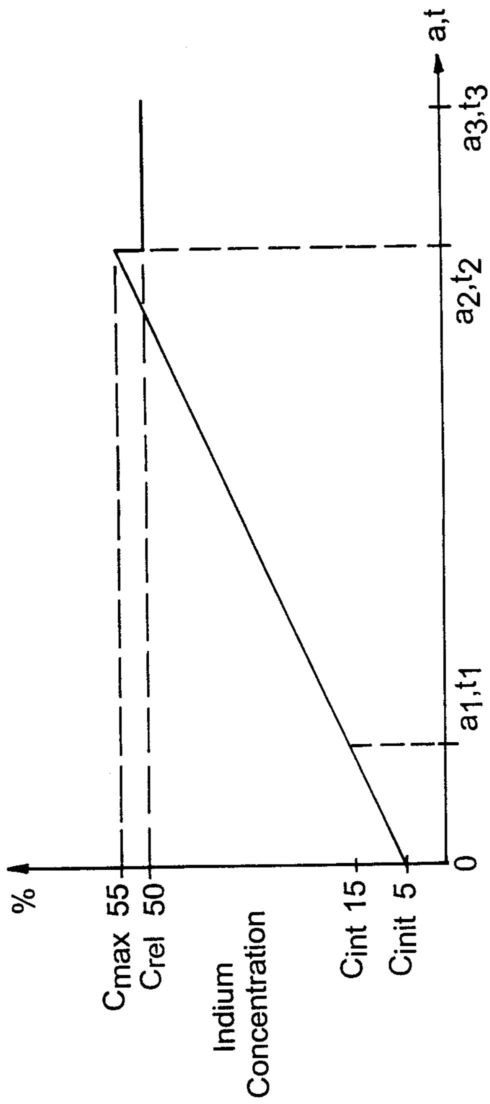

FIG. 2

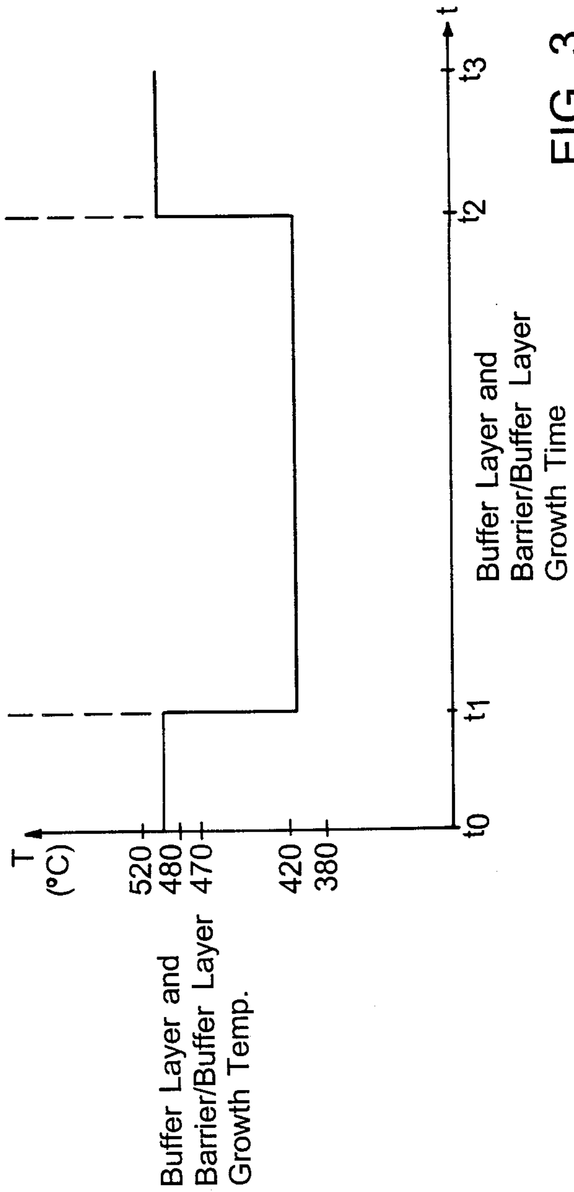

FIG. 3

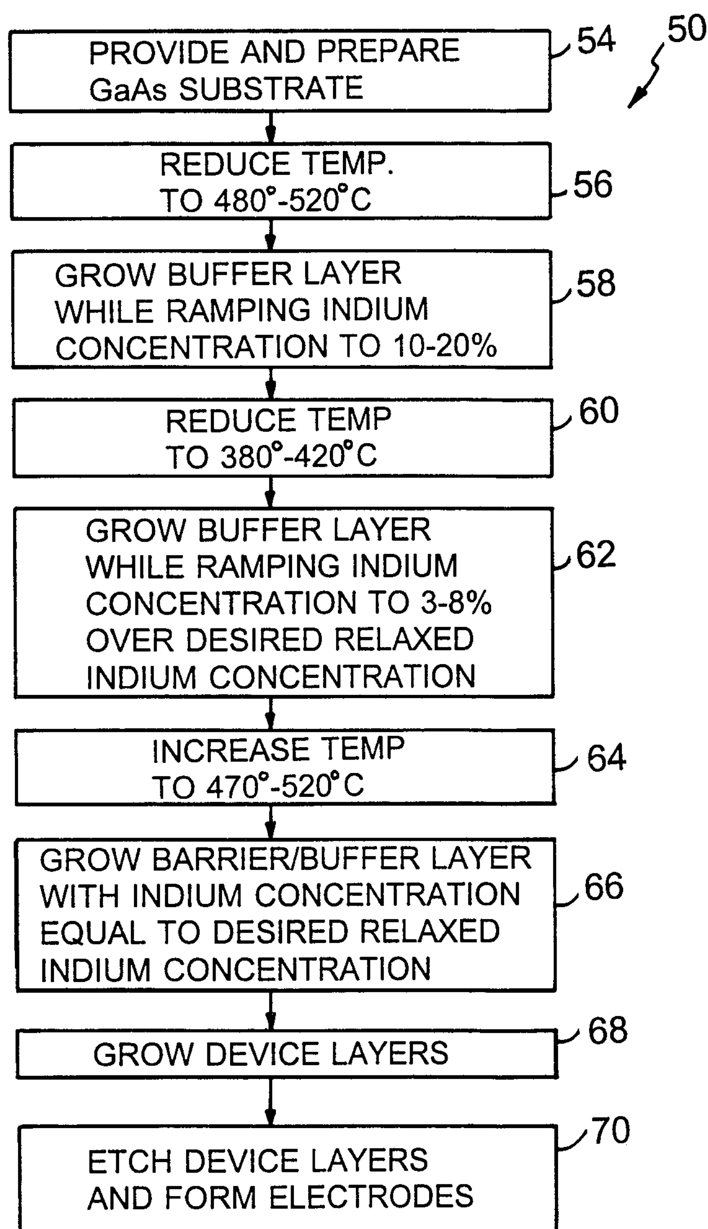

FIG. 4

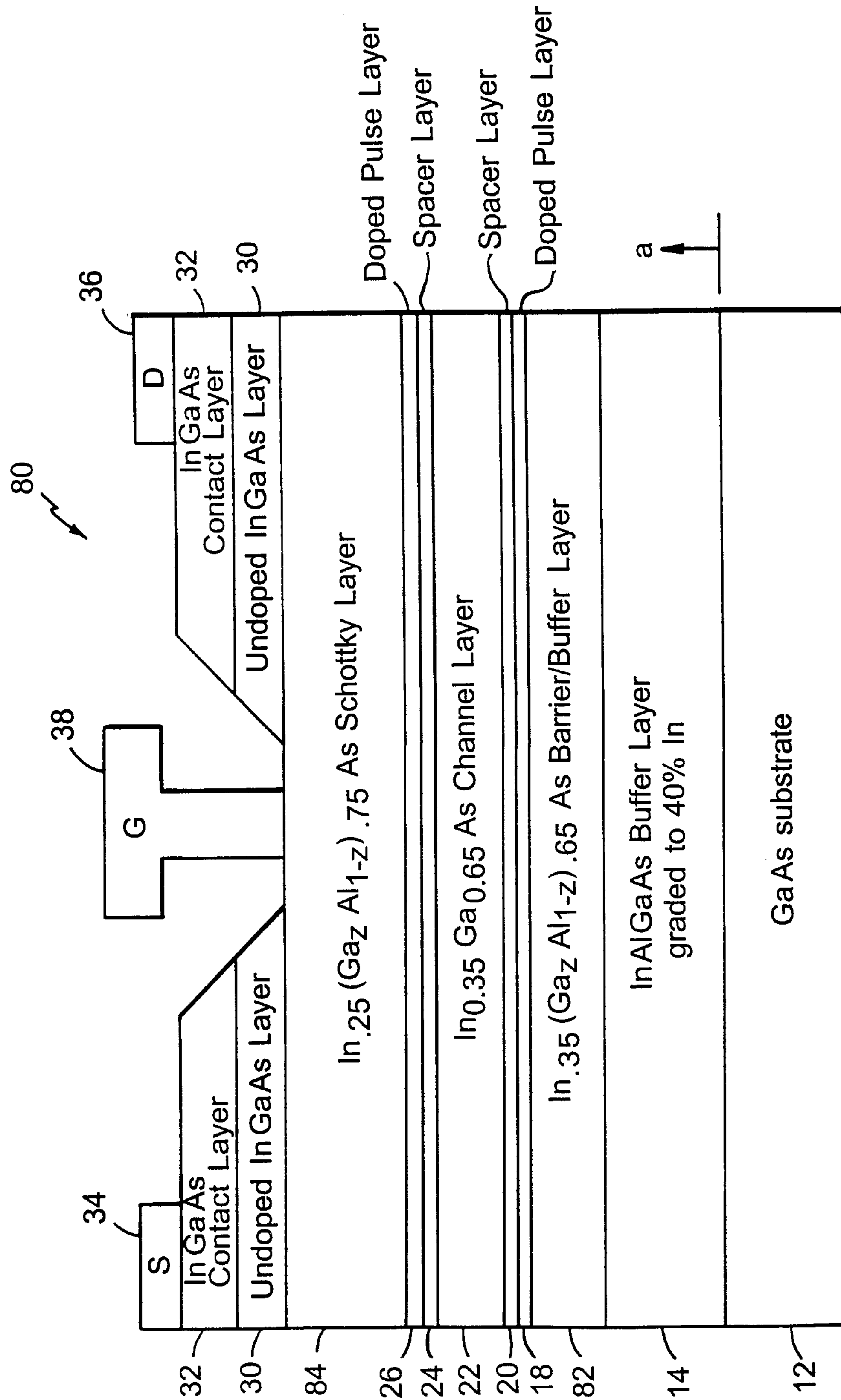

FIG. 5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/14805

A. CLASSIFICATION OF SUBJECT MATTER
IPC(6) :H01L 31/0328
US CL :257/194
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 257/190, 191, 194, 195; 438/87, 172

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

none

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

U.S. PTO APS search terms: HEMT, graded buffer

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5,319,223 A (FUJITA ET AL) 07 JUNE 1994 (07.06.94), column 4, lines 40-65.	1, 16, 25
X	US 4,963,949 A (WANLASS ET AL) 16 October 1990 (16.10.90), column 4, lines 50-54.	2-15, 17-21, 24, 26-31
A	US 5,633,516 A (MISHIMA ET AL) 27 May 1997 (27.05.97), see abstract.	1-31

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
13 SEPTEMBER 1999	21 OCT 1999

Name and mailing address of the ISA/US	Authorized officer
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