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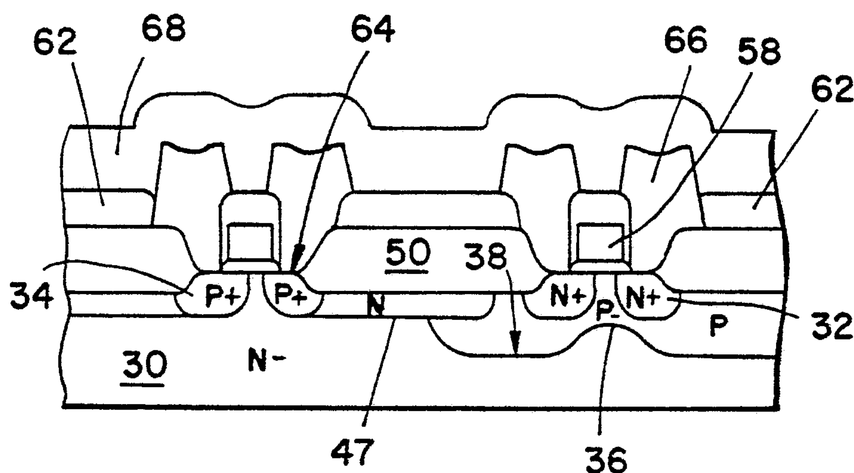
(54) Title: CMOS P-WELL SELECTIVE IMPLANT METHOD, AND A DEVICE MADE THEREFROM



(57) Abstract

A method for fabricating a complementary metal-oxide-silicon (CMOS) integrated circuit device by forming a composite layer of oxide and nitride on the surface of a silicon substrate defined into predetermined areas for the subsequent formation of transistors, marking the substrate to expose preselected areas for P-wells, ion implanting P-type material (44 and 46 in Fig. 4) in the exposed areas to form P-wells so that a relatively high doping level is established under the composite layer areas with the P-wells. The regions (42 and 40) of Fig. 2; (42 and 46) of Fig. 4 and (38 and 36) of Fig. 9 illustrate the inventive concept. Fig. 2 represents a CMOS device made in accordance with the present invention. The ion implantation of P-type material may be accomplished in either a single stage or a two stage procedure.

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CMOS P-WELL SELECTIVE IMPLANT METHOD, AND A DEVICE THEREFROM

Background of the Invention

This invention relates generally to semiconductor devices of the metal-oxide-silicon (MOS) type and to the production or fabrication of integrated circuits containing arrays of such devices. More particularly, the present invention relates to an improved method for fabricating complementary or CMOS type integrated circuits.

In conventional CMOS devices which use opposite polarity transistors to perform circuit functions, an important step in the fabrication process is the formation of lightly-doped areas of P-type diffusion, or "P-wells", within which the N-channel transistors are formed. These relatively deep P-well diffusions are normally formed at a low doping level and require extreme precision since the dopant concentration regulates both the threshold voltage V_T and the breakdown voltage of the N-channel MOSFET's. The formation of the P-wells is further complicated by the fact that in any integrated circuit array, parasitic transistors are created by conductive interconnect lines that extend over the field oxide areas. If the field oxide is thin enough to allow inversion, parasitic leakage can occur that could cause the circuit to malfunction or use excessive power. To overcome this problem, it was heretofore necessary to increase the field oxide thickness in the field area to several times the oxide thickness in the device area. For example, in prior art CMOS circuits, the field oxide to device oxide ratio was often required to be 15 to 1 or greater. A serious disadvantage with this requirement for a relatively thick field oxide was that it created large oxide step heights and limited the use of fine line geometrics in CMOS integrated circuits.

In addition to the aforesaid requirement for a relatively thick field oxide and the inherent "step" problems, a further disadvantage with prior CMOS integrated circuits

was that they also required "channel stop" diffusions to provide isolation and prevent leakage between transistor cells. Although such channel stops did not require extra processing steps, they did require extra area and thus substantially increased the size of the integrated circuit chip.

The present invention, as described herein, solves both of these problems with a fabrication process using field implants which removes the requirement for channel stops and also allows a thinner field oxide layer to be used. This improvement provides better thin film step coverage and easier, more efficient photolithography which in turn allows fine line widths and small spaces in the overall circuit topography, thereby making possible a smaller chip size for the circuit.

Yet another problem encountered with prior methods for fabricating CMOS devices with isolated P-wells was that a reduction of doping concentration inherently occurred at the edges of the P-wells under the field oxide at the exact location where the dopant was most needed. This doping reduction occurred because of the typical diffusion distribution which normally causes less dopant at the edges of a diffusion area and also the fact that field oxide has a tendency to deplete dopant at the silicon/oxide interface. Also, in prior CMOS processes, P-wells were formed by ion implantation using field oxide regions already formed as the implant barriers. This often resulted in an array having adjacent P-wells which were isolated from each other unless located closely together, an arrangement that required more topside contacts and therefore more chip area. One method previously suggested for alleviating this problem was to increase the P-well sidewall doping by increasing the original P-doping level and thereafter counterdoping with an N-type dopant. However, this approach proved to be unsatisfactory because it degraded majority carrier mobility and increased N+ area capacitance and hence reduced N-channel device performance. These problems are also solved by the present invention.

Accordingly, a general object of the invention is to provide an improved method for making CMOS integrated circuit devices that solves the aforesaid problems.

Another object of the invention is to provide a method for fabricating CMOS semiconductor devices that greatly reduces the ratio of field oxide to device oxide thickness and this eliminates relatively large steps for the conductive paths of the device.

Yet another object of the invention is to provide a method for fabricating CMOS semiconductor devices that provides a deeper and more concentrated doping level along the edges of each P-well extending under the edges of adjacent field oxide areas.

Another object of the invention is to provide an improved CMOS structure that provides a relatively small ratio of field oxide to device oxide thickness and thereby enables the use of relatively narrow conductive interconnect lines.

Another object of the invention is to provide an improved CMOS integrated circuit device structure wherein a single P-well diffusion area is utilized for adjacent N-type transistors of two or more CMOS elements.

Another object of the invention is to enable the reduction of field oxide thickness which reduces the height of oxide steps which subsequent thin film layers must traverse.

Summary of the Invention

The aforesaid objects of the present invention are accomplished by a method for forming a CMOS integrated circuit wherein P-wells for the N-channel transistors of the circuit are formed prior to the growth of field oxide. Preliminary steps in the present method are similar to conventional procedures for preparing the appropriate silicon material for processing. Thereafter, a first relatively thin oxide is formed on the silicon surface and is then covered with a similar layer of silicon nitride. This composite oxide/nitride barrier layer is then masked and portions are etched away to

leave only those areas where field oxide will subsequently be applied.

A second mask of photoresist material is now applied to define the P-well areas by covering some of the oxide/nitride areas and leaving others exposed. With the second mask in place, the P-wells are formed by boron ion implantation in the areas not covered by photoresist. When this implantation takes place, which can be done in one or two implantation steps, some of the boron atoms are trapped in the nitride cap of the exposed oxide/nitride areas. Thus, in areas surrounding the exposed oxide/nitride areas, the boron atoms are driven into the silicon substrate to a predetermined depth and at the prescribed doping level but directly under the exposed oxide/nitride areas, the doping reaches a lesser depth and intensity or level. Following implantation, the P-well implant is driven in by thermal diffusion which may be done prior to or during field oxide growth. Thereafter, in the areas not covered by the oxide/nitride layers, the field oxide is grown and subsequent processing is provided in the conventional manner to define the various P-channel and N-channel transistors and to form the necessary interconnect paths.

With CMOS devices completed in accordance with the principles of the present invention, closely adjacent P-wells may be connected together as one diffusion area, thereby reducing the number of surface contacts required. In these P-wells, the P-doping concentration is heavier under the field oxide areas where it is most needed to improve field threshold. The advantages of reduced field oxide thickness requirements which allows finer geometric lines and hence, CMOS circuits with greater device density, are provided with the improved process which has no additional steps.

Other objects, advantages and features of the invention may become apparent from the following detailed description, taken in conjunction with the accompanying drawing.

Brief Description of the Drawing

Fig. 1 is a view in section showing a portion of a CMOS device of the prior art with conventional P-wells;

Fig. 2 is a view in section showing a portion of a CMOS device made in accordance with the present invention;

Fig. 3 is a diagrammatic view in section showing the formation of a P-well by ion implantation according to one embodiment of the invention;

Fig. 4 is a diagrammatic view in section showing the formation of a P-well by ion implantation according to a second embodiment of the invention;

Figs. 5 - 9 are a series of fragmentary views in section, illustrating the method steps for fabricating a CMOS device according to the principles of the present invention.

Detailed Description of the Embodiment

With reference to the drawing, Fig. 1 shows diagrammatically, a portion of a typical complementary MOS integrated circuit device 20 having conventional selective field oxide areas 22 that are spaced apart to form open areas within which is an MOS transistor gate 24 on its thin layer of gate oxide 26. In such prior art, CMOS devices, lightly-doped "P-well" regions 28 for the N-channel transistors of each complementary device are diffused into the device substrate 30 after the field oxide areas have been defined. The N-channel transistors comprise N-type source and drain diffusions 32 provided later within each P-well, and complementary P-channel transistors are formed in the open areas outside the P-wells by P-type source and drain diffusions 34. The P-well regions 28 are fairly uniform gaussian diffused redistribution regions. However, along the outer edge portions 36 of these diffused P-well regions (defined by the dotted lines) the doping levels are lighter than the rest of the P-well, for two reasons. First, because of conventional

diffusion characteristics, there is less dopant source available at this edge location for dopant redistribution. Secondly, field oxide material has a natural tendency to deplete boron dopant at the silicon/oxide interface. Yet, in order to prevent field threshold inversion at lower voltages, the edge areas 36 are where the P-dopant concentration should be relatively high. It is also typical in the prior art, as illustrated in Fig. 1, that where field oxide regions are used as barriers when P-wells are formed by ion implantation, often closely adjacent P-wells are isolated from one another instead of being connected, thereby requiring additional chip area for added surface contacts. Also, in planar CMOS devices of the prior art, channel stop diffusions were required which further increased chip size.

In Fig. 2, a portion of a CMOS integrated circuit device 38, according to the present invention, is shown which overcomes the disadvantages of the device shown in Fig. 1. Here, P-channel and N-channel transistors of the CMOS device are shown located adjacent each other in an N-type substrate material 30. To illustrate a typical CMOS structure similar to the prior art of Fig. 1, but having advantages according to the present invention, another N-channel transistor of another CMOS device is located relatively close to the first N-channel device. Now, in accordance with the invention, the two adjacent N-channel transistors formed by N+ diffusions 32 are both located in the same coextensive P-well 40. Also, this enlarged P-well has edge areas 42 of higher dopant concentration of P-type material located substantially under the above field oxide areas 22 as required, to prevent field threshold inversion at low voltages.

The method steps for accomplishing the improved structure of Fig. 2, according to the present invention, may be best described with reference to Figs. 5 to 9.

The process commences, as shown in Fig. 5, with a wafer substrate 30 of (typically) N-type silicon <100> crystal plane material which has a (typical) resistivity of 3-5 ohm centimeter. On the surface of the silicon, is grown

a relatively thin layer 44 of silicon dioxide (e.g. 300-500 Å) which is called the base oxide. Immediately after this oxide application, a somewhat thicker layer 46 (e.g. 900-2000 Å) of silicon nitride is applied over it. Thereafter, a first mask 48 of photoresist material is used to etch away the composite oxide/nitride layers in all areas except those in which field oxide is to be formed later on.

In the next step of the method, as shown in Fig. 6, P-well areas are defined in the form of a second or reverse P-well mask 50 of photoresist material after the first mask has been removed. With this second mask in place, the unmasked areas are field implanted with an N-type material (e.g. arsenic), preferably by conventional ion implantation procedures, as indicated by the vertical arrows. After this field implant, the photo resist material 50 is removed from the P-well areas. This step of the process is optional depending on desired P-channel field threshold.

For the next step, as shown in Fig. 7, a third mask 52 of photoresist material is applied to cover all areas of the wafer that are not P-well areas. Now, the lightly-doped P-well regions are formed in the substrate 30 by ion implantation. This implantation may be made in a one step single charge procedure or it may be made in a two step or dual charge procedure. In the single energy implantation procedure, a uniform charge energy level (e.g. 50 KEV) may be used with conventional implantation equipment. As illustrated diagrammatically in Fig. 3, a substantial portion of this implantation charge of boron atoms (represented by the letter B) is absorbed by the nitride cap 46 of the composite layer covering the device area, while a percentage of the boron atoms penetrate completely through the composite oxide/nitride layers 44, 46 and into the substrate below as indicated by the spaced apart "B's". However, a full implantation charge of boron atoms (indicated by "B's" closer together) occurs in the open areas surrounding the device areas. Thus, the resulting P-well has a moderate depth of light P-doping in the device area and a higher P dopant concentration around the

device area. The photoresist 52, must be thick, enough (e.g. 0.5 micron) to absorb this implant for surrounding areas outside the P-well areas.

In an alternate or dual energy implantation procedure, illustrated diagrammatically in Fig. 4, a low-energy/high density charge is first implanted which provides a relatively high dopant level around the device area defined by the unmasked oxide/nitride composite layer. This low energy charge (e.g. 25 KEV) provides a relatively dense concentration (represented by "B's" that are close together) and these low energy boron atoms are completely absorbed by and do not pass through the nitride cap 46 of the composite layer. After completion of the low energy implant, a second implant is made with a relatively high energy (e.g. >100 KEV) and low density charge of boron atoms. This second charge (represented by the "B's" spaced farther apart) forces the P-dopant atoms deeper into the substrate around the device areas and it also penetrates through the composite layer 44, 46 of the device areas to form the P-well thereunder. The photoresist 52 must be thick enough (e.g. 1.0 micron) to absorb both of these implants. The result is essentially the same configuration of P-well as provided by the one charge procedure, that is, P-wells 40 (as shown in Fig. 2) with higher dopant concentration 42 around their peripheries and under field oxide areas than directly under the composite layer or device areas. This method allows a greater degree of process control than the single energy method.

It should be noted that the examples shown herein are silicon gate devices. However, the same technique, according to the invention, could be used for metal gate CMOS processes if desired.

Now, with the P-wells formed as described, the remaining fabrication steps for the CMOS device can proceed. As shown in Fig. 8, a relatively thick oxide layer 54 (e.g. 12,000 Å) is formed in the field areas while a thin oxide layer 56 (e.g. 1,000 Å) is grown in the device areas using conventional procedures. A layer of N+ doped polysilicon 58

is applied to the oxide layer. Thereafter, another mask 60 is used to form the polysilicon gate regions for all of the circuit. When the photoresist layer 60 is removed from the gates 58, the thin oxide around the gates is also etched away.

Fig. 9 shows a portion of the completed CMOS device made according to the method steps of the present invention. The processing steps occurring between Figs. 8 and 9 are conventional ones, well known to those skilled in the art and therefore, are not shown in detail. Essentially, they involve the formation of the N+ source-drain regions 32 and also, the P+ source-drain regions 34, by standard diffusion techniques; the formation of an intermediate oxide layer 62 which serves as a dielectric layer between polysilicon and metal layers; the formation of contact areas 64 for contact of metal to the various source-drain regions; the metallization 66 in the contact areas; and an upper scratch protection and passivation layer 68 that may be applied in the conventional manner and which may be silicon dioxide, silicon nitride or other passivation material.

With the process of the present invention, the field oxide layer can be kept to a minimum thickness which is substantially thinner than previously required for CMOS devices. This is primarily because the dopant level, being relatively high in the P-well field areas 42, allows a higher field threshold voltage for the device being produced. In other words, a preselected threshold voltage can be obtained by this selective doping process without requiring a relatively thick field oxide layer.

Thus, the CMOS device resulting from the aforesaid method, according to the present invention, with its P-wells 36, formed as previously described, makes possible a relatively low ratio of field oxide to device oxide which eliminates the step problems with conductive paths while providing favorable operating characteristics. Yet the fabrication of such an improved device is accomplished without the necessity for additional masks or complicated processing procedures.

To those skilled in the art to which this invention relates, many changes in construction and widely differing embodiments and applications of the invention, as well as variations in the method steps, will suggest themselves without departing from the spirit and scope of the invention. The disclosures and the description herein are purely illustrative and are not intended to be in any sense limiting.

I claim:

IN THE CLAIMS:

1. In the fabrication of a complementary MOS integrated circuit device, a method of forming P-wells for N-type transistors, comprising the steps of:

(a) forming a composite layer of oxide and nitride on the surface of a silicon substrate of N-type material;

(b) forming said composite layer into defined device areas for subsequent formation of transistors;

(c) masking the substrate to expose the P-well areas, including composite layer areas for N-type transistors;

(d) providing for ion implantation in the exposed P-well areas, so that a relatively high doping level to a relatively greater depth is established around the composite layer areas and a lower doping level with less depth is established under the composite layer areas.

2. The method as described in Claim 1 wherein said step of providing for ion implantation comprises creating a single ion implanting charge at an energy level and density that is sufficient to force a substantial portion of the charge through each composite layer in a P-well area, thereby providing a doped region under each composite layer, said single charge causing a deeper and more highly doped portion of each P-well area around each said composite layer.

3. The method as described in Claim 2 wherein said single ion implanting charge has an energy level of around 50 KEV.

4. The method as described in Claim 1 wherein said step of providing for ion implantation comprises creating dual implanting charges, including a first charge of relatively low energy and high density so that the implantation atoms are trapped in the nitride cap of each exposed composite layer while being driven into the silicon material surrounding said composite layers, and a second charge of relatively high energy and low density atoms that are driven completely through the composite layer to provide the "P" region under it, said second charge causing a deeper dopant penetration in the areas surrounding the composite layers.

5. The method as described in Claim 4 wherein said first charge has a relatively low energy of around 25 KEV and said second charge has a higher energy of around 80-100 KEV.

6. A method for fabricating complementary MOS integrated circuit devices comprising the steps of:

providing a substrate of N-type silicon material;

forming a layer of oxide on the surface of said silicon substrate;

forming a layer of nitride on said oxide to provide a composite layer;

forming said composite layer into defined device areas for subsequent formation of transistors;

masking the substrate to provide exposed areas for forming P-wells that include smaller areas of said composite layer for N-type transistors;

providing ion implantation of P-type material in the exposed P-well areas so that a relatively high doping concentration and greater depth of P-type material is provided around the composite layer within the P-well area than directly under said composite layer;

forming a field oxide layer on said substrate surrounding the transistor device areas within and outside of said P-well;

forming a gate oxide layer gate means, source and drain diffusions for transistors in said device areas; and

forming conductive paths between transistors within and outside of said P-wells.

7. The method as described in Claim 6 wherein said ion implanation is accomplished by a first charge of relatively low energy and high density, followed by a second charge of relatively high energy and low density.

8. The method as described in Claim 7 wherein said first charge is at an energy level of around 25 KEV and said second charge is at an energy level of around 80-100 KEV.

9. The method as described in Claim 6 wherein said field oxide layer is grown to a thickness of around 12,000 Å and said gate oxide layer is around 1,000 Å.

10. A complementary type metal-oxide-silicon device comprising:

a silicon substrate;

a series of P-wells in said substrate, each containing at least one pair of spaced apart N+ diffusions with gate means extending between said diffusions and surrounded by an open area of substrate covered by a layer of field oxide, each said P-well having a greater depth and concentration of P-type material in said areas that are at least partially under said field oxide and around said diffusions than in the substrate areas under said diffusions.

11. The device as described in Claim 10 wherein at least one of said P-wells has two pairs of N+ diffusions which are spaced apart and separated by a layer of field oxide between them said P-well having a greater depth and concentration of P-type material under said field oxide and around its outer edges.

12. The device as described in Claim 10 wherein said field oxide has a thickness of around 12,000 Å, and each said pair of N+ diffusions extend below a gate oxide having a thickness of around 1,000 Å.

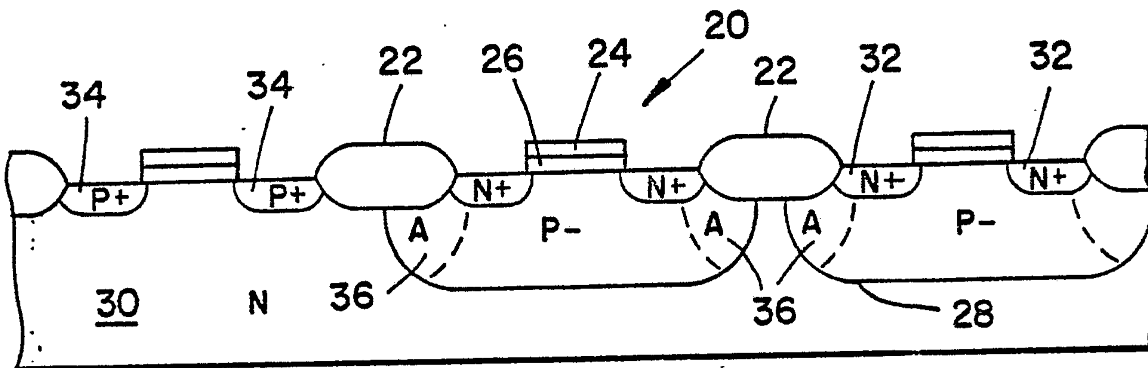

FIG _ 1 (PRIOR ART)

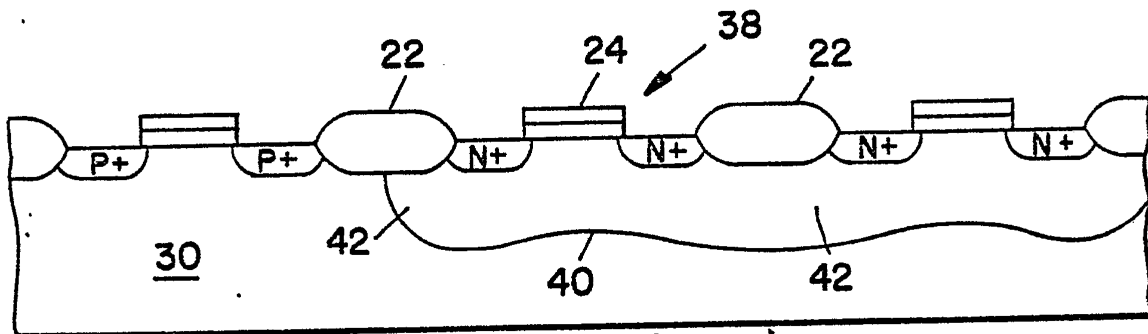

FIG _ 2

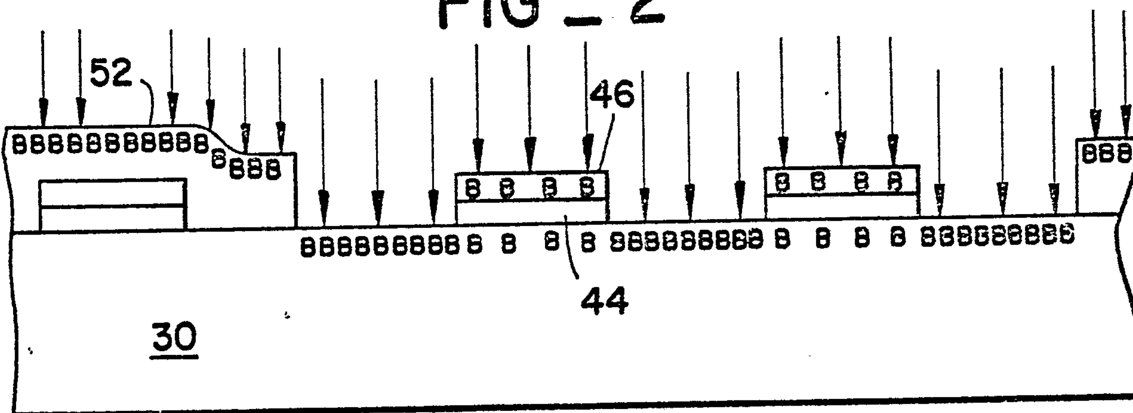

FIG _ 3

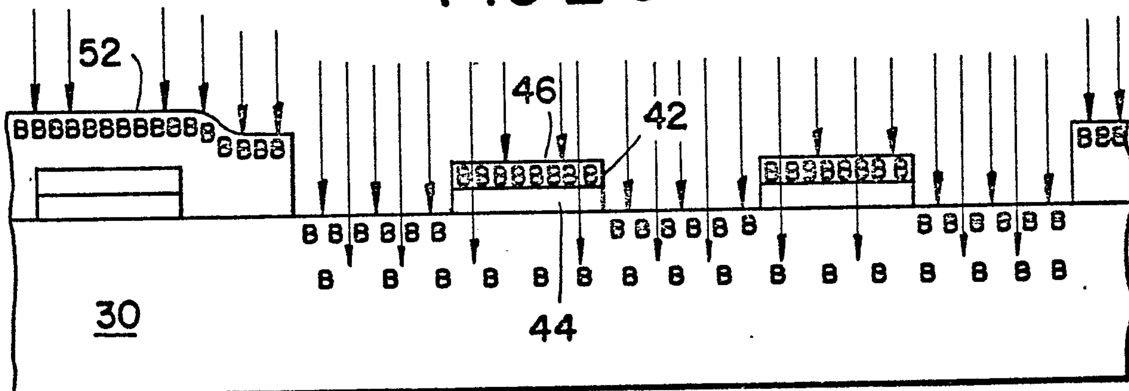

FIG _ 4

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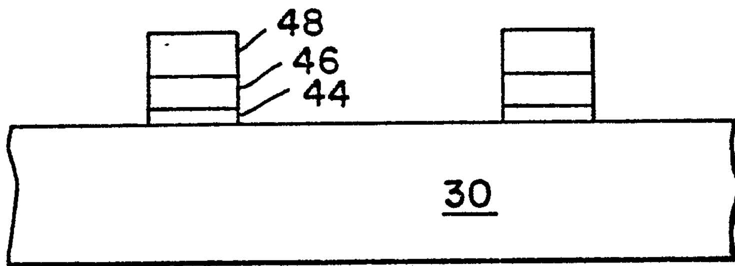

FIG _ 5

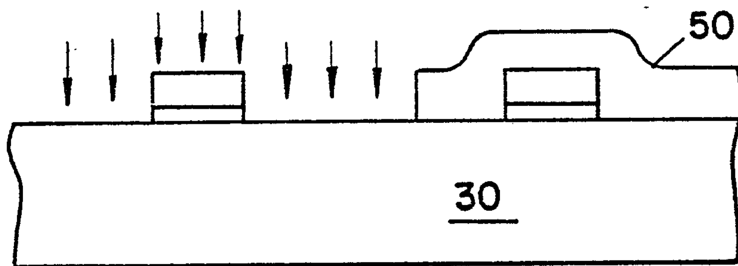

FIG _ 6

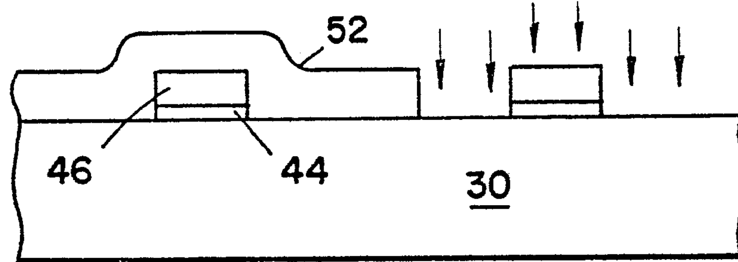

FIG _ 7

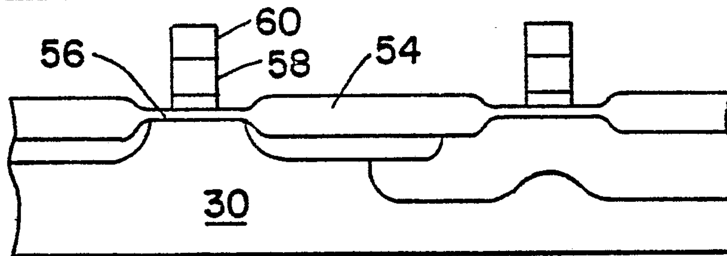

FIG _ 8

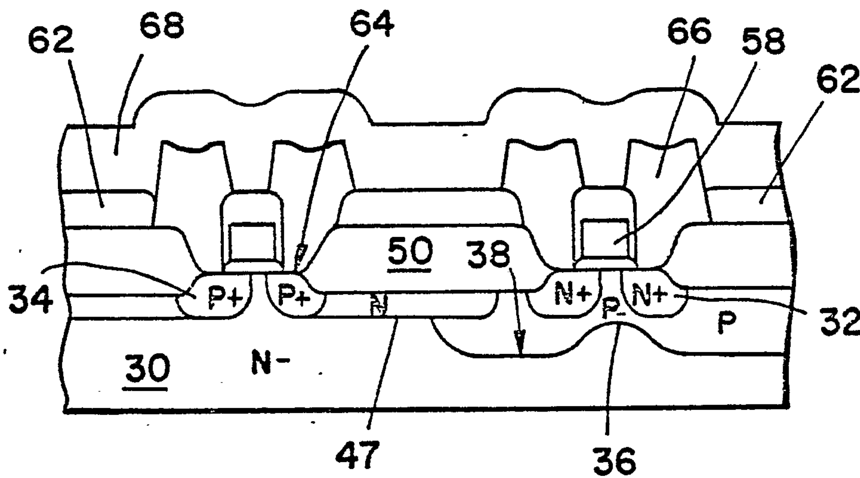

FIG _ 9

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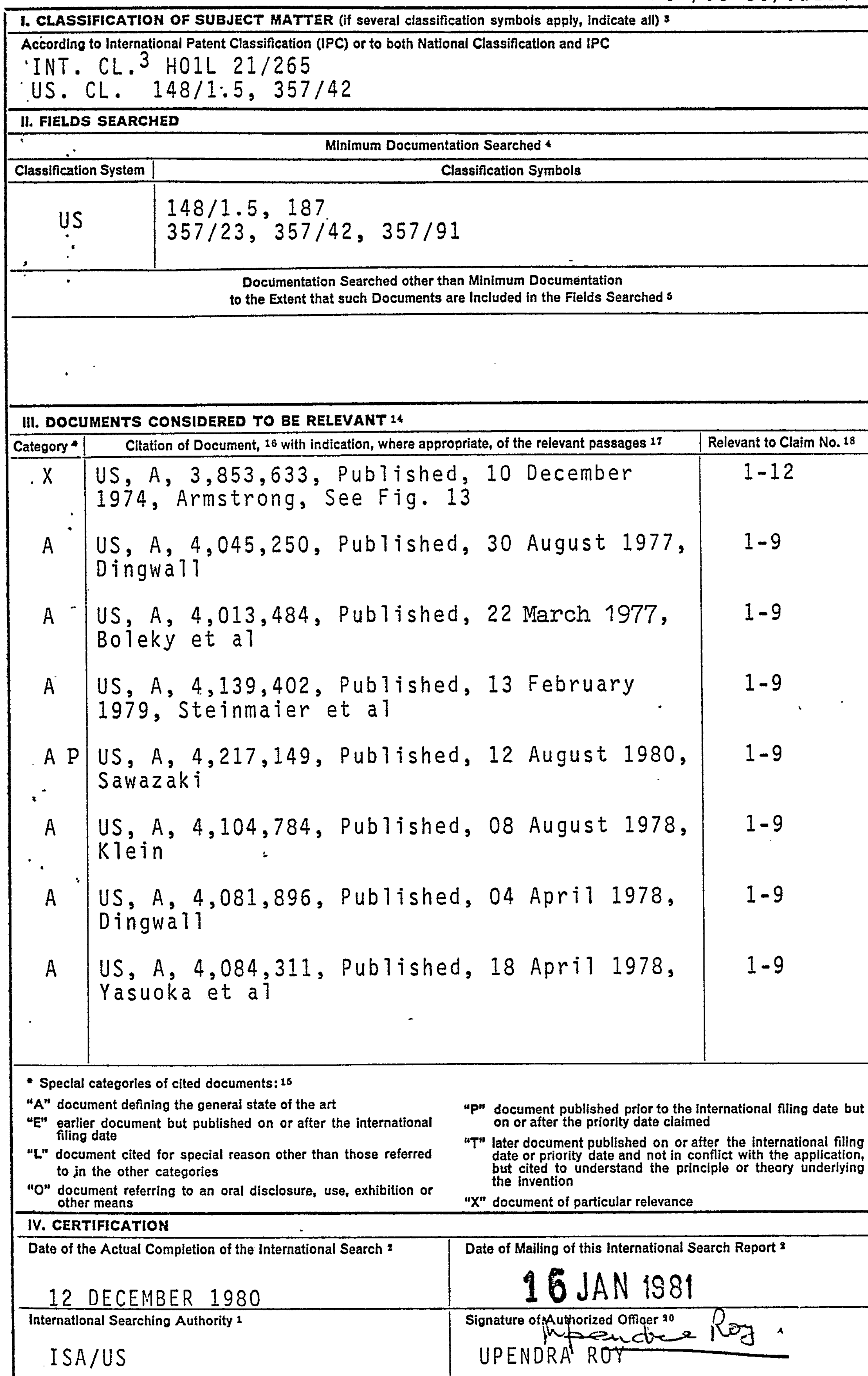

INTERNATIONAL SEARCH REPORT

International Application No PCT/US 80/01154

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

INT. CL.[3] H01L 21/265
US. CL. 148/1.5, 357/42

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
US	148/1.5, 187 357/23, 357/42, 357/91

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
X	US, A, 3,853,633, Published, 10 December 1974, Armstrong, See Fig. 13	1-12
A	US, A, 4,045,250, Published, 30 August 1977, Dingwall	1-9
A	US, A, 4,013,484, Published, 22 March 1977, Boleky et al	1-9
A	US, A, 4,139,402, Published, 13 February 1979, Steinmaier et al	1-9
A P	US, A, 4,217,149, Published, 12 August 1980, Sawazaki	1-9
A	US, A, 4,104,784, Published, 08 August 1978, Klein	1-9
A	US, A, 4,081,896, Published, 04 April 1978, Dingwall	1-9
A	US, A, 4,084,311, Published, 18 April 1978, Yasuoka et al	1-9

* Special categories of cited documents: [15]

"A" document defining the general state of the art
"E" earlier document but published on or after the international filing date
"L" document cited for special reason other than those referred to in the other categories
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but on or after the priority date claimed
"T" later document published on or after the international filing date or priority date and not in conflict with the application, but cited to understand the principle or theory underlying the invention
"X" document of particular relevance

IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
12 DECEMBER 1980	16 JAN 1981
International Searching Authority [1]	**Signature of Authorized Officer [20]**
ISA/US	Upendra Roy UPENDRA ROY

International Application No. PCT/US 80/01154

FURTHER INFORMATION CONTINUED FROM THE SECOND SHEET

A	US, A, 3,983,620, Published, 05 October 1976, Spadea	10-12
A	US, A, 3,615,938, Published, 26 October 1971, Tsui	10-12

V.☐ OBSERVATIONS WHERE CERTAIN CLAIMS WERE FOUND UNSEARCHABLE [10]

This international search report has not been established in respect of certain claims under Article 17(2) (a) for the following reasons:

1.☐ Claim numbers ...., because they relate to subject matter [12] not required to be searched by this Authority, namely:

2.☐ Claim numbers ...., because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out [13], specifically:

VI.☐ OBSERVATIONS WHERE UNITY OF INVENTION IS LACKING [11]

This International Searching Authority found multiple inventions in this international application as follows:

1.☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims of the international application.

2.☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims of the international application for which fees were paid, specifically claims:

3.☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claim numbers:

Remark on Protest

☐ The additional search fees were accompanied by applicant's protest.

☐ No protest accompanied the payment of additional search fees.