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Strandberg, Jr. et al.

[11] **3,721,809**

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[54] **AUTOMATIC THREAD COUNTER AND CONTROLLER FOR FABRIC PROCESSING APPARATUS**

[75] Inventors: **Charles F. Strandberg, Jr.; Robert C. Strandberg,** both of Greensboro; **James M. Gee,** Silver City, all of N.C.

[73] Assignee: **Strandberg Engineering Laboratories, Inc.,** Greensboro, N.C.

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[52] **U.S. Cl.** .....**235/92 PD,** 235/92 V, 250/219 R, 235/92 R, 235/92 CC, 235/92 TF

[51] **Int. Cl.** **G07c 3/10**

[58] **Field of Search**.....235/98 C, 92 PD, 92 EA, 235/92 PK, 92 CC, 92 V, 92 DN, 92 TF; 250/219 R, 217 R, 217 SS; 356/242

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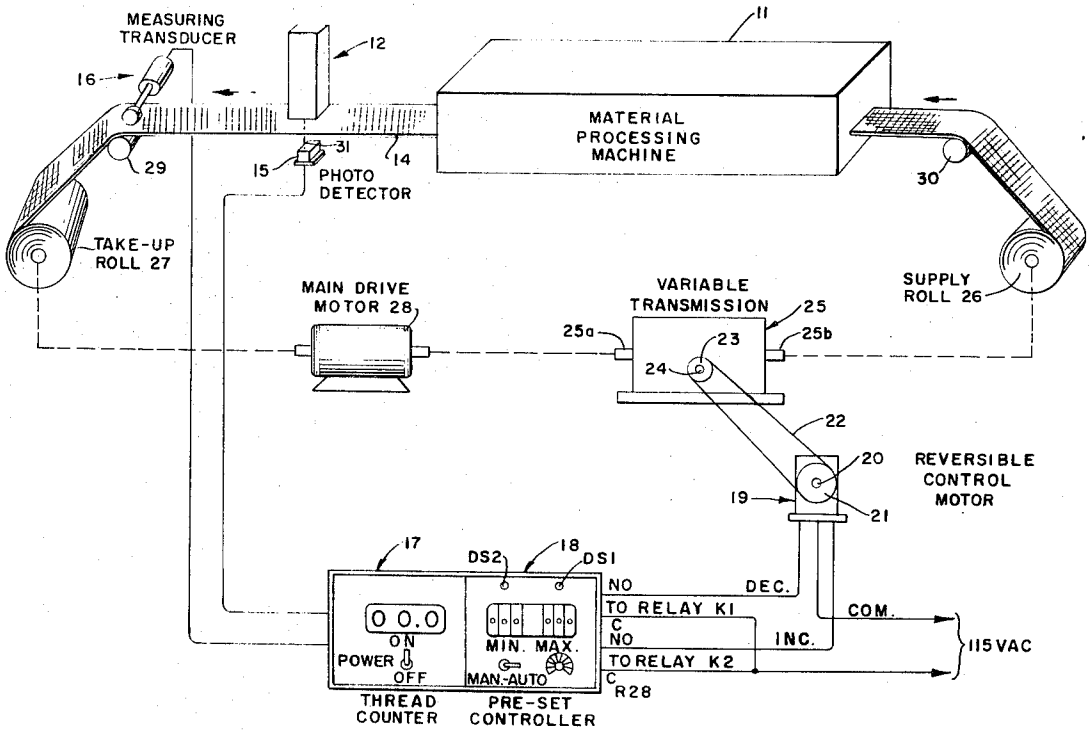
Primary Examiner—Maynard R. Wilbur
Assistant Examiner—Joseph M. Thesz, Jr.
Attorney—Munson H. Lane and Munson H. Lane, Jr.

[57] **ABSTRACT**

Apparatus for counting threads in a moving fabric comprising a laser source of light radiations for direct penetration of the fabric, a photo detector activated by the light radiations passing through the fabric for producing electrical signal variations caused by successive threads passing through the light radiations and a thread counter actuated by the electrical signal variations. A fabric length measuring transducer is provided to measure the fabric while the threads are being counted and to produce length related pulses which are used to control the thread counter so that the thread counter will indicate threads per unit length of fabric. Automatic control means is provided which will adjust the speed of a fabric supply roll relative to a fabric delivery roll in accordance with the thread count per unit length indicated by the thread counter in order to stretch or shrink the fabric and thereby adjust the threads per unit length of the fabric to be within a preselected minimum and maximum.

7 Claims, 5 Drawing Figures



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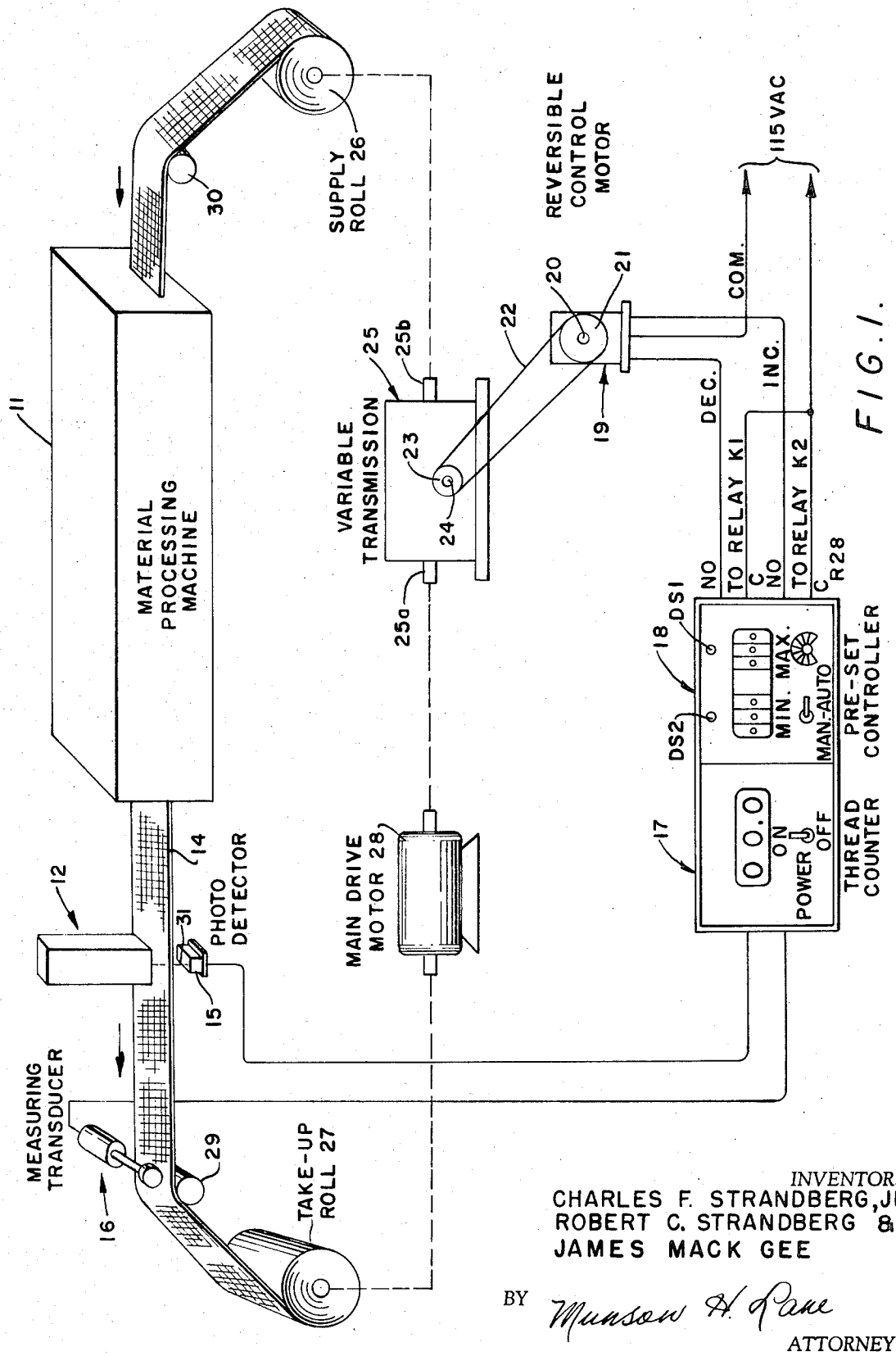

FIG. 1.

INVENTORS
CHARLES F. STRANDBERG, JR.
ROBERT C. STRANDBERG &
JAMES MACK GEE

BY Munson H. Pare
ATTORNEY

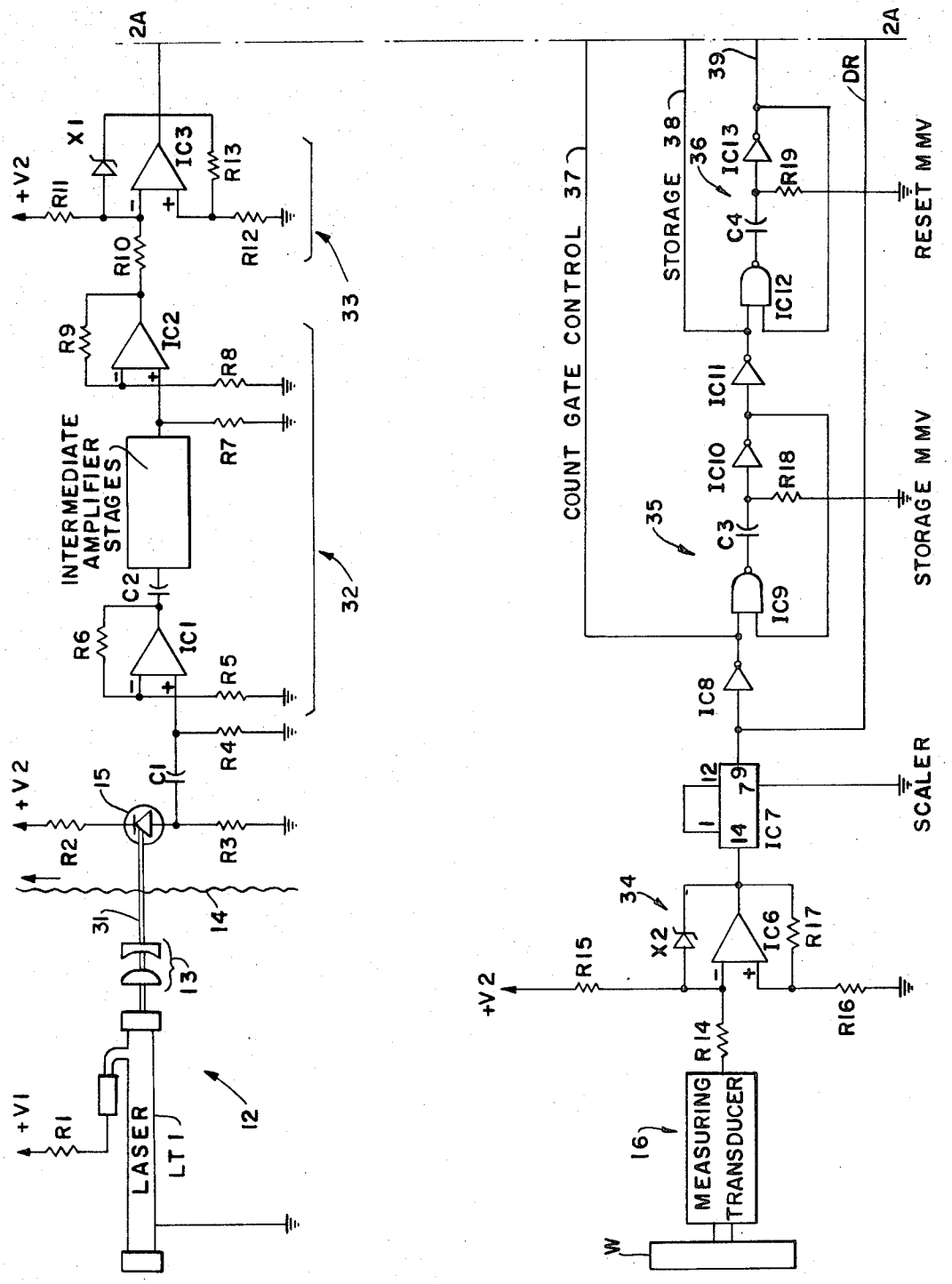

FIG. 2A.

INVENTORS
CHARLES F. STRANDBERG, JR.
ROBERT C. STRANDBERG &
JAMES MACK GEE

BY Munson H. Dane
ATTORNEY

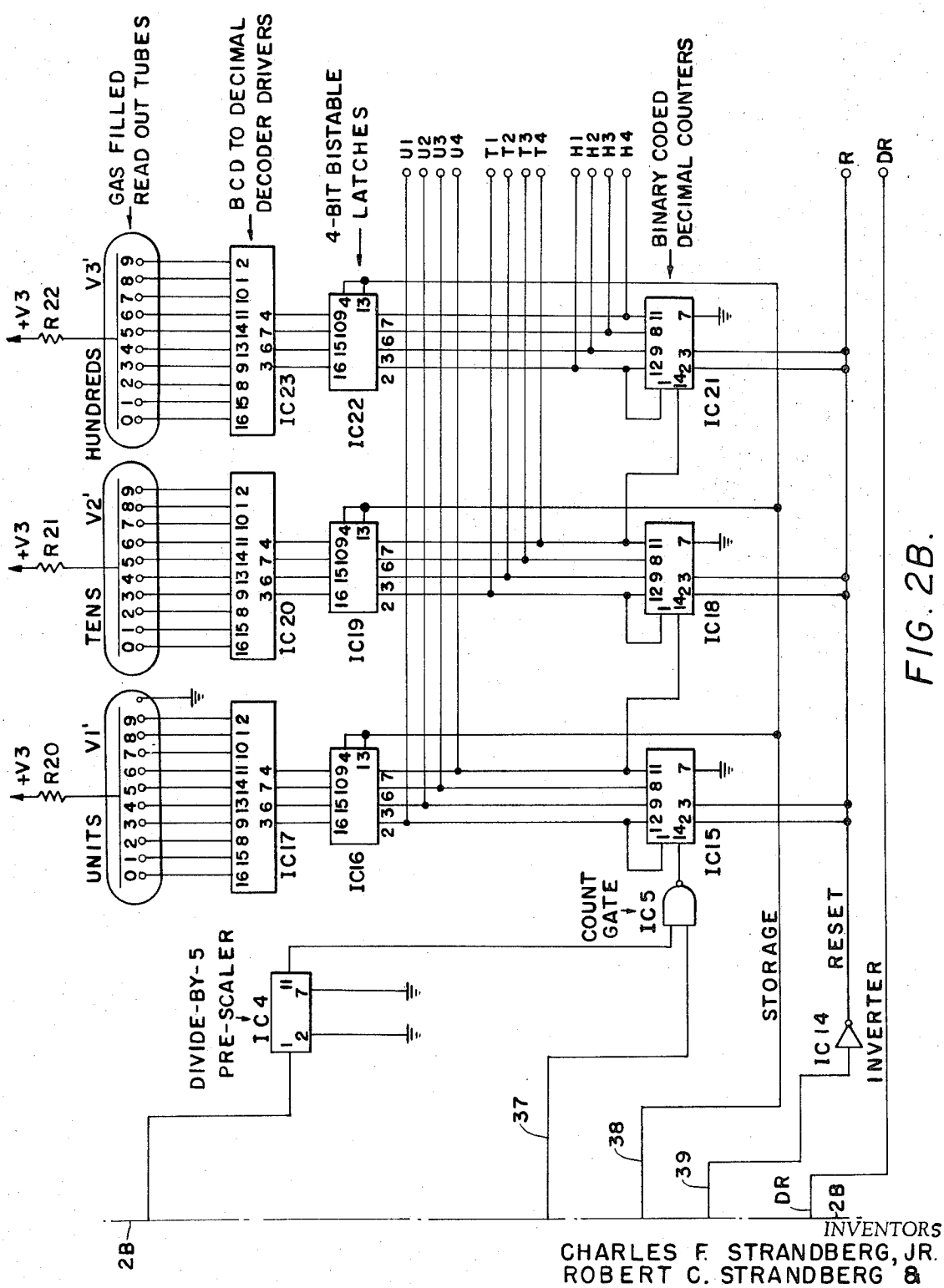

FIG. 2B.

INVENTORS
CHARLES F. STRANDBERG, JR.
ROBERT C. STRANDBERG &
JAMES MACK GEE

BY Munson H. Pane
ATTORNEY

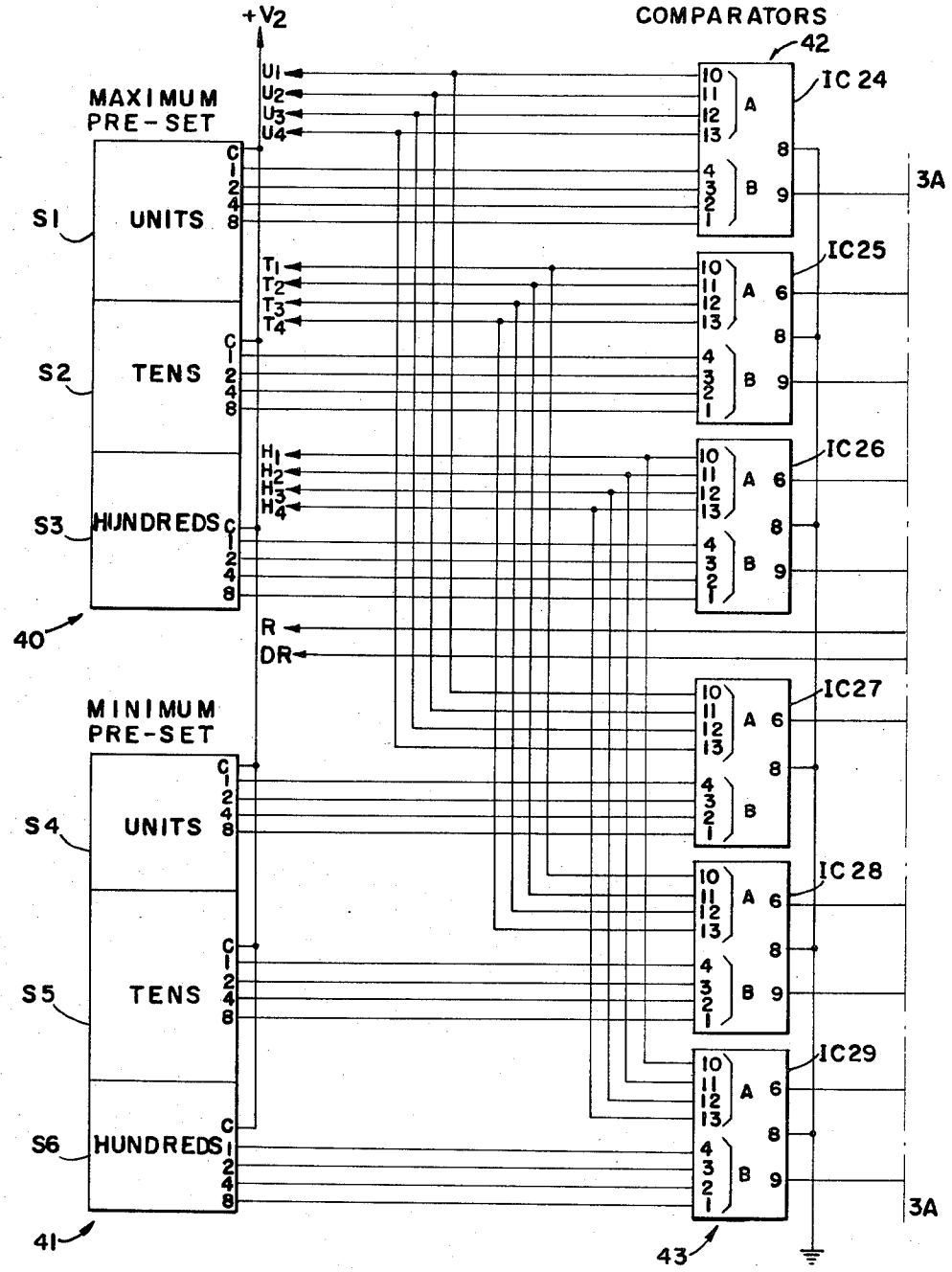

FIG. 3A.

INVENTORS
CHARLES F. STRANDBERG, JR.
ROBERT C. STRANDBERG &
JAMES MACK GEE

BY Munson H. Lane
ATTORNEY

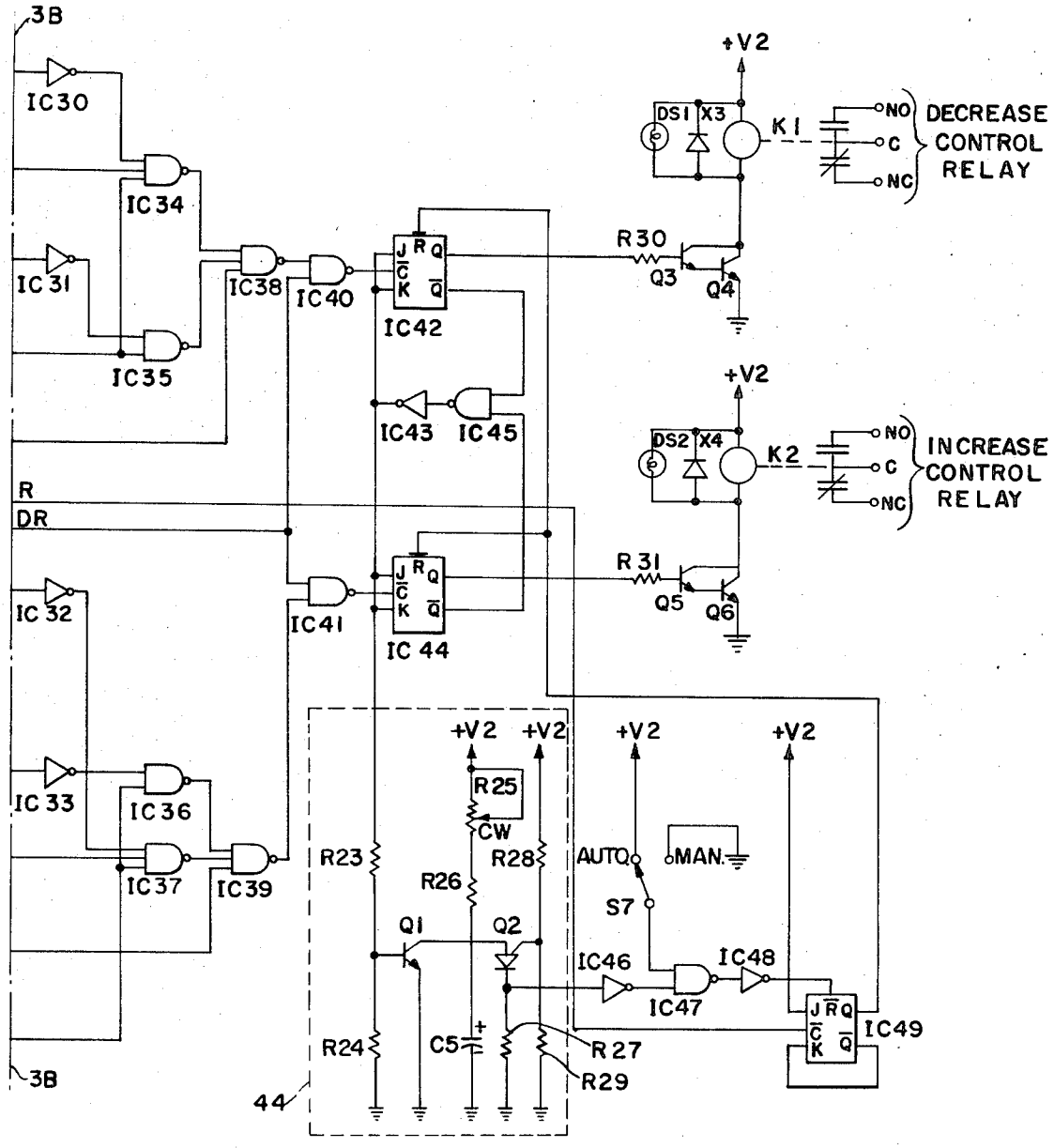

FIG. 3B.

INVENTORS
CHARLES F. STRANDBERG, JR.
ROBERT C. STRANDBERG &
JAMES MACK GEE

BY Munson H. Lane
ATTORNEY

AUTOMATIC THREAD COUNTER AND CONTROLLER FOR FABRIC PROCESSING APPARATUS

The invention relates to improved apparatus for counting the threads in a moving fabric and to an automatic controller which optionally may be used in conjunction with the improved thread counting apparatus to automatically adjust a fabric processing machine to maintain the required thread count per unit length within certain preset limits.

It is an object of the invention to provide an improved thread counting apparatus utilizing a laser source of light radiations for direct penetration of the fabric in conjunction with a photoelectric detector which is activated by the light passing through the fabric for producing electric signal variations as successive threads pass through the light, and a thread counter which is actuated by the electrical signal variations.

It is a further object of the invention to provide improved apparatus for counting the threads per unit length in a moving fabric which is capable of providing a count reading averaged over an extended distance to obtain a reading stability sufficiently high to permit automatic control.

it is another object of the invention to provide improved apparatus for counting the threads per unit length in a moving fabric which apparatus includes a thread counting channel and a fabric length measuring channel and a thread counter which produces a readout indication of threads per unit length averaged over a preselected length, and wherein the thread counting channel and the length measuring channel include pre-scaler devices which divide the thread count and the length respectively by predetermined whole numbers.

It is a further object of the invention to provide an improved thread counting apparatus including a three decade decimal counter with storage wherein each decade of the counter is a binary coded decimal counter.

It is a further object of the invention to provide an automatic controller for a material processing machine having a supply roll and a take up roll on opposite sides of the processing machine and drive means for driving the supply roll and the take up roll including means for varying the speed of the supply roll relative to the take up roll, the automatic controller having means for presetting minimum and maximum limits of threads per unit length and means for comparing the actual count of threads per unit length as determined by the thread counter portion of this invention with the preset minimum and maximum limits and producing control signals for adjusting the means for varying the speed of the supply roll relative to the take up roll such that the fabric will be stretched or shrunk as required to keep the number of threads per unit length of the fabric within the pre set limits.

It is a further object of the invention to provide the automatic controller with means for providing timed correction pulses when required to alter the input speed of fabric entering a processing machine with reference to the output speed of the fabric leaving the processing machine.

These and other objects, advantages and novel features will be apparent from the following description and the accompanying drawings.

In the drawings:

FIG. 1 is a diagrammatic view illustrating a fabric processing machine and the automatic thread counter and controller of this invention positioned for use in conjunction therewith;

FIGS. 2A and 2B taken in sequence are schematic diagrams showing the portion of the invention relating primarily to apparatus for counting the threads per unit length of the fabric; and

FIGS. 3A and 3B taken in sequence are schematic diagrams showing the pre-set controller portion of the invention. The output circuits shown on the right hand side of FIG. 2B feed into similarly marked circuits shown in FIG. 3A.

GENERAL DESCRIPTION

The following describes the basic operating theory of the invention used to measure and display in digital form the number of threads per unit length of textile fabric during processing and, if desired, to automatically adjust the processing machine to maintain the required thread count within certain preset limits. The invention utilizes a low-power, continuous-wave, Helium-Neon laser to provide intense and highly collimated light radiation for direct penetration of the fabric. Several advantages which accrue from the use of the laser are (1) high intensity — permitting penetration of heavy and highly dense fabrics; (2) collimated (unidirectional) radiation — eliminating stringent fabric positioning requirements since beam is in focus at all points between lens system and photo detector; (3) monochromatic (one color) radiation— providing optimum coupling to photo detector; and (4) absence of any attendant heat — eliminating any possibility of fabric burning.

FIG. 1 shows the invention applied to a typical fabric processing machine **11**. The laser unit **12**, complete with required beam-shaping lens system **13** (see FIG. 2A), is mounted on one side of the fabric **14**. A photo detector **15** is similarly positioned directly opposite the fabric **14** in line with the laser **12**. A measuring transducer **16** is located near the laser **12**. This transducer **16** can be either surface driven, as shown, using contact wheels directly on the fabric, or, if desired, can be shaft driven from some existing roll. The measuring transducer **16** and photo detector **15** are both connected to the thread counter **17**.

If automatic control is desired, a preset controller **18** can optionally be connected to the thread counter. This output of the preset controller is connected to a reversible control motor **19**, the shaft **20** of which is attached via a suitable drive, such as a belt **22** and pulleys **21, 23**, to the speed adjusting screw **24** of the existing variable-speed transmission **25** connected in the drive shaft between the main drive motor **28** and the feed roll **26**. This transmission **25** is normally used to vary the speed of the input feed roll **26** with reference to the speed of the delivery roll **27** which is directly driven by the main drive motor **28** to introduce stretch or shrinkage in the fabric **14** within the processing machine **11**. The addition of the preset controller **18** and reversible control motor **19** provides automatic means for controlling the stretch or shrinkage and, hence, the number of threads per unit length of material leaving the processing machine **11**.

Functional Analysis — Thread Counter

Referring to the thread counter functional logic diagram shown in FIGS. 2A and 2B in sequence, a laser tube LT1, with current limiting resistor R1, powered from a high voltage source V1, provides the necessary light radiation source as discussed above. After transmission through an appropriate beam shaping lens system 13 the resultant beam 31 is passed through the fabric 14 to the photo detector 15. The purpose of the lens system 13 is to convert the approximate 3mm circular laser beam into a thin, elongated slit of light approximately 0.1mm by 6mm. This slit of light is aligned parallel to the threads to be counted, so that alternately, the beam passes between adjacent threads and is then blocked by each thread. The lens system 13 may be made adjustable so that the width of the slit can be varied. While this feature offers no advantage on woven cloth, it does permit accurate counting of courses per inch in knitted fabric in which, one course may appear as several closely spaced threads. The photo detector 15 can be any one of many different types of photo transistors or diodes, but a PIN photo diode is preferred due to its extremely short response time, thereby permitting overall system operation at very high fabric speeds.

Bias current for the photo detector 15 is provided by resistors R2 and R3 in series with the photo detector 15 from voltage source V2 and ground. As the conduction of the photo detector varies in response to the light incident upon it, the resultant varying voltage across resistor R3 is fed via capacitor C1 to resistor R4 and into the plus (non-inverting) input of amplifier IC1. The action of resistor R3, capacitor C1, and resistor R4 is to provide zero restoration of the photo diode signal current. This ensures that only the varying voltage present across resistor R3, and not the d-c level, is passed to the input of amplifier IC1. The inclusion of the zero restoration circuit prevents the amplifier IC1 from amplifying the ambient radiation level, which would, most certainly, saturate the final stages. Therefore, no adjustment of the amplifier IC1 is required for various fabric colors and densities.

Amplifier IC1, along with gain setting resistors R5 and R6, forms the first stage of the high-gain, wideband amplifier 32. The overall amplifier design must provide adequate gain and band width to ensure that the smallest thread, traveling at the maximum speed, will fully saturate the final amplifier stage. In the preferred design, the amplifier 32 consists of four identical low-gain stages. The overall gain is, however, quite high, being the individual stage gain raised to the fourth power.

The output of the final amplifier stage IC2 is connected, via resistor R10, to the negative (inverting input) of amplifier IC3. Amplifier IC3, along with resistors R10, R11, R12, and R13, and zener diode X1, comprises a standard high-gain comparator 33. This comparator 33 is included to provide low-level and noise-free count pulses to the remaining counter circuits. Operation of the comparator is as follows: The inverting input of amplifier IC3 is at virtual ground potential. When the net current into this input is negative, the comparator output switches positive to the zero or reverse voltage of zener diode X1. When the net input current goes positive, the comparator output goes slightly negative to the forward diode drop of X1, approximately 0.6 volt. With a suitable constant positive input current through resistor R11, the comparator output will switch positive each time the output of amplifier IC2 goes sufficiently negative, nearly to saturation, and will switch negative when the output of amplifier IC2 swings back positive. Resistors R12 and R13 provide a slight amount of hysteresis to the comparator switching. This eliminates false counting due to noise spikes riding the signal line. The resultant output of the comparator 33 is a noise-free square-wave signal, switching in amplitude from $-0.6V$ to $+V_{X1}$ for each thread sensed by the photo detector 15.

The output of the comparator 33 is connected directly to a divide-by-5 pre-scaler, IC4, included to scale down the count to one-fifth. The purpose of this scaler will be made clear after the measuring transducer 16 and its associated circuitry is discussed. In the meantime, the resultant scaled-down count is next fed to the count gate IC5, the output of which feeds the input of IC15. IC15, IC18, and IC21, are binary coded decimal (BCD) counters (Texas Instruments Type SN7490, or equiv.). The binary coded decimal outputs of each of these are connected to the inputs of IC16, IC19, and IC22. These devices are 4-bit bistable latches used as counter storage elements (Texas Instruments Type SN7475, or equiv.). The stored BCD outputs of each of these are connected to the inputs of IC17, IC20, and IC23. These devices are BCD-to-decimal decoder/drivers used to convert the BCD code from the 4-bit bistable latches into 10-line decimal outputs (Texas Instruments Type SN7441A, or equiv.). The stored 10-line decimal outputs of each of these are connected to the appropriate number cathodes of gas-filled readout tubes V1', V2', and V3'. The anodes for each of these are connected, via resistors R20, R21, and R22 to a high voltage source V3. Also, an internal decimal point cathode on the left inside of the units tube is connected to ground and is, therefore, lit continuously. The decimal point was added to provide a resolution of ± 0.1 thread per inch. Therefore, the counter's units digit must represent tenths of threads. In addition to the above connections, the BCD outputs of IC15, IC18 and IC21 are brought out for connection to the Pre-Set controller, if automatic control is desired. With the exception of the divide-by-5 pre-scaler IC4, this completes the discussion of the counting circuits.

A measuring transducer 16 is required to provide means for control of the counter operating mode—that is to provide dimension related pulses for control of the count gate, storage, and reset circuitry. For convenience, the transducer was designed to deliver one pulse per revolution and preferably comprises a fixed magnetic reed switch and a shaft driven magnet. Also, for convenience, the transducer was fitted with a surface measuring wheel W of suitable circumference. A 10-inch circumference was chosen as being dimensionally compatible with the transducer and logically compatible with the desired end result.

Referring again to FIG. 2A, the output from the transducer 16 is fed, via resistor R14, to a standard high-gain comparator 34. Operation of the comparator 34 is similar to the operation of the comparator 33 following the laser amplifier. The resultant output of the

comparator 34, then, is a noise-free square wave signal switching in amplitude from −0.6V to $+V_{X2}$ for each rotation of the transducer measuring wheel W—that is, for each 10 inches of fabric travel.

The output from comparator 34 is connected directly to a divide-by-6 counter control scaler IC7. This device is a standard divide-by-12 counter connected to provide divide-by-6 operation (Texas Instruments Type SN7492, or equiv.). The purpose of this device is to provide separate count and storage-reset modes of operation for the digital counter circuitry. The modulus of 6 was arbitrarily selected to provide a count mode five times as long as the storage-reset mode. Since each pulse into IC7 from the comparator 34 is proportional to 10 inches of fabric travel, this gives a count mode interval of 50 inches and a storage-reset mode interval of 10 inches.

With the count mode of 50 inches arbitrarily set, as described above, and with the original requirement that the counter units digit represent tenths of threads, the purpose of the divide-by-5 pre-scaler IC4 is now clear. The required resolution of ±0.1 thread per inch alone would require a minimum count mode of 10 inches. With the count mode extended to 50 inches, this obviously requires that the counter input pulses be scaled down to one-fifth the actual thread rate.

It should be noted, however, that a count mode other than 50 inches could have been selected, in which case IC4 would have to have had some other modulus. As an example, if the count mode has been selected equal to the storage-reset mode with the divide-by-6 scaler IC7 changed to a divide-by-2 scaler, the resultant count mode of 10 inches would eliminate the requirement for IC4 completely. However, with the circuit as shown, IC4 is a binary coded decimal (BCD) counter element (Texas Instruments Type SN7490, or equiv.) connected to provide divide-by-5 operation.

Returning now to the divide-by-6 counter control scaler IC7, the output signal at pin 9 is low (logic level 0) during the count mode (five revolutions of W), and high (logic level 1) during the storage-reset mode (one revolution of W). While this output is low, the inverter IC8 presents a high to both the count gate IC5 and to the input of the storage monostable multivibrator 35, comprised of IC9, capacitor C3, resistor R18, and IC10. Operation of the count gate IC5 is such that if either input goes low, the output will go high. With the count gate control input line 37 from the output of inverter IC8 high, the output of the count gate IC5 will be the inverted output of IC4, and count pulses will enter IC15. However, when the count mode ends and the output of the counter control scaler IC7 goes high, inverter IC8 will present a low to the count gate IC5, thereby causing its output to go high and stop count pulses from entering the binary coded decimal counter IC15. At this same instant, the transition from high to low at the output of inverter IC8 triggers the storage multivibrator 35 and the output of IC10, normally high, goes low for a period equal approximately to the product of capacitor C3 and resistor R18. In practice, this time is approximately 50×10^{-9} seconds (50 nanoseconds). The inverter IC11 inverts this low-going pulse and delivers a high-going pulse, via the storage line 38, to each of the 4-bistable latches, IC16, IC19, and IC22. During this pulse, the BCD data present on input pins 2, 3, 6 and 7 of each of the 4-bistable latches is transferred, respectively, to the output pins 16, 15, 10 and 9. The decoder/drivers IC17, IC20 and IC23 immediately track the new BCD input data and convert it to 10-line decimal output with the appropriate output pin on each decoder/driver switching to ground, thereby causing a new digital readout to appear on the readout tubes V1′, V2′ and V3′.

When the high-going 50 nanosecond pulse at the output of inverter IC11 is complete and the output of IC11 goes low, thereby ending the storage pulse, this low-going transition triggers the reset monostable multivibrator 36. This reset multivibrator comprised of IC12, capacitor C4, resistor R19 and IC13, then delivers a low-going pulse, also approximately 50 nanoseconds wide, to the input of the inverter IC14. The output of IC14, a high-going 50 nanosecond pulse, is fed via the reset line to each of the binary coded decimal (BCD) counters IC15, IC18 and IC21, thereby resetting the output of each to zero.

When the storage-reset mode ends and the output of the counter control scaler IC7 goes low for the next five revolutions of W, the output of inverter IC8 goes high, opening the count gate IC5, and count pulses again begin entering IC15. The cycle will repeat continuously with the resultant display on the readout tubes in threads per inch, being updated every 60 inches.

Functional Analysis — Pre-Set Controller

Referring now to FIGS. 3A and 3B the pre-set controller 18 will be described. The required input data from the thread counter 17 to the pre-set controller 18 consists of the BCD data from the three binary coded decimal counters IC15, IC18, and IC21, output from the divide-by-6 counter control scaler IC7, labeled DR for data ready, and the reset output from IC14, labeled R.

The BCD data from the thread counter 17 is connected, as shown, to the A inputs of six 4-bit binary comparators, IC24 – IC29 (National Semiconductor Type DM8200, or equiv.). Switches S1 – S6 are connected, as shown to the B inputs of the comparators. Each of these switches is a binary coded decimal switch with 10 positions — reading on the dial 0 through 9, but presenting a BCD output (1–2–4–8) equivalent to the BCD output of each of the binary coded decimal counters in the thread counter 17.

Each comparator, IC24 – IC29, continually compares the two binary numbers A and B, and determines (1) whether A is less than B, (2) whether A equals B, or (3) whether A is greater than B. The following truth table shows the output states for the above three conditions:

Input Condition	Pin 6 OUtput	Pin 9 OUtput
A < B	Low	High
A = B	High	High
A > B	High	Low

The above states are only valid as long as pin 8 on each comparator is kept at a logic level 0. Pin 8 is an optional strobe used to set both outputs low. It is not used and so is grounded to ensure the logic 0 required for normal operation.

Observation shows that the comparators, IC24 – IC29, are arranged in two groups 42, 43 of three each,

corresponding to the maximum pre-set and minimum pre-set switch groups 40,41. Comparators IC24 – IC26, along with inverters IC30 and IC31 and nand gates IC34, IC35, IC38 and IC40 are employed to determine whether the number on the thread counter readout is (1) less than or equal to the number set on the maximum pre-set switches, S1 – S3, or (2) greater than the pre-set number. The comparators 42, 43 make the initial comparison on a per-digit basis, determining separately, at their outputs per the truth table, the comparison of the units, tens, and hundreds digits. The remaining inverters and gates determine, based on the combined comparator outputs, whether a correction is required, in the event that the combined A inputs are greater than the combined B inputs, or whether no correction is required, should the combined A inputs be equal or less than the combined B inputs. The actual decision to make correction or not to is allowed only when the thread counter 17 has entered the storage-reset mode. This is evidenced by the DR input to the pre-set controller 18 going high, enabling nand gate IC40. If the number on the thread counter readout, at that instant, is greater than the number set on the maximum pre-set switches, 40, the output of nand gate IC38 will go high. The presence of two highs on the inputs of nand IC40 causes its output to drop from a high to a low. This low-going transition on the C input of J-K flip-flop, IC42 toggles this flip-flop, resulting in operation of the decrease control relay K1. Before examining the operation of the remainder of the circuit, activated by the toggling of the J-K flip-flop IC42, further explanation of the comparator circuitry is in order.

It should be noted that the function of nand gate IC40 is to gate or enable the data present at the output of nand gate IC38 into the decrease control flip-flop IC42 at exactly the instant that the storage line in the thread counter 17 is pulsed. At this instant and only then is the comparison data at the output of nand gate IC38 valid, for it is indicative of the new readout number on the thread counter 17 compared to the number set on the maximum pre-set switches 40.

If, at the start of the thread counter storage-reset mode, the number of the thread counter readout was equal to or less than the maximum pre-set number, the output of nand gate IC38 would have been low. Therefore, even with the DR line going high, the presence of the low on the input of nand gate IC40 from nand gate IC38 would have kept the output of nand gate IC40 high and decrease control flip-flop IC42 would not have been toggled.

Operation of the comparators 43 and gates associated with the minimum pre-set switches, S4 – S6, is identical to that of the maximum pre-set circuitry with the exception that the output connections (pins 6 and 9) on each comparator are reversed. Examination of the comparator truth table in light of the required logic for the minimum pre-set circuitry will show that the operation and required gating is identical. Here, the comparators IC27 – IC29, inverters IC32 and IC33 and associated gates IC36, IC37, IC39 and IC41 are required to determine whether the number on the thread counter readout is (1) greater than or equal to the number set on the minimum pre-set switches S4 – S6, or (2) less than the pre-set number. If, at the start of the storage-reset mode in the thread counter, the number on the thread counter readout is less than the minimum pre-set number, the output of the nand gate IC39 will be high. With the DR line going high, resulting in both inputs to the nand gate IC41 being high, the output of nand gate IC41 will go low, the increase control J-K flip-flop IC44 will be toggled, resulting in operation of the increase control relay K2. If, however, at the start of the storage-reset mode in the thread counter 17, the number on the thread counter readout was equal to or greater than the minimum pre-set number, the output of the nand gate IC39 would have been low. Therefore, even with the DR line going high, the presence of the low on the input of the nand gate IC41 from nand gate IC39 would have kept the output of the nand gate IC41 high and the increase control flip-flop IC44 would not have been toggled.

While it has been stated that the output of either nand gate IC38 or nand gate IC39 will be high at the start of the storage-reset mode if a correction is required or low should no correction be required, and that the function of these gates along with the other interconnected gates, and inverters connected to the comparators was to determine the comparison of the combined A inputs to the combined B inputs the actual operation of these circuit elements has not been explained. Let us, then, examine the outputs of comparators IC24 – IC26 in order to understand the function of inverters IC30 and IC31, nand gates IC34 and IC35, and finally nand gate IC38. Note that each of the comparators is only capable of making a comparison of one digit of the thread counter to one digit of the pre-set switch. The ultimate output of nand gate IC38 must, however, be the result of the combined comparison in decade order of comparators IC24, IC25 and IC26. Therefore, IC26, the hundreds comparator, must have precedence over IC25, the tens comparator and IC24, the units comparator. In like manner, IC25 must have precedence over IC24. The inverters and gates force this rank order procedure in accordance with the following logic steps at the instant of comparison:

1. If pin 9 on comparator IC26 is low, the output of nand gate IC38 must go high, the required condition for correction. (Pin 9 on comparator IC26 being low indicates that the hundreds digit on the thread counter readout is greater than the number set on the maximum pre-set hundreds switch S3. No consideration of the tens and units comparators is necessary and control action to decrease the thread counter reading is required.) or
2. If pin 9 on comparator IC26 is high and pin 6 on IC26 is low, output of nand gate IC38 must go low, the required condition for no correction. (Pin 9 being high and pin 6 being low indicates that the hundreds digit on the thread counter readout is less than the number set on the maximum pre-set hundreds switch, S3. No consideration of the tens and units comparators is necessary and no control action is required.) or
3. If both pin 9 and pin 6 on comparator IC26 are high, this condition allows the tens comparator IC25 to make comparison. (A high on both pin 9 and pin 6 indicates that the hundreds digit on the thread counter readout is exactly equal to the number set on the maximum pre-set hundreds switch S3. A decision not to activate the decrease

control cannot be made without considering IC25, the tens comparator.) With both pin 9 and pin 6 on comparator IC26 high, if pin 9 on comparator IC25 is low, output of nand gate IC38 must go high, as in Step 1. (With the hundreds digits equal, a low on pin 9 of comparator IC25 indicates that the tens digit on the thread counter 17 is greater than the number set on the maximum pre-set tens switch S2. No consideration of the units comparator is necessary, and control action to decrease the thread counter reading is required.) or

4. With both pin 9 and pin 6 on comparator IC26 high, if pin 9 on comparator IC25 is high and pin 6 on comparator IC25 is low, output of the nand gate IC38 must go low, as in Step 2. (With the hundreds digits equal, a high on pin 9 and a low on pin 6 of comparator IC25 indicates that the tens digit on the thread counter readout is less than the number set on the maximum pre-set tens switch S2. No consideration of the units comparator is necessary and no control action is required.) or
5. If pins 9 and 6 on both comparators IC26 and IC25 are high, this condition allows the units comparator IC24 to make comparison. (A high on pins 9 and 6 on both comparators IC26 and IC25 indicates that both the hundreds and tens digit on the thread counter readout are exactly equal to the numbers set on the maximum pre-set hundreds and tens switches S3 and S2. A decision not to activate the decrease control cannot be made without considering IC24, the units comparator.) With the above conditions, if pin 9 on comparator IC24 is low, output of the nand gate IC38 must go high as in Step 1. (With the hundreds and tens digits equal, a low on pin 9 of comparator IC24 indicates that the units digit on the thread counter is greater than the number set on the maximum pre-set units switch S1. Control action to decrease the thread counter reading, is therefore, required.) or
6. With pins 9 and 6 on both comparators IC26 and IC25 high, if pin 9 on IC24 is high, output of nand gate IC38 must go low, the condition for no correction. (It is of no consequence whether pin 6 on comparator IC24 is high or low, since pin 9, being high, indicates that the units digit on the thread counter readout is equal to or less than the number set on the maximum pre-set units switch S1. No control action is required.)

The same exact order of events occurs, as regards the minimum pre-set circuitry, except that pins 9 and 6 on each comparator are interchanged and the conditions less than and greater than are reversed.

Returning to the point where the decrease control flip-flop IC42 was toggled by the low-going transition of the output of the nand gate IC40, a basic explanation of the operating characteristics of the J-K flip-flop, typical of the three employed in the pre-set controller 18, is in order (Texas Instruments Type SN7473, or equiv.). The J-K flip-flop, like the various gates and inverters, is a basic digital building block. Unlike ordinary gates, however, the J-K flip-flop has the added advantage of memory capability. This means, essentially, that once toggled by an input pulse, the outputs of the J-K flip-flop remain as toggled until another input pulse again changes the output states. Additionally, the J-K flip-flop includes means (the J and K inputs) to control the output states and means (the not reset terminal) to override all other inputs and reset the outputs to a fixed state. The reset terminal is called a 'not' reset ($\overline{R}$) because it is activated by a logic 0, not a logic 1. The clock or toggle input is likewise called a 'not' clock ($\overline{C}$), because the outputs can only change state when the input receives a low-going logic 0 input transition. The two outputs are referred to as Q and $\overline{Q}$, which simply means that when Q is a logic 1 (high), $\overline{Q}$ is a logic 0 (low). The following truth table gives the output conditions for various input states:

t_n			t_{n-1}	
$\overline{R}$	J	K	Q	$\overline{Q}$
1	0	0	Q_n	$\overline{Q}_n$
1	0	1	0	1
1	1	0	1	0
1	1	1	$\overline{Q}n$	Qn
0	(DO NOT CARE)		0	1

t_n means time prior to low-going clock pulse on the $\overline{C}$ input. t_{n-1} means the time immediately following the low-going clock pulse on the $\overline{C}$ input. Q_n means the same state as it was before the clock pulse and $\overline{Q}_n$ means the opposite state as it was before the clock pulse.

To complete the analysis of operation of the pre-set controller 18, let us assume that the controller has just completed a required correction and the thread counter 17 is in the count mode of operation. Therefore, the DR input is low and the R input is also low. Furthermore, the following states exist within the circuit:

1. Output of IC40 is high.
2. Output of IC41 is high.
3. Q output of IC42 is low.
4. Q output of IC44 is low.
5. Output of IC45 is low.
6. Output of IC43 is high.
7. Transistors Q3 – Q4 and Q5 – Q6 are off.
8. Transistor Q1 is on.
9. Capacitor C5 is shorted by Q1.
10. Output at Q2 (junction with R27) is low.
11. Mode switch S7 is an Auto. position.
12. Output of IC47 is low.
13. $\overline{R}$ input of IC49 is high.
14. Q output of IC49 is high.

Now, let us assume that at the beginning of the storage-reset mode in the thread counter 17, the number on the readout exceeds the number set on the maximum pre-set switches 40. At this instant both inputs to nand gate IC40 go high, and the output of nand gate IC40 immediately goes low, thereby causing the decrease control flip-flop IC42 to toggle. The outputs of the flip-flop IC42 change state since the $\overline{R}$ reset input is at a logic 1 (high) and since both the J and K inputs are also high. As the outputs of the decrease control flip-flop IC42 change state, the high on the Q output causes transistors Q3 and Q4 to switch on, thereby energizing the decrease control relay K1, and the decrease light DS1, signifying that a decrease correction has been instituted. At this same time, the $\overline{Q}$ output of the decrease control flip-flop IC42 goes low causing the output of nand gate IC45 to go high and the output of inverter IC43 to go low. The presence of this low on the J and K inputs J-K of flip-flops IC42 and

IC44 locks the output of IC42 and IC44 so that neither flip-flop can be toggled on the $\overline{C}$ input again. It will be necessary for the $\overline{R}$ inputs on IC42 and IC44 to be placed at a logic 0 (low) momentarily in order for the flip-flops to again accept correction data on their $\overline{C}$ inputs. The decrease control relay K1 and decrease light DS1 are also locked in an energized state and the increase control relay K2 and increase light DS2 are similarly locked in a de-energized state until the J-K flip-flops IC42 and IC44 are reset. This will occur at the termination of the time set on the correction timer 44, comprised of resistors R23, R24, R25, R26, R27, R28 and R29, capacitor C5 and transistors Q1 and Q2, in the following manner: When the output of the inverter IC43 went low, when control action was initiated, base turn-on drive to transistor Q1, via resistor R23, was removed, and transistor Q1 turned off. With the new high collector-to-emitter resistance of transistor Q1 across capacitor C5, C5 begins to be charged from voltage source V2 through resistors R25 and R26. After the voltage across capacitor C5 reaches the trigger level of Q2, a programmable unijunction transistor, Q2 conducts from anode to cathode and effectively dumps the charge on capacitor C5 into resistor R27, thereby causing a momentary high-going pulse to appear across resistor R27. Resistors, R28 and R29, are employed to set the trigger voltage level of Q2. The high-going pulse across resistor R27 drives the output of inverter IC46 low causing the output of gate IC47 to go high. Inverter IC48 inverts this high-going pulse and delivers to the $\overline{R}$ input of the J-K flip-flop IC49 a low-going pulse. This action immediately resets the Q output of the J-K flip-flop IC49 low. This low provides the required reset for the J-K flip-flops IC42 and IC44, and the Q output of IC42 is reset low terminating the control action. With the $\overline{Q}$ outputs of IC42 and IC44, both high, the output of nand gate IC45 goes low and the output of inverter IC43 goes high, again causing transistor Q1 to turn on, thereby resetting the correction timer 44 and preventing it from starting again until a new correction is required. With the $\overline{R}$ inputs of J-K flip-flops IC42 and IC44 both now low via the low signal from the Q output of the J-K flip-flop IC49, the controller is locked out until IC49 changes state. This occurs when the R line is next pulsed. At the end of this pulse, the low-going transition toggles the J-K flip-flop IC49 at its $\overline{C}$ input causing the Q output of IC49 to go high and the $\overline{Q}$ output to go low. The connection from $\overline{Q}$ to K ensures that no further toggling via the $\overline{C}$ input can occur. The only way now that the outputs of the J-K flip-flop IC49 can change state is via the $\overline{R}$ input. This input will remain high until either a new pulse is delivered from the correction timer or the mode switch S7 is positioned to manual (Man.). If the mode switch S7 is positioned to Man. the $\overline{R}$ input of IC49 will be held low and, in like manner, the $\overline{R}$ inputs of the J-K flip-flops IC42 and IC44 will be held low. Under these conditions, no control action is possible.

From the preceding discussion, it is apparent that once control action is initiated by the comparator circuits, the required correction will be instituted, and will continue for a time controlled by the setting of the correction timer 44. During this correction time, which may be quite long — sufficiently long for one or more complete updates in the thread counter readout to occur, the entire control circuitry is locked and no new data from the thread counter can be accepted, nor will the pre-set controller 18 permit resetting of its own locking circuits by the thread counter 17 via the R line to the $\overline{C}$ input of the J-K flip-flop IC49 until the control action has terminated.

The decrease relay K1 and the increase relay K2 are both connected in circuit with the reversible control motor 19 in such a way as to appropriately energize and de-energize the motor 19 and determine its direction of rotation when corrective action is called for by the pre-set controller 18. The decrease relay K1 is energized when the thread counter readout exceeds the selected maximum count set into the pre-set controller 18. At such time the threads per unit length of the fabric exceed the selected maximum, therefore the fabric must be stretched to reduce the number of threads per unit length. This is accomplished by reducing the speed of the feed roll 26 relative to the speed of the take-up (delivery) roll 27 so that the fabric will be stretched as a result of the difference in speed between the feed roll and the take-up roll. To reduce the speed of the feed roll 26 the decrease relay K1 causes the reversible control motor 19 to rotate in a direction to adjust the variable speed transmission 25 so that the speed of the transmission output shaft 25*b* is reduced.

When the increase relay K2 is energized as a result of corrective action being called for by the pre-set controller 18, the threads per unit length in the fabric as counted by the thread counter 17 are less than the selected minimum number of threads set into the pre-set controller. This condition requires that the speed of the feed roll 26 be increased; therefore the increase relay K2 causes the reversible control motor 19 to rotate in a direction which will adjust the variable speed transmission 25 to increase its output speed and thereby increase the speed of the feed roll 26. When the relays K1 and K2 are de-energized, the reversible control motor 19 will cease to operate, and the output speed of the variable transmission 25 relative to its input speed will remain constant.

Other modifications and variations of the present invention are possible in the light of the above teachings. Accordingly, it is not desired to limit the invention to the present disclosure and various modifications and equivalents may be resorted to falling within the spirit and scope of the invention as claimed.

What is claimed is:

1. Apparatus for counting threads per unit length in a moving fabric comprising a laser source of light radiations for direct penetration of the fabric, means activated by said light radiations for producing electrical thread count pulses caused by successive threads passing through said light radiations, thread count accumulating means responsive to said thread count pulses for accumulating the thread count over a predetermined length of said fabric, count storage and indicator means for indicating the threads per unit length of said fabric, transfer means responsive to a storage signal pulse for periodically transferring the count accumulated by said thread count accumulating means to said count storage and indicator means, measuring means for measuring the length of said fabric and producing dimension related electrical pulses representing increments of length of said fabric, count gate means

responsive to said dimension related pulses for alternately admitting thread count pulses to said thread count accumulating means during a count mode and for blocking thread count pulses from said thread count accumulating means during a storage-reset mode, a storage pulse producing means actuated in response to said dimension related pulses to produce and send a storage pulse to said transfer means at the beginning of said storage-reset mode, reset means for resetting said count accumulating means to zero, and reset pulse producing means responsive to said storage pulse for producing a reset pulse and actuating said reset means to reset said count accumulating means to zero.

2. The apparatus set forth in claim 1 wherein a count pre-scaler is provided between said thread count pulse producing means and said count gate to scale down the thread count pulses by a predetermined ratio and a dimension pre-scaler is provided in circuit with said dimension related pulse producing means to scale down the dimension related pulses by a predetermined ratio.

3. The apparatus set forth in claim 2 wherein said thread count is accumulated over 50 units of length of said fabric, and wherein said dimension related pulse producing means produces one pulse for every ten units of length of said fabric, said count pre-scaler being a divide-by-five pre-scaler, and said dimension pre-scaler being a divide-by-six pre-scaler.

4. The apparatus set forth in claim 1 wherein said count accumulating means comprises plural decade connected binary coded decimal counters.

5. The apparatus set forth in claim 4 wherein said count storage and indicator means includes gas filled digital indicator tubes, there being one indicator tube for each binary coded decimal counter present and wherein said count transfer means includes storage pulse actuated latching means connected between each binary coded decimal counter and a corresponding one of said gas filled indicator tubes, said latching means being unlatched in response to each storage pulse to transfer the count from each of the binary coded decimal counters to the corresponding gas filled indicator tube.

6. The apparatus set forth in claim 5 wherein said latching means comprises 4-bit bistable latches.

7. The apparatus set forth in claim 6 wherein a binary coded data-to-decimal decoder driver is interposed between each of the 4-bit bistable latches and a corresponding one of said digital indicator tubes.

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