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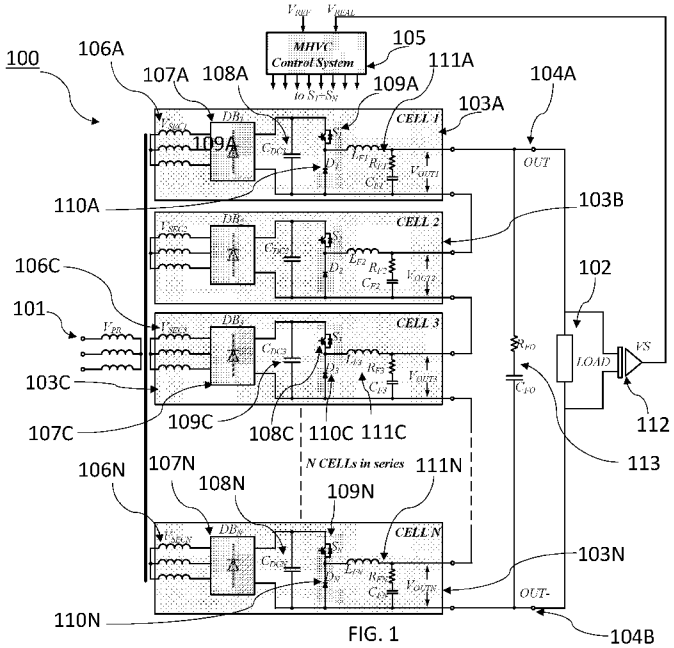

FIG. 1

(57) Abstract: Systems and methods that facilitate multilevel hysteresis voltage control methods for cascaded multilevel voltage modulators having a plurality of power cells connected in series and has any positive integer number of output voltage levels to control any unipolar voltage on the load of the voltage modulator, and transfer electrical power from an electrical grid via AC/DC converters or directly from energy storage elements of the power cells to that load. A method of operational rotation of the power cells of a multilevel voltage modulator, which ensures an equal power sharing among the power cells and voltage balancing of the energy storage elements of the power cells of the modulator.

[Continued on next page]

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MULTI-LEVEL HYSTERESIS VOLTAGE CONTROLLERS FOR VOLTAGE MODULATORS AND METHODS FOR CONTROL THEREOF

TECHNICAL FIELD

[0001] The present disclosure relates to power electronic circuits, and more particularly to multi-level hysteresis voltage controllers for voltage modulators and methods for control thereof.

BACKGROUND

[0002] Voltage modulators have been used widely for broadcast, medical, industrial and research applications. The most common voltage modulation techniques include Pulsed Step Modulation, Coarse Step Modulation, Pulsed Width Modulation, and hybrid modifications thereof.

[0003] These common modulation techniques have several drawbacks. For instance, these common modulation techniques are linear methods that require a proportional-integral (PI) controller with an additional feedforward loop in a control system to estimate a modulation index or duty cycle at every step of discretization. In addition, low frequency pulsations of output voltage usually occur in these common modulation techniques due to unbalance of DC-link voltages, variation in parameters of passive elements, and deviations of duty cycles of series connected modules. Lastly, there is a strong correlation between parameters of the PI-controller and load parameters in these common modulation techniques. Therefore, if load characteristics change rapidly and over a wide range, then the PI-controller is not capable of operating efficiently and fast enough to minimize a control error in transient periods.

[0004] Hysteresis is a phenomenon in which the response of a physical system to an external influence depends not only on the present magnitude of that influence but also on the previous history of the system. Expressed mathematically, the response to the external influence is a doubled-valued function; one value applies when the influence is increasing, while the other value applies when the influence is decreasing.

[0005] Among existing control techniques, nonlinear hysteresis band voltage control remains the simplest and fastest method. Beyond a fast response of a voltage control loop, the nonlinear hysteresis band voltage control method does not require any knowledge of variation of load parameters. However, the hysteresis voltage control technique for voltage modulators becomes increasingly complicated with an increased number of power cells connected in series.

[0006] In view of the foregoing limitations, it is desirable to provide a multilevel hysteresis voltage controller (MHVC) for voltage modulators having any number of series connected power cells while providing very accurate voltage regulation in a wide range of load parameters fluctuations.

SUMMARY

[0007] The embodiments of the present disclosure are directed to systems and methods that facilitate simple and effective multilevel hysteresis voltage control methods for cascaded multilevel voltage modulators. In embodiments, a cascaded multilevel modulator comprises a plurality of power cells connected in series and has any positive integer number of output voltage levels to quickly, effectively, and precisely control any unipolar voltage on the load of the voltage modulator, and transfer electrical power from an electrical grid via AC/DC converters or directly from energy storage elements of the power cells to that load. The embodiments are also directed to a method of operational rotation of the power cells of a multilevel voltage modulator, which ensures an equal power sharing among the power cells and voltage balancing of the energy storage elements of the power cells of the modulator.

[0008] The embodiments presented herein may advantageously be used in a variety of applications in which voltage regulated modulators are employed. Examples of such applications may include, without limitation, power electronics circuits comprising: electrode biasing power supplies for Tokamak and FRC plasma reactors; power supplies for neutral beam injectors; magnetron modulators; klystron modulators; E-gun modulators; high power X-ray power supplies; mediumwave and longwave transmitters; and shortwave solid-state transmitters.

[0009] Other systems, methods, features and advantages of the example embodiments will be or will become apparent to one with skill in the art upon examination of the following figures and detailed description.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] The details of the example embodiments, including structure and operation, may be gleaned in part by study of the accompanying figures, in which like reference numerals refer to like parts. The components in the figures are not necessarily to scale, emphasis instead being placed upon illustrating the principles of the disclosure. Moreover, all illustrations are intended to convey concepts, where relative sizes, shapes and other detailed attributes may be illustrated schematically rather than literally or precisely.

[0011] FIG. 1 illustrates a schematic of a multi-level voltage modulator according to embodiments of the present disclosure.

[0012] FIG. 2 illustrates an exemplary multi-level hysteresis voltage controller according to embodiments of the present disclosure.

[0013] FIG. 3 illustrates an exemplary voltage level estimator according to embodiments of the present disclosure.

[0014] FIGS. 4A, 4B, 4C and 4D illustrate exemplary operation of an exemplary voltage level estimator according to embodiments of the present disclosure.

[0015] FIG. 5 illustrates an exemplary switching pattern generator according to embodiments of the present disclosure.

[0016] FIG. 6A illustrates an exemplary 1VDC rotation block according to embodiments of the present disclosure.

[0017] FIG. 6B illustrates an exemplary 2VDC rotation block according to embodiments of the present disclosure.

[0018] FIG. 6C illustrates an exemplary 3VDC rotation block according to embodiments of the present disclosure.

[0019] FIG. 6D illustrates an exemplary 4VDC rotation block according to embodiments of the present disclosure.

[0020] FIG. 6E illustrates an exemplary (N-1)VDC rotation block according to embodiments of the present disclosure.

[0021] FIGS. 7A, 7B, 7C and 7D illustrate exemplary operation of an exemplary switching pattern generator according to embodiments of the present disclosure.

[0022] FIG. 8 illustrates exemplary switching and Levels signals for an exemplary seven (7) level voltage modulator according to embodiments of the present disclosure.

[0023] FIGS. 9A, 9B and 9C illustrate simulation results of operation of the exemplary seven (7) level voltage modulator according to embodiments of the present disclosure.

[0024] FIGS. 10A, 10B and 10C illustrate simulation results (zoomed traces) of operation of the exemplary seven (7) level voltage modulator according to embodiments of the present disclosure.

[0025] FIGS. 11A, 11B and 11C illustrate exemplary experimental results of operation of an exemplary seven (7) level voltage modulator operated with active electrodes of diverts of an FRC reactor and according to embodiments of the present disclosure.

[0026] FIGS. 12A, 12B and 12C illustrate exemplary experimental results of operation of an exemplary seven (7) level voltage modulator operated with active electrodes of diverts of an FRC reactor and according to embodiments of the present disclosure.

[0027] It should be noted that elements of similar structures or functions are generally represented by like reference numerals for illustrative purpose throughout the figures. It should also be noted that the figures are only intended to facilitate the description of the preferred embodiments.

DETAILED DESCRIPTION

[0028] The following embodiments are described in detail to enable those skilled in the art to make and use various embodiments of the present disclosure. It is understood that other embodiments would be evident based on the present disclosure, and that system, process, or changes may be made without departing from the scope of the present embodiments.

[0029] In the following description, numerous specific details are given to provide a thorough understanding of the present embodiments. However, it will be apparent that the present embodiments may be practiced without these specific details. In order to increase clarity, some well-known circuits, system configurations, and process steps may not be described in detail.

[0030] The drawings showing embodiments of the present disclosure are semi-diagrammatic and not to scale and, particularly, some of the dimensions are for the clarity of presentation and are shown exaggerated in the drawing Figures.

[0031] The embodiments of the present disclosure are directed to systems and methods that facilitate simple and effective multilevel hysteresis voltage control methods for cascaded multilevel voltage modulators. In embodiments, a cascaded multilevel modulator comprises a plurality of power cells connected in series and has any positive integer number of output voltage levels to quickly, effectively, and precisely control any unipolar voltage on the load of the voltage modulator, and transfer electrical power from an electrical grid via AC/DC converters or directly from energy storage elements of the power cells to that load. The embodiments are also directed to a method of operational rotation of the power cells of a multilevel voltage modulator, which ensures an equal power sharing among the power cells and voltage balancing of the energy storage elements of the power cells of the modulator

[0032] In embodiments, an exemplary multilevel hysteresis voltage controller (MHVC) has a robust structure, which is free from the above-mentioned drawbacks and does not have any additional regulation loops other than a voltage hysteresis loop. The output voltages of all power cells of the voltage modulator are adjusted dynamically and in an automated manner by MHVC to maintain a minimum preset value of output voltage regulation error, excluding an influence of variation of parameters of passive components and the propagation delays of control signals on the output voltage oscillations. There are three major and interlinked tasks that are performed by the MHVC: 1) maintenance of an voltage modulator's output voltage within the preset boundaries of regulation error; 2) identification of appropriate output voltage level at any moment of time; and 3) rotation of the power cells.

[0033] Embodiments are directed to a fast MHVC design which can be realized on any FPGA or similar design component and can be operated at a high clock rate (tens of megahertz). The design comprises a hysteresis block, a voltage level estimator as described herein, and a switching pattern generator as described herein.

[0034] FIG. 1 illustrates a schematic of a multi-level voltage modulator (voltage modulator) 100 according to embodiments of the present disclosure. A multi-level voltage modulator 100 is connected to a three-phase grid 101 on a lower voltage side and to a load 102 on higher voltage side, as well as a control system 105 having a MHVC. Functions of the control system 105 may be implemented using either software or hardware processors including software routines, hardware components, or combinations thereof.

[0035] The exemplary multi-level voltage modulator 100 comprises N series connected cells 103A-103N, where each cell 103A-103N comprises a secondary winding of isolation transformer (V_{SECN}) 106A-106N connected to a three-phase diode bridge (DB_N) 107A-107N, a capacitive storage element (C_{DCN}) 108A-108N on a DC side (DC-link) of the DB_N 107A-107N, and a standard buck converter with an active bidirectional switch (S_N) 109A-109N (*e.g.*, for high voltage modulators the S_N may include IGBT with freewheeling diode, while for lower voltage modulators the S_N may include low voltage MOSFETs) and a diode (D_N) 110A-110N. It will be appreciated that N is a positive integer. Each cell 103A-103N may also be equipped with an optional LCR filter (L_{FN}, C_{FN}, R_{FN}) 11A-111Nat its output and the voltage modulator 100 may also be equipped with an optional CR filter (C_{FO}, R_{FO}) 113 at its output. The DC-links of all of the power cells 103A-103N are isolated from each other at the maximum load voltage level by means of a three-phase multi-winding transformer (V_{SECN}) 106A-106N.

[0036] The voltage modulator 100 is assumed to be working in continuous mode, transferring the energy from the three-phase grid 101 to the load 102. It is also possible to operate the voltage modulator 100 completely disconnected from the grid 101 for a certain period of time using the energy accumulated in the storage elements (*e.g.*, capacitors, supercapacitors, batteries) 108A-108N of the cells 103A-103N if the voltage on the storage elements 108A-108N is not significantly reduced during an operational time in order to maintain a desired output voltage on the load 102.

[0037] Each DC-link voltage of the voltage modulator's 100 power cells 103A-103N of the voltage modulator 100 may be considered a DC voltage source of a fixed magnitude (VC_{DCN}) which, in practice according to certain embodiments, may be on the order of 12 to 1200 Volts. The total voltage across the series connected power cells 103A-103N (*i.e.*, between terminals OUT+

104A and OUT- 104B) is dependent upon the number of cells that have been turned on by closure of the associated switches S_1 through S_N 109A-109N. For example, if all of the switches S_1 through S_N 109A-109N are closed at the same time, then all of DC-link storage elements (*e.g.*, capacitors) with voltage V_{DC1-N} are connected together in series and added together (*i.e.*, summed) to provide an output voltage equal to N times voltage V_{DC1-N}. If each DC-link voltage source V_{DC1-N} has a value on the order of 800 Volts and N is on the order of 20, then the total output voltage of the voltage modulator 100 may be on the order of 16,000 Volts.

[0038] If the switch S_N 109N in the power cell 103N is open (*i.e.*, not in conducting mode) then this particular cell is "bypassed" and its output voltage is zero. Thus, the output voltage of the voltage modulator 100 can be synthesized and modulated by the number of cells that are turned ON and OFF.

[0039] Referring to FIG. 1 to contrast, in the standard Pulse Step Modulation (PSM) technique, if there are N power cells in series in a voltage modulator and each cell has a commutation period T(s), the switch S1 of CELL 1 will be switched on at time t1, but the switch S2 of CELL 2 is turned on T/n (s) later than the first one, the third (S3) is turned on 2T/n(s) later than the second (S2), and so on. This rotation method of PSM ensures very low ripples at the output of the voltage modulator, as their amplitude is reversely proportional to the frequency of AC component f_{AC} of the output voltage of the voltage modulator. All power cells are switched at the same fixed switching frequency f_{SW}, then $f_{AC}=N*f_{SW}$.

[0040] Regulation of the output voltage using PSM is performed via linear regulation concepts (PI, feedforward or their combination) by calculating the required number of power cells which have to be turned on (Coarse Step Modulation), and/or regulation of duty cycle D (Pulse Width Modulation), which has to be the same for all power cells in case the passive components (C_{DC}, L_F, R_F, C_F) of all power cells are absolutely identical, the stray capacitances are the same, as well as the propagation delays of the control signals. However, in reality all passive components always have a slight variation of parameters, and the propagation delays of control signals for power cells are not always the same. As a result, each power cell has to be switched on with a different required duty cycle D_N, which has to be corrected in PSM based control system by additional regulation loop using a DC-link voltage feedback signal. Moreover, additional adjustment of turn on times t1, t2…tN can be necessary to eliminate the low frequency oscillations of output voltage of the voltage modulator.

[0041] As discussed above, embodiments herein are directed to a multilevel hysteresis voltage controller (MHVC) having a robust structure, which is free from the above-mentioned drawbacks

and does not have any additional regulation loops other than a single voltage hysteresis loop. The output voltages of all power cells 103A-103N of the voltage modulator 100 are adjusted dynamically and in an automated manner by the MHVC to maintain a minimum preset value of output voltage regulation error, excluding an influence of variation of parameters of passive components and the propagation delays of control signals on the output voltage oscillations.

[0042] FIG. 2 illustrates an exemplary multi-level hysteresis voltage controller 200 of the control system 105 (see FIG. 1) according to embodiments of the present disclosure. An exemplary multi-level hysteresis voltage controller 200 comprises a low pass filter (LP-filter) Filter1 201, a summation block Sum1 202, a hysteresis block Hyst1 203, a voltage level estimator 204, and a switching pattern generator 205. A real feedback voltage signal V_{REAL} from a voltage sensor VS 112 (see FIG. 1) goes through a low pass filter Filter1 201 to a negative input of the summation block Sum1 202, where it is subtracted from the reference voltage V_{REF} to generate a voltage error signal ΔV, as their difference. The voltage error signal ΔV is input into the hysteresis block Hyst1 203, which has the settings of high boundary (HB) and low boundary (LB) thresholds. When ΔV reaches the high boundary (HB) of the hysteresis block Hyst1 203, the output value of the hysteresis block Hyst1 203 is set to "1" and remains at this level until ΔV crosses its low boundary (LB) of the hysteresis block Hyst1 203. When ΔV crosses its low boundary (LB) of the hysteresis block Hyst1 203, the output value of the hysteresis block Hyst1 203 is set to "0" and the output is maintained at this level until ΔV reaches HB again.

[0043] FIG. 3 illustrates an exemplary voltage level estimator 204 according to embodiments of the present disclosure. FIGS. 4A-4D illustrate exemplary operation of the exemplary voltage level estimator 204 according to embodiments of the present disclosure.

[0044] The voltage level estimator 204 operates in parallel with the hysteresis block Hyst1 203. The voltage level estimator 204 receives the same HB and LB setting signals together with ΔV from the output of summation block Sum1 202. The exemplary voltage level estimator 204 comprises a clock counting circuit formed by a clock generator Clock 210, a logic switch Switch1 211 and a resettable counter Counter1 212. The exemplary voltage level estimator 204 further comprises a level decrement circuit 220comprising a logic element AND1 221, a rising edge detector Rising Edge 2 222 and a free running counter Counter2 223. The exemplary voltage level estimator 204 further comprises a level increment circuit 230 having a logic element AND2 231, a rising edge detector Rising Edge 3 232 and a free running counter Counter3 233. The exemplary voltage level estimator 204 further comprises an enable and reset circuit 240 for Counter1 212, which comprises of a logic element XOR1 241, a rising edge detector Rising Edge

1 242 and a logic element OR1 243. The exemplary voltage level estimator 204 further comprises a summation block Sum1 250.

[0045] The block Counter1 212 is enabled when the clock signal goes through the upper input channel of Switch1 211(in case of a True signal on its middle input channel), and starts counting a number of clock cycles generated by the Clock 210 in any of the following cases: If the output of Comp1 213 is True, i.e. the signal ΔV is lower than the low boundary hysteresis threshold LB ($\Delta V < LB$). This case is illustrated in FIGS. 4A-4D, where at the point C2 the signal ΔV becomes lower than LB and the Counter1 212 starts incrementing a count until ΔV returns to the hysteresis boundaries at the point D2 and the output signal of Comp1 213 becomes False; If the output of Comp2 214 is True, i.e. the signal ΔV is higher than the high boundary hysteresis threshold HB ($\Delta V > HB$). This case is illustrated in FIGS. 4A-4D, where at the point B1 the signal ΔV becomes higher than HB and the Counter1 212 starts incrementing a count until ΔV returns to the hysteresis boundaries at the point C1 and the output signal of Comp2 214 becomes False.

[0046] The block Counter2 223 increments its output counting signal, which is applied to the negative input of summation block Sum1 250, decrementing a number of Levels at the output of voltage level estimator 204, if both of the following cases are true at the same time: If the output of Comp1 213 is True, i.e. the signal ΔV is lower than the low boundary hysteresis threshold LB ($\Delta V < LB$); If the value of the output counting signal of Counter1 212 is higher than a preset value of Time Constant (in cycles).

[0047] If both of the above mentioned conditions are satisfied, then the output of AND1 221 becomes True and this fact is detected by the block Rising Edge 2 222, which generates a pulse of one clock cycle duration, and the block Counter2 223 increments and holds its output count decrementing a value at the output of Sum1 250 (the signal Levels at the output of voltage level estimator 204).

[0048] The block Counter3 233 increments its output counting signal, which is applied to the positive input of summation block Sum1 250, incrementing a number of Levels at the output of voltage level estimator 204, if both of the following cases are true at the same time: If the output of Comp2 214 is True, i.e. the signal ΔV is higher than the high boundary hysteresis threshold HB ($\Delta V > HB$); If the value of the output counting signal of Counter1 212 is higher than a preset value of Time Constant (in cycles).

[0049] If both of the above mentioned conditions are satisfied, then the output of AND2 231 becomes True and this fact is detected by the block Rising Edge 3 232, which generates a pulse of one clock cycle duration, and the block Counter3 233 increments and holds its output count

incrementing a value at the output of Sum1 250 (signal Levels at the output of voltage level estimator 204).

[0050] This case of incrementing of levels signal (increment of Counter3 233) is illustrated in FIGS. 4A-4D, where the point A2 satisfies the first of two presented above conditions and the point B2 corresponds to the second condition, when the output counting signal of Counter1 212 is higher than a value of Time Constant preset at 500 clock cycles.

[0051] There are three conditions to be true to reset the Counter1 212 as can be seen from FIG. 3. If one of the output signals of the blocks Rising Edge 1 242, Rising Edge 2 222 and Rising Edge 3 232 is True, then the output of block OR1 243 is also True what actually resets the Counter1.

[0052] FIG. 5 illustrates an exemplary switching pattern generator 205 according to embodiments of the present disclosure. The exemplary switching pattern generator enables a unique method of rotation of an operation duty of the power cells 103A-103N of voltage modulator 100, which ensures an automatic power sharing among the power cells 103A-103N, as well as an adjustment of duty cycle and phase shift of commutation of each power cell 103A-103N.

[0053] In embodiments, the exemplary switching pattern generator 205 comprises a resettable Counter4 260 with a reset signal forming a circuit based on the comparator block Comp4 262. The exemplary switching pattern generator 205 further comprises a multiplexer Switch 1 263 with N input signals of constant values from 1 to N, where N is a number of power cells of voltage modulator 100. The exemplary switching pattern generator 205 further comprises a multiplexer Switch 1 263 with N+1 input signals, where each input signal is represented as an array of switching states and N-1 of them (1VDC Rotation, 2VDC Rotation … (N-1)VDC Rotation) are dynamic arrays and only two arrays OVDC and NVDC are static and have the constant values. The exemplary switching pattern generator 205 receives the signal Levels from voltage level estimator 204 and the signal State form the hysteresis block Hyst1 203. The output signals of the switching pattern generator 205 are N switching commands to all N switching elements (said IGBTs) of voltage modulator 100.

[0054] FIGS. 7A-7D illustrate exemplary operation of the exemplary switching pattern generator 205 according to embodiments of the present disclosure. The exemplary switching pattern generator for which operation is depicted in FIGS. 7A-7D is implemented in a seven-level voltage modulator consisting of seven power cells.

[0055] The Counter4 260 increments its output value at every rising edge of the signal State (see FIGS. 7A-7D) up to value N, which sets the output of Comp4 261 to True and resets the

Counter4 260. This output signal of Counter4 260 chooses a constant value at the corresponding input of the multiplexer Switch 1 262 at every count and redirects it to the output of the multiplexer Switch 1 262 forming the signal Cell_rot, which is presented in FIGS. 7A-7D. Thus, the signal Cell_rot is changed repetitively from N to 1 with a decrement of 1 at every rise edge of the signal State.

[0056] The signal Levels coming from the voltage level estimator 204 passes through the summation block Sum2 263, where it is incremented by 1, and goes to the control input of the multiplexer block Switch 2 264. This multiplexer commutates N+1 arrays of switching states corresponding to the output voltage levels from 0VDC, when all switching signals are False (zero volts at the output of voltage modulator 100) to NVDC level, corresponding to the maximum output voltage of voltage modulator 100, when all switching signals are True. These two voltage levels, the minimum and the maximum output voltage levels, are created by the static arrays (OVDC and NVDC, see FIG. 5) of switching states (signals) of the voltage modulator 100 and no rotation of power cells is required.

[0057] The functional diagrams of N-1 blocks of dynamic arrays from 1VDC Rotation to (N-1)DC rotation are presented in FIGS. 6A-6E.

[0058] FIG. 6A illustrates an exemplary 1VDC rotation block 265Aaccording to embodiments of the present disclosure. FIG. 6B illustrates an exemplary 2VDC rotation block 265B according to embodiments of the present disclosure. FIG. 6C illustrates an exemplary 3VDC rotation block 265C according to embodiments of the present disclosure. FIG. 6D illustrates an exemplary 4VDC rotation block 265D according to embodiments of the present disclosure. FIG. 6E illustrates an exemplary (N-1)VDC rotation block 265E according to embodiments of the present disclosure.

[0059] Each of the blocks 265A-265E depicted in FIGS. 6A-6E comprises a multiplexer with a control input, which receives a signal Cell_rot from the block Switch 2 264, and having N commutated inputs. Each of the blocks 265A-265E depicted in FIGS. 6A-6E further comprises N static arrays containing the specific switching states for correct rotation of the power cells 103A-103N of voltage modulator 100.

[0060] If the signal Levels takes the values 0 and 1 only, performing a regulation of the output voltage of the voltage modulator 100 between 0VDC and 1VDC levels, then the 1VDC rotation block 265A is involved in operation together with a static array OVDC. As can be seen from FIG. 6A, each of N static arrays from 1VDC1 to 1VDCN of the block 1VDC rotation has only one high (True) switching state, which position in array depends on a value of signal Cell_rot. For example

if Cell_rot=1, then only first power cell 103A is operated providing a voltage of its storage element to the output of voltage modulator 100 via opened switching element S_1 109A (e.g., an IGBT) while all other power cells 103B-103N are bypassed. A rotation of the power cells involved in providing 1VDC level of output voltage is ensured by the signal Cell_rot, which is changed repetitively from N to 1 with a decrement of 1 at every rise edge of the signal State.

[0061] If the signal Levels takes the values 1 and 2 only, performing a regulation of the output voltage of the voltage modulator 100 between 1VDC and 2VDC levels, then the 1VDC rotation block 265A and the 2VDC rotation block 265B are involved in operation together. As can be seen from FIG. 6B, each of N static arrays from 2VDC1 to 2VDCN of the 2VDC rotation block 265B has two high (True) switching states, which positions in array depend on a value of signal Cell_rot. For example if Levels = 2 and Cell_rot=1, then the first and the second power cells 103A and 103B are operated providing a sum of the voltages of their storage elements to the output of voltage of the voltage modulator 100 via opened switching elements S_1 and S_2 (109A and 109B) while all other power cells 103C-103N are bypassed. When the signal Levels changes to 1 at every rising edge of the signal State, then only one power cell remains connected to the output and its number will be decremented by 1, because the signal Cell_rot is changed also with a rising edge of the signal State. In this case a rotation of the power cells involved in providing 1VDC and 2VDC levels of output voltage is ensured not only by the signal Cell_rot, which is changed repetitively from N to 1 with a decrement of 1 at every rise edge of the signal State, but by the distribution of the high (said True) switching states in the dynamic arrays of both the 1VDC and 2VDC rotation blocks 265A and 265B.

[0062] FIG. 8 illustrates exemplary switching signals for an exemplary seven (7) level voltage modulator according to embodiments of the present disclosure. FIG. 8 provides an example of the operation of the switching pattern generator 205 for a case of a seven-level voltage modulator comprising seven power cells connected in series. As can be seen from FIG. 8, the Levels signal is changed first from 5 to 6 when the voltage modulator 100 provides an output voltage between 5VDC and 6VDC levels, and then the Levels signals is switched between 6 and 7, when the voltage modulator 100 regulates its output voltage between 6VDC and 7VDC levels. In both cases the switching signals S_1 - S_7 (109A-109G) are shifted from each other ensuring a rotation of the power cells with an equal distribution of consumed power and providing an output frequency of the output voltage to be seven times higher than the switching frequency of each individual power cell.

[0063] FIGS. 9A-9C illustrates simulation results of operation of the exemplary seven (7) level voltage modulator according to embodiments of the present disclosure. FIG. 10 illustrates simulation results (zoomed traces) of operation of the exemplary seven (7) level voltage modulator according to embodiments of the present disclosure. The seven-level voltage modulator comprises seven power cells connected in series. The reference output voltage V_{REF} is a sinusoidal waveform of 100Hz with amplitude of 3kV and DC-offset of 3.5kV, thus a maximum output voltage is 6.5kV and the minimum value is 0.5kV (FIGS. 9A-9C). The proposed multi-level hysteresis voltage controller operates in such a way to maintain a regulation error ΔV in boundaries of preset values of HB and LB (30V and -30V respectively, see FIGS. 9A-9C and FIGS. 10A-10C). An overshoot of ΔV in the level transition regions depends on the Time Constant value and can be reduced further to the certain level by adjusting a value of Time Constant. The signal Levels presented in FIGS. 9A-9C and FIGS. 10A-10C is increasing and decreasing following the reference voltage dynamic. The real output voltage V_{REAL} is maintained around V_{REF} with a regulation error ΔV.

[0064] FIGS. 11A-11C and FIGS. 12A-12C show the experimental results of a single-phase seven (7) level modulator comprising seven (7) cells connected in series with capacitive storage element on DC-link side as depicted in FIG. 1. The seven (7) level modulator is operated with active electrodes installed in the diverters of the colliding beam FRC based reactor. The active electrodes are in touch with the plasma and the PSU provides the current of up to 5kA to the plasma with an output voltage of up to 5kV. The plasma parameters during a plasma discharge significantly and rapidly change and thus the required bias voltage has to be regulated and stabilized at the desired reference value.

[0065] The reference voltage V_{REF} and real output voltage of the PSU V_{OUT} are shown as functions of time in FIG. 11B. As can be seen, V_{OUT} is regulated and stabilized around V_{REF} with a voltage control error signal presented in FIG. 11A while not exceeding a preset value of +/-100A. The required number of levels of the output voltage calculated by the Voltage Level Estimator block (204, see FIG. 2) is shown in FIG. 11B. As the capacitor banks in the DC-links of power cells are discharging it requires more levels of output voltage to be set up to maintain a constant output voltage of 3.5kV and the proposed methodology calculates it accordingly. At the end of the pulse all capacitor banks are discharged to the voltage, at which a setting of all 8 levels is not enough regulate V_{OUT}, which causes an increase of output voltage error signal.

[0066] FIG. 12 shows the experimental results of operation of the same Active Electrode PSU with a triangle reference voltage V_{REF}, demonstrating a high dynamic capability of proposed voltage hysteresis controller to regulate and stabilize a voltage with a fast changing dV/dt value.

[0067] Embodiments of the present disclosure are directed to a multi-level cascaded voltage modulator connectable to a load. In embodiments, the multi-level cascaded voltage modulator comprises a plurality of power cells connected in series, wherein each cell of the plurality of cells comprises a of bidirectional switch and a storage element, and a control system coupled to the plurality of cells and having a multi-level hysteresis voltage controller. In embodiments, the control system is configured to cause the plurality of cells to output N levels of voltage on the load, wherein N is a positive integer corresponding to the number of power cells of the plurality of power cells.

[0068] In embodiments, each cell of the plurality of cells includes a secondary winding isolation transformer, a three-phase diode bridge coupled to the transformer and the storage element, and a diode.

[0069] In embodiments, the bidirectional switch is one of an IGBT or a MOSFET.

[0070] In embodiments, each cell of the plurality of cells further comprises an LCR filter at its output.

[0071] In embodiments, the modulator further comprises a CR filter at the output of the plurality of cells.

[0072] In embodiments, the control system is further configured to cause the transfer of electrical power from the energy storage elements of the power cells to the load.

[0073] In embodiments, the control system is further configured to balance voltages on the storage elements.

[0074] In embodiments, the storage element is a capacitor.

[0075] In embodiments, the control system including one or more processors coupled to a non-transitory memory comprising a plurality of instructions that when executed causes the one or more processors to control a level of voltage on the load.

[0076] In embodiments, the plurality of instructions when executed causes the one or more processors to control an output voltage level of the modulator as a function of the level of voltage on the load, a reference voltage and a voltage error equal to the difference between the level of voltage on the load and the reference voltage.

[0077] In embodiments, the plurality of instructions when executed causes the one or more processors to subtract from a reference voltage signal V_{REF} a real feedback voltage signal V_{REAL} received from a voltage sensor, produce, by a voltage level estimator, an estimated voltage level

signal, Levels, using a high boundary (HB) threshold of a hysteresis block, a low boundary (LB) threshold of the hysteresis block, and the voltage difference signal ΔV, and generate, by a switching pattern generator, a plurality of switching signals based on the estimated voltage level, Levels, and a state of the hysteresis block.

[0078] In embodiments, to subtract from a reference voltage signal V_{REF} a real feedback voltage signal V_{REAL}, the plurality of instructions when executed causes the one or more processors to feed the real feedback voltage signal V_{REAL} to a low-pass filter input, feed a low-pass filter output signal to a negative input of a first summation block, feed the reference voltage signal V_{REF} to a positive input of the first summation block, and produce a voltage difference signal ΔV at an output of the first summation block.

[0079] In embodiments, when ΔV reaches the high boundary (HB) threshold of the hysteresis block, the plurality of instructions when executed causes the one or more processors to set the state of the hysteresis block to "1."

[0080] In embodiments, when ΔV reaches the low boundary (LB) threshold of the hysteresis block, the plurality of instructions when executed causes the one or more processors to set the state of the hysteresis block to "0."

[0081] In embodiments, to produce the estimated voltage level Levels, the plurality of instructions when executed causes the one or more processors to apply a clock signal to a clock generator, count, by a resettable counter, a number of clock signals generated by the clock generator when one or more of the following conditions is true: ΔV is lower than the low boundary (LB) threshold of the hysteresis block; or ΔV is higher than the high boundary (HB) threshold of the hysteresis block.

[0082] In embodiments, the plurality of instructions when executed causes the one or more processors further to, increment, by a free running counter, a free running counter output signal, apply the free running counter output signal to a second summation block, and decrement a number of Levels at an output of the voltage level estimator when both of the following cases are true at the same time: the signal ΔV is lower than the low boundary hysteresis threshold LB; and the value of an output counting signal of the resettable counter is higher than a preset value of a time constant.

[0083] In embodiments, when both the signal ΔV is lower than the low boundary hysteresis threshold LB and the value of the output counting signal of the resettable counter is higher than the preset value of a time constant, the plurality of instructions when executed causes the one or more processors to set the output of a logic element of a level decrement circuit to True, detect the

output of the logic element with a rising edge detector, and increment the free running counter, and thereby decrement an output level at a summation block.

[0084] In embodiments, the multi-level hysteresis voltage controller comprises a low pass filter having a low-pass filter input and a low-pass filter output, a first summation block having a positive input and a negative input, a hysteresis block having a high boundary (HB) threshold and a low boundary (LB) threshold, a voltage level estimator having a plurality of voltage level estimator inputs and a voltage level output signal Levels, and a switching pattern generator having a plurality of switching pattern generator inputs and a plurality of switching pattern generator outputs.

[0085] In embodiments, the switching pattern generator comprises a comparator block, a resettable counter, a first multiplexer having a first plurality of input signals, and a second multiplexer having a second plurality of input signals.

[0086] In embodiments, each input signal of the second plurality of input signals represents an array of switching states each corresponding to a one of plurality of output levels for a voltage modulator.

[0087] In embodiments, the plurality of output levels ranges from 0VDC when all switching signals are false to a maximum output voltage when all switching signals are true.

[0088] In embodiments, the voltage level estimator comprises, a clock counting circuit, a level decrement circuit, an enable and reset circuit for the resettable counter, and a second summation block.

[0089] In embodiments, the clock counting circuit comprises a clock generator, a logic switch, and a resettable counter.

[0090] In embodiments, the level decrement circuit comprises a first logic element, a rising edge detector, and a free running counter.

[0091] In embodiments, the enable and reset circuit comprises a second logic element, a rising edge detector and a third logic element.

[0092] In embodiments, the first logic element is an AND gate, the second logic element is an XOR gate, and the third logic element is an OR gate.

[0093] In embodiments, when ΔV reaches the high boundary (HB) threshold of the hysteresis block, the state of the hysteresis block is set to "1."

[0094] In embodiments, when ΔV reaches the low boundary (LB) threshold of the hysteresis block, the state of the hysteresis block is set to "0."

[0095] In embodiments, the load is in a power electronic circuit in one or more of an electrode biasing power supply for a Tokamak plasma reactor, an electrode biasing power supply for a FRC

plasma reactor, a power supply for a neutral beam injector, a magnetron modulator, a klystron modulator, an E-gun modulator, a high power X-ray power supply, a mediumwave transmitter, a longwave transmitter, and a shortwave solid-state transmitter.

[0096] Embodiments of the present disclosure are directed to a multi-level hysteresis voltage controller connectable to a load. In embodiments, the multi-level hysteresis voltage controller (MHVC) comprises a low pass filter having a low-pass filter input and a low-pass filter output, a first summation block having a positive input and a negative input, a hysteresis block having a high boundary (HB) threshold and a low boundary (LB) threshold, a voltage level estimator having a plurality of voltage level estimator inputs and a voltage level output signal Levels; and a switching pattern generator having a plurality of switching pattern generator inputs and a plurality of switching pattern generator outputs.

[0097] In embodiments, the switching pattern generator comprises a comparator block, a resettable counter, a first multiplexer having a first plurality of input signals, and a second multiplexer having a second plurality of input signals.

[0098] In embodiments, each input signal of the second plurality of input signals represents an array of switching states each corresponding to a one of plurality of output levels for a voltage modulator.

[0099] In embodiments, the plurality of output levels ranges from 0VDC when all switching signals are false to a maximum output voltage when all switching signals are true.

[00100] In embodiments, the voltage level estimator comprises a clock counting circuit, a level decrement circuit comprising, an enable and reset circuit for the resettable counter, and a second summation block.

[00101] In embodiments, the clock counting circuit comprises a clock generator, a logic switch, and a resettable counter.

[00102] In embodiments, the level decrement circuit comprises a first logic element, a rising edge detector, and a free running counter.

[00103] In embodiments, the enable and reset circuit comprises a second logic element, a rising edge detector and a third logic element.

[00104] In embodiments, the first logic element is an AND gate, the logic second element is an XOR gate, and the third logic element is an OR gate.

[00105] In embodiments, when ΔV reaches the high boundary (HB) threshold of the hysteresis block, the state of the hysteresis block is set to "1."

[00106] In embodiments, when ΔV reaches the low boundary (LB) threshold of the hysteresis block, the state of the hysteresis block is set to "0."

[00107] In embodiments, the load is in a power electronic circuit in one or more of an electrode biasing power supply for a Tokamak plasma reactor, an electrode biasing power supply for a FRC plasma reactor, a power supply for a neutral beam injector, a magnetron modulator, a klystron modulator, an E-gun modulator, a high power X-ray power supply, a mediumwave transmitter, a longwave transmitter, and a shortwave solid-state transmitter.

[00108] Embodiments of the present disclosure are directed to a method of controlling a voltage supplied to a load using a multi-level hysteresis voltage controller. In embodiments, the method comprises receiving a real feedback voltage signal V_{REAL} from a voltage sensor. In embodiments, the method further comprises subtracting the real feedback voltage signal V_{REAL} from a reference voltage signal V_{REF} by: feeding the real feedback voltage signal V_{REAL} to a low-pass filter input, feeding a low-pass filter output signal to a negative input of a first summation block, feeding the reference voltage signal V_{REF} to a positive input of the summation block, and producing a voltage difference signal ΔV at an output of the first summation block.

[00109] In embodiments, the method further comprises producing, by a voltage level estimator, an estimated voltage level signal, Levels, using a high boundary (HB) threshold of a hysteresis block, a low boundary (LB) threshold of the hysteresis block, and the voltage difference signal ΔV. In embodiments, the method further comprises generating, by a switching pattern generator, a plurality of switching signals based on the estimated voltage level, Levels, and a state of the hysteresis block.

[00110] In embodiments, when ΔV reaches the high boundary (HB) threshold of the hysteresis block, the state of the hysteresis block is set to "1."

[00111] In embodiments, when ΔV reaches the low boundary (LB) threshold of the hysteresis block, the state of the hysteresis block is set to "0."

[00112] In embodiments, the voltage level estimator produces the estimated voltage level Levels by: applying a clock signal to a clock generator; counting, by a resettable counter, a number of clock signals generated by the clock generator when one or more of the following conditions is true: ΔV is lower than the low boundary (LB) threshold of the hysteresis block, or ΔV is higher than the high boundary (HB) threshold of the hysteresis block; incrementing, by a free running counter, a free running counter output signal; applying the free running counter output signal to a summation block; and decrementing a number of Levels at an output of the voltage level estimator when both of the following cases are true at the same time: the signal ΔV is lower than the low

boundary hysteresis threshold LB, and the value of an output counting signal of the resettable counter is higher than a preset value of a time constant.

[00113] In embodiments, when both the signal ΔV is lower than the low boundary hysteresis threshold LB and the value of the output counting signal of the resettable counter is higher than the preset value of a time constant, a first logic element output of a level decrement circuit becomes True; a rising edge detector detects the first logic element output; and the free running counter is incremented, thereby decrementing an output level at a summation block.

[00114] The processors of the control systems and controllers of the present disclosure may be configured to perform the computations and analyses described in the present disclosure and may include or be communicatively coupled to one or more memories including non-transitory computer readable medium. It may include a processor-based or microprocessor-based system including systems using microcontrollers, reduced instruction set computers (RISC), application specific integrated circuits (ASICs), logic circuits, and any other circuit or processor capable of executing the functions described herein. The above examples are exemplary only, and are thus not intended to limit in any way the definition and/or meaning of the term "processor" or "computer."

[00115] Functions of the processor may be implemented using either software routines, hardware components, or combinations thereof. The hardware components may be implemented using a variety of technologies, including, for example, integrated circuits or discrete electronic components. The processor unit typically includes a readable/writeable memory storage device and typically also includes the hardware and/or software to write to and/or read the memory storage device.

[00116] The processors may include a computing device, an input device, a display unit and an interface, for example, for accessing the Internet. The computer or processor may include a microprocessor. The microprocessor may be connected to a communication bus. The computer or processor may also include a memory. The memory may include Random Access Memory (RAM) and Read Only Memory (ROM). The computer or processor may also include a storage device, which may be a hard disk drive or a removable storage drive such as, e.g., an optical disk drive and the like. The storage device may also be other similar means for loading computer programs or other instructions into the computer or processor.

[00117] The processor executes a set of instructions that are stored in one or more storage elements, in order to process input data. The storage elements may also store data or other information as desired or needed. The storage element may be in the form of an information source or a physical memory element within a processing machine.

[00118] The set of instructions may include various commands that instruct the processors as a processing machine to perform specific operations such as the methods and processes of the various embodiments of the subject matter described herein. The set of instructions may be in the form of a software program. The software may be in various forms such as system software or application software. Further, the software may be in the form of a collection of separate programs or modules, a program module within a larger program or a portion of a program module. The software also may include modular programming in the form of object-oriented programming. The processing of input data by the processing machine may be in response to user commands, or in response to results of previous processing, or in response to a request made by another processing machine.

[00119] As used herein, the terms "software" and "firmware" may be interchangeable, and include any computer program stored in memory for execution by a computer, including RAM memory, ROM memory, EEPROM memory, and non-volatile RAM (NVRAM) memory. The above memory types are exemplary only, and are thus not limiting as to the types of memory usable for storage of a computer program.

[00120] All features, elements, components, functions, and steps described with respect to any embodiment provided herein are intended to be freely combinable and substitutable with those from any other embodiment. If a certain feature, element, component, function, or step is described with respect to only one embodiment, then it should be understood that that feature, element, component, function, or step can be used with every other embodiment described herein unless explicitly stated otherwise. This paragraph therefore serves as antecedent basis and written support for the introduction of claims, at any time, that combine features, elements, components, functions, and steps from different embodiments, or that substitute features, elements, components, functions, and steps from one embodiment with those of another, even if the following description does not explicitly state, in a particular instance, that such combinations or substitutions are possible. Express recitation of every possible combination and substitution is overly burdensome, especially given that the permissibility of each and every such combination and substitution will be readily recognized by those of ordinary skill in the art upon reading this description.

[00121] In many instances entities are described herein as being coupled to other entities. It should be understood that the terms "coupled" and "connected" or any of their forms are used interchangeably herein and, in both cases, are generic to the direct coupling of two entities without any non-negligible e.g., parasitic intervening entities and the indirect coupling of two entities with one or more non-negligible intervening entities. Where entities are shown as being directly coupled together, or described as coupled together without description of any intervening entity, it should

be understood that those entities can be indirectly coupled together as well unless the context clearly dictates otherwise.

[00122] While the embodiments are susceptible to various modifications and alternative forms, specific examples thereof have been shown in the drawings and are herein described in detail. It should be understood, however, that these embodiments are not to be limited to the particular form disclosed, but to the contrary, these embodiments are to cover all modifications, equivalents, and alternatives falling within the spirit of the disclosure. Furthermore, any features, functions, steps, or elements of the embodiments may be recited in or added to the claims, as well as negative limitations that define the inventive scope of the claims by features, functions, steps, or elements that are not within that scope.

WHAT IS CLAIMED IS:

1. A multi-level cascaded voltage modulator connectable to a load, comprising:

a plurality of power cells connected in series, wherein each cell of the plurality of cells comprises a of bidirectional switch and a storage element; and

a control system coupled to the plurality of cells and having a multi-level hysteresis voltage controller, wherein the control system is configured to cause the plurality of cells to output N levels of voltage on the load, wherein N is a positive integer corresponding to the number of power cells of the plurality of power cells.

2. The modulator of claim 1, wherein each cell of the plurality of cells includes

a secondary winding isolation transformer;

a three-phase diode bridge coupled to the transformer and the storage element; and

a diode.

3. The modulator of claim 2, wherein the bidirectional switch is one of an IGBT or a MOSFET.

4. The modulator of claim 2, wherein each cell of the plurality of cells further comprises an LCR filter at its output.

5. The modulator of claim 2, further comprising a CR filter at the output of the plurality of cells.

6. The modulator of claim 2, wherein the control system is further configured to cause the transfer of electrical power from the energy storage elements of the power cells to the load.

7. The modulator of claim 2, wherein the control system is further configured to balance voltages on the storage elements.

8. The modulator of claim 2, wherein the storage element is a capacitor.

9. The modulator of claims 1-8, wherein the control system including one or more processors coupled to a non-transitory memory comprising a plurality of instructions that when executed causes the one or more processors to control a level of voltage on the load.

10. The modulator of claim 9, wherein the plurality of instructions when executed causes the one or more processors to control an output voltage level of the modulator as a function of the level of voltage on the load, a reference voltage and a voltage error equal to the difference between the level of voltage on the load and the reference voltage.

11. The modulator of claim 9, wherein the plurality of instructions when executed causes the one or more processors to:

subtract from a reference voltage signal V_{REF} a real feedback voltage signal V_{REAL} received from a voltage sensor;

produce, by a voltage level estimator, an estimated voltage level signal, Levels, using a high boundary (HB) threshold of a hysteresis block, a low boundary (LB) threshold of the hysteresis block, and the voltage difference signal ΔV; and

generate, by a switching pattern generator, a plurality of switching signals based on the estimated voltage level, Levels, and a state of the hysteresis block.

12. The modulator of claim 9, wherein to subtract from a reference voltage signal V_{REF} a real feedback voltage signal V_{REAL}, the plurality of instructions when executed causes the one or more processors to:

feed the real feedback voltage signal V_{REAL} to a low-pass filter input;

feed a low-pass filter output signal to a negative input of a first summation block;

feed the reference voltage signal V_{REF} to a positive input of the first summation block; and

produce a voltage difference signal ΔV at an output of the first summation block.

13. The modulator of claim 11, wherein:

when ΔV reaches the high boundary (HB) threshold of the hysteresis block, the plurality of instructions when executed causes the one or more processors to set the state of the hysteresis block to "1."

14. The modulator of one of claims 11 or 13, wherein:

when ΔV reaches the low boundary (LB) threshold of the hysteresis block, the plurality of instructions when executed causes the one or more processors to set the state of the hysteresis block to "0."

15. The modulator of claim 11, wherein to produce the estimated voltage level Levels, the plurality of instructions when executed causes the one or more processors to:

apply a clock signal to a clock generator;

count, by a resettable counter, a number of clock signals generated by the clock generator when one or more of the following conditions is true:

ΔV is lower than the low boundary (LB) threshold of the hysteresis block; or

ΔV is higher than the high boundary (HB) threshold of the hysteresis block;

increment, by a free running counter, a free running counter output signal;

apply the free running counter output signal to a second summation block; and

decrement a number of Levels at an output of the voltage level estimator when both of the following cases are true at the same time:

the signal ΔV is lower than the low boundary hysteresis threshold LB; and

the value of an output counting signal of the resettable counter is higher than a preset value of a time constant.

16. The modulator of claim 15, wherein when both the signal ΔV is lower than the low boundary hysteresis threshold LB and the value of the output counting signal of the resettable counter is higher than the preset value of a time constant, the plurality of instructions when executed causes the one or more processors to:

set the output of a logic element of a level decrement circuit to True;

detect the output of the logic element with a rising edge detector; and

increment the free running counter, and thereby decrement an output level at a summation block.

17. The modulator of claim 1, wherein the multi-level hysteresis voltage controller comprises:

a low pass filter having a low-pass filter input and a low-pass filter output;

a first summation block having a positive input and a negative input;

a hysteresis block having a high boundary (HB) threshold and a low boundary (LB) threshold;

a voltage level estimator having a plurality of voltage level estimator inputs and a voltage level output signal Levels; and

a switching pattern generator having a plurality of switching pattern generator inputs and a plurality of switching pattern generator outputs.

18. The modulator of claim 17, wherein the switching pattern generator comprises:

a comparator block;

a resettable counter;

a first multiplexer having a first plurality of input signals; and

a second multiplexer having a second plurality of input signals.

19. The modulator of claim 18, wherein each input signal of the second plurality of input signals represents an array of switching states each corresponding to a one of plurality of output levels for a voltage modulator.

20. The modulator of claim 19, wherein the plurality of output levels ranges from 0VDC when all switching signals are false to a maximum output voltage when all switching signals are true.

21. The modulator of claim 17, wherein the voltage level estimator comprises:

a clock counting circuit;

a level decrement circuit;

an enable and reset circuit for the resettable counter; and

a second summation block.

22. The modulator of claim 21, wherein the clock counting circuit comprises a clock generator, a logic switch, and a resettable counter.

23. The modulator of claim 21 or 22, wherein the level decrement circuit comprises a first logic element, a rising edge detector, and a free running counter.

24. The modulator of claims 21-23, wherein the enable and reset circuit comprises a second logic element, a rising edge detector and a third logic element.

25. The modulator of claim 24, wherein the first logic element is an AND gate, the second logic element is an XOR gate, and the third logic element is an OR gate.

26. The modulator of claim 17, wherein when ΔV reaches the high boundary (HB) threshold of the hysteresis block, the state of the hysteresis block is set to "1."

27. The modulator of claims 17 or 26, wherein when ΔV reaches the low boundary (LB) threshold of the hysteresis block, the state of the hysteresis block is set to "0."

28. The modulator of any one of claims 17-27, wherein the load is in a power electronic circuit in one or more of an electrode biasing power supply for a Tokamak plasma reactor, an electrode biasing power supply for a FRC plasma reactor, a power supply for a neutral beam injector, a magnetron modulator, a klystron modulator, an E-gun modulator, a high power X-ray power supply, a mediumwave transmitter, a longwave transmitter, and a shortwave solid-state transmitter.

29. A multi-level hysteresis voltage controller for a multi-level voltage modulator connectable to a load, comprising:

a low pass filter having a low-pass filter input and a low-pass filter output;

a first summation block having a positive input and a negative input;

a hysteresis block having a high boundary (HB) threshold and a low boundary (LB) threshold;

a voltage level estimator having a plurality of voltage level estimator inputs and a voltage level output signal Levels; and

a switching pattern generator having a plurality of switching pattern generator inputs and a plurality of switching pattern generator outputs.

30. The multi-level hysteresis voltage controller of claim 29, wherein the switching pattern generator comprises:

a comparator block;

a resettable counter;

a first multiplexer having a first plurality of input signals; and

a second multiplexer having a second plurality of input signals.

31. The multi-level hysteresis voltage controller of claim 30, wherein each input signal of the second plurality of input signals represents an array of switching states each corresponding to a one of plurality of output levels for a voltage modulator.

32. The multi-level hysteresis voltage controller of claim 31, wherein the plurality of output levels ranges from 0VDC when all switching signals are false to a maximum output voltage when all switching signals are true.

33. The multi-level hysteresis voltage controller of claim 29, wherein the voltage level estimator comprises:

a clock counting circuit;

a level decrement circuit ;

an enable and reset circuit for the resettable counter; and

a second summation block.

34. The multi-level hysteresis voltage controller of claim 33, wherein the clock counting circuit comprises a clock generator, a logic switch, and a resettable counter.

35. The multi-level hysteresis voltage controller of claim 33 or 34, wherein the level decrement circuit comprises a first logic element, a rising edge detector, and a free running counter.

36. The multi-level hysteresis voltage controller of and of claims 33-35, wherein the enable and reset circuit comprises a second logic element, a rising edge detector and a third logic element.

37. The multi-level hysteresis voltage controller of claim 36, wherein the first logic element is an AND gate, the second logic element is an XOR gate, and the third logic element is an OR gate.

38. The multi-level hysteresis voltage controller of claim 29, wherein when ΔV reaches the high boundary (HB) threshold of the hysteresis block, the state of the hysteresis block is set to "1."

39. The multi-level hysteresis voltage controller of claims 29 or 38, wherein when ΔV reaches the low boundary (LB) threshold of the hysteresis block, the state of the hysteresis block is set to "0."

40. The multi-level hysteresis voltage controller of any one of claims 29-39, wherein the load is in a power electronic circuit in one or more of an electrode biasing power supply for a Tokamak plasma reactor, an electrode biasing power supply for a FRC plasma reactor, a power supply for a neutral beam injector, a magnetron modulator, a klystron modulator, an E-gun modulator, a high power X-ray power supply, a mediumwave transmitter, a longwave transmitter, and a shortwave solid-state transmitter.

41. A method of controlling a voltage supplied to a load using a multi-level hysteresis voltage controller, comprising:

receiving a real feedback voltage signal V_{REAL} from a voltage sensor;

subtracting the real feedback voltage signal V_{REAL} from a reference voltage signal V_{REF} by

feeding the real feedback voltage signal V_{REAL} to a low-pass filter input;

feeding a low-pass filter output signal to a negative input of a first summation block;

feeding the reference voltage signal V_{REF} to a positive input of the first summation block; and

producing a voltage difference signal ΔV at an output of the first summation block;

producing, by a voltage level estimator, an estimated voltage level signal, Levels, using a high boundary (HB) threshold of a hysteresis block, a low boundary (LB) threshold of the hysteresis block, and the voltage difference signal ΔV; and

generating, by a switching pattern generator, a plurality of switching signals based on the estimated voltage level, Levels, and a state of the hysteresis block.

42. The method of claim 41, wherein:

when ΔV reaches the high boundary (HB) threshold of the hysteresis block, the state of the hysteresis block is set to "1."

43. The method of one of claims 41 or 42, wherein:

when ΔV reaches the low boundary (LB) threshold of the hysteresis block, the state of the hysteresis block is set to "0."

44. The method of claim 43, wherein the voltage level estimator produces the estimated voltage level Levels by:

applying a clock signal to a clock generator;

counting, by a resettable counter, a number of clock signals generated by the clock generator when one or more of the following conditions is true:

ΔV is lower than the low boundary (LB) threshold of the hysteresis block; or

ΔV is higher than the high boundary (HB) threshold of the hysteresis block;

incrementing, by a free running counter, a free running counter output signal;

applying the free running counter output signal to a second summation block; and

decrementing a number of Levels at an output of the voltage level estimator when both of the following cases are true at the same time:

the signal ΔV is lower than the low boundary hysteresis threshold LB; and

the value of an output counting signal of the resettable counter is higher than a preset value of a time constant.

45. The method of claim 44, wherein when both the signal ΔV is lower than the low boundary hysteresis threshold LB and the value of the output counting signal of the resettable counter is higher than the preset value of a time constant:

a logic element output of a level decrement circuit becomes True;

a rising edge detector detects the logic element output; and

the free running counter is incremented, thereby decrementing an output level at a summation block.

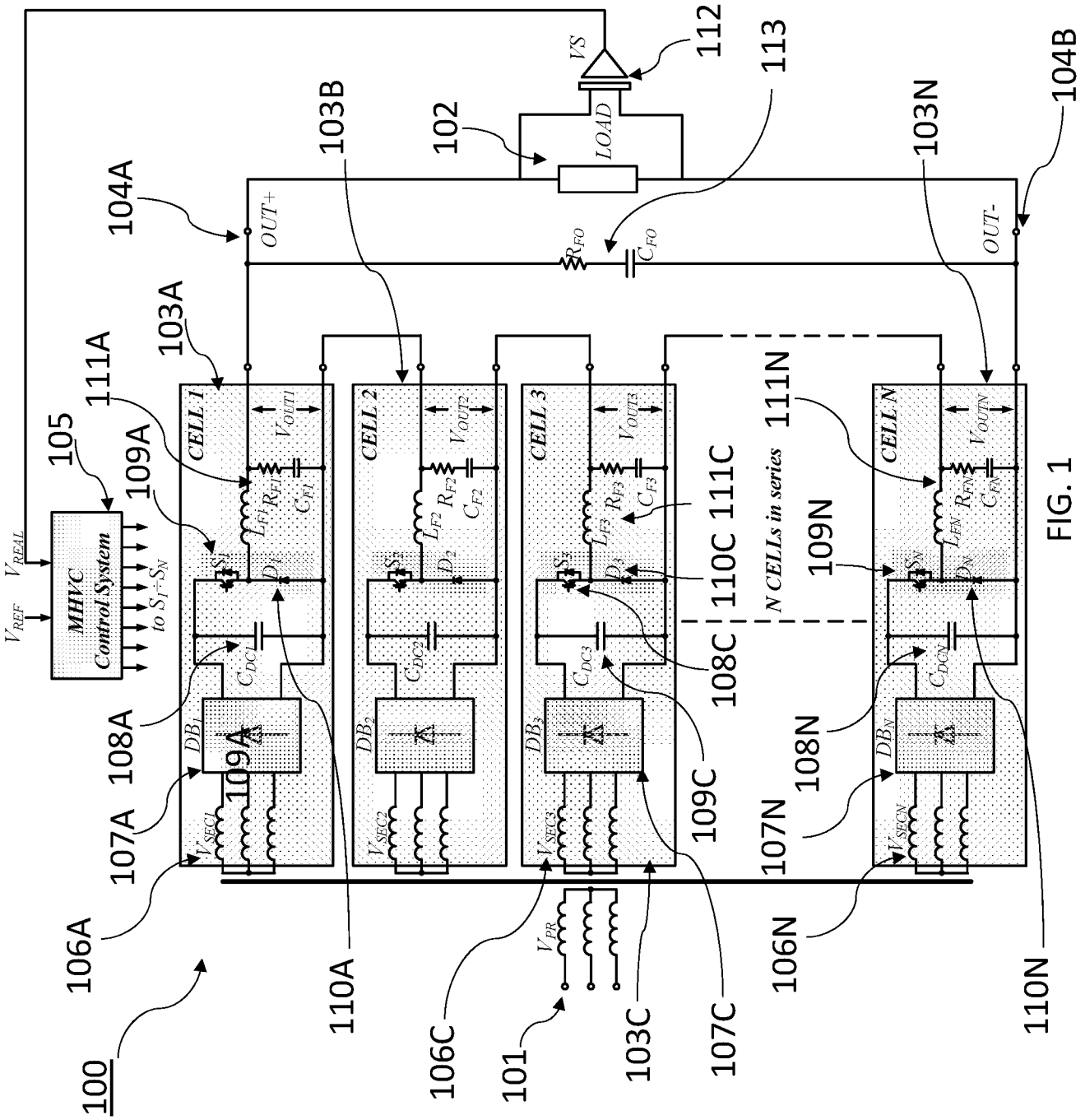
100
101
102
103A
103B
103C
103N
104A
104B
105
106A
106C
106N
107A
107C
107N
108A
108C
108N
109A
109C
109N
110A
110C
110N
111A
111C
111N
112
113
MHVC Control System
V_{REAL}
V_{REF}
to S_1÷S_N
CELL 1
CELL 2
CELL 3
CELL N
N CELLs in series
LOAD
VS
OUT+
OUT-
R_{FO}
C_{FO}
V_{PR}

FIG. 1

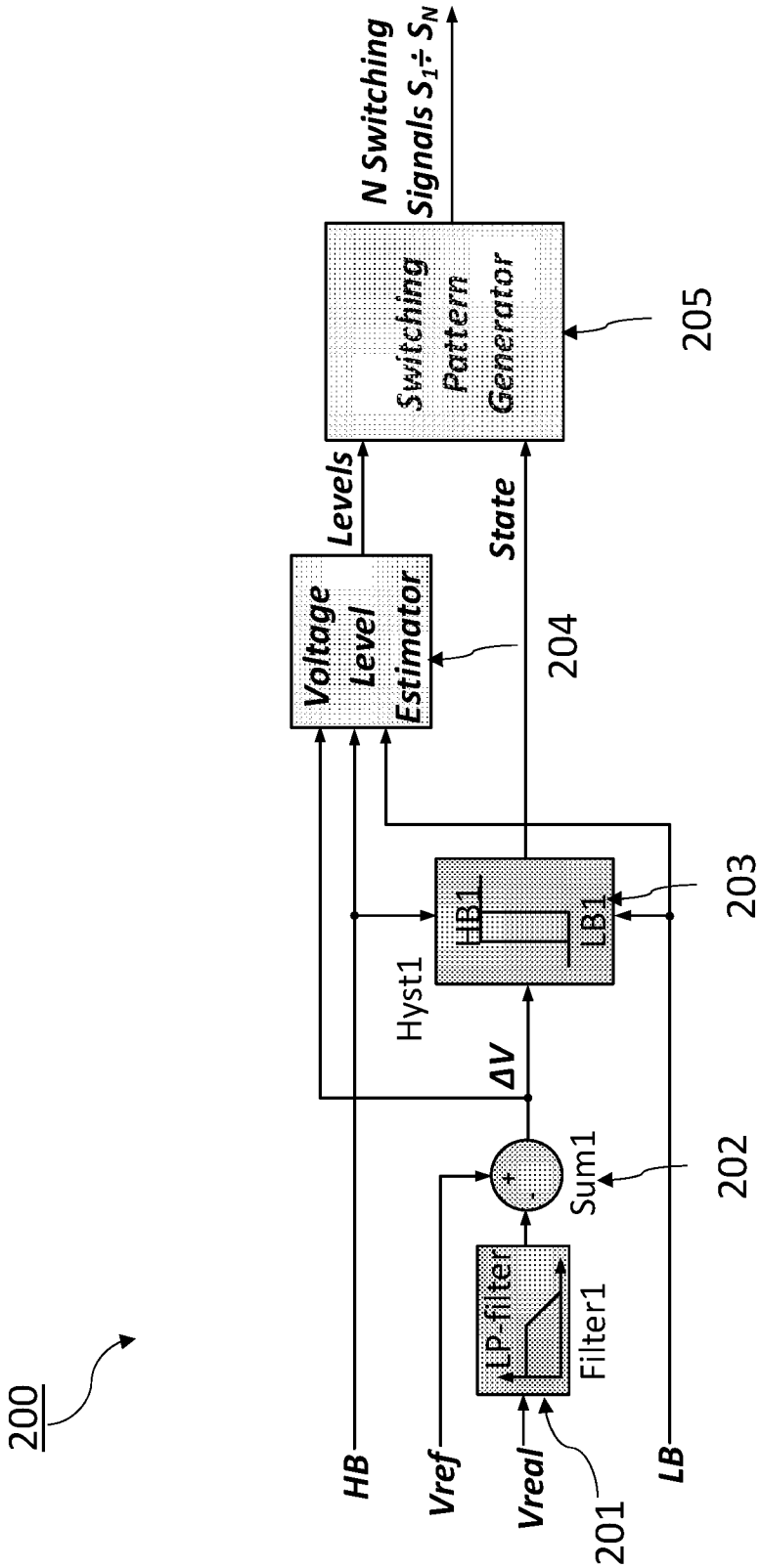
200
HB
Vref
Vreal
201
LB
LP filter
Filter1
Sum1
202
ΔV
Hyst1
HB1
LB1
203
Voltage Level Estimator
204
Levels
State
Switching Pattern Generator
205
N Switching Signals $S_1 \div S_N$

FIG. 2

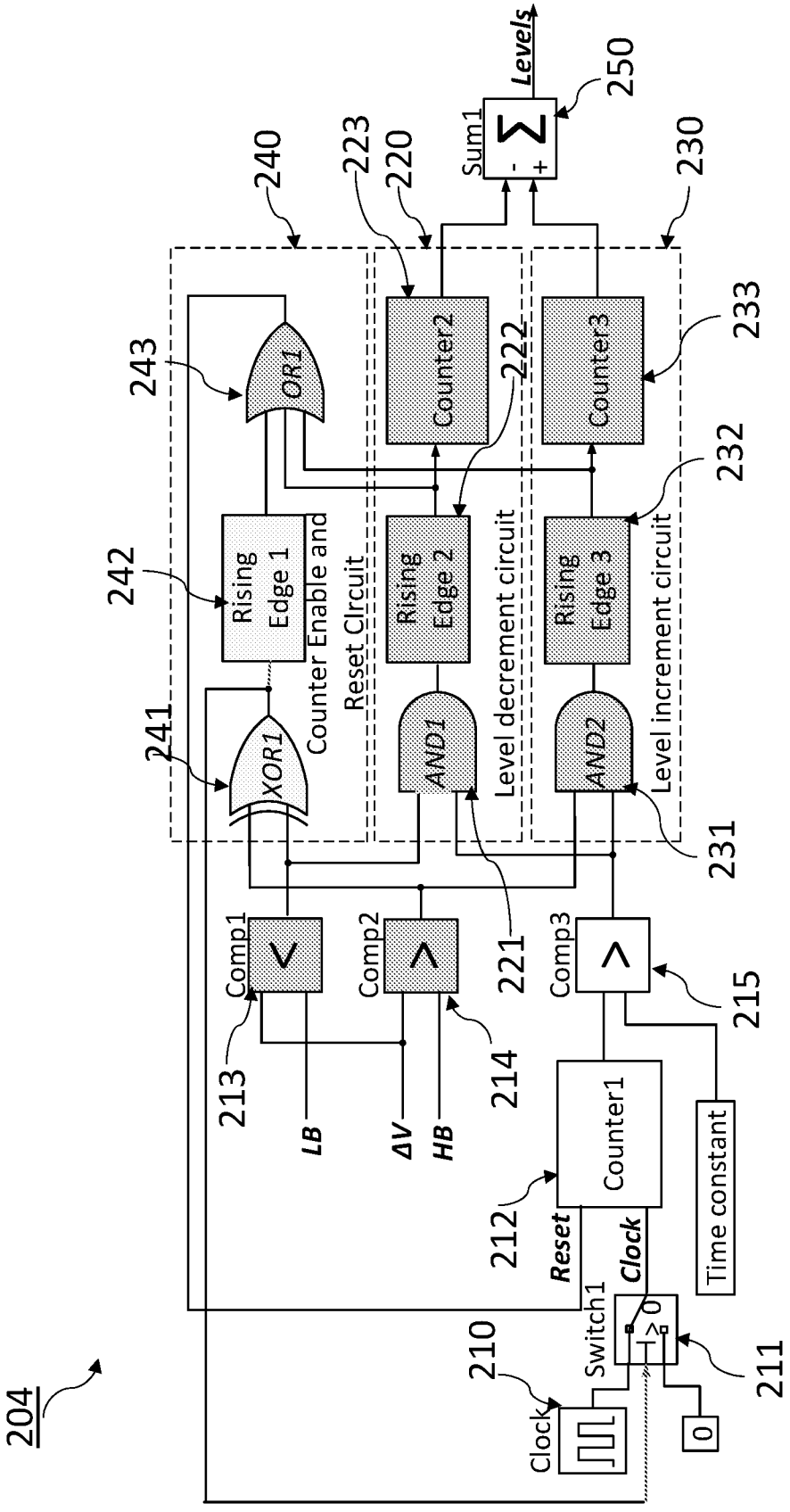
204
210
Clock
211
Switch1
≥ 0
0
212
Reset
Clock
Counter1
Time constant
213
LB
214
ΔV
HB
215
Comp1
Comp2
Comp3
221
222
223
220
Sum1
Levels
250
230
240
233
232
231
243
OR1
242
Rising Edge 1
Counter Enable and Reset CIrcuit
241
XOR1
Counter2
Rising Edge 2
AND1
Level decrement circuit
Counter3
Rising Edge 3
AND2
Level increment circuit

FIG. 3

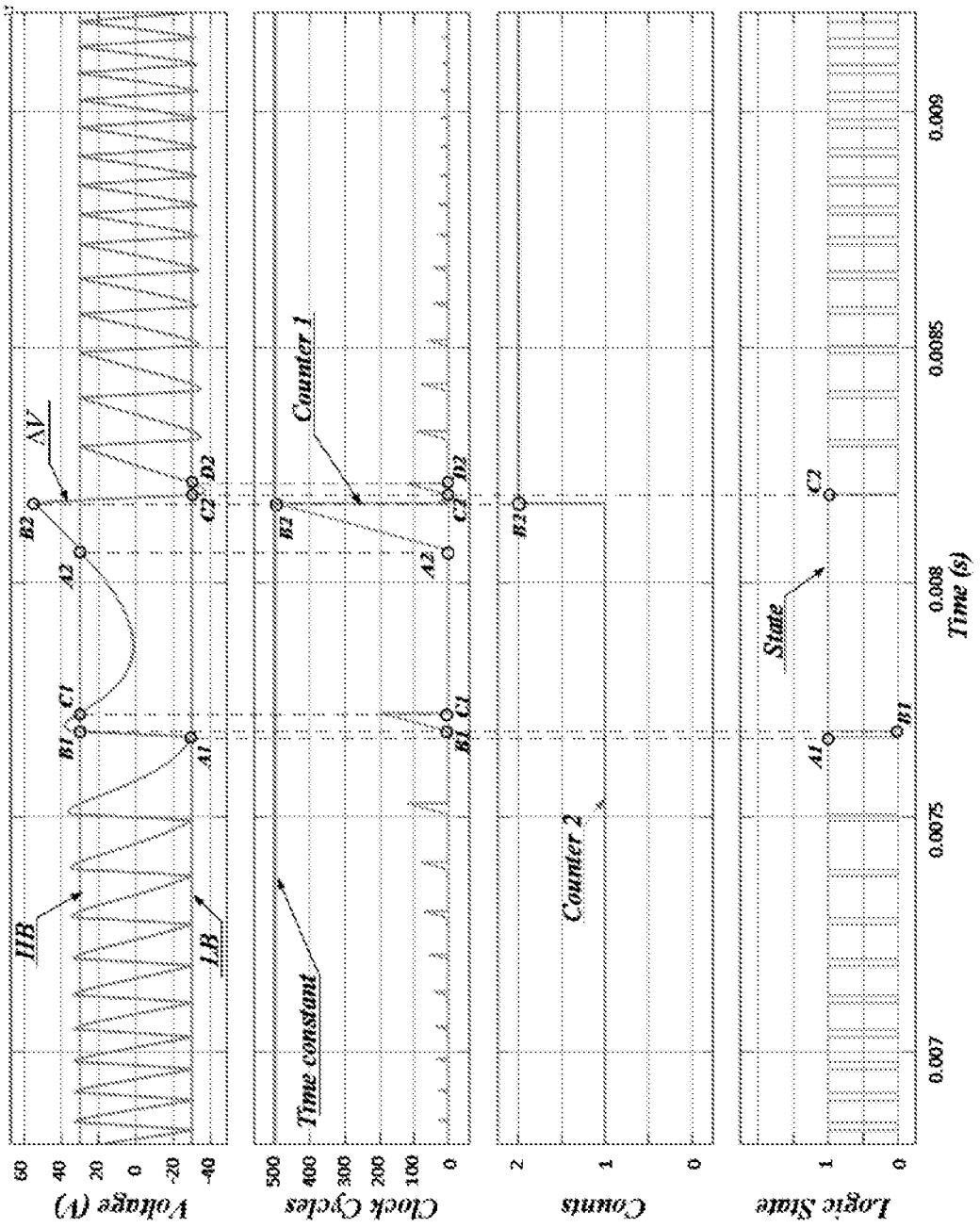

FIG. 4A

FIG. 4B

FIG. 4C

FIG. 4D

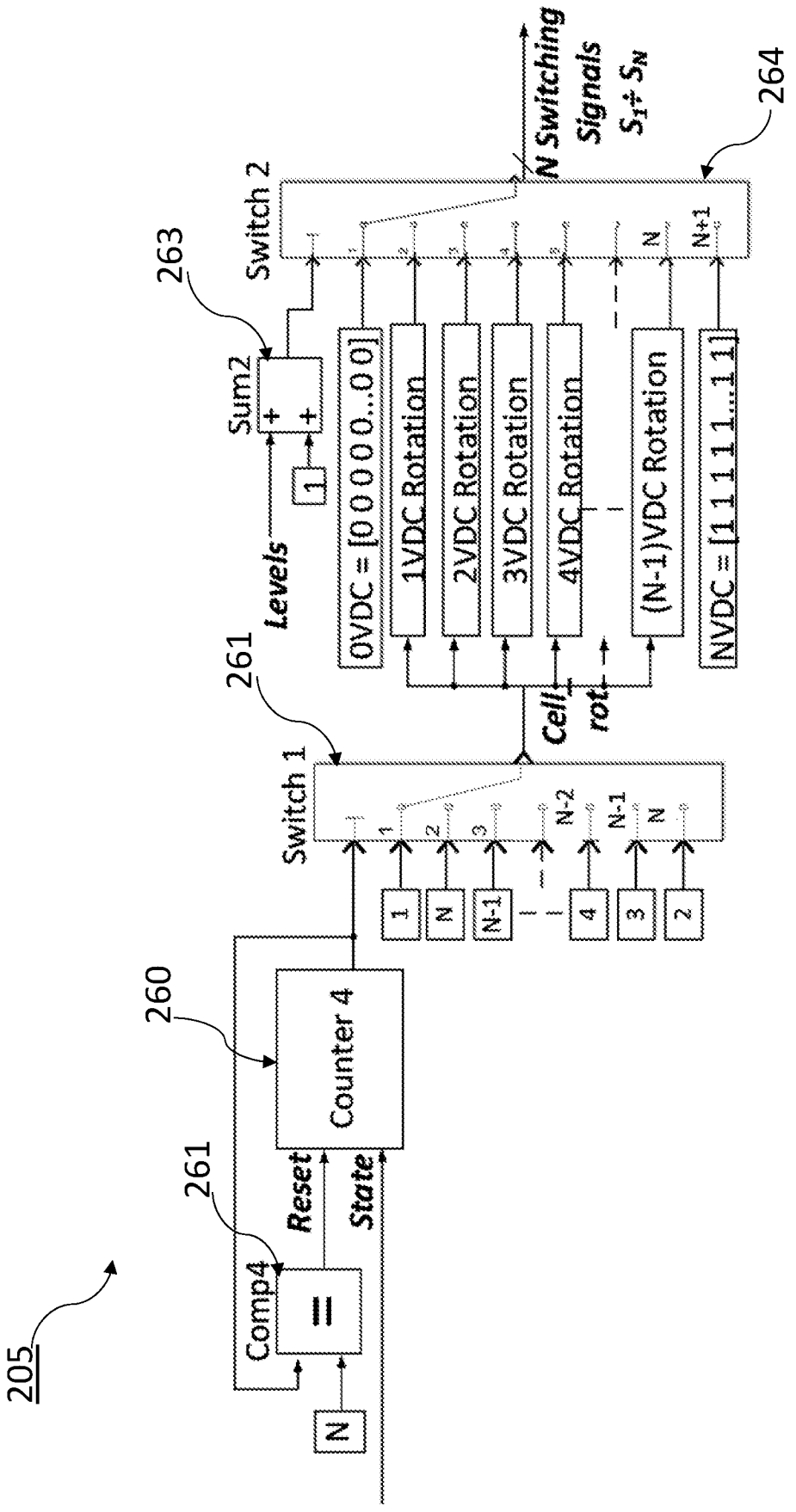
205
260
Counter 4
Reset
State
261
Comp4
=
N
261
Switch 1
Levels
Cell rot
1
N
N-1
4
3
2
263
Sum2
+
+
1
264
Switch 2
N Switching Signals
S_1 - S_N
0VDC = [0 0 0 0 0 0...0 0]
1VDC Rotation
2VDC Rotation
3VDC Rotation
4VDC Rotation
(N-1)VDC Rotation
NVDC = [1 1 1 1 1 1...1 1]

FIG. 5

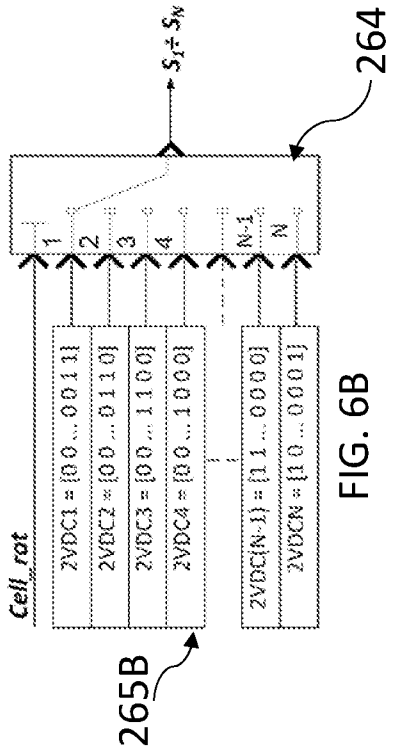

FIG. 6A

FIG. 6B

FIG. 6C

FIG. 6D

FIG. 6E

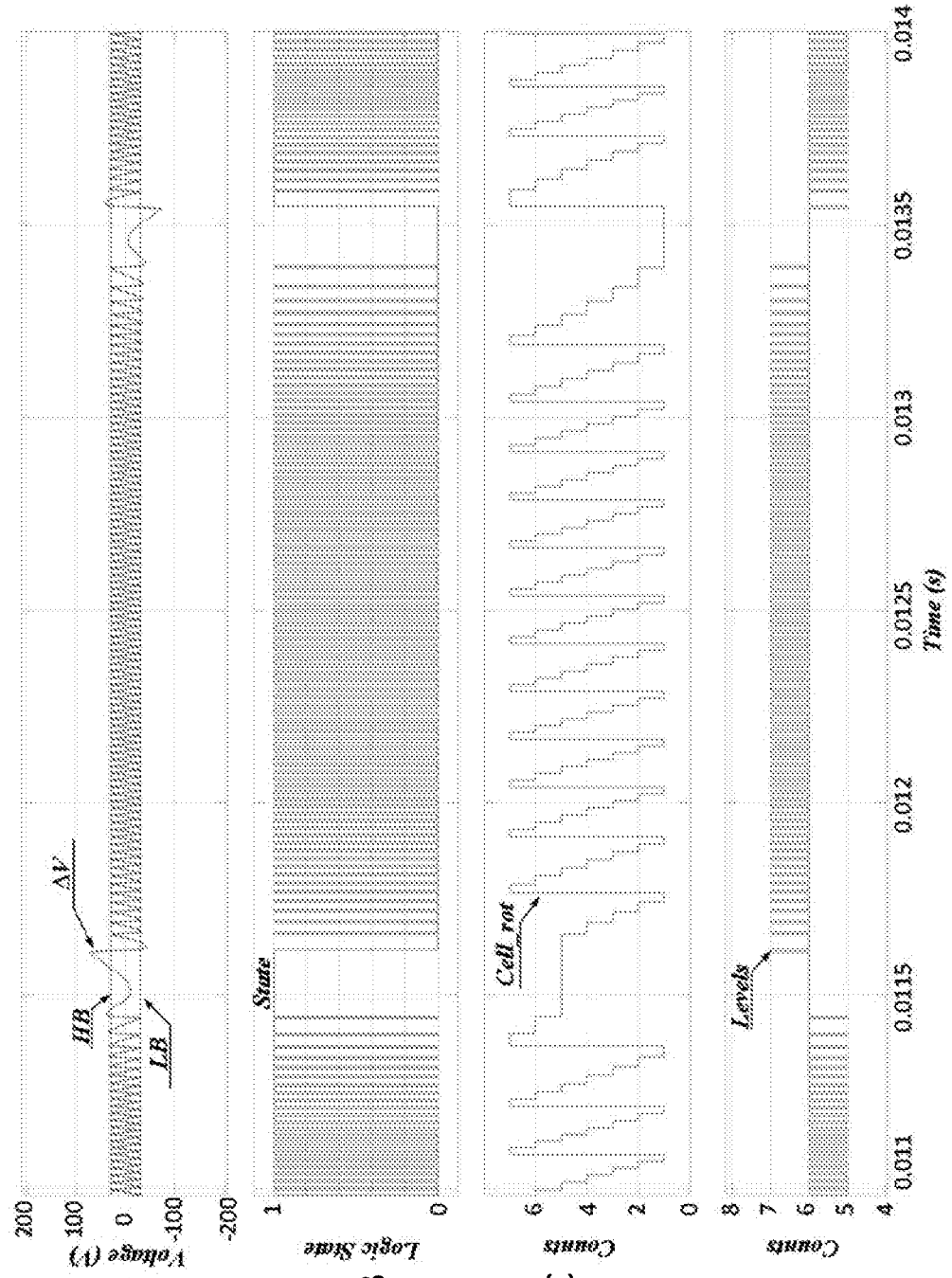

FIG. 7A

FIG. 7B

FIG. 7C

FIG. 7D

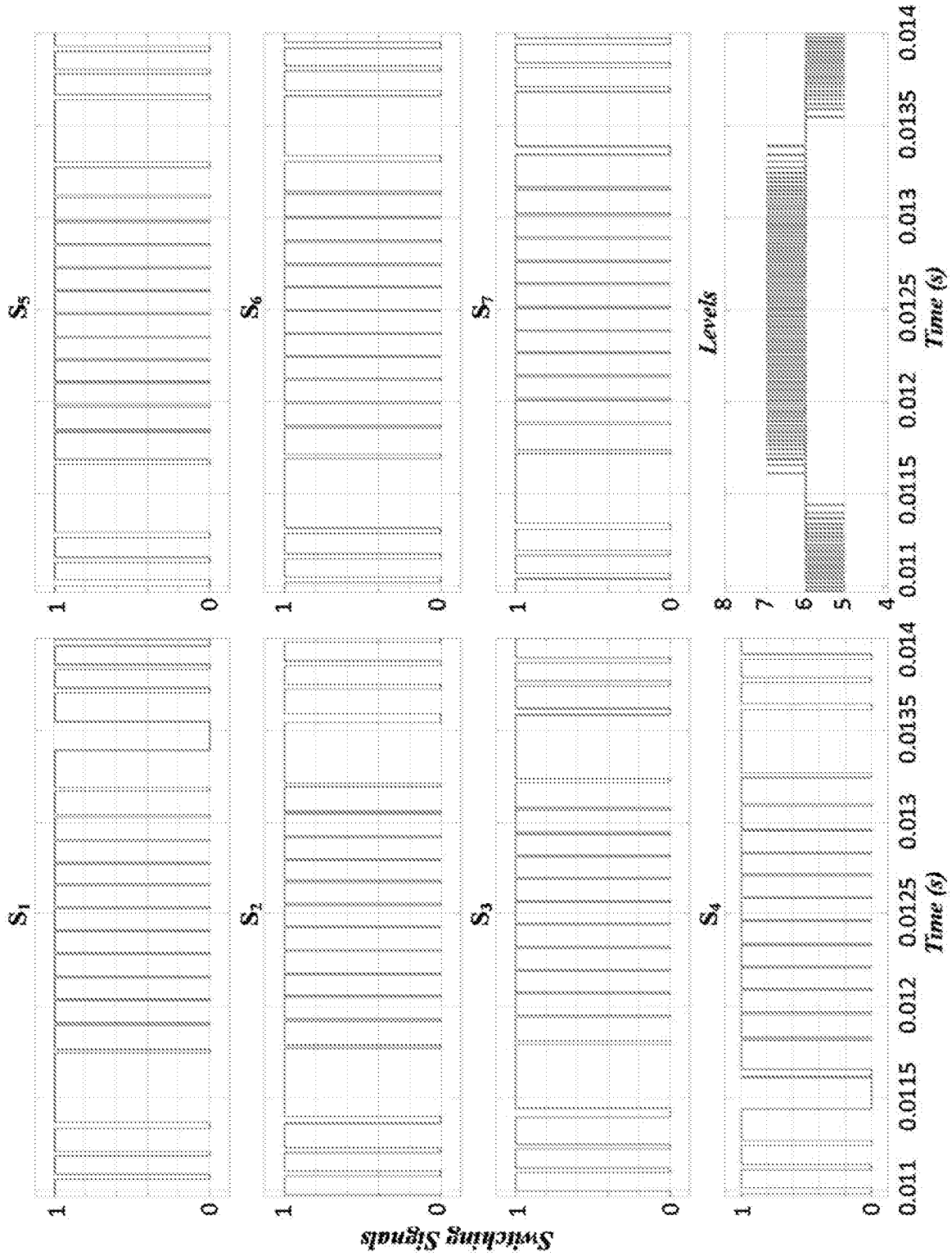
Switching Signals
S1
S2
S3
S4
S5
S6
S7
Levels
Time (s)
Time (s)
0.011
0.0115
0.012
0.0125
0.013
0.0135
0.014
1
0
8
7
6
5
4

FIG. 8

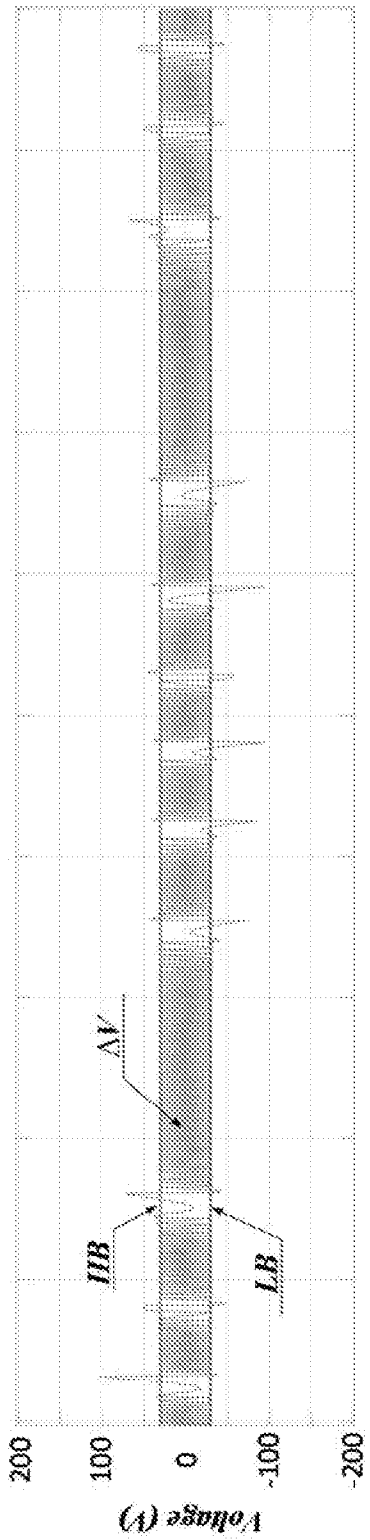

FIG. 9A

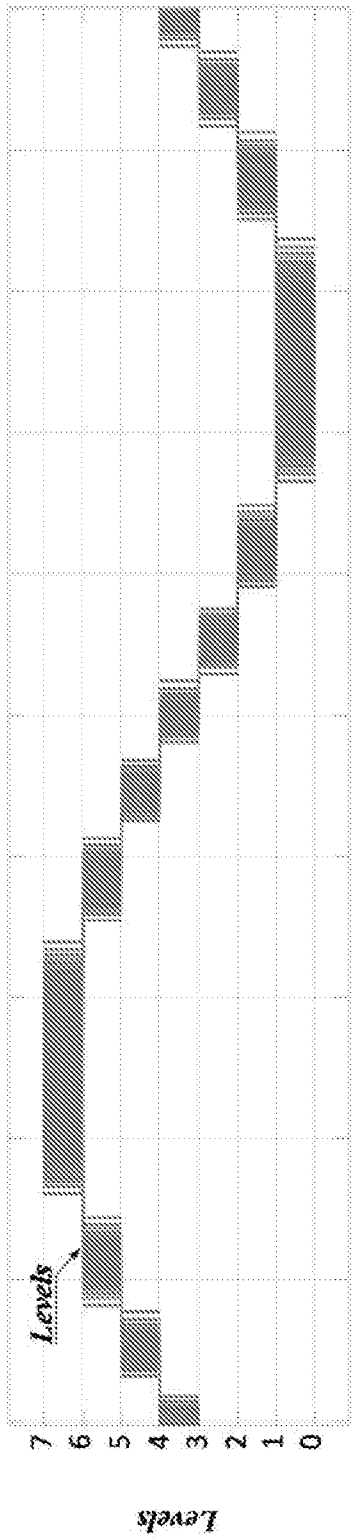

FIG. 9B

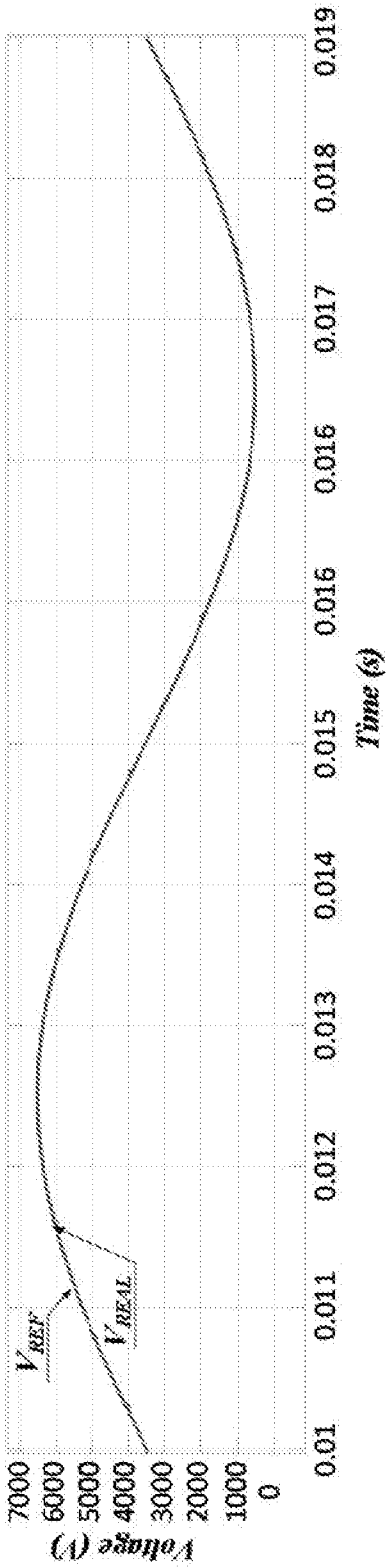

FIG. 9C

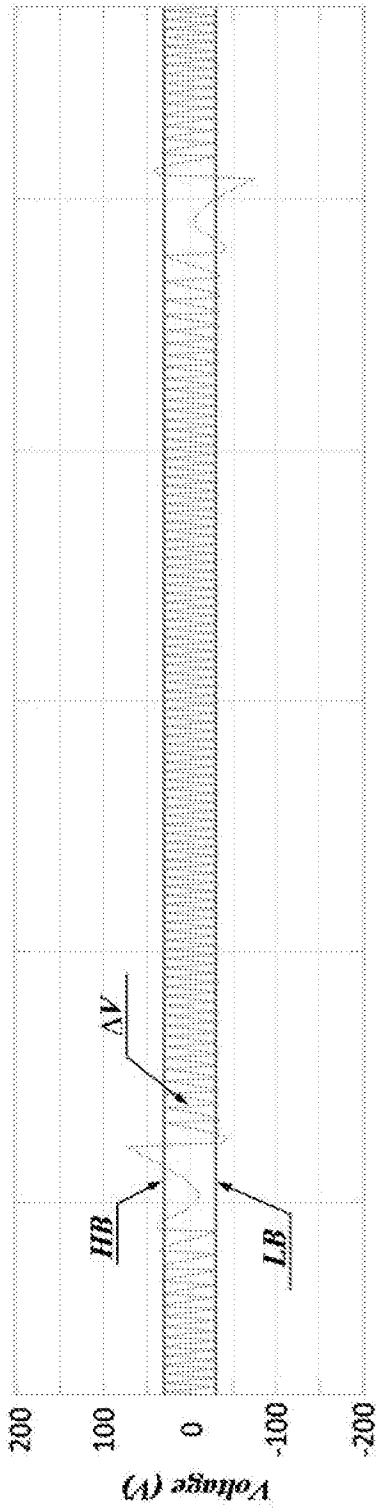

FIG. 10A

FIG. 10B

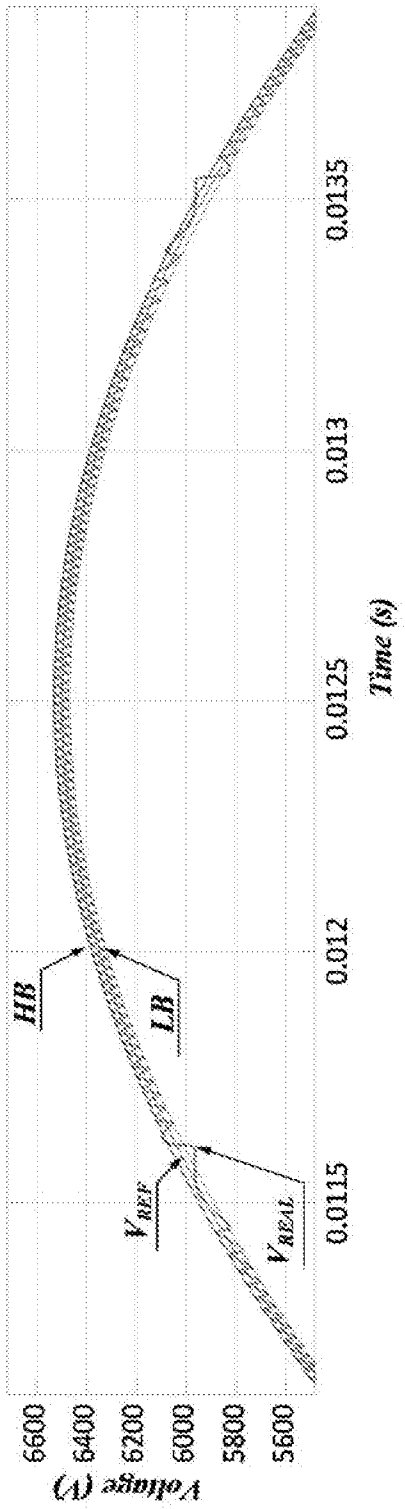

FIG. 10C

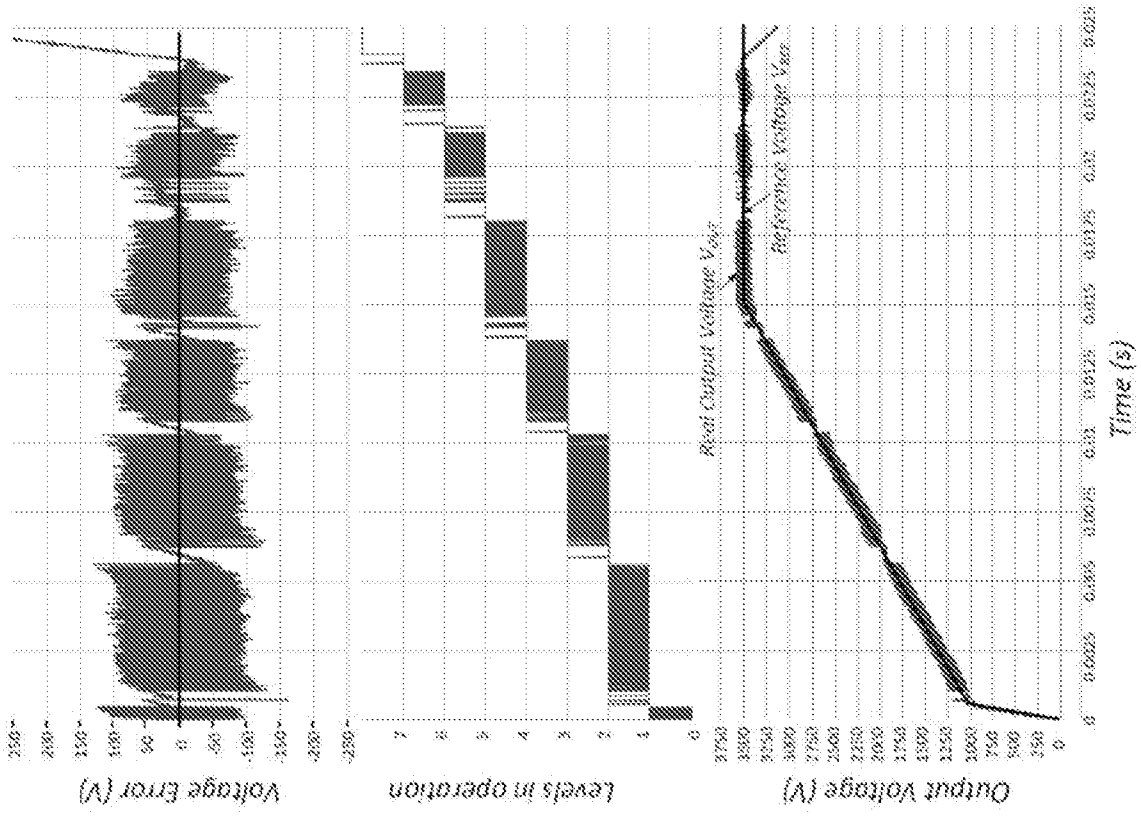

FIG. 11A

FIG. 11B

FIG. 11C

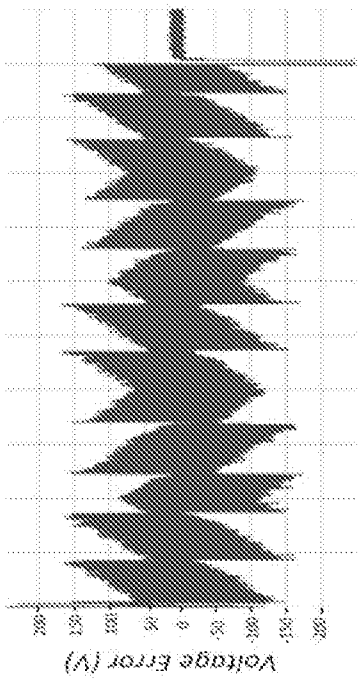

FIG. 12A

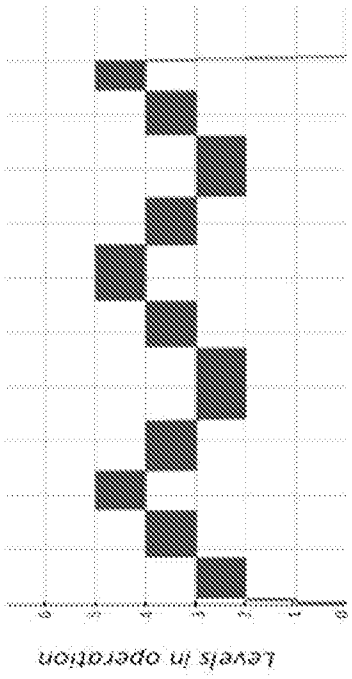

FIG. 12B

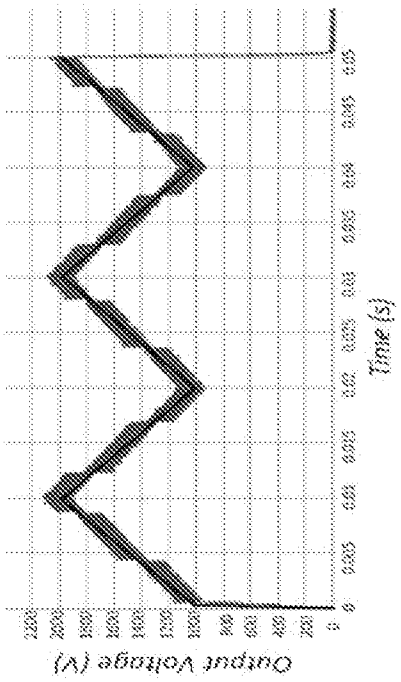

FIG. 12C

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US18/38089

A. CLASSIFICATION OF SUBJECT MATTER
IPC - H02M 7/483, 7/54, 7/86 (2018.01)
CPC - H02M 7/483, 7/54, 7/86; H01M 10/441

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
See Search History document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
See Search History document

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
See Search History document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2011/0198936 A1 (GRAOVAC, D et al.) August 18, 2011; FIG. 1, paragraphs [0027], [0029]-[0036], [0054], & [0077]	1-10
Y	WO 2014/193254 A1 (INSTITUTO SUPERIOR TECNICO et al.) December 4, 2014; page 4, lines 24-30, page 14, lines 21-32, page 15	1-10
Y	US 2015/0303820 A1 (GEO27 S.A.R.L) October 22, 2015; FIG. 3, paragraphs [0052], [0053], & [0057]	2, 3, 6-8, 9/2, 9/3, 9/6-9/8, 10/9/2, 10/9/3, & 10/9/6-10/9/8
Y	US 2013/0083563 A1 (WANG, D et al.) April 4, 2013; paragraph [0028]	4, 5, 9/4, 9/5, 10/9/4, & 10/9/5
A	US 2014/0239927 A1 (FREESCALE SEMICONDUCTOR, INC.) August 28, 2014; paragraphs [0030]-[0032] & [0036], claim 4	1-13, 15-23, 26-27, 29-35, 38-39, & 41-45
A	US 2013/0088254 A1 (HOANG, A et al.) April 11, 2013; paragraphs [0043] & [0047]	1-13, 15-23, 26-27, 29-35, 38-39, & 41-45
A	US 2010/0301827 A1 (CHEN, W et al.) December 2, 2010; FIG. 4, paragraphs [0025], [0029], & [0046]	1-13, 15-23, 26-27, 29-35, 38-39, & 41-45
A	US 2004/0008016 A1 (SUTARDJA, S et al.) January 15, 2004; FIG. 12A, paragraphs [0097]-[0099] & [0135]	1-13, 15-23, 26-27, 29-35, 38-39, & 41-45

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
11 October 2018 (11.10.2018)	29 OCT 2018
Name and mailing address of the ISA/ Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-8300	Authorized officer Shane Thomas PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (January 2015)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US18/38089

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☒ Claims Nos.: 14, 24-25, 28, 36-37, & 40
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:
See extra sheet.

1. ☒ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☒ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US18/38089

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6,373,734 B1 (MARTINELLI, R) April 16, 2002; FIG. 2, FIG. 2, column 6, lines 6-13 & 61-67, column 7, lines 3-14	1-13, 15-23, 26-27, 29-35, 38-39, & 41-45
A	US 2006/0097782 A1 (EBNER, C) May 11, 2006; FIG. 3, paragraphs [0047] & [0048]	1-13, 15-23, 26-27, 29-35, 38-39, & 41-45
A	US 2010/0085789 A1 (ULRICH, J et al.) April 8, 2010; FIG. 9, FIG. 10, paragraphs [0039], [0043], [0083]-[0088], & [00092]-[0093]	1-13, 15-23, 26-27, 29-35, 38-39, & 41-45
A	US 2013/0088903 A1 (SAGONA, J et al.) April 11, 2013; FIG. 1, paragraphs [0008], [0009], & [0012]	1-13, 15-23, 26-27, 29-35, 38-39, & 41-45
A	US 2015/0296292 A1 (APPLE INC.) October 15, 2015; FIG. 1A, paragraph [0027], claim 14	1-13, 15-23, 26-27, 29-35, 38-39, & 41-45

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US18/38089

-***-Continued from Box III: Observations where unity of invention is lacking-***-

This application contains the following inventions or groups of inventions which are not so linked as to form a single general inventive concept under PCT Rule 13.1. In order for all inventions to be examined, the appropriate additional examination fee must be paid.

Group I: Claims 1-13, 15-23, and 26-27 are directed towards a multi-level cascaded voltage modulator.
Group II: Claims 29-35, 38-39, and 41-45 are directed towards a multi-level hysteresis voltage controller and a method of controlling a voltage.

The inventions listed as Groups I-II do not relate to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons:

The special technical features of Group I include at least a plurality of power cells connected in series, wherein each cell of the plurality of cells comprises a of bidirectional switch and a storage element; and wherein the control system is configured to cause the plurality of cells to output N levels of voltage on the load, wherein N is a positive integer corresponding to the number of power cells of the plurality of power cells, which are not present in Group II.

The special technical features of Group II include at least a low pass filter having a low-pass filter input and a low-pass filter output; a first summation block having a positive input and a negative input; a hysteresis block having a high boundary (HB) threshold and a low boundary (LB) threshold; a voltage level estimator having a plurality of voltage level estimator inputs and a voltage level output signal Levels; and a switching pattern generator having a plurality of switching pattern generator inputs and a plurality of switching pattern generator outputs, which are not present in Group I.

The common technical features shared by Groups I-II are a multi-level hysteresis voltage controller. However, these common features are previously disclosed by US 2013/0335043 A1 to TDK-LAMBDA CORPORATION (hereinafter "TDK"). TDK discloses a multi-level hysteresis voltage controller (a multi-level voltage regulator using Vin voltage step hysteresis).

Since the common technical features are previously disclosed by the TDK reference, these common features are not special and so Groups I-II lack unity.