(12) UK Patent Application (19) GB (11) 2 312 525 (13) A

(43) Date of A Publication 29.10.1997

(21) Application No 9608615.2

(22) Date of Filing 24.04.1996

(71) Applicant(s)
Northern Telecom Limited

(Incorporated in Canada - Quebec)

World Trade Center of Montreal,
380 St Antoine Street West,8th Floor, Montreal,
Quebec H2Y 3Y4, Canada

(72) Inventor(s)
Suresh Mishrilal Ojha
Jonathan Paul Stagg

(74) Agent and/or Address for Service
Nortel Patents
London Road, HARLOW, Essex, CM17 9NA,
United Kingdom

(51) INT CL^6
G02B 6/10 , C23C 16/56

(52) UK CL (Edition O)
G2J JGDA
C7F FHE FHX FP905 FQ913 FQ914 FR901 FR903 FR913 FR919 F802
U1S S1915

(56) Documents Cited

GB 2292468 A	**GB 2066805 A**	**EP 0617301 A1**
EP 0607884 A1	**EP 0603530 A2**	**EP 0545432 A1**
EP 0476688 A2	**EP 0331335 A2**	**EP 0281800 A2**
WO 93/16403 A1		

Applied Optics 1 Sept 1993 Vol32 No25 pp4916-21
Electronics Letters 10 June 1993 Vol29 No12 pp1123-4
Electronics Letters 27 Feb 1992 Vol28 No5 pp437-8

(58) Field of Search
UK CL (Edition O) **G2J JGDA**
INT CL^6 **G02B**

(54) Providing cladding on planar optical waveguide by heating to flow

(57) A cladding layer on the core of an optical waveguide is heated until it flows in a rapid thermal annealing process preferably either: in a multi-stage furnace in which the waveguide substrate can be transported rapidly on a carriage 69 between stages 72,73,74 at different temperatures; or in a quartz chamber 32 adjacent a bank of quartz halogen lamps 35 of low thermal inertia and easily switched rapidly between different intensities of thermal radiation through the chamber. Unstable products may be removed form the cladding by heating to 700°C. The temperature may then be raised to 1100 - 1200°C for densification. The substrate may be silicon or quartz. The cladding layer may be BPSG and be deposited by PECVD.

Fig.3.

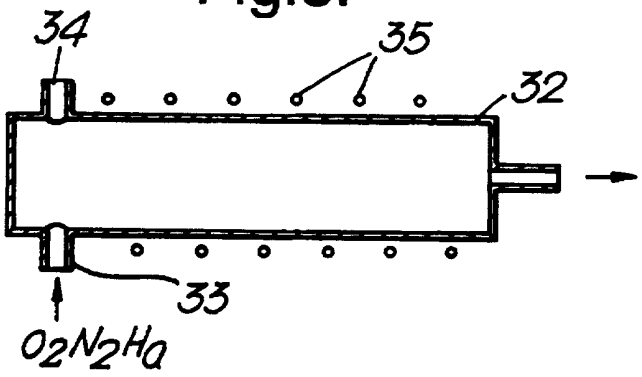
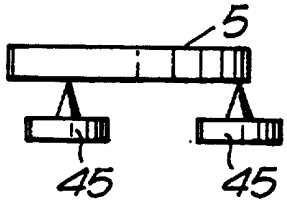


Fig.5.



GB 2 312 525 A

At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

Fig.1.

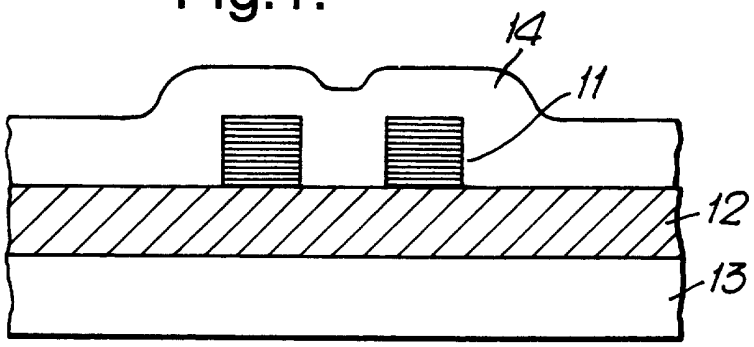


Fig.2.

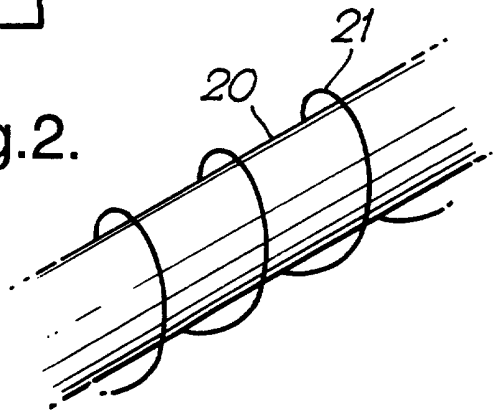


Fig.3.

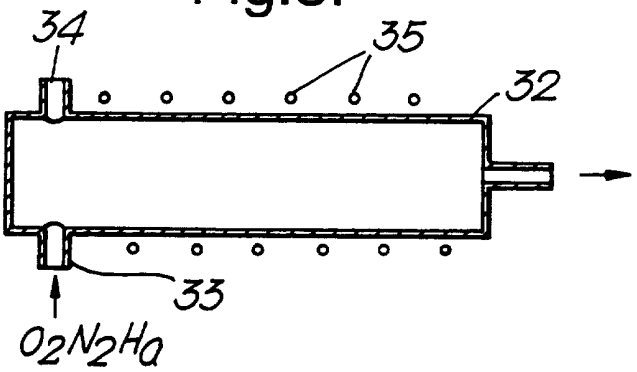


Fig.4.

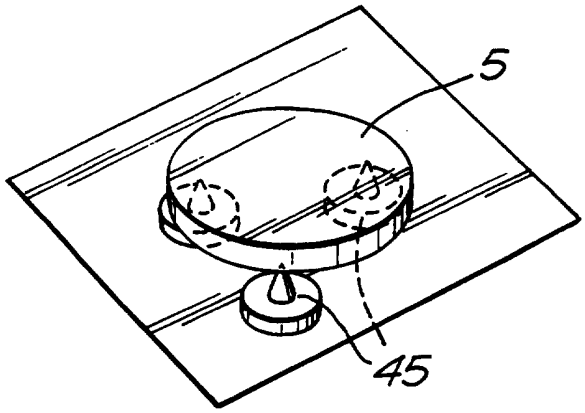


Fig.5.

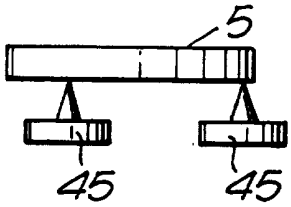
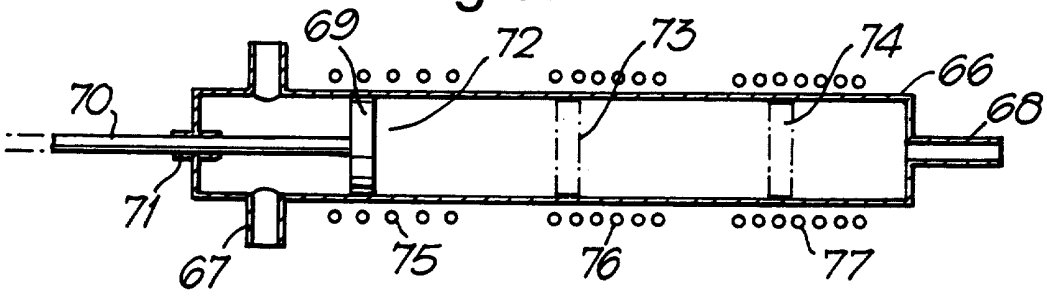


Fig.6.



2312525

PLANAR WAVEGUIDES

The present invention relates to a waveguide and to a method of annealing a planar waveguide cladding deposited after the production of a buffer and a core, e.g. after a thick cladding layer has been produced on the buffer and core by a plasma enhanced chemical vapour phase deposition (PECVD) process.

An annealing proceedure in the production of such a waveguide cladding can be critical because the precursor materials for the deposition, i.e. the plasma creating substances (typically hydrides and N20), are liable to create unwanted chemical substances such as radicals with bonded hydrogen in the films. The annealing procedure may expel the undesired elements in such a combination, but the sites of the expelled elements are likely to contain voids, gaps and other imperfections in the stnucture of a deposited waveguide layer. These imperfections may not only detract from the strength and dimensional predictability of a waveguide so treated, but may lead to inhomogeneities in its refractive index, thus prejudicing its optical operation. Since a typical operating wavelength may be 1.55 microns, and the operation of a planar waveguide may depend on such small differences in refractive index as 0.7% between the cladding and the core and the buffer on which it rests, even minor errors in refractive index are unacceptable.

Annealing tends to reduce any imperfections, and to consolidate or densify the material deposited by a PECVD process, but an annealing procedure can take a long time, and arrangements to be described below provide a reliable improvement in a structure without the employment of an unduly long annealing time. Previously proposed methods of annealing deposited layers, especially thick layers usually involved slow heating in attempts to avoid the

disadvantage, even when layers are produced by means other than a PECVD process, of a tendency to cause stresses and cracking. The films deposited by PECVD, low pressure chemical vapour deposition (LPCVD) or by atmospheric pressure chemical vapour deposition (APCVD) are coherently bonded, hard and stable, unlike the films deposited by previous flame hydrolysis techniques which are soot-like, soft and porous. The properties of these PECVD, LPCVD or APCVD deposited films provide a reduced tendency to cracking or blistering during an annealing process. The cracking probably results from a physical mismatch between the waveguide core, its substrate, the intermediate buffer layer which is usually present, especially with thick films, and the deposited cladding. With a PECVD process, the precursor materials used are of such a nature, as explained above that they tend to add to the problems of annealing.

Many materials such as those of interest herein can also be deposited in layers by spincoating from liquid sources generally referred to as Solgel. Such a technique is described for example by R A A Syms and A S Holmes in J. Non-crystalline Solids, 170, 1994, pp223 to 233. However, the resulting layers are severely limited in thickness, and each layer may take three minutes or so to produce. Therefore there is no substantial advantage in techniques for their rapid annealing. With the more rapid PECVD process, need for rapid annealing is much more significant.

Fast rate annealing of very thick (≥15 micron) borophosphosilicate glass (BPSG) cladding layers which have been deposited using PECVD (the cladding oxide may be undoped or contain dopants such as germania) was carried out by first removing unstable products, such as bonded hydrogen and water vapours at low temperatures e.g. 700°C and then step by step raising the temperature till the cladding layer fills up the gaps between and around the etched core layers. The annealing time and temperatures are determined by the composition of the cladding layer. Annealing temperature-time combination is critical for controlling all the

requisites for a low loss cladding layer such as refractive index homogeneity across the thickness of the film, and also around the channel waveguides.

As an example, one prior proposed cladding process consists of depositing 1,3,6 and 6 microns thick BPSG film by PECVD. Each of the layers is separately annealed. This prior proposed annealing is carried out by slowly ramping a resistively heated furnace containing the wafers, from 300°C to 1000 or 1050°C. The total time for annealing each layer is around 16 hours, thus making the total time of anneal for a 15 microns thick layer up to 64 hours. The slow ramping was believed to be necessary to prevent cracking or degradation of the film, which may occur if the film is suddenly exposed to temperatures close to the flow temperatures of the BPSG. Such long annealing times are undesirable for manufacturing of planar waveguide devices, as this will slow down the product throughput.

Rapid annealling of phosphosilicate and borophosphosilicate glasses for the purposes of integrated circuit application has been described for example by R Thakur et al. in Proceedings of 11th VMIC Conference, California, June 7-8, 1994, pp117 to 119. The glass film, typically $\leq$ 2 microns in thickness in the case of IC technology is used as an interlayer dielectric where the key requirement of the material is its electrical insulation rather than any optical properties. In planar waveguide applications as envisaged herein, the glass thickness is not only significantly greater, typically $\geq$ 16 microns, but the control of the refractive index of the film across the substrate, and more importantly through the thickness of the film, needs to be accurate to about 0.0002 of the refractive index value to provide a high quality device. An acurate control of this nature is not a feature of the processes employed to form an IC interlayer dielectric film.

The basis of embodiments of this invention is the identification of the temperature and time required for removing unstable products,

mentioned earlier, so that after their removal, the film could be exposed to very high temperatures (~1,050°C). In one embodiment the cladding layers were heated to 700°C for 300 seconds, followed by 850°C for 300 seconds, followed by 950°C for 300 seconds, followed by 11 50°C for 90 seconds. The total time for anneal was 14 minutes and 30 seconds. This annealing was carried out on cladding layers deposited on silicon wafers with etched waveguide cores. The equipment used was a rapid thermal annealer (RTA), consisting of a quartz furnace, heated by quartz halogen lamps. Silicon wafers, placed in the centre of this quartz furnace, are purged by flowing nitrogen gas, before, during and after annealing. The nitrogen gas may be replaced by helium, argon, oxygen or their mixtures. The substrate temperature can be raised from 500° to 1250°C within 10 seconds and maintained at the desired temperature from a few seconds to several minutes. The entire annealing schedule is controlled by a computer. In the processes described above, the properties of the rapidly annealed cladding films of 15 microns thickness were found to be similar to those obtained by the prior proposed slow furnace annealing, with regard to the flowing, conformity and index homogeneity requirements of planar waveguide devices, thus reducing the process time by a factor of 40.

Since the key feature for the improvements claimed in embodiments are related to understanding the causes of instability during heat treatment at high temperatures and judiciously choosing a low temperature initial anneal to remove instabilities in the very thick films, thus enabling us to attain higher temperatures within a few seconds, this invention is not restricted to any specific types of annealing equipment, but proposes selecting the temperature-time profiles for a given BPSG film. Resistively heated furnaces, with the required temperature zones, can also be used and would be the preferred method of annealing for devices fabricated on quartz substrates. The variations in the PECVD deposited BPSG compositions, with regard to phosphorous or boron content, may alter the initial annealing temperatures of 700°C by ± 50°C.

In one arrangement to be described below, as an example, a waveguide layer, made by a PECVD process from hydrides and nitrous oxide, is first brought, in steps, to around 700°C to 1 000°C, and kept at this temperature for one or two minutes. The temperature is then raised more slowly to about 1200°C, for instance it is raised from 1 000°C to 11 00°C in twenty minutes. The waveguide layer, which may typically be oxide, doped or undoped, is then maintained at 1210°C for 15 - 30 minutes, and then allowed to cool to around 1000°C in twenty minutes, before the temperature is finally reduced to room temperature. It has been found that improvements in the structure result from the employment of these steps.

It is believed that removal of hydrogen, e.g. bonded hydrogen and water vapour, prior to raising th temperature to its highest value contributes to the successful annealing of the oxide layer. Following the annealing process another cladding layer may be applied, e.g. also using a PECVD process.

The preparation for the PECVD process may have involved the use of silane or nitrous oxide, as sources for hydrogen and oxygen ions, respectively, for the generation of the plasma. The dopant may be germania selected to provide a given refractive index, but the amount of such dopants used may also affect the ideal length of time, or the ideal top temperature of annealing, i.e. around 11001 200°C.

The heating steps may either be carried out in a single stage or multistage furnace in the arrangement described above, or the heating may alternatively be provided by an adjacent bank of quartz or halogen lamps of adjustable intensity heating the waveguide directly, such heating by direct radiation being more rapid than that provided by a furnace.

The preferred materials for the waveguide are a substrate of silicon, a buffer layer thereon of undoped silica, a waveguide core of silica glass doped with germania (GeO2) and a cladding of boron and phosphorus doped glass or silica. The cladding layer is however not

limited to borophosphosilicate glass, but may also comprise a combination of other materials such as germania, titania or arsenic so as to achieve low temperature flow properties and suitable optical proprties. The germania doped core has a flowing temperature somewhat lower than that of the buffer due to the doping, but the cladding has an even lower flow temperature, so that it can flow without affecting the waveguide. The buffer layer and/or the core layer, preferably both, may be deposited by a PECVD process and annealed, as described below.

The required cladding layer thickness may be provided by a number of separate deposition stages, each deposited layer being separately annealed. Alternatively, the deposition can be carried out as a single step provided that the conformity of the film is adequate to avoid formation of voids and discontinuities. The annealing temperature of a single layer is similar to an equivalent multilayer structure.

In a preferred embodiment, the annealing process incorporates two annealing stages. In the first stage, a low temperature anneal at 700 ± 50°C removes undesirable contaminants such as bonded hydrogen and adsorbed water vapour. In the second stage, a high temperature anneal above the glass flow temperature (T_f) at 1100 ± 50°C consolidates the deposited material and allows the material to flow into any gaps in the substrate waveguide structure. The initial low temperature anneal allows the second higher anneal temperature to be reached rapidly thus reducing the overrall process time.

Arrangements illustrative of the invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 shows in cross section a device structure to which the annealing process is applicable.

Figure 2 shows diagrammatically and in perspective a furnace and a heating coil,

Figure 3 shows diagrammatically and in a cross-sectional view a chamber heated by adjacent quartz halogen lamps,

Figure 4 and Figure 5 show in diagrammatic perspective and side views respectively a typical mounting of a sample for heating by radiations in a chamber heated by halogen lamps, and

Figure 6 shows a diagrammatic sectional view through a furnace heated in three successive compartments or regions to different temperatures.

Referring to Figure 1, the device structure comprises a closely spaced pair of waveguides 11 disposed on a layer of buffer oxide 12 on a silicon or quartz substrate wafer 13. A BPSG cladding layer 14 is provided over and between the waveguides 11. The cladding layer 14 is deposited from a PECVD process and is required the narrow gap, wich is typically of the order of 1 micron, between the waveguides. this is achieved by the annealing process described below.

The rapid annealing, which is a feature of the arrangements being described, takes place in a first embodiment to be described in a furnace. The arrangements to be described employ a comparatively short annealing and densification programme time. A furnace illustrated diagrammatically in Figure 2 has a refractory (quartz or SiC) cylindrical chamber 20 surrounded by an adjustable high current heating coil 21. Wafers e.g. comprising cladded waveguide on a silicon or quartz substrate as aforesaid, may be introduced, in batches of say 200, directly into an environment in the chamber 20 at a temperature between 900° and 1 000°C which is then raised over a period of 20 minutes to 1100° - 1200°C (i.e. at about 5°C to 15°C per minute) and the final ambient temperature is maintained at 1100° - 1200°C for from 15 minutes to 36 minutes. From this point, the

temperature is allowed to cool to 850 to 950°C (prefrerably 900°C) steadily, again at about 5° -15° per minute, and at the temperature of 900°C the wafers are unloaded from the chamber 20 to room temperature. The whole process takes about 80 minutes, which compares most favourably with hitherto typical periods of 24 hours or so.

It is believed that unwanted hydrogen and water derived from the silane and other gases of the PECVD process are expelled from lattice sites in such layers as a silicon oxide layer, but that the empty sites leave porosities that require compacting or densification after the rapid first heating to 900° - 1000°. After this, the slower rate of heating to 1100° -1200° is believed to achieve most of the required densification without structural damage.

The further heating step at 1200°C or so, and the subsequent slow cooling, have been found to complete the densification process, while minimizing any possible damage due to thermal shock.

A furnace of the type shown in Figure 2 may in some instances not be considered to be sufficiently flexible in producing the changes of temperature required and in Figure 3 there is shown another form of heating which is particularly suitable for the batch treatment of, for example, a smaller number such as five to ten or so samples at a time. In Figure 3 there is a quartz chamber 32 which has a feed 33 on one side for inert gases e.g nitrogen or helium, or for oxygen for the easy removal of hydrogen, and an exit 34 at the other side for extracting the gases and enabling a continuous flow to be provided. The quartz chamber 32 does not absorb the radiation from a bank of quartz halogen lamps 35 adjacent the chamber 32 and it is possible to raise the temperature of objects in the chamber 32 very rapidly, as a result of radiations passing through the walls of the chamber 32 from the lamps 35. The same programme of heating, and of holding the temperatures as has been described with reference to Figure 2 is employed, and the cooling down steps can easily be controlled. As shown in Figs. 4 and 5, the wafers 5 may be suspended at three

points by supports 45, or otherwise, in such a way that the supports 45 have little effect on the heating or cooling of the wafers 5. The thermal inertia of the wafers 5 and of their supports 45 is kept at a minimum, and rapid warm-up and cooling of the wafers can be achieved by the control of the lamps 14a and of the gases introduced at 33. Many other types of heat insulated support for the wafers may be preferred.

In another method of carrying out the heating steps, which is particularly suitable for small batches of, for example, 20 or so wafers at a time, reference is now made to Figure 6 which shows a three stage furnace 66. The furnace has an inlet 67 at one end suitable for the introduction of non-reactive or scavenging gases, an exhaust gas exit 18 at the other end, and a mobile wafer carrier 69 which can be moved along the furnace chamber 66, e.g. by means of a rod 70 passing through a seal 71, between differently heated regions. There may be a cool site 72, e.g. at 700°C, an intermediate temperature site 73 at, say, 850°C, and a hot site 74 at 1150°C, the differential heating being achieved by arranging three high current heating coils 75, 76 and 77 to be of differing powers or energizations. The wafers 5 may be transferred from one temperature environment to another in precise ways, which may be relatively slow, or rapid as required. The period for cooling down the wafers 5 can equally well be controlled precisely, and be long or short, as is required. The rapid annealing and densification of the deposited layer is achieved in a reliable manner, and the buffer layer of silica doped or undoped, may have been produced by a PECVD process, or otherwise. The refractive index of the cladding can be chosen appropriately for cooperation with the (slightly larger) refractive index of the underlying core resting on the buffer.

The previous depositions of the inner waveguide components and dopants may also have been deposited on the substrate by PECVD.

It will be understood that, although particular arrangements illustrative of the invention have been described, by way of example,

variations and modifications thereof, as well as other embodiments, may be made within the scope of the protection sought by the appended claims.

CLAIMS

1. A method of providing a waveguide cladding layer on a substrate supporting a waveguide core, including heating the substrate to a first temperature so as to remove unstable products from the cladding, and raising the temperature of the substrate until the cladding flows to provide a coherent coating on the core.

2. A method of depositing a waveguide cladding layer on a substrate supporting a core, including removal of unstable products at low temperatures of 700°C ± 50°C, and then step by step raising the temperature of the substrate till the cladding fills gaps with underlying layers, and for durations and temperatures determined by the composition of the cladding layer to be deposited.

3. A method of depositing a waveguide cladding which includes preparing and annealing an arrangement having a layer of a silicon oxide, doped or undoped, deposited on a silicon substrate, including the steps of heating the arrangement to a temperature lying between 700°C and 900°C, then raising its temperature at a rate of between 5° to 1 5°C per minute to between 1100° and 1200°C, maintaining the arrangement at this temperature for 15 - 36 minutes, allowing the arrangement to cool at a rate of 5° to 1 5°C per minute to 850 to 950°C, and then allowing the arrangement to cool to room temperature.

4. A method as claimed in claim 1, 2 or 3, wherein the heating is provided by radiant heat from quartz halogen discharge lamps or other rapid thermal annealing (RTA) furnace.

5. A method as claimed in claim 3, in which the layer of a silicon oxide doped or undoped is deposited by a PECVD process.

6. A method as claimed in claim 5, wherein silane SiH4 or other silicon carrying vapour/gas source is used in the PECVD deposition process.

7. A method as claimed in any one of the preceding claims wherein the layer of a silicon oxide combination provides the core for a waveguide.

8. A method as claimed in any one of the preceding claims wherein an underlying layer of a silicon oxide provides the buffer for a waveguide.

9. A method of making a waveguide including depositing a buffer layer by a PECVD process, depositing a core layer by a PECVD process on the deposited buffer layer, and including the steps of depositing a cladding layer by PECVD as set out in any preceding claim.

10. A method as claimed in any one of claims 1 to 9 wherein the heating is provided by a furnace.

11. A method as claimed in claim 10 wherein three banks of differently powered heaters or other means are arranged to produce three different temperature regions in the furnace, and the substrate is moved appropriately between the regions, for heating or cooling steps.

12. A method as claimed in claim 1, 2 or 3 including a step substantially as described herein with reference to any one of the accompanying drawings.

13. A waveguide made by the method of any one of claims 1-12.

14. A waveguide as claimed in claim 13 having an annealed BPSG cladding layer enveloping a core.

The Patent Office

13

Application No: GB 9608615.2 **Examiner:** Chris Ross
Claims searched: 1-14 **Date of search:** 18 June 1996

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.O): G2J(JGDA)

Int Cl (Ed.6): G02B

Other:

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X	GB 2292468 A	(FURUKAWA) Fig 6,p3	1 at least
"	GB 2066805 A	(NT&T) Figs 8G,18E	"
"	EP 0617301 A1	(NEC) col 4 l1 on	"
"	EP 0607884 A1	(SUMITOMO) p9 l24 on	"
"	EP 0603530 A2	(MOTOROLA) layer 6	"
"	EP 0545432 A1	(SUMITOMO) p5 l4 on	"
"	EP 0476688 A2	(") Ex 1,2	"
"	EP 0331335 A2	(AT&T) col 5 l35 on	"
"	EP 0281800 A2	(HITACHI) col 6 l11 on	"
"	WO 93/16403 A1	(BT) p3 l14 on	"
"	Applied Optics 1 Sept 1993 Vol32 No25 pp4916-21,Fig 7		"
"	Electronics Letters 10 June 1993 Vol29 No12 pp1123-4		"
"	Electronics Letters 27 Feb 1992 Vol28 No5 pp437-8,cladding layer Fig 1		"

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.