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(71) Applicant *(for all designated States except US)*: **TINGGI TECHNOLOGIES PRIVATE LIMITED** [SG/SG]; 83 Science Park Drive, #03-01/02 The Curie, Science Park I, Singapore 118258 (SG).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **KANG, Xuejun** [CN/SG]; Tinggi Technologies Private Limited, 83 Science Park Drive, #03-01/02, The Curie, Science Park 1, Singapore 118258 (SG). **YUAN, Shu** [AU/SG]; Tinggi Technologies Private Limited, 83 Science Park Drive, #03-01/02, The Curie, Science Park 1, Singapore 118258 (SG). **LAM, Jenny** [SG/SG]; Tinggi Technologies Private Limited, 83 Science Park Drive, #03-01/02, The Curie, Science Park 1, Singapore 118258 (SG). **LIN, Shiming** [CN/SG]; Tinggi Technologies Private Limited, 83 Science Park Drive, #03-01/02, The Curie, Science Park 1, Singapore 118258 (SG).

(74) Agent: **CALLINAN, Keith, William**; LLoyd Wise, Tanjong Pagar, P.O. Box 636, Singapore 910816 (SG).

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(54) Title: SEPARATION OF SEMICONDUCTOR DEVICES

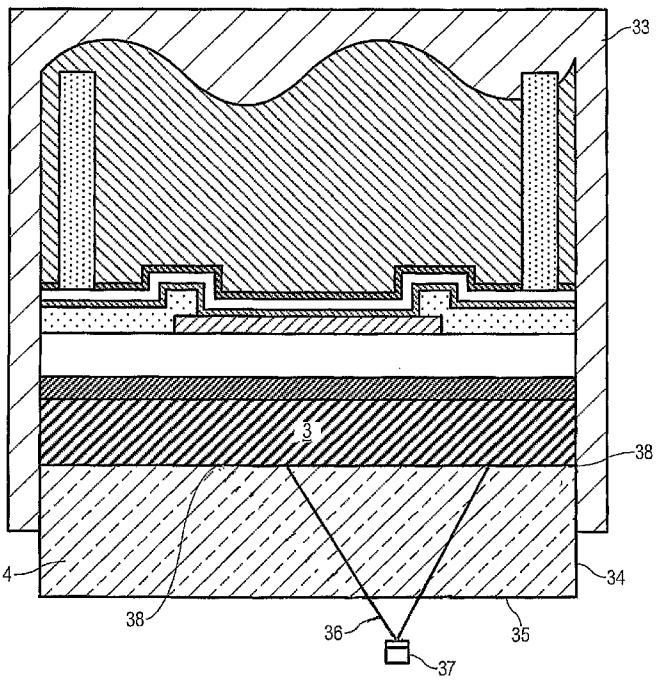

FIG. 9

(57) Abstract: A method of fabricating semiconductor devices is disclosed. The method comprises providing a substrate with a plurality of epitaxial layers mounted on the substrate and separating the substrate from the plurality of epitaxial layers while the plurality of epitaxial layers is intact. This preserves the electrical, optical, and mechanical properties of the plurality of epitaxial layers.

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Separation of Semiconductor Devices

Technical Field

This invention relates to the separation of semiconductor devices and refers particularly, though not exclusively, to the separation of such semiconductor devices after removal of a sapphire substrate.

Background

GaN semiconductor devices such as, for example, light emitting diodes ("LEDs"), laser diodes, photo detectors, transistors, switches, and so forth, are widely used in many applications. Well known applications include, but are not limited to, traffic signals, mobile telephone display backlighting, liquid crystal display ("LCD") back lighting, flash lights for cameras, and so forth. The fabrication of gallium nitride semiconductors for use as LEDs, laser diodes or lighting, gives relatively low productivity. Also, known techniques result in semiconductor devices with a light output that is not optimized. Furthermore, those that form a second substrate have great difficulty managing the second substrate due to warping, and dicing through the second substrate, particularly after removal of the first substrate.

Summary

According to an exemplary aspect there is provided a method of fabricating semiconductor devices. The method comprises providing a substrate with a plurality of epitaxial layers mounted on the substrate and separating the substrate from the plurality of epitaxial layers while the plurality of epitaxial layers is intact. This preserves the electrical, optical, and mechanical properties of the plurality of epitaxial layers.

Subsequent to separation of the substrate, a first stage of device isolation may be performed by trench etching. Mesas may be formed sequent to separation of the substrate, the trench etching being along edges of each mesa. The mesas may be formed in an area defined by the trench. The trench etching may be through the epitaxial layer.

After the first stage of device isolation the method may further comprise pad etching. After pad etching a final stage of die isolation may be performed.

Prior to the first stage of die isolation a photoresist layer may be applied to protect regions of an n-type layer of the plurality of epitaxial layers during the etching process. Following the first stage of die isolation a first insulating layer may be exposed around the mesa, and the photoresist layer may be removed. A second insulating layer may be applied over the exposed surfaces of the first insulating layer, the sides of the epitaxial layers, and a center of the epitaxial layers. Pad etching may take place to remove at least a part of the second insulating layer to expose part of the surface of the epitaxial layers. A further photoresist layer may be applied over exposed surfaces of the second insulating layer and the center of the exposed surface of the epitaxial layers leaving a gap for etching of the exposed surface of the epitaxial layers. Etching may take place through the gap to surface texture the exposed surface of the epitaxial layers. The further photoresist layer may be removed. A new photoresist layer may be applied. Etching may take place to expose ends of thick patterns.

After die isolation an array of n-type ohmic contacts may be formed on the n-type layer. The method may further comprise die separation as a final step in the process.

The method may further comprise: prior to separation of the substrate from the plurality of epitaxial layers, forming at least one seed layer on the plurality of epitaxial layers, and forming an outer layer on the at least one seed layer, the outer layer being relatively thick and being for at least one of: a structural support, a heat sink, a heat dissipater, a current dissipater, and as a terminal, for the semiconductor devices.

Before the at least one seed layer is formed:

(a) a p-type metal ohmic contact layer may be applied to a p-type layer of a plurality of epitaxial layers;

(b) a layer of a dielectric may be applied over the p-type metal ohmic contact layer and the p-type layer;

(c) the dielectric layer may be removed from above the metal ohmic contact layer; and

(d) the at least one seed layer may be deposited on the dielectric layer and the metal ohmic contact layer.

After (d) and before the outer layer is formed, the thick patterns may be applied to the at least one seed layer, the outer layer being formed between the thick patterns. The dielectric may be an oxide or a nitride. Die separation may be a final step in the process.

According to a further exemplary aspect there is provided a method of fabricating semiconductor devices. The method comprises providing a substrate with a plurality of epitaxial layers mounted on the substrate and applying patterns. An outer layer is formed between the patterns. The outer layer is at least 0.3 mm thick and is for at least one of: a new substrate, a structural support, a heat sink, a heat dissipater, a current dissipater, and as a terminal, for the semiconductor devices; and separating the substrate from the plurality of epitaxial layers.

The outer layer may be at least 1 mm thick or at least 2 mm thick.

The patterns may be of a material that does not adhere to the outer layer such that the outer layer does not require dicing for die separation. The separating the substrate from the plurality of epitaxial layers may be while the plurality of epitaxial layers are intact and preserves electrical, mechanical and optical properties of the plurality of epitaxial layers. The patterns may define individual devices of the semiconductor devices.

Prior to applying the patterns, there may be included forming at least one seed layer on the plurality of epitaxial layers, the patterns being applied on the at least one seed layer. Before the at least one seed layer is formed a p-type metal ohmic contact layer may be applied to a p-type layer of the plurality of epitaxial layers and a layer of a dielectric may be applied over the p-type metal ohmic contact layer and the p-type layer. The dielectric layer may be removed from above the metal ohmic contact layer. The at least one seed layer may be deposited on the dielectric layer and the metal ohmic contact layer.

Brief Description of Drawings

In order that the present invention may be fully understood and readily put into practical effect, there shall now be described by way of non-limitative example only exemplary embodiments of the present invention, the description being with reference to the accompanying illustrative drawings.

In the drawings:

Figure 1 is a non-scale schematic, cross-sectional view of a semiconductor at a first stage in the fabrication process;

Figure 2 is a non-scale schematic, cross-sectional view of a semiconductor at a second stage in the fabrication process;

Figure 3 is a non-scale schematic, cross-sectional view of a semiconductor at a third stage in the fabrication process;

Figure 4 is a non-scale schematic, cross-sectional view of a semiconductor at a fourth stage in the fabrication process;

Figure 5 is a non-scale schematic, cross-sectional view of a semiconductor at a fifth stage in the fabrication process;

Figure 6 is a non-scale schematic, cross-sectional view of a semiconductor at a sixth stage in the fabrication process;

Figure 7 is a non-scale schematic, cross-sectional view of a semiconductor at a seventh stage in the fabrication process;

Figure 8 is a non-scale schematic, cross-sectional view of a semiconductor at an eighth stage in the fabrication process;

Figure 9 is a non-scale schematic, cross-sectional view of a semiconductor at a ninth stage in the fabrication process;

Figure 10 is a non-scale schematic, cross-sectional view of a semiconductor at a tenth stage in the fabrication process;

Figure 11 is a non-scale schematic, cross-sectional view of a semiconductor at an eleven stage in the fabrication process;

Figure 12 is a non-scale schematic, cross-sectional view of a semiconductor at a twelfth stage in the fabrication process;

Figure 13 is a non-scale schematic, cross-sectional view of a semiconductor at a thirteenth stage in the fabrication process;

Figure 14 is a non-scale schematic, cross-sectional view of a semiconductor at a fourteenth stage in the fabrication process;

Figure 15 is a non-scale schematic, cross-sectional view of a semiconductor at a fifteenth stage in the fabrication process; and

Figure 16 is a non-scale schematic, cross-sectional view of a semiconductor at a sixteenth stage in the fabrication process.

Detailed Description of the Exemplary Embodiments

The GaN devices described below are fabricated from epitaxial wafers that consist of a stack of thin semiconductor layers (called epitaxial layers) on a sapphire substrate. The composition and thickness of the epitaxial layers depends on the wafer design, and determine the light colour (wavelength) of light that will be emitted by the devices that are fabricated from the wafer. Usually a thin buffer layer is first deposited on the sapphire substrate with a thickness often in the range 10 to 30 nm, and can be either AlN or GaN. In this specification this layer is not described or illustrated. On top of the thin buffer layer may be another buffer layer that may be a relatively thick buffer layer. It may be in the range 1 to 7 micrometers. The relatively thick buffer layer is followed by other layers of, for example, GaN, AlGaN, InN, InGaN, AlGaInN, and so forth. To achieve high wafer quality, n-type layers are often deposited on the buffer layers, followed by an active region. Finally, p-type doped layers are deposited. The active region is usually a double heterostructure made of a single quantum well, or multiple quantum wells and is for light generation. But it may be in other forms such as, for example, quantum dots. The deposition of epitaxial layers is usually by metal organic chemical vapor deposition ("MOCVD") or molecular bean epitaxy ("MBE"). The thickness of the epitaxial layers is in the range from a few nanometers to a few microns.

The process starts after the sapphire substrate 4 has applied to it the n-type layer 3 of gallium nitride (GaN), the quantum well or active layer 2, and the p-type layer 1 of GaN. For simplicity, the n-type layer 3 includes all layers below the active layer 2, including the two buffer layers, and the other layers referred to above. The p-type layer 1 is relatively thin – normally no more, but preferably less, than 1 micron. A p-metal layer 5 is then applied over the p-type layer 1. The p-type metal layer 5 may be of nickel-gold (NiAu) or other suitable metal and is preferably relatively thin so that it is transparent. Alternatively, it may be reflective. More preferably it acts as a diffusion barrier to prevent or minimize diffusion into the epitaxial layers 1, 2 and 3.

Standard photolithography and etching are then used to pattern layer 5. This is done by applying a thin layer of photoresist (layer 6(a) in Figure 2) on to metal layer 5, followed by resist exposure and development. The resist pattern 6(a) serves as an etching mask for etching the metal layer 5. The etching may be by wet chemical etching or plasma dry etching (see Figure 2). The photoresist 6(a) is then removed. The patterned layer 5 that remains on the surface of p-type GaN layer 1 will serve as an Ohmic contact layer to the p-type GaN layer 1. Annealing may take place either before or after layer 5 is patterned.

A layer 7 of silicon dioxide (SiO_2) is deposited over the remaining p-metal layer portions 5 and the p-type GaN layer 1 (Figure 3) by a standard thin film deposition method. This may be by plasma enhanced chemical vapor deposition ("PECVD"), sputtering, evaporation, or other suitable techniques.

As shown in Figure 4, a second photoresist layer 6(b) is applied over the oxide layer 7. The resist is then patterned and serves as mask for patterning the oxide layer 7. Wet etching or dry etching (plasma etching) of the oxide layer 7 is carried out. The oxide 7 in the areas 7(a) where there is no photoresist 6(b) is removed, while oxide 7 protected by the resist 6(b) remains after etching. The patterned second resist layer 6(b) is larger in area than the NiAu layer 5 so that the SiO_2 layer 7 remaining extends across the NiAu layer 5 and down the sides of NiAu layer 5 to the p-type GaN layer 1, as shown in Figure 4.

As shown in Figure 5, the second resist layer 6(b) is removed. Seed layer deposition follows, as is shown in Figure 5. The seed layer 8 is of different metal layers, preferably three different metal layers, as shown. The first seed layer 11 contacts with and adheres well to the NiAu layer 5 and the SiO_2 layer 7. It may be of chromium or titanium. It is followed by second layer 10 and third layer 9 of tantalum and copper respectively. Other materials may be used. The first seed layer 11 preferably has good reflectivity for the reflection of light generated in the light emitting device. The second seed layer 10 acts as a diffusion barrier, preventing copper or other materials placed on top of it (such as, for example, the third seed layer 9) from diffusing into the Ohmic contact layer 5 and the semiconductor epitaxial layers 1, 2, 3. The third seed layer 9 acts as a seeding layer for subsequent layer formation.

The coefficients of thermal expansion of the seed layers 9, 10, 11 may be different from that of GaN which is 3.17. While the thermal expansion coefficients of the Ohmic contact layers (Ni and Au) are also different from that of GaN (they are 14.2 and 13.4 respectively), they are relatively thin (a few nanometers) and do not pose serious stress problems to the underlining GaN epitaxial layers. However, a copper layer to be added later may be as thick as hundreds of microns and thus may cause severe stress problems. Thus, the seed layers 9, 10, 11 can be used to buffer the stress. This may be by one or more of:

(a) by having sufficient flexibility to absorb the stress,

(b) by having sufficient internal slip characteristics to absorb the stress,

(c) by having sufficient rigidity to withstand the stress, and

(d) by having graded thermal expansion coefficients.

In the case of graded thermal coefficients, that of the first layer 11 is preferably less than that of the second layer 10, and that of the second layer 10 is preferably less than that of the third layer 9. For example, the first layer 11 may be chromium with a coefficient of thermal expansion of 4.9, the second layer 10 may be tantalum with a coefficient of thermal expansion of 6.3, and the third layer 9 may be copper with a coefficient of thermal expansion of 16.5. In this way the coefficients of thermal expansion are graded from the Ohmic contact 5 and SiO_2 layer 7 to the third copper layer 9. The thicknesses of the seed layers 9, 10, 11 are chosen in such a way that the stress on the epitaxial layers 1, 2, 3 is minimized.

If the outer, copper layer 9 was applied directly to the SiO_2 layer 7 and Ohmic contact 7, the differences in their thermal expansion rates may cause cracking, separation, and/or failure. By depositing a plurality of seed layers 9, 10 and 11 of different materials, particularly metals each having a different coefficient of thermal expansion, the stresses of thermal expansion are spread through the layers 9, 10 and 11 with the resultant lower likelihood of cracking, separation and/or failure. The first seed layer 11 should be of a material with a relatively low coefficient of thermal expansion, whereas the final layer 9 may have a higher coefficient of thermal expansion. If there are intermediate layer(s) 10, the intermediate layer(s) should have coefficient(s) of expansion between those of layers 11 and 9, and should be graded from that of the first layer 11 to that of the final layer 9. There may be no intermediate layer 10, or there may be any required or desired number of intermediate layers 10 (one, two, three and so forth).

Alternatively, the seed layers 9, 10 and 11 may be replaced by a single layer of dielectric such as, for example, AlN with vias or holes therethrough to enable the copper layer 9 to connect to the p-type metal layer 5.

For patterned plating of a relatively thick metal layer 29 of a conductive metal such as, for example, copper, that will serve as the new substrate, electrical contact, heat dissipater, current dissipater, heat-sink and physical support after the removal of the original substrate 4, a pattern of thick resists 12 is applied to or in the outer third seed layer 9 by standard photolithography (Figure 6). The thick metal layer 29 is formed in the regions 30 between and as defined by the thick resists 12 (Figure 7). The thick layer 29 may be formed by electroplating, and may be formed over the thick resists 12 to form a single

metal support layer 29. As the p-type layer 1 is relatively thin, the heat generated in active layer 2 is more easily able to be conducted to the thick layer 30. The thick layer 29 may be of any suitable thickness such as, for example, 0.3 mm, 1 mm, 2 mm, or more than 2 mm.

Alternatively, before the application of the thick resists 12, the third seed layer 9 may be partially etched in the center of the street 31 between the mesas 32 for the formation of the thick photoresists 12 (Figure 6) and plating of the main copper layer 29 (Figure 7). This has the advantage of improved adhesion.

The resists 12 may be of a material such as, for example, SU-8 or any other material able to form high aspect ratio patterns. The pattern of the resists 12 defines the ultimate shape and size of the devices.

The removal or lift-off of the sapphire substrate 4 then takes place (Figures 8 and 9). A soft buffer material 33 is provided that encapsulates the entire wafer, or part of the material of the wafer, and the exposed lower surface 35 of the sapphire substrate 4. The buffer material 33 may be, for example, a rubber emulsion, a silicone, an epoxy, an emulsion, a glue, a thermal glue, Crystal Bond™, wax, or the like.

A laser 37 is used to apply a beam 36 through the sapphire substrate 4 to the interface between the sapphire substrate 4 and n-type GaN layer 3 to separate the sapphire substrate 4 from the n-type GaN layer 3. The beam 36 may be diverging (as shown) or collimated. As a result, the sapphire substrate 4 is removed from the plurality of epitaxial layers while the plurality of epitaxial layers is intact. This preserves the electrical, mechanical and optical properties of the plurality of epitaxial layers 1, 2, 3. The soft buffer layer 33 may then be removed.

This exposes the lowermost surface 13 of the n-type GaN layer 3. It is preferred for lift-off of the substrate 4 to take place while the epitaxial layers are intact to improve the quality of removal, and for structural strength. By having the epitaxial layers intact at the time of removal the electrical, mechanical and optical properties of the epitaxial layers are preserved.

As shown in Figure 10, the individual devices are then isolated from each other by trench etching from the newly exposed surface along the edges 40 of the mesa 39, as shown in Figures 12 to 14, with a photoresist layer 41 protecting the regions of the n-type GaN-

layer 3 during the etching process. This leaves the SiO_2 layer 7 exposed around the mesa 39. The resist 41 is then removed.

Alternatively, the lowermost surface 13 of the n-type layer 3 may be cleaved at locations in alignment with the photoresists 12 and the dies separated. This is of advantage for laser diodes as the exposed side surfaces of the n-type layer 3 are substantially parallel, thereby forming mirrors, and thus causing a large amount of total internal reflection. This acts as a light amplification system for improved, and directed, light output.

A layer 42 of SiO_2 is applied over the exposed surfaces of the SiO_2 layer 7, the sides of the n-type GaN layer 3, and the center of the n-type GaN layer 3 (Figure 11). Pad etching then takes place to remove the SiO_2 layer to expose the surface 13 of the n-type layer 3.

A further resist layer 43 is applied over the exposed surfaces of the SiO_2 layer 42 and the center of the exposed surface 13 leaving a gap 16 for etching of the exposed surface 13. Etching takes place through the gap 16 to surface texture the exposed surface 13.

The resist 43 is removed and a new resist layer 44 is applied over all exposed lower-surfaces except those aligned with thick patterns 12. Etching then takes place (Figure 14) through the SiO_2 layers 42 and 7, and seed layers 8, until the ends of the thick patterns 12 are exposed.

A layer or layers 18 of metals are then applied over the resist 44 with the layer 18 having a gap 17 at the center of the n-type GaN layer 3 so that the layers 18 are applied directly to the GaN layer 3 (Figure 15). The resist layer 44, with the layer 18 attached, is removed leaving the layer 18 attached to the center 17 of the n-type GaN layer 3 where gap 17 was previously located. The layers 18 may be one or more layers. All layers 18 may be the same or different. They may be, for example, 18(a) titanium, 18(b) aluminum, 18(c) titanium and 18(d) gold, respectively.

The thick copper layer 29 is then polished flat (Figure 16). The dies are then each separated by physical separation as the patterns 12 do not adhere to the copper of the thick layer 29. This means that dicing, or another method of cutting, of the thick layer 29 into individual devices is not required.

In this way the seed layers 11, 10, 9 and the copper layer 29 act as reflectors to increase light output, with copper layer 29 being one terminal, thus not interfering with light output. The second terminal is layer 18 on the n-type layer 3 of GaN.

Whilst there has been described in the foregoing description preferred embodiments of the present invention, it will be understood by those skilled in the technology concerned that many variations or modifications in details of design or construction may be made without departing from the present invention.

CLAIMS

1. A method of fabricating semiconductor devices, the method comprising:

providing a substrate with a plurality of epitaxial layers mounted on the substrate; and

separating the substrate from the plurality of epitaxial layers while the plurality of epitaxial layers are intact while preserving electrical, mechanical and optical properties of the plurality of epitaxial layers.

2. A method as claimed in claim 1, wherein subsequent to separation of the substrate a first stage of device isolation is performed by trench etching.

3. A method as in claim 2, wherein mesas are formed subsequent to separation of the substrate, the trench etching being along edges of each mesa.

4. A method as in claim 3, wherein the mesas are formed in an area defined by the trench.

5. A method as claimed in claim 4 or claim 5, wherein the trench etching is through the epitaxial layer.

6. A method as claimed in any one of claims 2 to 7, wherein after the first stage of device isolation the method further comprises pad etching.

7. A method as claimed in claim 6, wherein after pad etching a final stage of die isolation is performed.

8. A method as claimed in any one of claims 3 to 7, wherein prior to the first stage of die isolation a photoresist layer is applied to protect regions of an n-type layer of the plurality of epitaxial layers during the etching process.

9. A method as claimed in claim 8, wherein following the first stage of die isolation a first insulating layer is exposed around the mesa, and the photoresist layer is removed.

10. A method as claimed in claim 9, wherein a second insulating layer is applied over the exposed surfaces of the first insulating layer, the sides of the epitaxial layers,

and a center of the epitaxial layers; and pad etching takes place to remove at least a part of the second insulating layer to expose part of the surface of the epitaxial layers.

11. A method as claimed in claim 10, wherein a further photoresist layer is applied over exposed surfaces of the second insulating layer and the center of the exposed surface of the epitaxial layers leaving a gap for etching of the exposed surface of the epitaxial layers; etching taking place through the gap to surface texture the exposed surface of the epitaxial layers.

12. A method as claimed in claim 11, wherein the further photoresist layer is removed and a new photoresist layer is applied; etching taking place to expose ends of thick patterns.

13. A method as claimed in any one of claims 8 to 12, wherein after die isolation an array of n-type ohmic contacts is formed on the n-type layer.

14. A method as claimed in any one of claims 1 to 13 further comprising:

prior to separation of the substrate from the plurality of epitaxial layers, forming at least one seed layer on the plurality of epitaxial layers; and

forming an outer layer on the at least one seed layer, the outer layer being relatively thick and being for at least one selected from the group consisting of: a new substrate, a structural support, a heat sink, a heat dissipater, a current dissipater, and as a terminal, for the semiconductor devices.

15. A method as claimed in claim 14, wherein before the at least one seed layer is formed:

a p-type metal ohmic contact layer is applied to a p-type layer of the plurality of epitaxial layers;

a layer of a dielectric is applied over the p-type metal ohmic contact layer and the p-type layer;

the dielectric layer is removed from above the metal ohmic contact layer; and

the at least one seed layer is deposited on the dielectric layer and the metal ohmic contact layer.

16. A method as claimed in claim 14 when dependent on claim 12, wherein after the at least one seed layer is deposited and before the outer layer is formed, the thick patterns are applied to the at least one seed layer, the outer layer being formed between the thick patterns.

17. A method as claimed in claim 15 or claim 16, wherein the dielectric is selected from the group consisting of: an oxide, and a nitride.

18. A method as claimed in claim 13 further comprising die separation as a final step in the process.

19. A method as claimed in any one of claims 1 to 18, wherein a laser is used to apply a beam through the substrate to an interface between the substrate and n-the plurality of epitaxial layers to separate the substrate from the plurality of epitaxial layers, the beam being selected from the group consisting of: diverging, and collimated.

20. A method of fabricating semiconductor devices, the method comprising:

providing a substrate with a plurality of epitaxial layers mounted on the substrate;

applying patterns to the plurality of epitaxial layers;

forming an outer layer between the patterns;

the outer layer being at least 0.3 mm thick and being for at least one selected from the group consisting of: a new substrate, a structural support, a heat sink, a heat dissipater, a current dissipater, and as a terminal, for the semiconductor devices; and

separating the substrate from the plurality of epitaxial layers.

21. A method as claimed in claim 20, wherein the outer layer is at least 1 mm thick.

22. A method as claimed in claim 20 or claim 21, wherein the outer layer is at least 2 mm thick.

23. A method as claimed in any one of claims 20 to 22, wherein the patterns are of a material that does not adhere to the outer layer such that the outer layer does not require dicing for die separation.

24. A method as claimed in any one of claims 20 to 23, wherein the separating the substrate from the plurality of epitaxial layers is while the plurality of epitaxial layers are intact and preserves electrical, mechanical and optical properties of the plurality of epitaxial layers.

25. A method as claimed in any one of claims 20 to 24, wherein the patterns define individual devices of the semiconductor devices.

26. A method as claimed in any one of claims 20 to 25, wherein prior to applying the patterns, there is included forming at least one seed layer on the plurality of epitaxial layers, the patterns being applied on the at least one seed layer.

27. A method as claimed in claim 26, wherein before the at least one seed layer is formed:

a p-type metal ohmic contact layer is applied to a p-type layer of the plurality of epitaxial layers;

a layer of a dielectric is applied over the p-type metal ohmic contact layer and the p-type layer;

the dielectric layer is removed from above the metal ohmic contact layer; and

the at least one seed layer is deposited on the dielectric layer and the metal ohmic contact layer.

28. A method as claimed in any one of claims 20 to 27, wherein a laser is used to apply a beam through the substrate to an interface between the substrate and n-the plurality of epitaxial layers to separate the substrate from the plurality of epitaxial layers, the beam being selected from the group consisting of: diverging, and collimated.

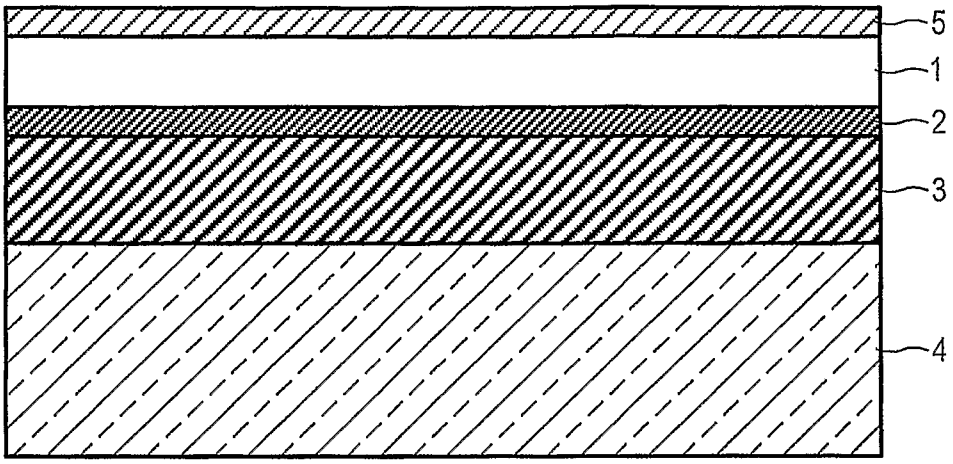

FIG. 1

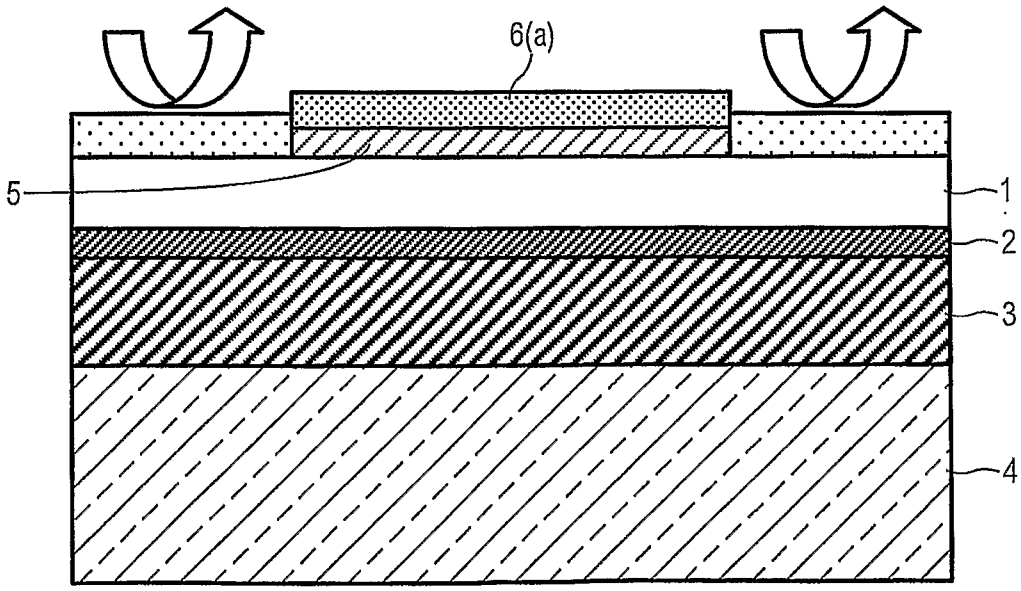

FIG. 2

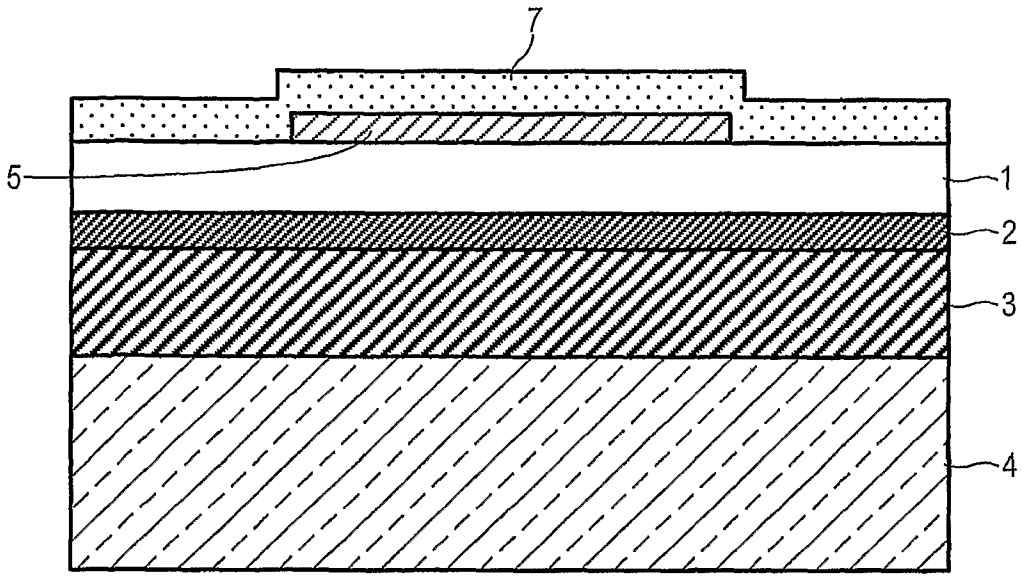

FIG. 3

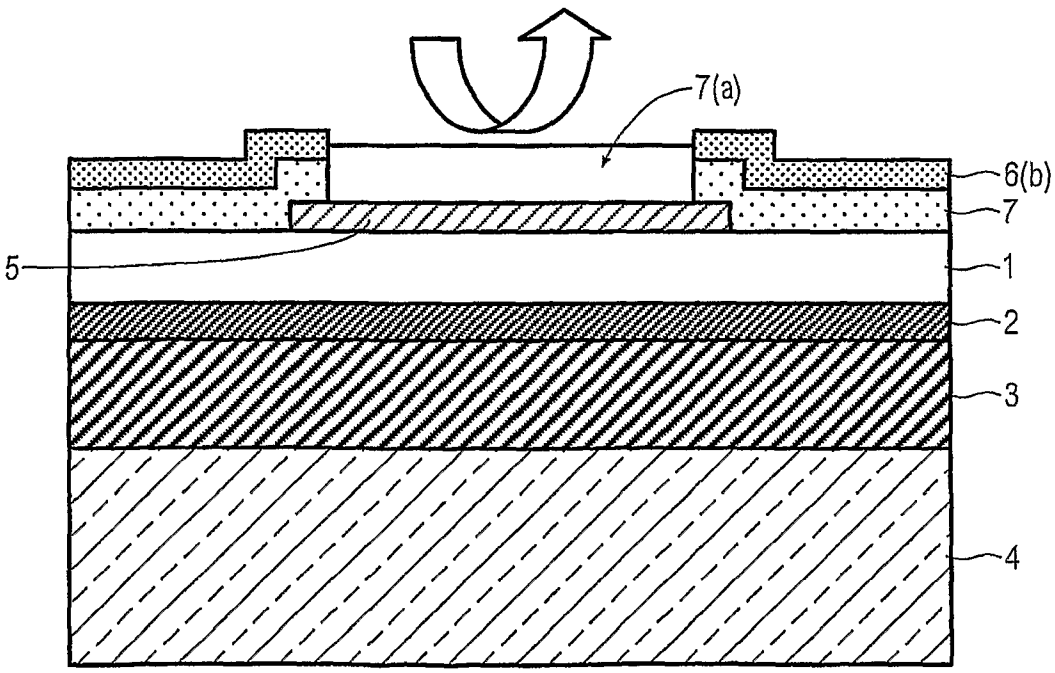

FIG. 4

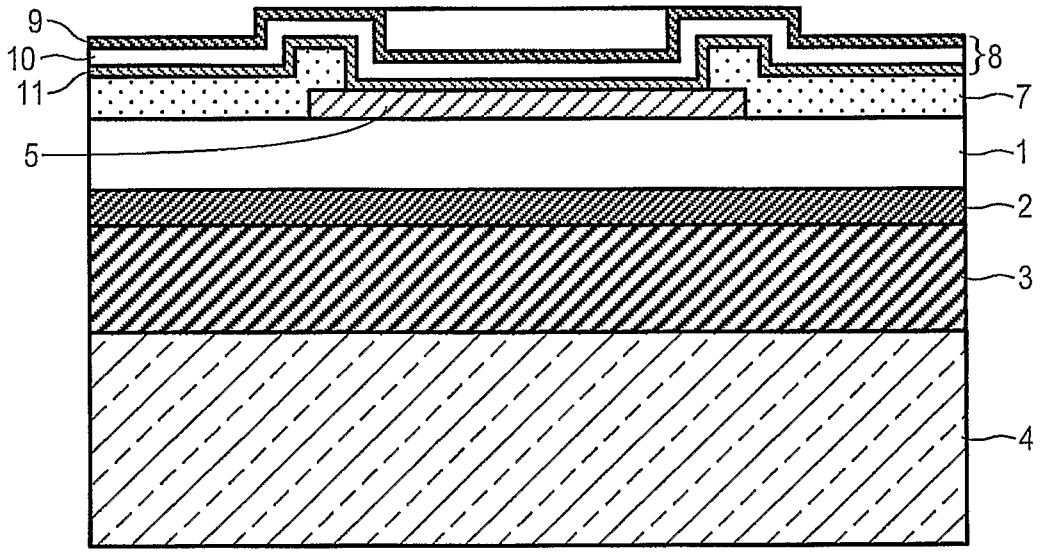

FIG. 5

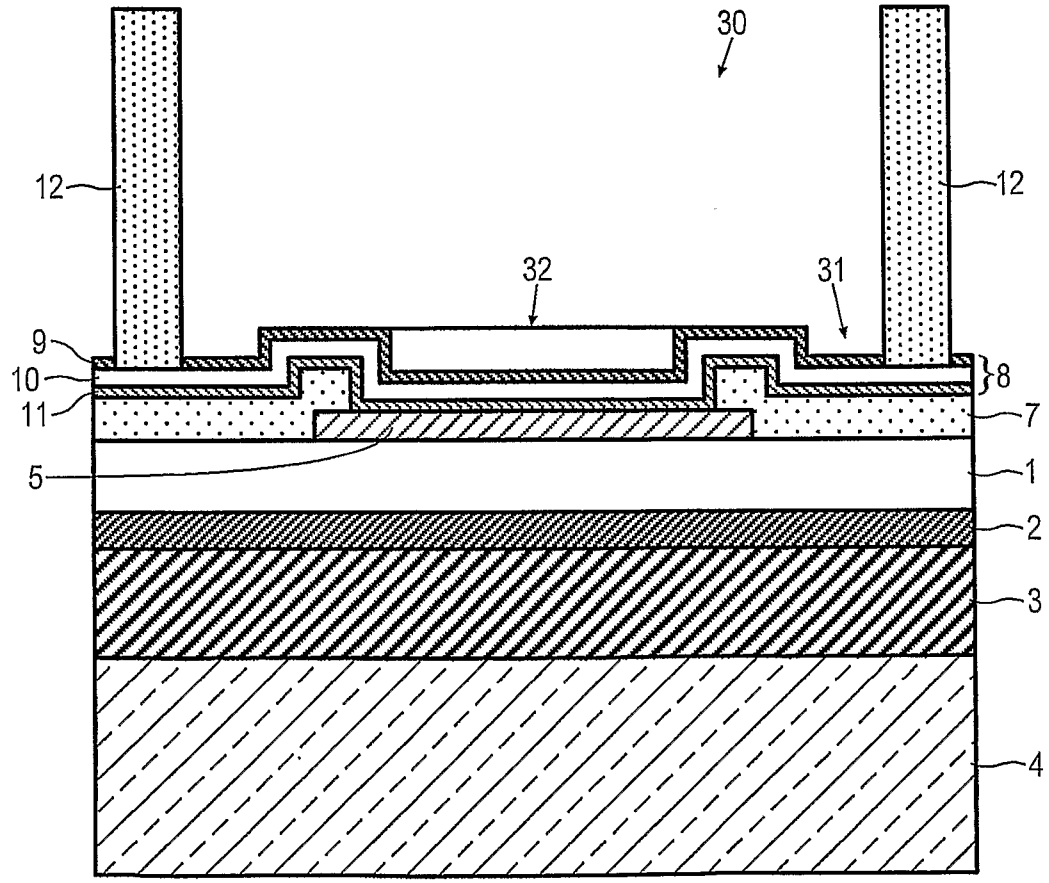

FIG. 6

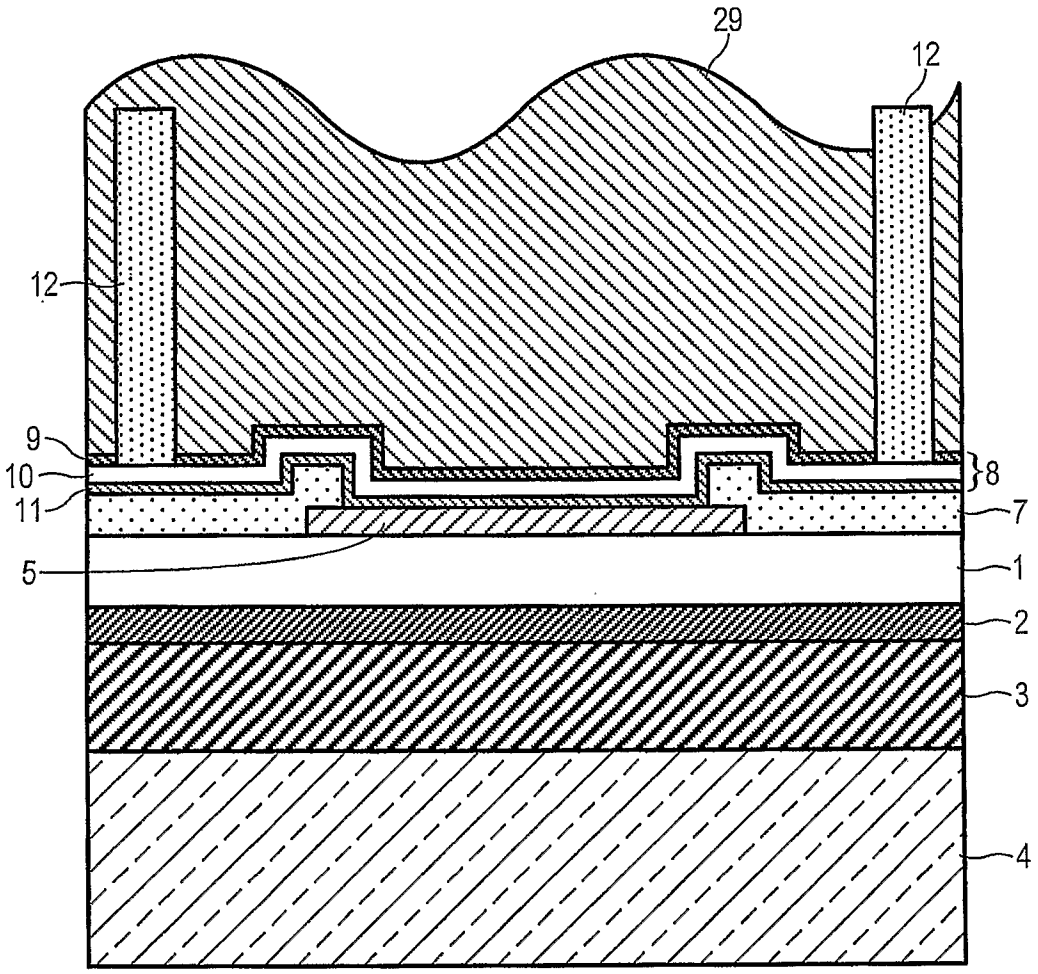

FIG. 7

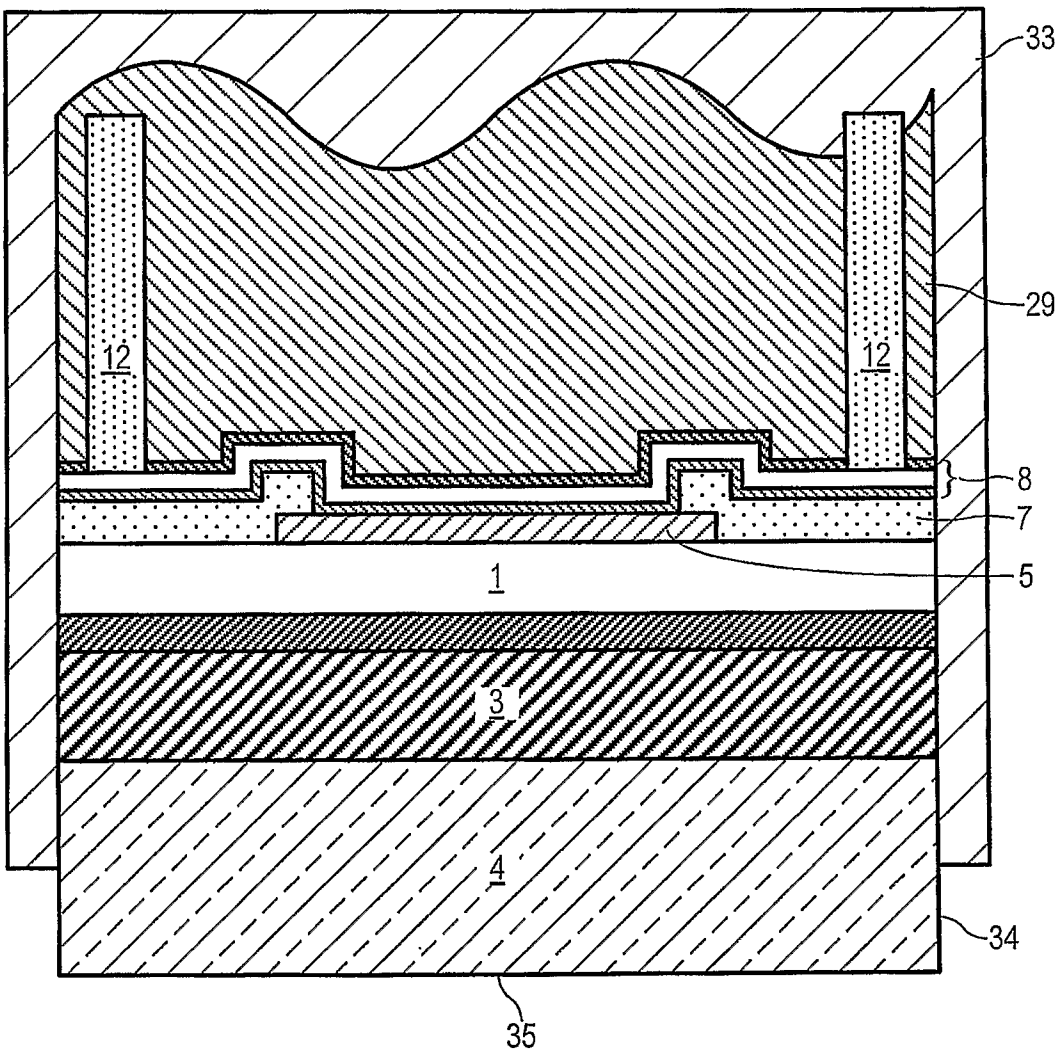

FIG. 8

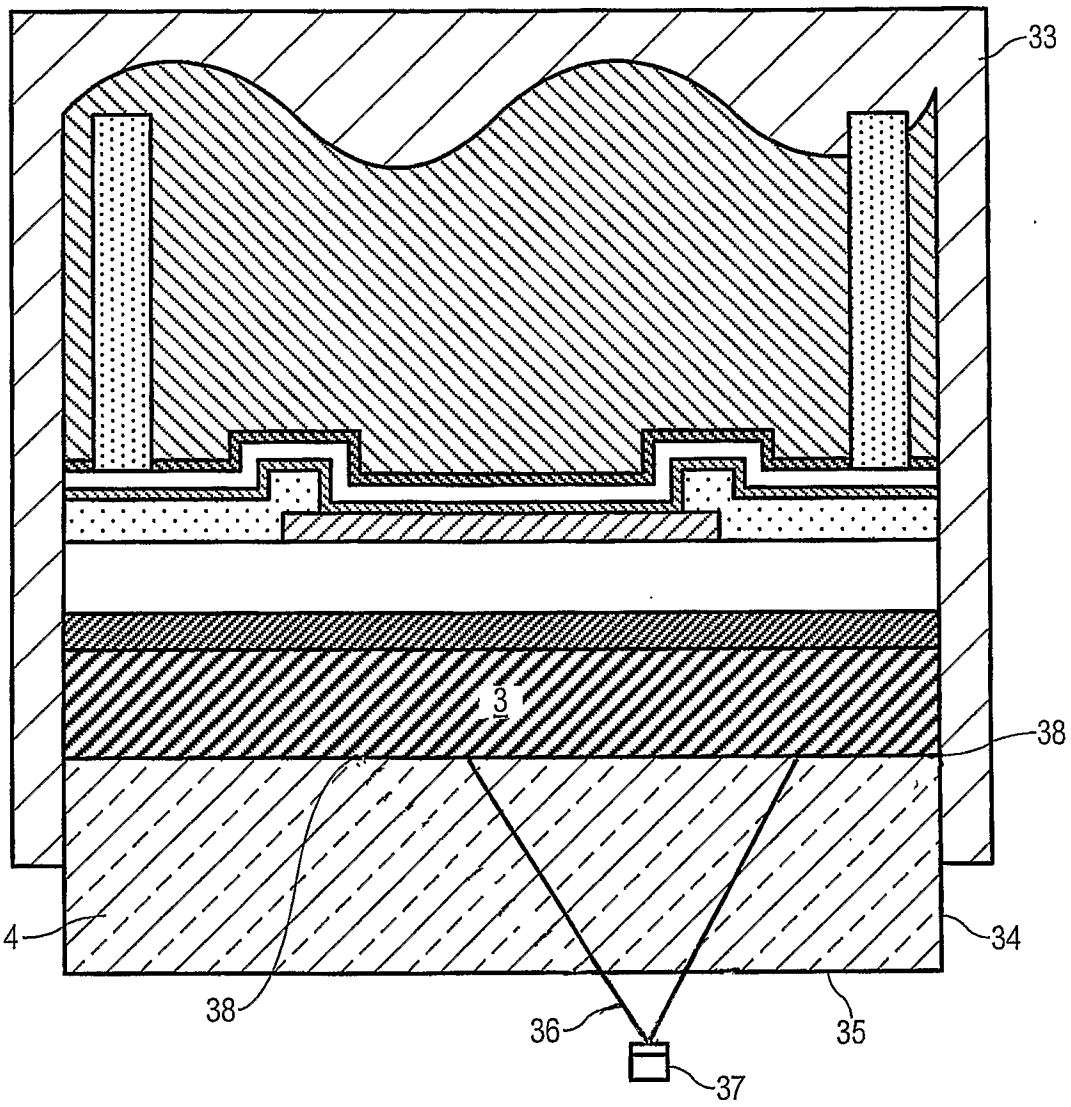

FIG. 9

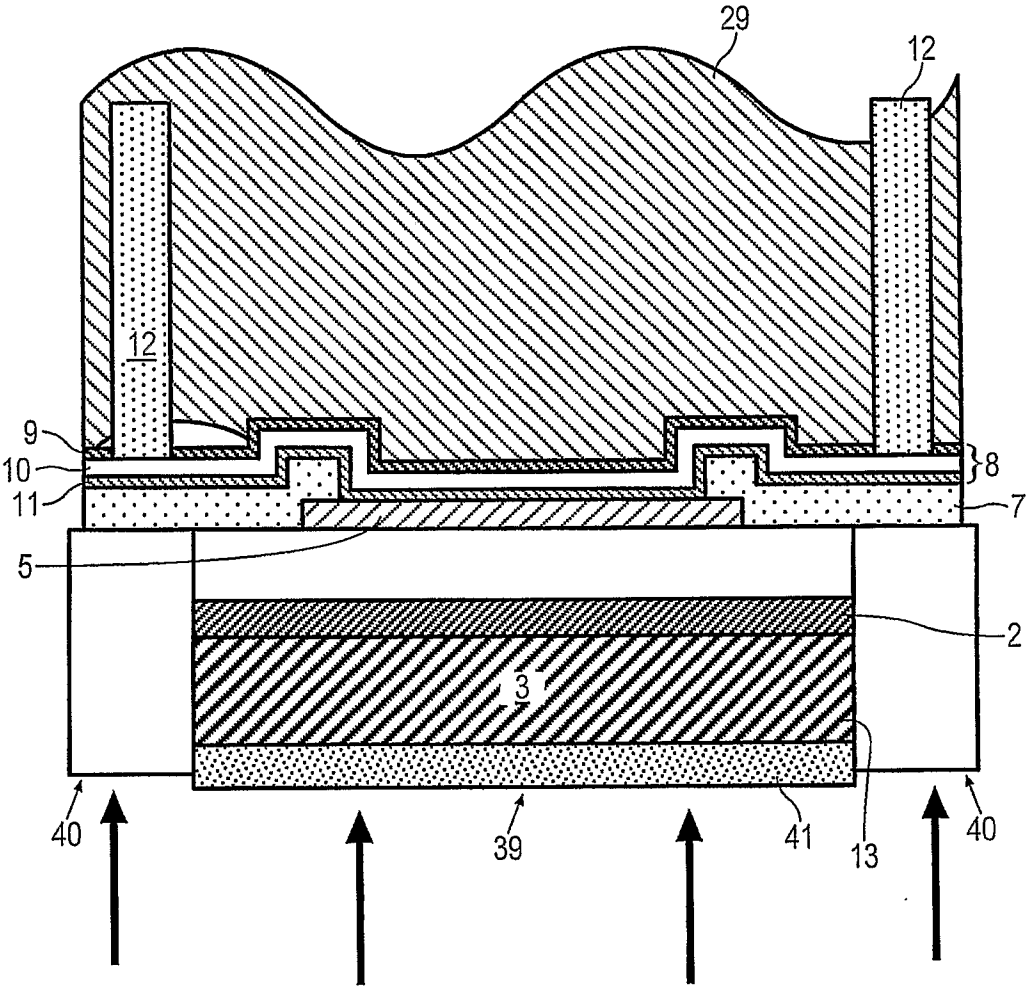

FIG. 10

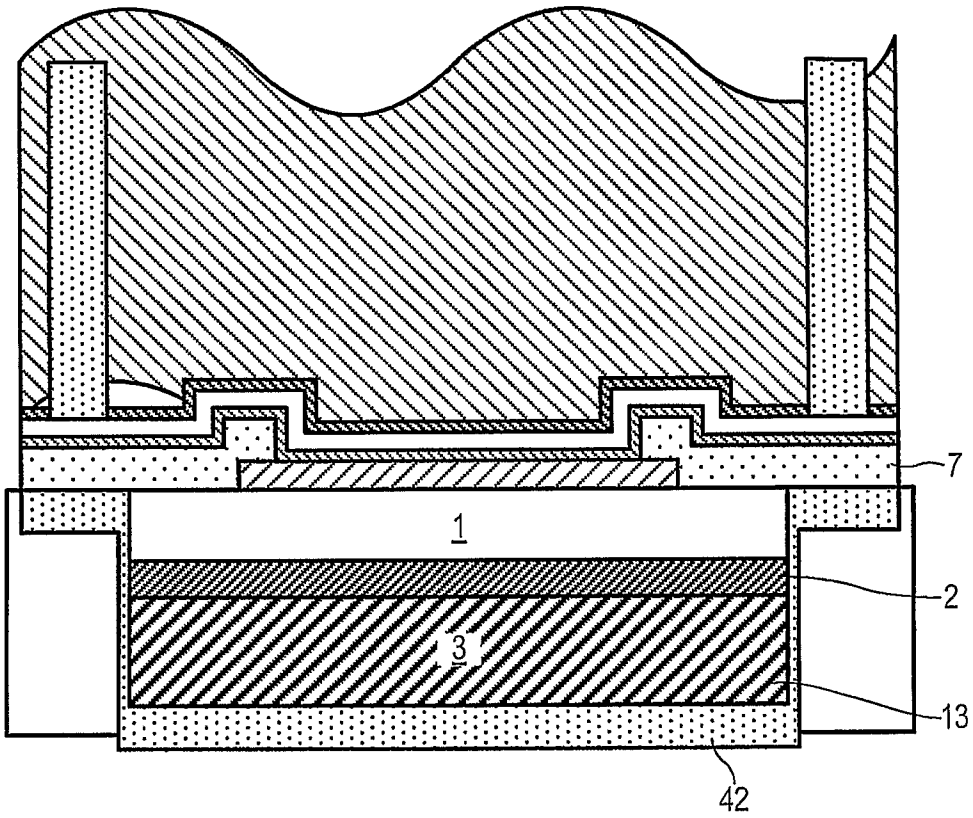

FIG. 11

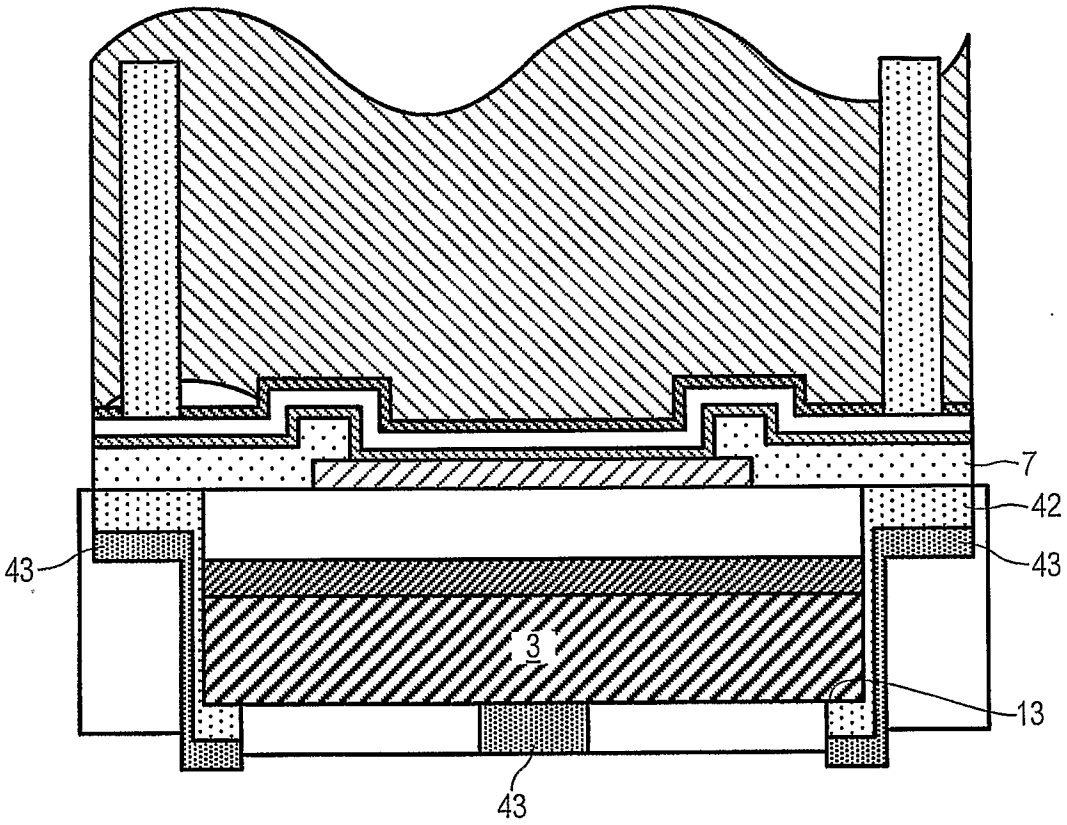

FIG. 12

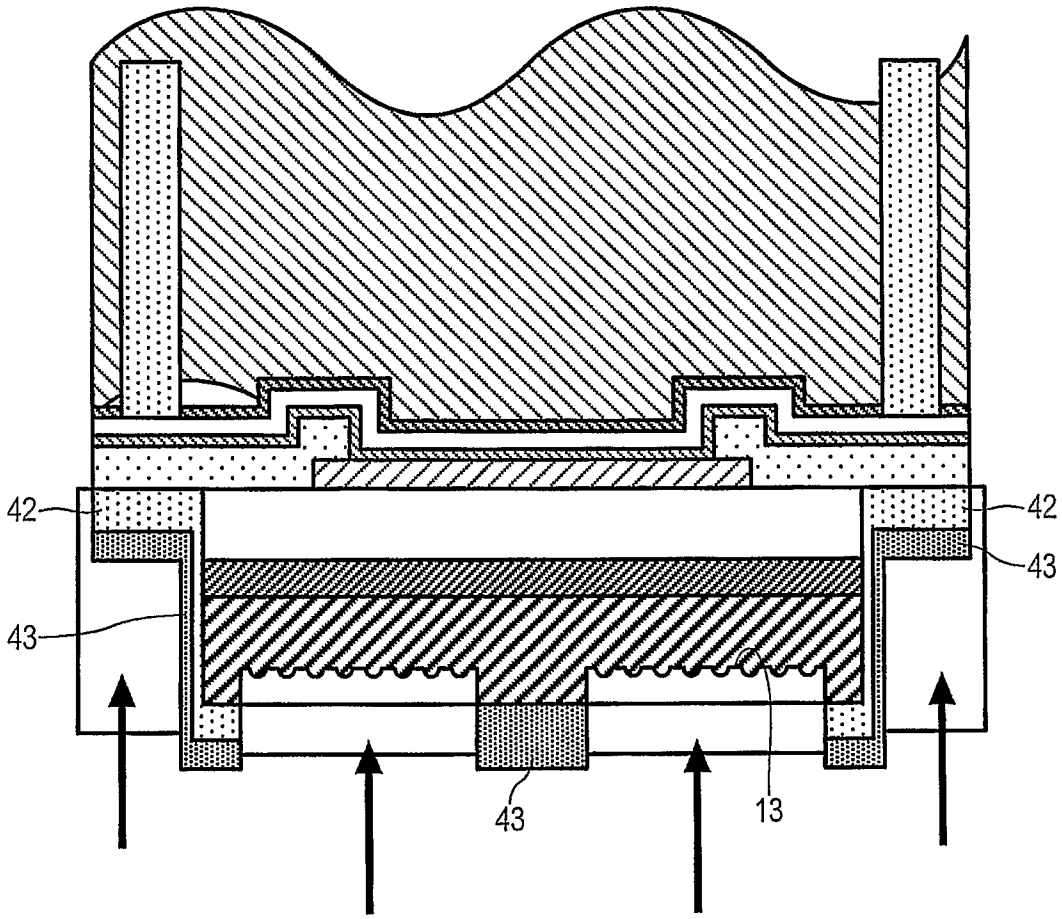

FIG. 13

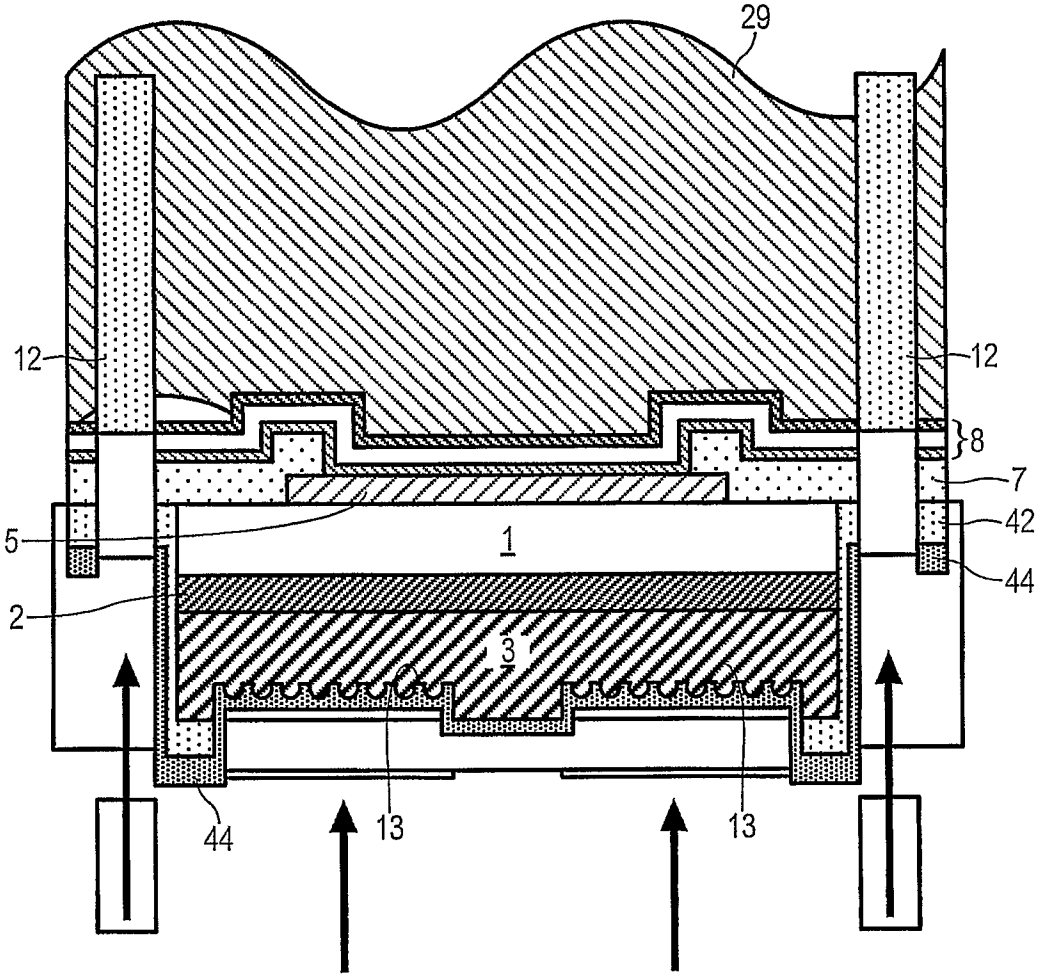

FIG. 14

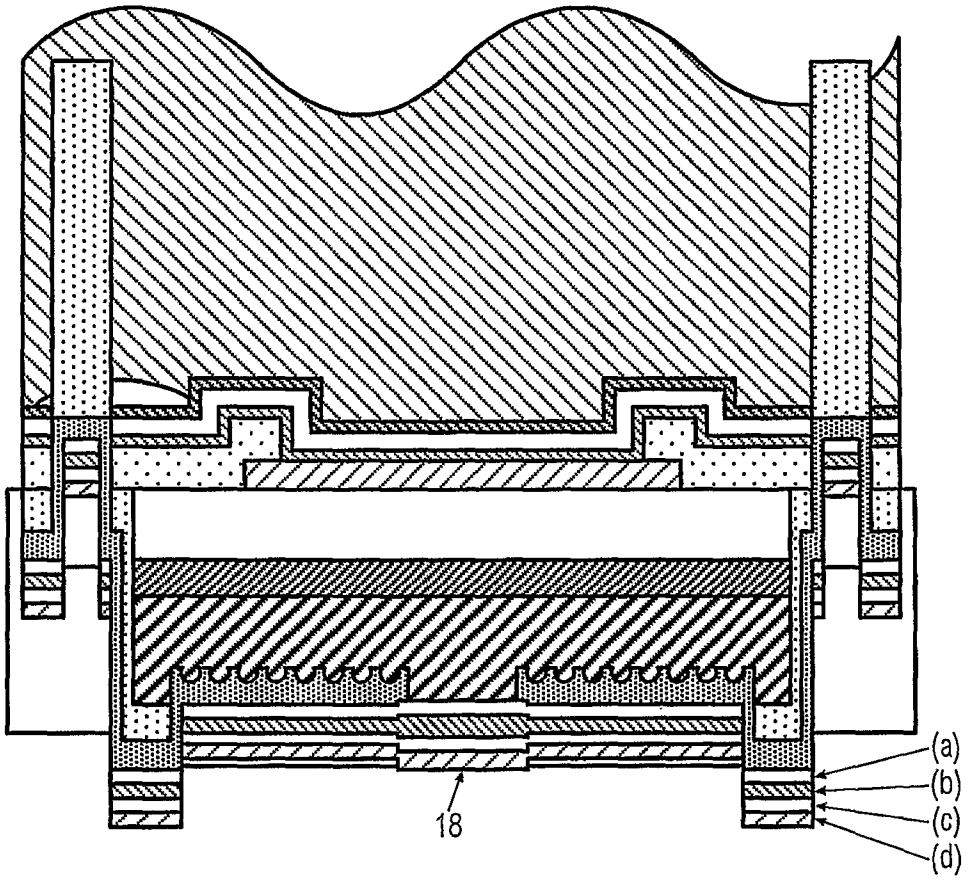

FIG. 15

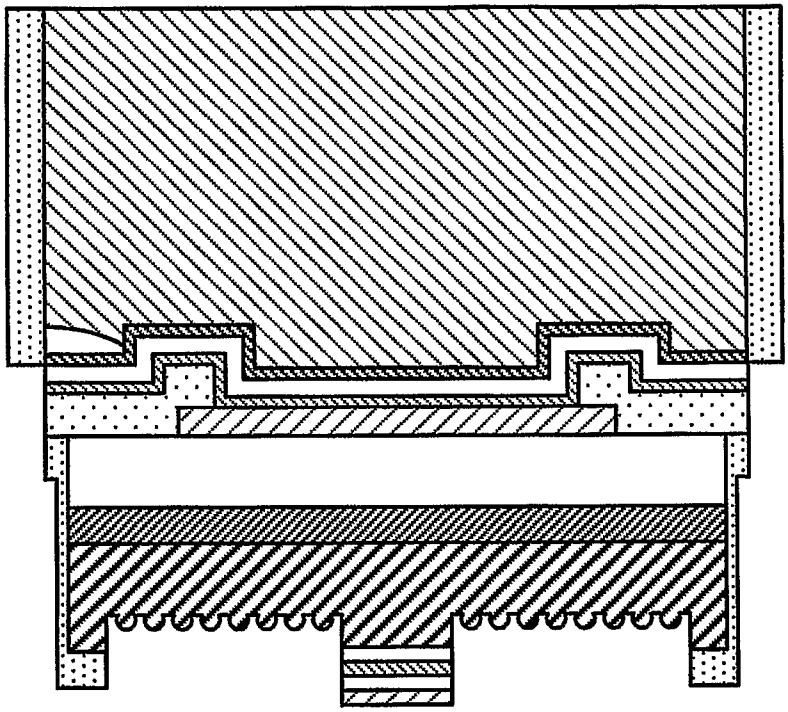

FIG. 16

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SG2008/000238

A. CLASSIFICATION OF SUBJECT MATTER

Int. Cl.

H01L 21/26 (2006.01) ***H01L 23/12*** (2006.01)
H01L 21/36 (2006.01) ***H01L 27/00*** (2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
DWPI & keywords (semiconductor, substrate, epitaxial, separate, laser, prior and similar terms); INSPEC & keywords (LED, sapphire, epitaxial, detach, laser, before and similar terms); Espacenet and keyword (Tinggi)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2007/037762 A1 (TINGGI TECHNOLOGIES PRIVATE LIMITED) 5April 2007 See abstract, page 8 line 33 to page 9 line 26, page 11 lines 20-28, page 12 lines 1-25	1-10,13-28
X	WO 2005/029572 A1 (TINGGI TECHNOLOGIES PRIVATE LIMITED) 31 March 2005 See page 7 line 25 to page 11	1-9,13-28
X	WO 2005/008740 A2 (ALLEGIS TECHNOLOGIES INC) 27 January 2005 See abstract, page 8 line 1 to page 11 line 3, page 11 line 21 to page 12 line 6	1,14,19-25,28

[X] Further documents are listed in the continuation of Box C [X] See patent family annex

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
01 August 2008	06 AUG 2008
Name and mailing address of the ISA/AU AUSTRALIAN PATENT OFFICE PO BOX 200, WODEN ACT 2606, AUSTRALIA E-mail address: pct@ipaustralia.gov.au Facsimile No. +61 2 6283 7999	Authorized officer **STEPHEN CLARK** AUSTRALIAN PATENT OFFICE (ISO 9001 Quality Certified Service) Telephone No : +61 2 6283 2781

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SG2008/000238

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2005/0247950 A1 (NAKAMURA et al) 10 November 2005 See paragraphs 0033, 0034, 0036, 0039, 0041, 0043	1,14,19
A	US 5972781 A (WEGLEITER et al) 26 October 1999 See whole document (indicates art in trench etching for isolating chips-may be used as Y with citation 2 above if that disclosure not regarded as sufficient)	2-7
A	Derwent Abstract Accession No. 2006-690443/72, Class L03, CN 1779996 A (UNIVERSITY OF BEIJING) 31 May 2006 See English abstract	1,19,20,28

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/SG2008/000238

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report		Patent Family Member					
WO	2007037762	EP	1949458	SG	130975		
WO	2005029572	AU	2003263726	CN	1839470	EP	1668687
WO	2005008740	EP	1664393	US	7015117	US	7393705
		US	2005042845				
US	2005247950	CA	2564957	CN	1950957	EP	1759424
		KR	2007001329	WO	2005112138		
US	5972781	NONE					
CN	1779996	NONE					

Due to data integration issues this family listing may not include 10 digit Australian applications filed since May 2001.

END OF ANNEX