(12) UK Patent Application (19) GB (11) 2 454 193 (13) A

(43) Date of A Publication 06.05.2009

(21) Application No: 0721269.9

(22) Date of Filing: 30.10.2007

(51) INT CL:
H03M 13/27 (2006.01) *H04L 27/26* (2006.01)

(56) Documents Cited:
EP 1463256 A1 **WO 2006/136883 A1**
US 20070250742 A1

(58) Field of Search:
INT CL **H03M, H04L**
Other: **EPODOC, WPI, Inspec**

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(continued on next page)

(54) Abstract Title: **DVB interleaver for odd/even symbol streams splits memory for sub-carrier number up to half maximum/has common memory and immediate location reuse otherwise**

(57) DVB-T or H uses OFDM transmission in 2k, 4k or 8k modes with approximately those numbers of sub carriers. In a known interleaving method symbols to be placed on to sub-carriers are split into odd and even streams. The odd symbols are written into sequential memory locations (132) and then read out in a permuted order (134), meanwhile the even symbols are written into permuted memory locations (120) and read out in a sequential order (126). By making the permuted orders identical it is possible to read out an odd/even symbol and the immediately read an even/odd symbol into the memory location that has just been 'vacated'.

In practice the sequential write permuted read interleaving performs better. Therefore the invention proposes splitting the memory and using this scheme for both odd and even symbol streams when the number of sub-carriers is less than or equal to half the maximum number, and the memory can accommodate the two streams without the need to immediately reuse memory locations.

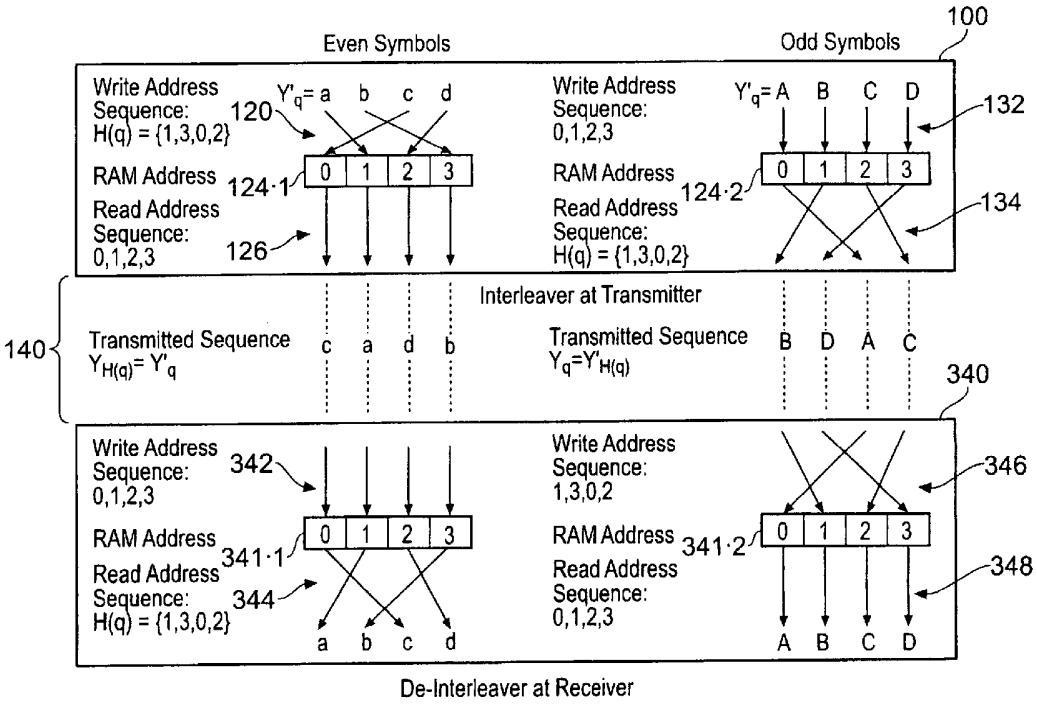

FIG. 4

At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

This print takes account of replacement documents submitted after the date of filing to enable the application to comply with the formal requirements of the Patents Rules 1995

Original Printed on Recycled Paper

GB 2 454 193 A

GB 2454193 A continuation

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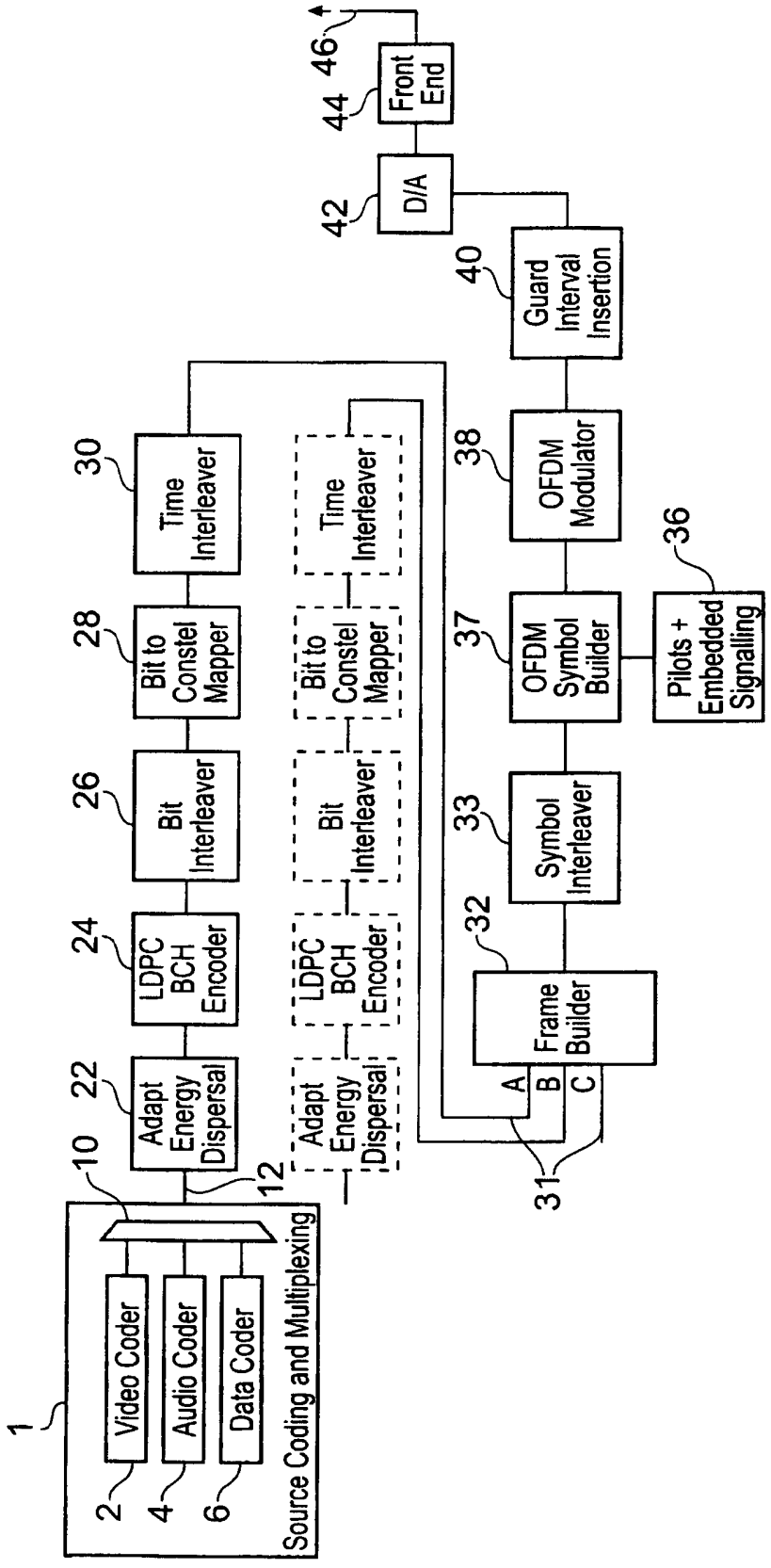
1
Source Coding and Multiplexing
Video Coder
Audio Coder
Data Coder
2
4
6
10
12
22
Adapt Energy Dispersal
24
LDPC BCH Encoder
26
Bit Interleaver
28
Bit to Constel Mapper
30
Time Interleaver
Adapt Energy Dispersal
LDPC BCH Encoder
Bit Interleaver
Bit to Constel Mapper
Time Interleaver
31
32
Frame Builder
A
B
C
33
Symbol Interleaver
37
OFDM Symbol Builder
36
Pilots + Embedded Signalling
38
OFDM Modulator
40
Guard Interval Insertion
42
D/A
44
Front End
46

FIG. 1

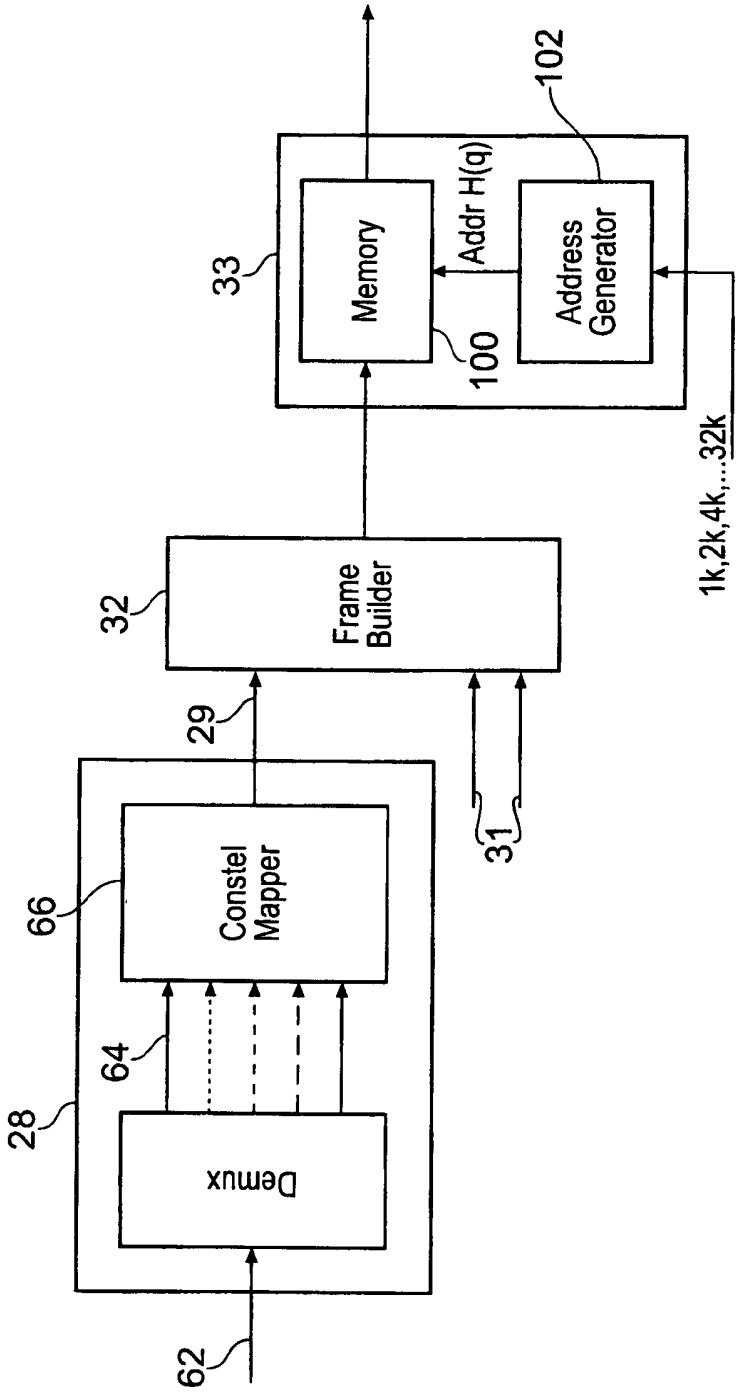
62
28
64
66
Demux
Constel Mapper
29
32
Frame Builder
31
33
Memory
100
Addr H(q)
Address Generator
102
1k,2k,4k,...32k

FIG. 2

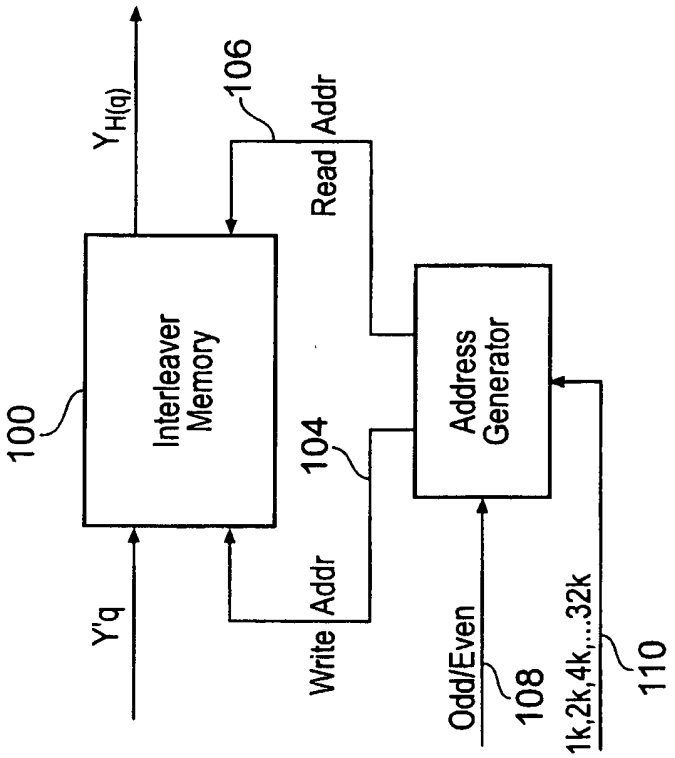
100
Interleaver Memory
$Y_{H(q)}$
106
Read Addr
104
Write Addr
Y'q
Address Generator
Odd/Even
108
1k,2k,4k,...32k
110

FIG. 3

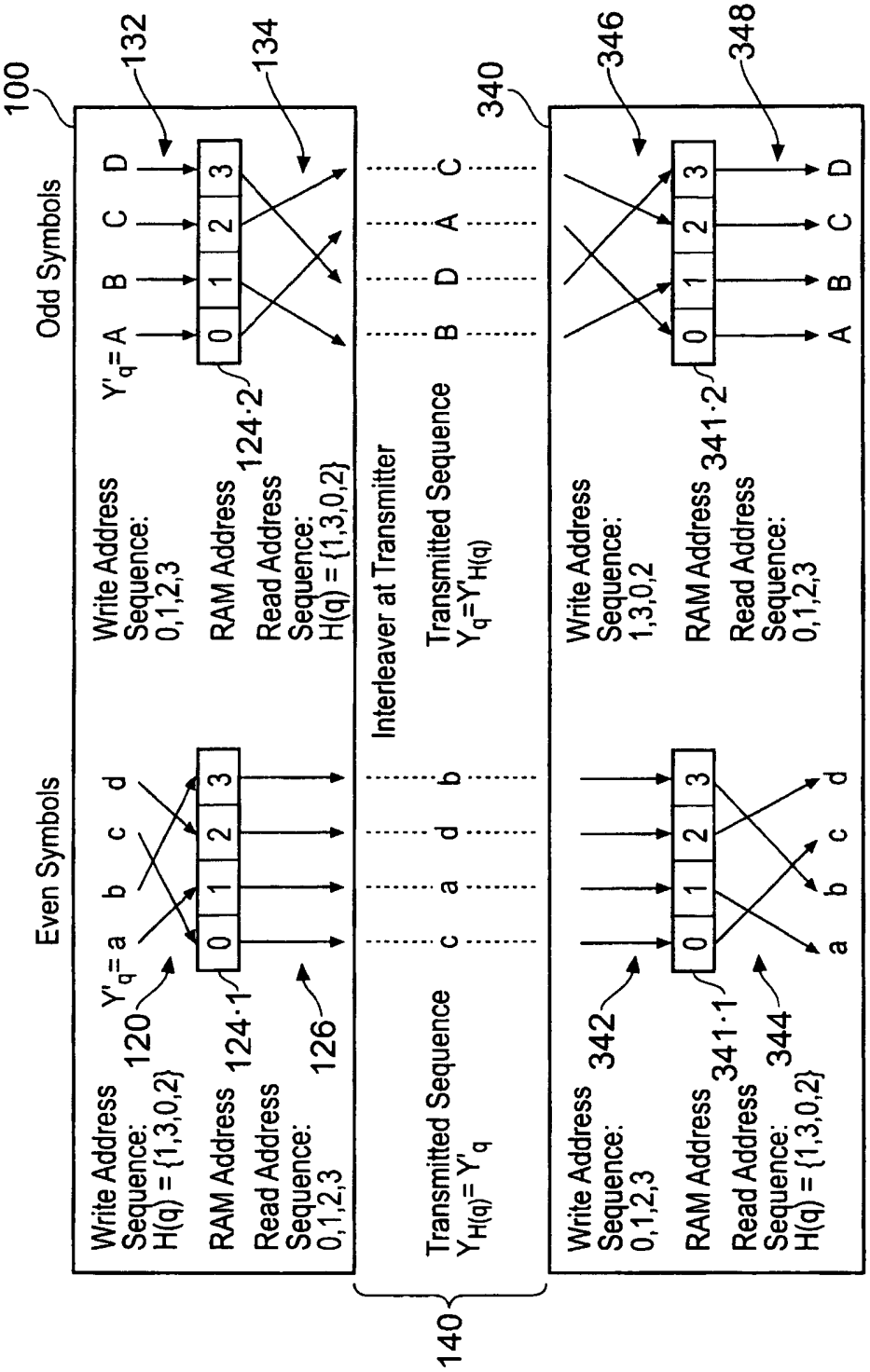
100
Even Symbols
Odd Symbols
Write Address Sequence: H(q) = {1,3,0,2}
120
Y'q= a b c d
RAM Address
124·1
Read Address Sequence: 0,1,2,3
126
Y'q= A B C D
132
RAM Address
124·2
Read Address Sequence: H(q) = {1,3,0,2}
134
Interleaver at Transmitter
Transmitted Sequence YH(q)= Y'q
c a d b
Transmitted Sequence Yq=Y'H(q)
B D A C
140
340
Write Address Sequence: 0,1,2,3
342
RAM Address
341·1
Read Address Sequence: H(q) = {1,3,0,2}
344
a b c d
Write Address Sequence: 1,3,0,2
346
RAM Address
341·2
Read Address Sequence: 0,1,2,3
348
A B C D
De-Interleaver at Receiver

FIG. 4

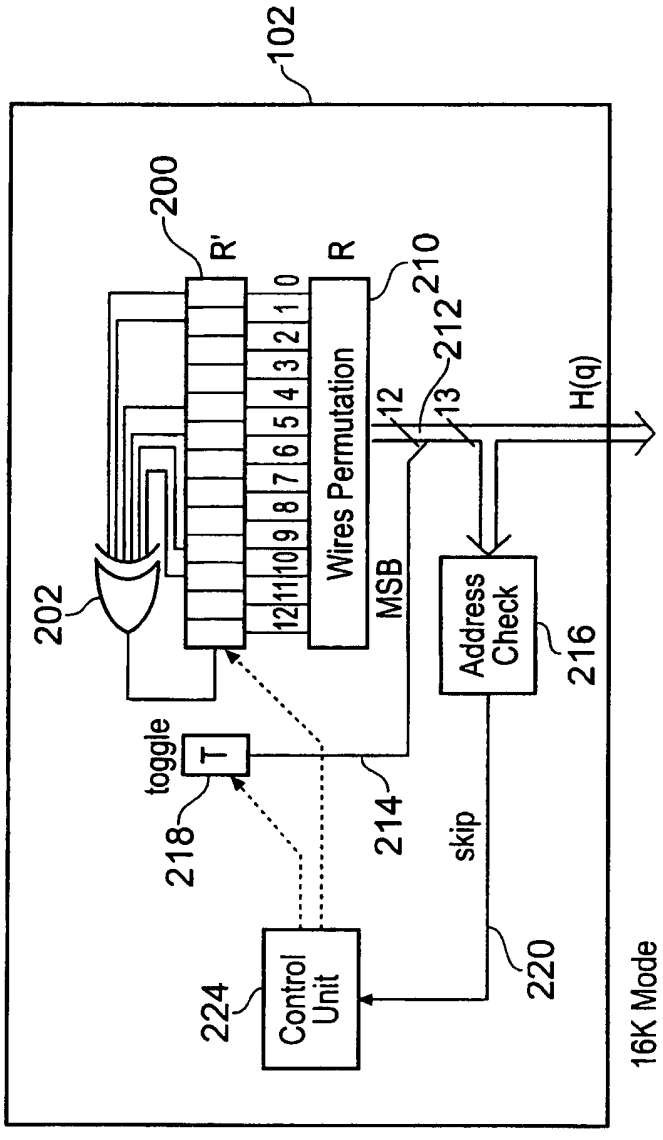
102
200
R'
R
210
212
202
12|11|10|9|8|7|6|5|4|3|2|1|0
Wires Permutation
MSB
12
13
H(q)
Address Check
216
toggle
T
218
214
skip
220
224
Control Unit
16K Mode

FIG. 5

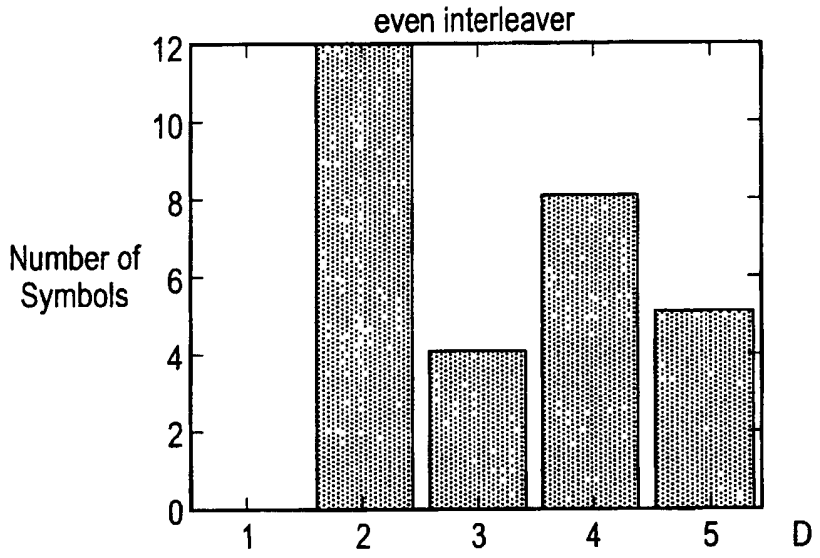
even interleaver
Number of Symbols
0
2
4
6
8
10
12
1
2
3
4
5
D

FIG. 6(a)

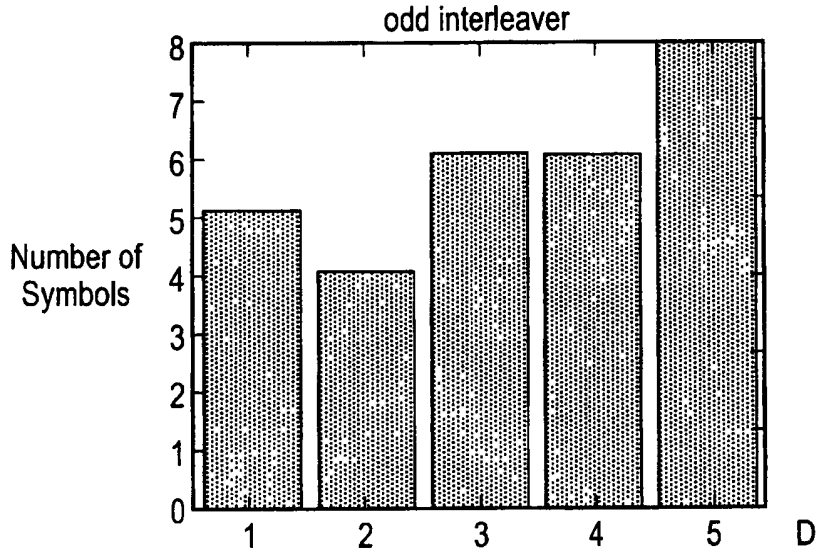
odd interleaver
Number of Symbols
0
1
2
3
4
5
6
7
8
1
2
3
4
5
D

FIG. 6(b)

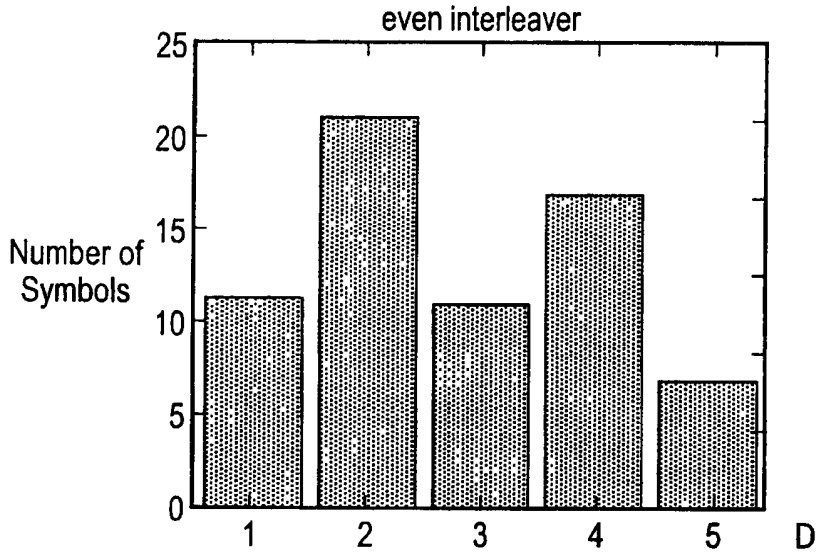
even interleaver
Number of Symbols
25
20
15
10
5
0
1
2
3
4
5
D

FIG. 6(c)

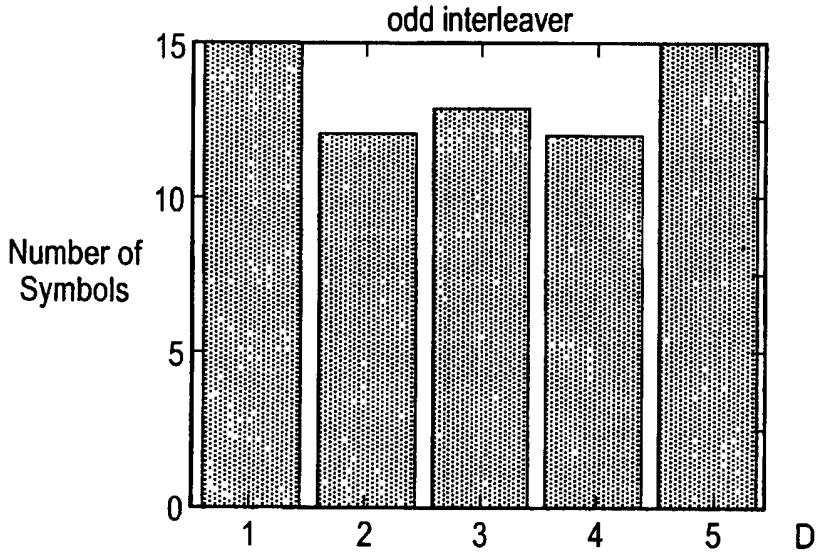
odd interleaver
Number of Symbols
15
10
5
0
1
2
3
4
5
D

FIG. 6(d)

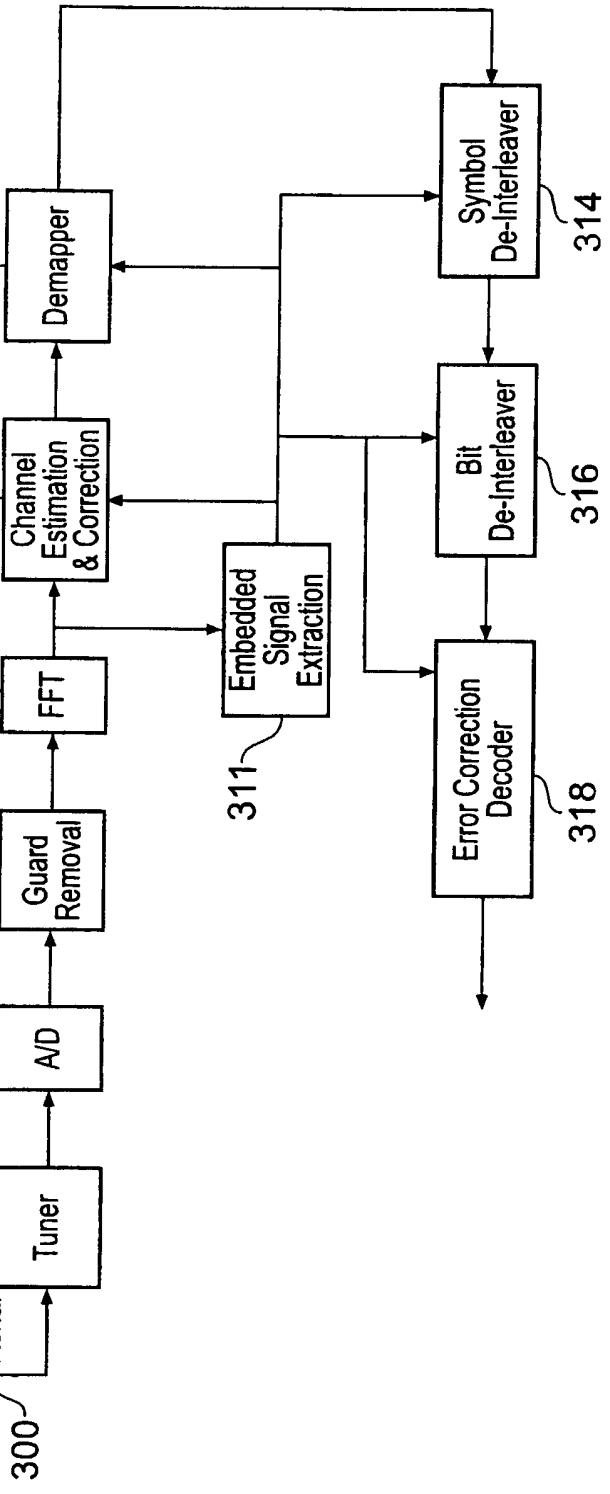
From Aerial
300
Tuner
302
A/D
304
Guard Removal
306
FFT
308
Channel Estimation & Correction
310
Demapper
312
Embedded Signal Extraction
311
Symbol De-Interleaver
314
Bit De-Interleaver
316
Error Correction Decoder
318

FIG. 7

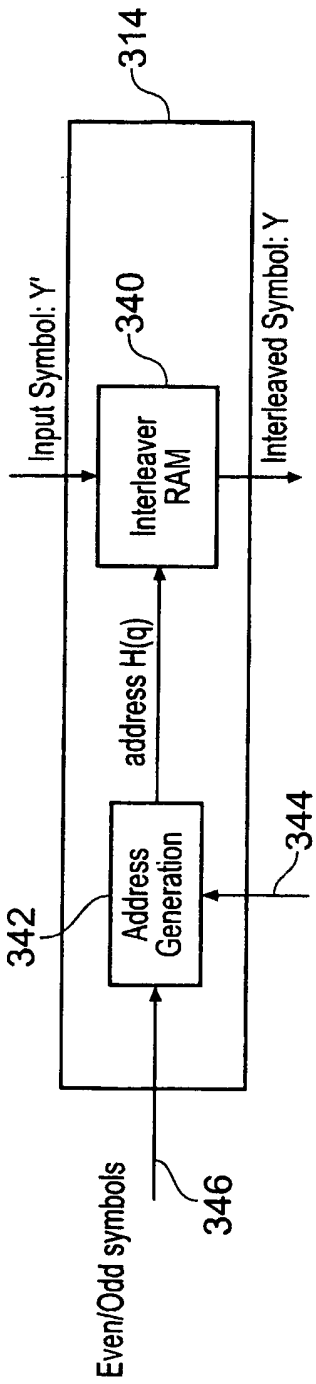
314
Input Symbol: Y'
340
Interleaver RAM
Interleaved Symbol: Y
address H(q)
342
Address Generation
344
Mode
Even/Odd symbols
346

FIG. 8

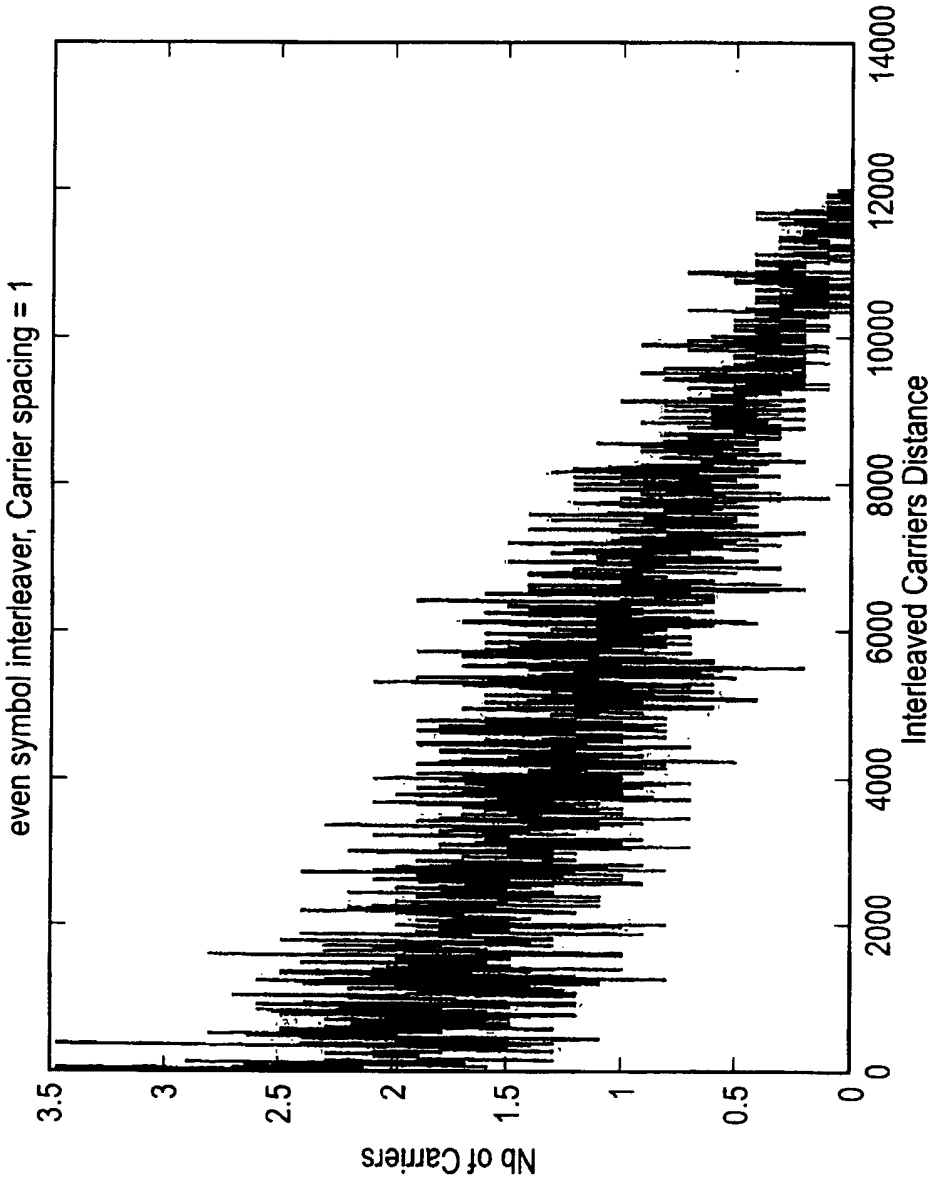
even symbol interleaver, Carrier spacing = 1
Nb of Carriers
Interleaved Carriers Distance
0
0.5
1
1.5
2
2.5
3
3.5
0
2000
4000
6000
8000
10000
12000
14000

FIG. 9(a)

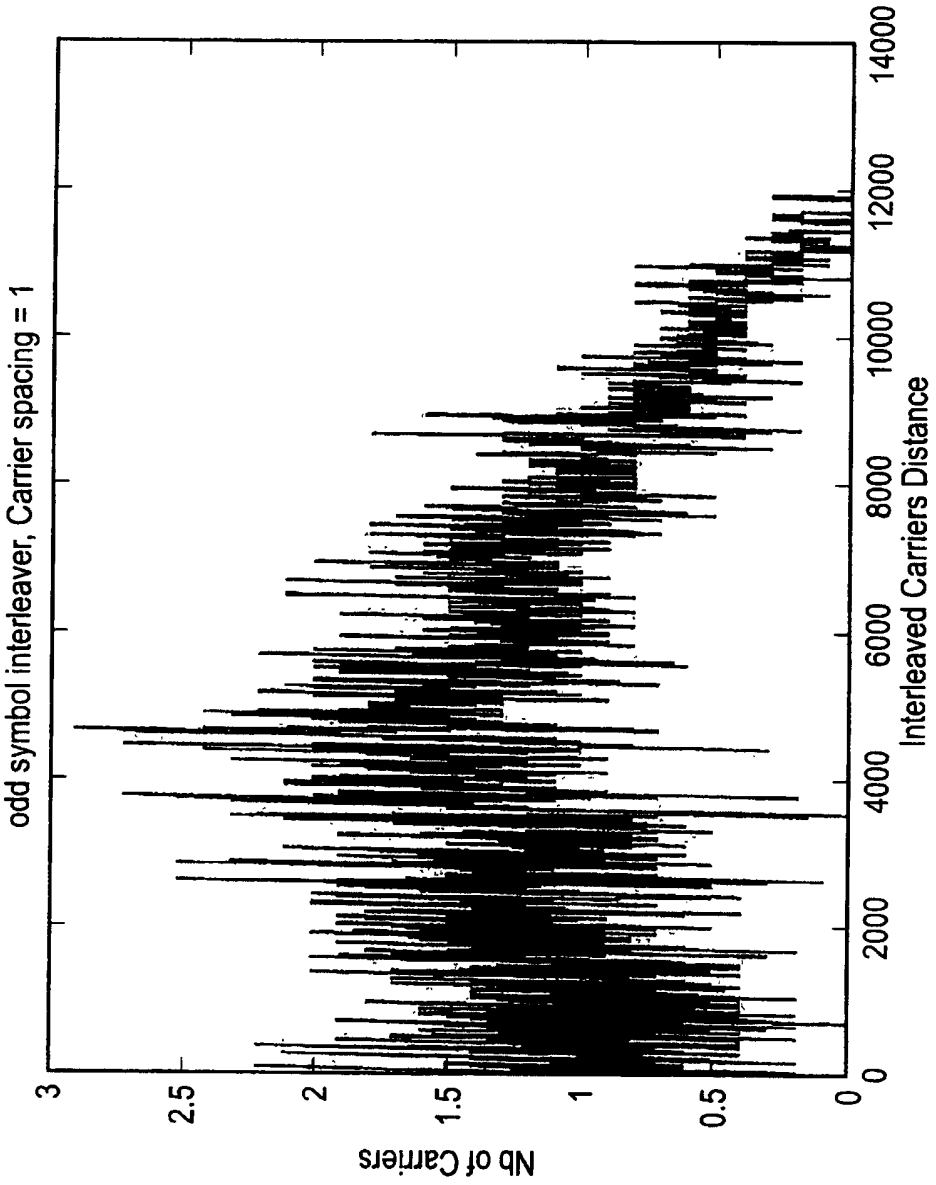
odd symbol interleaver, Carrier spacing = 1
Nb of Carriers
Interleaved Carriers Distance
0
0.5
1
1.5
2
2.5
3
0
2000
4000
6000
8000
10000
12000
14000

FIG. 9(b)

DATA PROCESSING APPARATUS AND METHOD

Field of Invention

The present invention relates to data processing apparatus operable to map input symbols onto sub-carrier signals of an Orthogonal Frequency Division Multiplexed (OFDM) symbol. The present invention also relates to an address generator for use in writing symbols to/reading symbols from an interleaver memory.

The present invention also relates to data processing apparatus operable to map symbols received from a predetermined number of sub-carrier signals of an OFDM symbol into an output symbol stream.

Embodiments of the present invention can provide an OFDM transmitter/receiver.

Background of the Invention

The Digital Video Broadcasting-Terrestrial standard (DVB-T) utilises Orthogonal Frequency Division Multiplexing (OFDM) to communicate data representing video images and sound to receivers via a broadcast radio communications signal. There are known to be two modes for the DVB-T standard which are known as the 2k and the 8k mode. The 2k mode provides 2048 sub-carriers whereas the 8k mode provides 8192 sub-carriers. Similarly for the Digital Video Broadcasting-Handheld standard (DVB-H) a 4k mode has been provided, in which the number of sub-carriers is 4096.

In order to improve the integrity of data communicated using DVB-T or DVB-H a symbol interleaver is provided in order to interleave input data symbols as these symbols are mapped onto the sub-carrier signals of an OFDM symbol. Such a symbol interleaver comprises an interleaver memory in combination with an address generator. The address generator generates an address for each of the input symbols, each address indicating one of the sub-carrier signals of the OFDM symbol onto which the data symbol is to be mapped. For the 2k mode and the 8k mode an arrangement has been disclosed in the DVB-T standard for generating the addresses for the mapping. Likewise for the 4k mode of DVB-H standard, an arrangement for generating addresses for the mapping has been provided and an address generator for

implementing this mapping is disclosed in European Patent application 04251667.4. The address generator comprises a linear feed back shift register which is operable to generate a pseudo random bit sequence and a permutation circuit. The permutation circuit permutes the order of the content of the linear feed back shift register in order to generate an address. The address provides an indication of one of the OFDM sub-carriers for carrying an input data symbol stored in the interleaver memory, in order to map the input symbols onto the sub-carrier signals of the OFDM symbol.

In accordance with a further development of the Digital Video Broadcasting-Terrestrial broadcasting standard, known as DVB-T2 there has been proposed that further modes for communicating data be provided.

Summary of Invention

According to an aspect of the present invention there is provided a data processing apparatus operable to map input symbols to be communicated onto a predetermined number of carrier signals of an Orthogonal Frequency Division Multiplexed (OFDM) symbol, the predetermined number of carrier signals corresponding to a modulation mode and the input symbols including first data symbols for mapping onto a first OFDM symbol and second data symbols for mapping onto a second OFDM symbol. The data processing apparatus comprises an interleaver operable to perform an odd interleaving process which interleaves first input data symbols on to the carrier signals and an even interleaving process which interleaves second input data symbols on to the carrier signals, the odd interleaving process writing the first input data symbols into an interleaver memory in accordance with a sequential order of the first input data symbols and reading out the first data symbols from the interleaver memory on to the carrier signals in a accordance with an order defined by a permutation code, the even interleaving process writing the second input data symbols into an interleaver memory in a accordance with an order defined by the permutation code and reading out the second data symbols from the interleaver memory on to the carrier signals in accordance with a sequential order such that while a first input data symbol is being read from a location in the interleaver memory, a second symbol can be written to the location just read from and when a second symbol is read from the location in the interleaver memory, a following first symbol can be written to the location just read from. When the modulation mode is a mode which includes half or less than half a number of carrier signals than a total number of carriers that can be accommodated by the interleaver memory, the data apparatus is operable to interleave both first and second input symbols in accordance with the odd interleaving process.

In some embodiments a data processing apparatus is operable to map input symbols to be communicated onto a predetermined number of carrier signals of an Orthogonal Frequency Division Multiplexed (OFDM) symbol. The predetermined number of carrier signals correspond to a modulation mode and the input symbols including odd data symbols and even data symbols. The data processing apparatus

comprising an interleaver operable to perform a first interleaving process which interleaves odd input data symbols on to the carrier signals and an even interleaving process which interleaves even input data symbols on to the carrier signals. The first odd interleaving process and even interleaving process reads-in and reads out the data symbols for mapping onto the OFDM carrier signals to an interleaver memory the read-out being in a different order than the read-in such that while an odd symbol is being read from a location in the memory, an even symbol can be written to the location just read from and when an even symbol is read from the location in the memory, a following odd symbol can be written to the location just read from, the odd interleaving process reading-in and reading-out odd data symbols from the interleaver memory in accordance with an odd interleaving scheme. The even interleaving process reading-in and reading-out even data symbols from the interleaver memory in accordance with an even interleaving scheme. When the modulation mode is a mode which includes half or less than half carrier signals than a total number of carriers that can be accommodated by the interleaver memory, the data apparatus is operable to assign a portion of the interleaving memory to the first odd interleaving process and assign a second portion of the interleaving memory to a second odd interleaving process operating in accordance with the first, the second odd interleaving process interleaving the even input symbols.

In some conventional OFDM transmitters and in accordance with the 2k and 8k modes for DVB-T and the 4k mode for DVB-H, two symbol interleaving processes are used in the transmitter: one for even symbols and one for odd symbols. However, analysis has shown that the interleaving schemes designed for the 2k and 8k symbol interleavers for DVB-T and the 4k symbol interleaver for DVB-H work better for odd symbols than even symbols. Therefore, embodiments of the present invention are arranged so that only the odd symbol interleaving process is used unless the transmitter/receiver is in the mode with the maximum number of sub-carriers.

Various aspects and features of the present invention are defined in the appended claims. Further aspects of the present invention include a data processing apparatus operable to map symbols received from a predetermined number of sub-carrier signals of an Orthogonal Frequency Division Multiplexed (OFDM) symbol into an output symbol stream, as well as a transmitter and a receiver.

Brief Description of Drawings

Embodiments of the present invention will now be described by way of example only with reference to the accompanying drawings, wherein like parts are provided with corresponding reference numerals, and in which:

Figure 1 is a schematic block diagram of a Coded OFDM transmitter which may be used, for example, with the DVB-T2 standard;

Figure 2 is a schematic block diagram of parts of the transmitter shown in Figure 1 in which a symbol mapper and a frame builder illustrate the operation of an interleaver;

Figure 3 is a schematic block diagram of the symbol interleaver shown in Figure 2;

Figure 4 is a schematic block diagram of an interleaver memory shown in Figure 3 and the corresponding symbol de-interleaver in the receiver;

Figure 5 is a schematic block diagram of an address generator shown in Figure 3 for the 16k mode;

Figure 6(a) is diagram illustrating results for an interleaver using the address generator shown in Figure 5 for even symbols and Figure 6(b) is a diagram illustrating design simulation results for odd symbols, whereas Figure 6(c) is a diagram illustrating comparative results for an address generator using a different permutation code for even and Figure 6(d) is a corresponding diagram for odd symbols;

Figure 7 is a schematic block diagram of a Coded OFDM receiver which may be used, for example, with the DVB-T2 standard;

Figure 8 is a schematic block diagram of a symbol de-interleaver which appears in Figure 7; and

Figure 9(a) is diagram illustrating results for an interleaver using the address generator shown in Figure 5 for even symbols and Figure 9(b) is a diagram illustrating results for odd symbols. Figures 9(a) and 9(b) show plots of the distance at the interleaver output of sub-carriers that were adjacent at the interleaver input.

Description of Preferred Embodiments

It has been proposed that the number of modes, which are available within the DVB-T2 standard should be extended to include a 1k mode, a 16k mode and a 32k mode. The following description is provided to illustrate the operation of a symbol interleaver in accordance with the present technique, although it will be appreciated that the symbol interleaver can be used with other modes and other DVB standards.

Figure 1 provides an example block diagram of a Coded OFDM transmitter which may be used for example to transmit video images and audio signals in accordance with the DVB-T2 standard. In Figure 1 a program source generates data to be transmitted by the COFDM transmitter. A video coder 2, and audio coder 4 and a data coder 6 generate video, audio and other data to be transmitted which are fed to a program multiplexer 10. The output of the program multiplexer 10 forms a multiplexed stream with other information required to communicate the video, audio and other data. The multiplexer 10 provides a stream on a connecting channel 12. There may be many such multiplexed streams which are fed into different branches A, B etc. For simplicity, only branch A will be described.

As shown in Figure 1 a COFDM transmitter 20 receives the stream at a multiplexer adaptation and energy dispersal block 22. The multiplexer adaptation and energy dispersal block 22 randomises the data and feeds the appropriate data to a forward error correction encoder 24 which performs error correction encoding of the stream. A bit interleaver 26 is provided to interleave the encoded data bits which for the example of DVB-T2 is the LDCP/BCH encoder output. The output from the bit interleaver 26 is fed to a bit into constellation mapper 28, which maps groups of bits onto a constellation point, which is to be used for conveying the encoded data bits. The outputs from the bit into constellation mapper 28 are constellation point labels that represent real and imaginary components. The constellation point labels represent data symbols formed from two or more bits depending on the modulation scheme used. These will be referred to as data cells. These data cells are passed through a time-interleaver 30 whose effect is to interleaver data cells resulting from multiple LDPC code words.

The data cells are received by a frame builder 32, with data cells produced by branch B etc in Figure 1, via other channels 31. The frame builder 32 then forms many data cells into sequences to be conveyed on COFDM symbols, where a COFDM symbol comprises a number of data cells, each data cell being mapped onto one of the sub-carriers. The number of sub-carriers will depend on the mode of operation of the system, which may include one of 1k, 2k, 4k, 8k, 16k or 32k, each of which provides a different number of sub-carriers according, for example to the following table:

Mode	Sub-carriers
1K	756
2K	1512
4K	3024
8K	6048
16K	12096
32K	24192

Number of Sub-carriers Adapted from DVB-T/H

Thus in one example, the number of sub-carriers for the 16k mode is twelve thousand and ninety six.

Each frame comprises many such COFDM symbols. The sequence of data cells to be carried in each COFDM symbol is then passed to the symbol interleaver 33. The COFDM symbol is then generated by a COFDM symbol builder block 37 which uses the constellation data labels to generate the real and imaginary parts of the constellation points and also introducing pilot and synchronising signals fed from a pilot and embedded signal former 36. An OFDM modulator 38 then forms the OFDM symbol in the time domain which is fed to a guard insertion processor 40 for generating a guard interval between symbols, and then to a digital to analogue convertor 42 and finally to an RF amplifier within an RF front 44 for eventual broadcast by the COFDM transmitter from an antenna 46.

Providing a 16k Mode

To create a new 16K mode, several elements are to be defined, one of which is the 16K symbol interleaver 33. The bit to constellation mapper 28, symbol interleaver 33 and the frame builder 32 are shown in more detail in Figure 2.

As explained above, the present invention provides a facility for providing a quasi-optimal mapping of the data symbols onto the OFDM sub-carrier signals. According to the example technique the symbol interleaver is provided to effect the optimal mapping of input data symbols onto COFDM sub-carrier signals in accordance with a permutation code and generator polynomial, which has been verified by simulation analysis.

As shown in Figure 2 a more detailed example illustration of the bit to symbol constellation mapper 28 and the frame builder 32 is provided to illustrate an example embodiment of the present technique. Data bits received from the bit interleaver 26 via a channel 62 are grouped into sets of bits to be mapped onto a data cell, in accordance with a number of bits per symbol provided by the modulation scheme. The groups of bits, which forms a data word, are fed in parallel via data channels 64 the a mapping processor 66. The mapping processor 66 then selects one of the data symbols, in accordance with a pre-assigned mapping. The constellation point, is represented by a real and an imaginary component but only its label is provided to the output channel 29 as one of a set of inputs to the frame builder 32.

The frame builder 32 receives the data cells from the bit to constellation mapper 28 through channel 29, together with data cells from the other channels 31. After building a frame of many COFDM cell sequences, the cells of each COFDM symbol are then written into an interleaver memory 100 and read out of the interleaver memory 100 in accordance with write addresses and read addresses generated by an address generator 102. According to the write-in and read-out order, interleaving of the data cells is achieved, by generating appropriate addresses. The operation of the address generator 102 and the interleaver memory 100 will be described in more detail shortly with reference to Figures 3, 4 and 5. The interleaved data cells are then mapped to real and imaginary components of data symbols, which are combined with pilot and synchronisation symbols received from the pilot and embedded signalling former 36 into an OFDM symbol builder 37, to form the COFDM symbol, which is fed to the OFDM modulator 38 as explained above.

Interleaver

Figure 3 provides an example of parts of the symbol interleaver 33, which illustrates the present technique for interleaving symbols. In Figure 3 the input data cells from the frame builder 32 are written into the interleaver memory 100. The data cells are written into the interleaver memory 100 according to a write address fed from the address generator 102 on channel 104, and read out from the interleaver memory 100 according to a read address fed from the address generator 102 on a channel 106. The address generator 102 generates the write address and the read address as explained below, depending on whether the COFDM symbol is odd or even, which is identified from a signal fed from a channel 108, and depending on a selected mode, which is identified from a signal fed from a channel 110. As explained, the mode can be one of a 1k mode, 2k mode, 4k mode, 8k mode, 16k mode or a 32k mode. As explained below, the write address and the read address are generated differently for odd and even symbols as explained with reference to Figure 4, which provides an example implementation of the interleaver memory 100.

In the example shown in Figure 4, the interleaver memory is shown to comprise an upper part 100 illustrating the operation of the interleaver memory in the transmitter and a lower part 340, which illustrates the operation of the de-interleaver memory in the receiver. The interleaver 100 and the de-interleaver 340 are shown together in Figure 4 in order to facilitate understanding of their operation. As shown in Figure 4 a representation of the communication between the interleaver 100 and the de-interleaver 340 via other devices and via a transmission channel has been simplified and represented as a section 140 between the interleaver 100 and the de-interleaver 340. The operation of the interleaver 100 is described in the following paragraphs:

Although Figure 4 provides an illustration of only four input data cells onto an example of four sub-carrier signals of a COFDM symbol, it will be appreciated that the technique illustrated in Figure 4 can be extended to a larger number of sub-carriers such as 756 for the 1k mode 1512 for the 2k mode, 3024 for the 4k mode and 6048 for the 8k mode, 12096 for the 16k mode and 24192 for the 32k mode.

The input and output addressing of the interleaver memory 100 shown in Figure 4 is shown for odd and even symbols. For an even COFDM symbol the data cells are taken from the input channel 77 and written into the interleaver memory 124.1 in accordance with a sequence of addresses 120 generated for each COFDM

symbol by the address generator 102. The write addresses are applied for the even symbol so that as illustrated interleaving is effected by the shuffling of the write-in addresses. Therefore, for each interleaved symbol $y(h(q)) = y'(q)$.

For odd symbols the same interleaver memory 124.2 is used. However, as shown in Figure 4 for the odd symbol the write-in order 132 is in the same address sequence used to read out the previous even symbol 126. This feature allows the odd and even symbol interleaver implementations to only use one interleaver memory 100 provided the read-out operation for a given address is performed before the write-in operation. The data cells written into the interleaver memory 124 during odd symbols are then read out in a sequence 134 generated by the address generator 102 for the next even COFDM symbol and so on. Thus only one address is generated per symbol, with the read-in and write-out for the odd/even COFDM symbol being performed contemporaneously.

In summary, as represented in Figure 4, once the set of addresses H(q) has been calculated for all active sub-carriers, the input vector $Y' = (y_0', y_1', y_2', \ldots y_{Nmax-1}')$ is processed to produce the interleaved vector $Y = (y_0, y_1, y_2, \ldots y_{Nmax-1})$ defined by:

$$y_{H(q)} = y'_q \text{ for even symbols for } q = 0,\ldots,N_{max}-1$$

$$y_q = y'_{H(q)} \text{ for odd symbols for } q = 0,\ldots,N_{max}-1$$

In other words, for even OFDM symbols the input words are written in a permutated way into a memory and read back in a sequential way, whereas for odd symbols, they are written sequentially and read back permutated. In the above case, the permutation H(q) is defined by the following table:

q	0	1	2	3
H(q)	1	3	0	2

Table 1: permutation for simple case where Nmax =4

As shown in Figure 4, the de-interleaver 340 operates to reverse the interleaving applied by the interleaver 100, by applying the same set of addresses as generated by an equivalent address generator, but applying the write-in and read-out addresses in reverse. As such, for even symbols, the write-in addresses 342 are in sequential order, whereas the read out address 344 are provided by the address

generator. Correspondingly, for the odd symbols, the write-in order 346 is determined from the set of addresses generated by the address generator, whereas read out 348 is in sequential order.

Address Generation for the 16k Mode

A schematic block diagram of the algorithm used to generate the permutation function H(q) is represented in Figure 5 for the 16K mode.

An implementation of the address generator 102 for the 16k mode is shown in Figure 5. In Figure 5 a linear feed back shift register is formed by thirteen register stages 200 and a xor-gate 202 which is connected to the stages of the shift register 200 in accordance with a generator polynomial. Therefore, in accordance with the content of the shift register 200 a next bit of the shift register is provided from the output of the xor-gate 202 by xoring the content of shift registers R[0], R[1], R[4], R[5], R[9], R[11] according to the generator polynomial:

$$R_i'[12] = R_{i-1}'[0] \oplus R_{i-1}'[1] \oplus R_{i-1}'[4] \oplus R_{i-1}'[5] \oplus R_{i-1}'[9] R_{i-1}'[11]$$

According to the generator polynomial a pseudo random bit sequence is generated from the content of the shift register 200. However, in order to generate an address for the 16k mode as illustrated, a permutation circuit 210 is provided which effectively permutes the order of the bits within the shift register 200.1 from an order $R'_i[n]$ to an order $R_i[n]$ at the output of the permutation circuit 210. Thirteen bits from the output of the permutation circuit 210 are then fed on a connecting channel 212 to which is added a most significant bit via a channel 214 which is provided by a toggle circuit 218. A fourteen bit address is therefore generated on channel 212. However, in order to ensure the authenticity of an address, an address check circuit 216 analyses the generated address to determine whether it exceeds a predetermined maximum value. The predetermined maximum value may correspond to the maximum number of sub-carrier signals, which are available for data symbols within the COFDM symbol, available for the mode which is being used. However, the interleaver for the 16k mode may also be used for other modes, so that the address generator 102 may also be used for the 2k mode, 4k mode, 8k mode, 16k mode and the 32k mode, by adjusting accordingly the number of the maximum valid address.

If the generated address exceeds the predetermined maximum value then a control signal is generated by the address check unit 216 and fed via a connecting channel 220 to a control unit 224. If the generated address exceeds the predetermined maximum value then this address is rejected and a new address regenerated for the particular symbol.

For the 16k mode, an (N_r - 1) bit word R'_i is defined, with $N_r = \log_2 M_{max}$, where $M_{max} = 16384$ using a LFSR (Linear Feedback Shift Register).

The polynomials used to generate this sequence is:

16K mode: $R'_i[12] = R'_{i-1}[0] \oplus R'_{i-1}[1] \oplus R'_{i-1}[4] \oplus R'_{i-1}[5] \oplus R'_{i-1}[9] R'_{i-1}[11]$

where i varies from 0 to $M_{max} - 1$

Once one R'_i, word has been generated, the R'_i, word goes through a permutation to produce another (N_r - 1) bit word called R_i. R_i is derived from R'_i by the bit permutations given as follows:

R'_i bit positions	12	11	10	9	8	7	6	5	4	3	2	1	0
R_i bit positions	8	4	3	2	0	11	1	5	12	10	6	7	9

Bit permutation for the 16K mode

As an example, this means that for the mode 16K, the bit number 12 of R'_i is sent in bit position number 8 of R_i.

The address H(q) is then derived from R_i through the following equation:

$$H(q) = (i \bmod 2) \cdot 2^{N_r - 1} + \sum_{j=0}^{N_r - 2} R_i(j) \cdot 2^j$$

The $(i \bmod 2) \cdot 2^{N_r - 1}$ part of the above equation is represented in Figure 5 by the toggle block T 218.

An address check is then performed on H(q) to verify that the generated address is within the range of acceptable addresses: if ($H(q) < N_{max}$), where N_{max} =12096 for example in the 16K mode, then the address is valid. If the address is not valid, the control unit is informed and it will try to generate a new H(q) by incrementing the index i.

The role of the toggle block is to make sure that we do not generate an address exceeding N_{max} twice in a row. In effect, if an exceeding value was generated, this

means that the MSB (i.e. the toggle bit) of the address H(q) was one. So the next value generated will have a MSB set to zero, insuring to produce a valid address.

The following equations sum up the overall behaviour and help to understand the loop structure of this algorithm:

$q = 0;$

for $(i = 0; i < M_{max}; i = i + 1)$

$$\{ H(q) = (i \bmod 2) \cdot 2^{N_r - 1} + \sum_{j=0}^{N_r - 2} R_i(j) \cdot 2^j;$$

if $(H(q) < N_{max})$ $q = q+1;$ }

Analysis Supporting the Address Generator for the 16k Mode

The selection of the polynomial generator and the permutation code explained above for the address generator 102 for the 16k mode has been identified following simulation analysis of the relative performance of the interleaver. The relative performance of the interleaver has been evaluated using a relative ability of the interleaver to separate successive symbols or an "interleaving quality". As mentioned above, effectively the interleaver must perform for both odd and even symbols, in order to use a single interleaver memory. The relative measure of the interleaver quality is determined by defining a distance D (in number of sub-carriers). A criterion C is chosen to identify a number of sub-carriers that are at distance ≤ D at the output of the interleaver that were at distance ≤ D at the input of the interleaver, the number of sub-carriers for each distance D then being weighted with respect to the relative distance. The criterion C is evaluated for both odd and even COFDM symbols. Minimising C produces a superior quality interleaver.

$$C = \sum_{1}^{d=D} N_{even}(d) / d + \sum_{1}^{d=D} N_{odd}(d) / d$$

where

N_{even} = number of sub - carriers in an even symbol within at the output of the interleaver that remain within d sub - carriers of each other

N_{even} = number of sub - carriers in an even symbol within at the output of the interleaver that remain within d sub - carriers of each other

Analysis of the interleaver identified above for the 16k mode for a value of D = 5 is shown in Figure 6(a) for the even COFDM symbols and in Figure 6(b) for the odd COFDM symbol. According to the above analysis, the value of C for the permutation code identified above for the 16k mode produced a value of C = 22.43, that the weighted number of sub-carriers with symbols which are separated by five or less in the output according to the above equation was 22.43.

A corresponding analysis is provided for an alternative permutation code for even COFDM symbols in Figure 6(c) for odd COFDM symbols in Figure 6(d). As can be seen in comparison to the results illustrated in Figures 6(a) and 6(b), there are more components present which represent symbols separated by small distances such as D = 1, and D = 2, when compared with the results shown in Figure 6(a) and 6(b), illustrating that the permutation code identified above for the 16k mode symbol interleaver produces a superior quality interleaver.

Alternative Permutation Codes

The following nine alternative possible codes ($[n]R_i$ bit positions, where n = 1 to 9) have been found to provide a symbol interleaver with a good quality as determined by the criterion C identified above.

R'_i bit positions	12	11	10	9	8	7	6	5	4	3	2	1	0
[1]R_i bit positions	7	12	5	8	9	1	2	3	4	10	6	11	0
[2]R_i bit positions	8	5	4	9	2	3	0	1	6	11	7	12	10
[3]R_i bit positions	7	5	6	9	11	2	3	0	8	4	1	12	10
[4]R_i bit positions	11	5	10	4	2	1	0	7	12	8	9	6	3
[5]R_i bit positions	3	9	4	10	0	6	1	5	8	11	7	2	12
[6]R_i bit positions	4	6	3	2	0	7	1	5	8	10	12	9	11
[7]R_i bit positions	10	4	3	2	1	8	0	6	7	9	11	5	12
[8]R_i bit positions	10	4	11	3	7	1	5	0	2	12	8	6	9
[9]R_i bit positions	2	4	11	9	0	10	1	7	8	6	12	3	5

Bit permutation for the 16K mode

Receiver

Figure 7 provides an example illustration of a receiver which may be used with the present technique. As shown in Figure 7, a COFDM signal is received by an antenna 300 and detected by a tuner 302 and converted into a digital form by an analogue-to-digital converter 304. A guard interval removal processor 306 removes the guard interval from a received COFDM symbol, before the data is recovered from the COFDM symbol using a Fast Fourier Transform (FFT) processor 308 in combination with a channel estimator and correction 310 in co-operation with a embedded-signalling decoding unit 311, in accordance with known techniques. The demodulated data is recovered from a mapper 312 and fed to a symbol de-interleaver 314, which operates to effect the reverse mapping of the received data symbol to re-generate an output data stream with the data de-interleaved.

The symbol de-interleaver 314 is formed from a data processing apparatus as shown in Figure 7 with an interleaver memory 340 and an address generator 342. The interleaver memory is as shown in Figure 4 and operates as already explained above to effect de-interleaving by utilising sets of addresses generated by the address generator 342. The address generator 342 is formed as shown in Figure 8 and is arranged to

generate corresponding addresses to map the data symbols recovered from each COFDM sub-carrier signals into an output data stream.

The remaining parts of the COFDM receiver shown in Figure 7 are provided to effect error correction decoding 318 to correct errors and recover an estimate of the source data.

One advantage provided by the present technique for both the receiver and the transmitter is that a symbol interleaver and a symbol de-interleaver operating in the receivers and transmitters can be switched between the 1k, 2k, 4k, 8k, 16k and the 32k mode by changing the generator polynomials and the permutation order. Hence the address generator 342 shown in Figure 8 includes an input 344, providing an indication of the mode as well as an input 346 indicating whether there are odd/even COFDM symbols. A flexible implementation is thereby provided because a symbol interleaver and de-interleaver can be formed as shown in Figures 3 and 8, with an address generator as illustrated in either of Figures 5. The address generator can therefore be adapted to the different modes by changing to the generator polynomials and the permutation orders indicated for each of the modes. For example, this can be effected using a software change. Alternatively, in other embodiments, an embedded signal indicating the mode of the DVB-T2 transmission can be detected in the receiver in the embedded-signalling processing unit 311 and used to configure automatically the symbol de-interleaver in accordance with the detected mode.

Optimal Use of Odd Interleavers

As shown in Figure 4, two symbol interleaving processes, one for even symbols and one for odd symbols allows the amount of memory used during interleaving to be reduced. In the example shown in Figure 4, the write in order for the odd symbol is the same as the read out order for the even symbol therefore while an odd symbol is being read from the memory, an even symbol can be written to the location just read from; subsequently, when that even symbol is read from the memory, the following odd symbol can be written to the location just read from.

As discussed above, during analysis and for example shown in Figure 9(a) and Figure 9(b) it has been shown that the interleaving schemes designed for the 2k and 8k symbol interleavers for DVB-T and the 4k symbol interleaver for DVB-H work better

for odd symbols than even symbols. This can be seen by comparing Figure 9(a) which shows results for an interleaver for even symbols and Figure 6(b) illustrating results for odd symbols: it can be seen that the average distance at the interleaver output of sub-carriers that were adjacent at the interleaver input is greater for an interleaver for odd symbols than an interleaver for even symbols.

As will be understood, the amount of interleaver memory required to implement a symbol interleaver is dependent on the number of data symbols to be mapped onto the COFDM carrier symbols. Thus a 16k mode symbol interleaver requires half the memory required to implement a 32k mode symbol interleaver and similarly, the amount of memory required to implement an 8k symbol interleaver is half that required to implement a 16k interleaver. Therefore for a transmitter or receiver that can implement a symbol interleaver of a given mode, that receiver or transmitter will include sufficient memory to implement two odd interleaving processes for a mode half or smaller than that given mode. For example a receiver or transmitter including a 32K interleaver will have enough memory to accommodate two 16K odd interleaving processes each with their own 16K memory.

Therefore, in order to address the fact that even interleaving processes appear not to perform as well as odd interleaving processes a symbol interleaver capable of accommodating multiple modulation modes can be arranged so that only an odd symbol interleaving process is used if in a mode which comprises half or less of the number of carriers in the maximum mode. For example in a transmitter/receiver capable of the 32K mode, when operating in a mode with fewer carriers (i.e. 16K, 8K, 4K or 1K) then rather than employing separate odd and even symbol interleaving processes, two odd interleavers would be used.

Various modifications may be made to the embodiments described above without departing from the scope of the present invention. In particular, the example representation of the generator polynomial and the permutation order which have been used to represent aspects of the invention are not intended to be limiting and extend to equivalent forms of the generator polynomial and the permutation order.

As will be appreciated the transmitter and receiver shown in Figures 1 and 7 respectively are provided as illustrations only and are not intended to be limiting. For example, it will be appreciated that the position of the symbol interleaver and the de-

interleaver with respect, for example to the bit interleaver and the mapper and mapper can be changed. As will be appreciated the effect of the interleaver and de-interleaver is un-changed by its relative position, although the interleaver may be interleaving I/Q symbols instead of v-bit vectors. A corresponding change may be made in the receiver. Accordingly the interleaver and de-interleaver may be operating on different data types, and may be positioned differently to the position described in the example embodiments.

As explained above the permutation codes and generator polynomial of the interleaver, which has been described with reference to an implementation of a particular mode, can equally be applied to other modes, by changing the predetermined maximum allowed address in accordance with the number of carriers for that mode.

As mentioned above, embodiments of the present invention find application with DVB standards such as DVB-T and DVB-H, which are incorporated herein by reference. For example embodiments of the present invention may be used in a transmitter or receiver operating in accordance with the DVB-H standard, in hand-held mobile terminals. The mobile terminals may be integrated with mobile telephones (whether second, third or higher generation) or Personal Digital Assistants or Tablet PCs for example. Such mobile terminals may be capable of receiving DVB-H or DVB-T compatible signals inside buildings or on the move in for example cars or trains, even at high speeds. The mobile terminals may be, for example, powered by batteries, mains electricity or low voltage DC supply or powered from a car battery. Services that may be provided by DVB-H may include voice, messaging, internet browsing, radio, still and/or moving video images, television services, interactive services, video or near-video on demand and option. The services might operate in combination with one another. It will be appreciated that the present invention is not limited to application with DVB and may be extended to other standards for transmission or reception, both fixed and mobile.

CLAIMS

1. A data processing apparatus operable to map input symbols to be communicated onto a predetermined number of sub-carrier signals of an Orthogonal Frequency Division Multiplexed (OFDM) symbol, the predetermined number of sub-carrier signals corresponding to a modulation mode and the input symbols including odd data symbols and even data symbols, the data processing apparatus comprising

an interleaver operable to perform a first interleaving process which interleaves odd input data symbols on to the sub-carrier signals and an even interleaving process which interleaves even input data symbols on to the sub-carrier signals, the first odd interleaving process and even interleaving process which reads-in and reads out the data symbols for mapping onto the OFDM sub-carrier signals to an interleaver memory the read-out being in a different order than the read-in such that while an odd symbol is being read from a location in the memory, an even symbol can be written to the location just read from and when an even symbol is read from the location in the memory, a following odd symbol can be written to the location just read from, the odd interleaving process reading-in and reading-out odd data symbols from the interleaver memory in accordance with an odd interleaving scheme and the even interleaving process reading-in and reading-out even data symbols from the interleaver memory in accordance with an even interleaving scheme, wherein

when the modulation mode is a mode which includes half or less than half sub-carrier signals than a total number of sub-carriers that can be accommodated by the interleaver memory, the data apparatus is operable to assign a portion of the interleaving memory to the first odd interleaving process and assign a second portion of the interleaving memory to a second odd interleaving process operating in accordance with the first, the second odd interleaving process interleaving the even input symbols.

2. A data processing apparatus operable to map input symbols to be communicated onto a predetermined number of sub-carrier signals of an Orthogonal Frequency Division Multiplexed (OFDM) symbol, the predetermined number of sub-carrier signals corresponding to a modulation mode and the input symbols including

first data symbols for mapping onto a first OFDM symbol and second data symbols for mapping onto a second OFDM symbol, the data processing apparatus comprising

an interleaver operable to perform an odd interleaving process which interleaves first input data symbols on to the sub-carrier signals and an even interleaving process which interleaves second input data symbols on to the sub-carrier signals, the odd interleaving process writing the first input data symbols into an interleaver memory in accordance with a sequential order of the first input data symbols and reading out the first data symbols from the interleaver memory on to the sub-carrier signals in a accordance with an order defined by a permutation code, the even interleaving process writing the second input data symbols into an interleaver memory in a accordance with an order defined by the permutation code and reading out the second data symbols from the interleaver memory on to the sub-carrier signals in accordance with a sequential order such that while a first input data symbol is being read from a location in the interleaver memory, a second symbol can be written to the location just read from and when a second symbol is read from the location in the interleaver memory, a following first symbol can be written to the location just read from, wherein

when the modulation mode is a mode which includes half or less than half a number of sub-carrier signals than a total number of sub-carriers that can be accommodated by the interleaver memory, the data apparatus is operable to interleave both first and second input symbols in accordance with the odd interleaving process.

3. A method of mapping input symbols to be communicated onto a predetermined number of sub-carrier signals of an Orthogonal Frequency Division Multiplexed (OFDM) symbol, the method comprising

mapping first data symbols onto a first OFDM symbol and mapping second data symbols onto a second OFDM symbol, wherein

the mapping is performed in accordance with an odd interleaving process which interleaves first input data symbols on to the sub-carrier signals and an even interleaving process which interleaves second input data symbols on to the sub-carrier signals, the odd interleaving process writing the first input data symbols into an interleaver memory in accordance with a sequential order of the first input data

symbols and reading out the first data symbols from the interleaver memory on to the sub-carrier signals in a accordance with an order defined by a permutation code, the even interleaving process writing the second input data symbols into an interleaver memory in a accordance with an order defined by the permutation code and reading out the second data symbols from the interleaver memory on to the sub-carrier signals in accordance with a sequential order such that while a first input data symbol is being read from a location in the interleaver memory, a second symbol can be written to the location just read from and when a second symbol is read from the location in the interleaver memory, a following first symbol can be written to the location just read from, and when the modulation mode is a mode which includes half or less than half a number of sub-carrier signals than a total number of sub-carriers that can be accommodated by the interleaver memory, both first and second input symbols in are interleaved in accordance with the odd interleaving process.

4. A data processing apparatus substantially as herein before described with reference to the accompanying drawings.

5. A method substantially as herein before described with reference to the accompanying drawings.

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Application No: GB0721269.9 **Examiner:** Owen Wheeler

Claims searched: 1-5 **Date of search:** 15 February 2008

Patents Act 1977: Search Report under Section 17

Documents considered to be relevant:

Category	Relevant to claims	Identity of document and passage or figure of particular relevance
A	-	EP 1463256 A1 [SONY] See abstract.
A	-	WO 2006/136883 A1 [ADAPTIVE SPECTRUM AND SIGNAL] See abstract.
A	-	US 2007/250742 A1 [KOWALSKI] See abstract.

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Field of Search:

Search of GB, EP, WO & US patent documents classified in the following areas of the UKC[X] :

Worldwide search of patent documents classified in the following areas of the IPC

H03M; H04L

The following online and other databases have been used in the preparation of this search report

EPODOC, WPI, Inspec

International Classification:

Subclass	Subgroup	Valid From
H03M	0013/27	01/01/2006
H04L	0027/26	01/01/2006