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GB 2587374 B

21 10 19

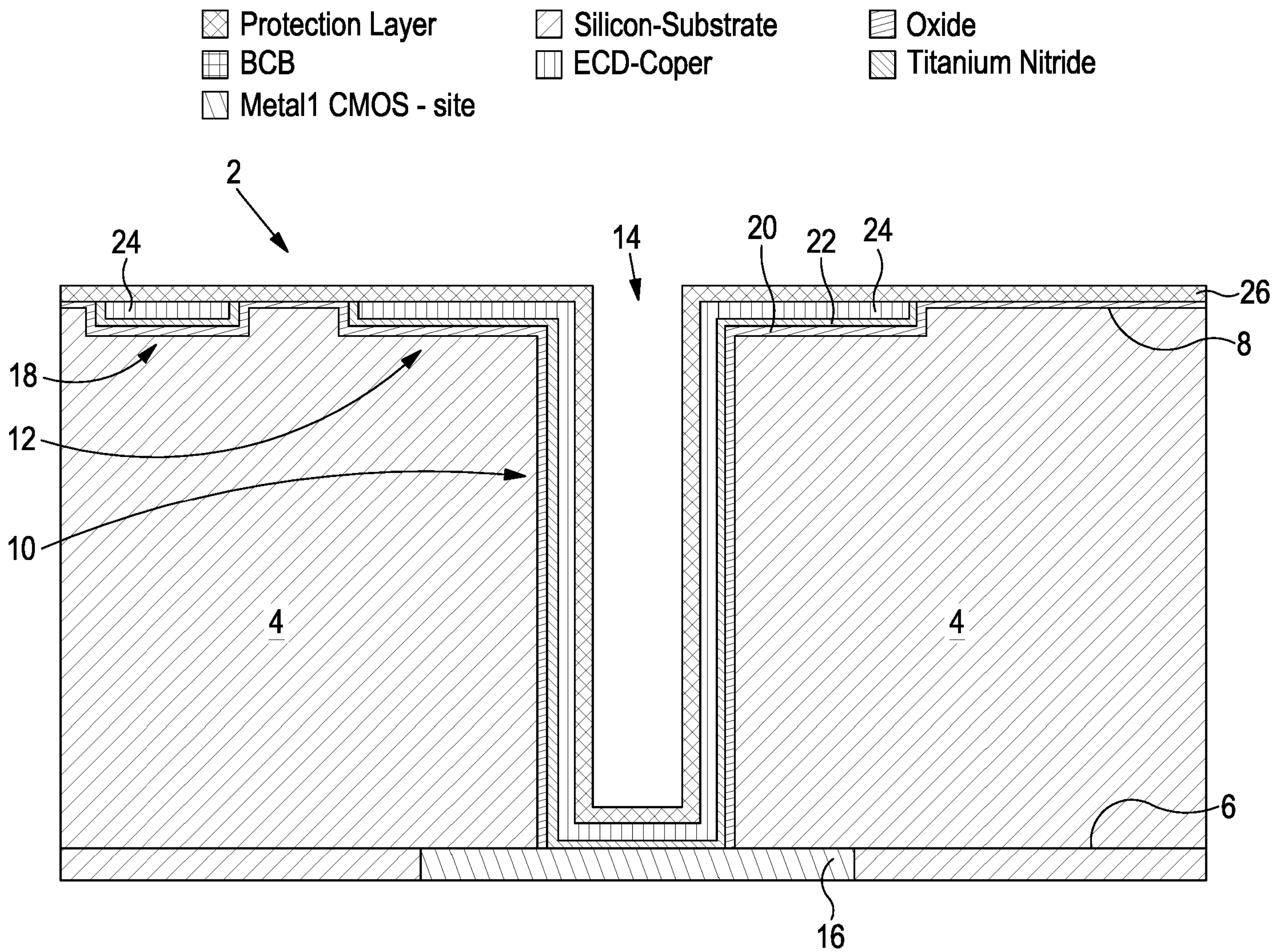

Figure 1

21 10 19

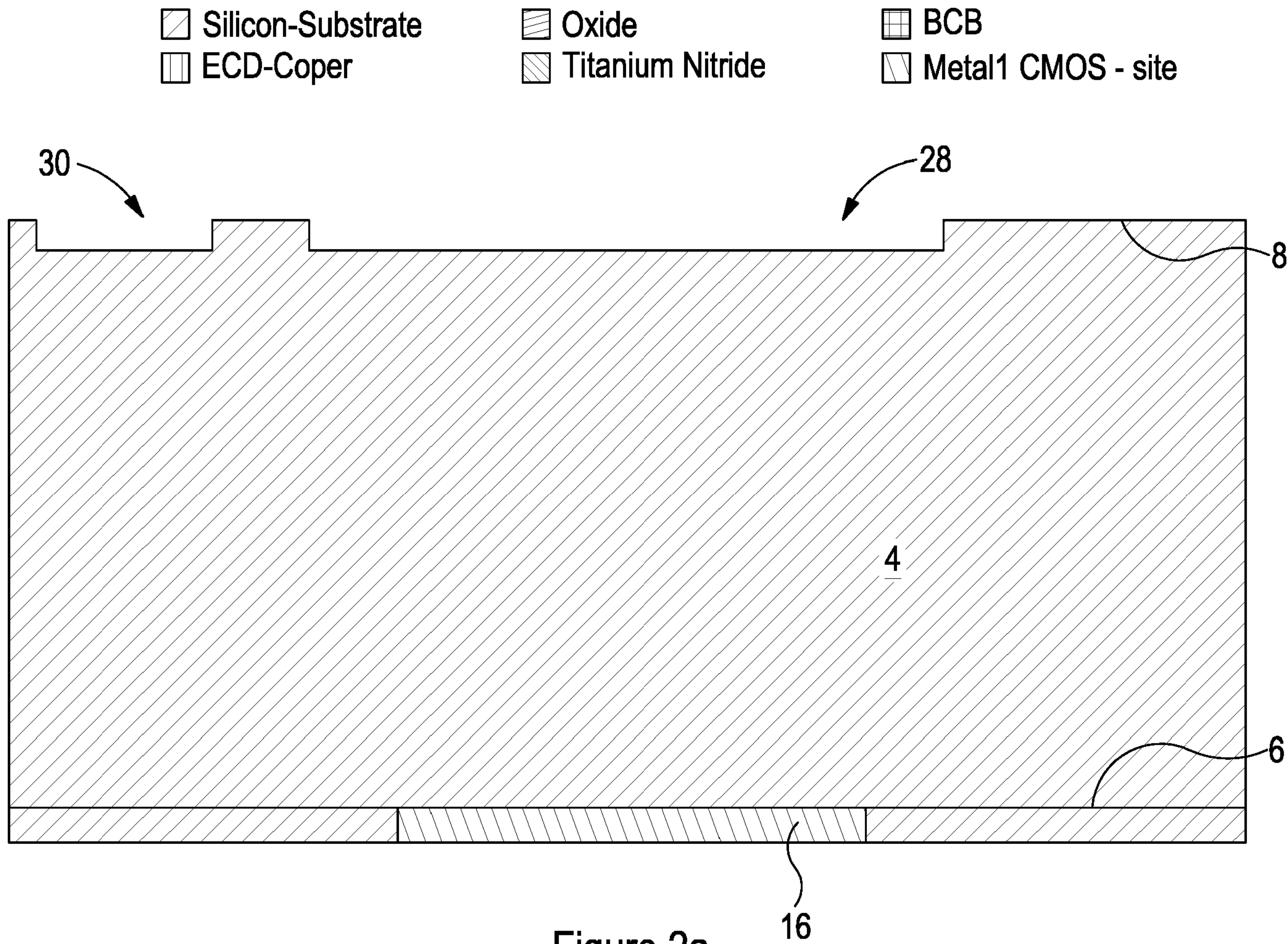

Figure 2a

21 10 19

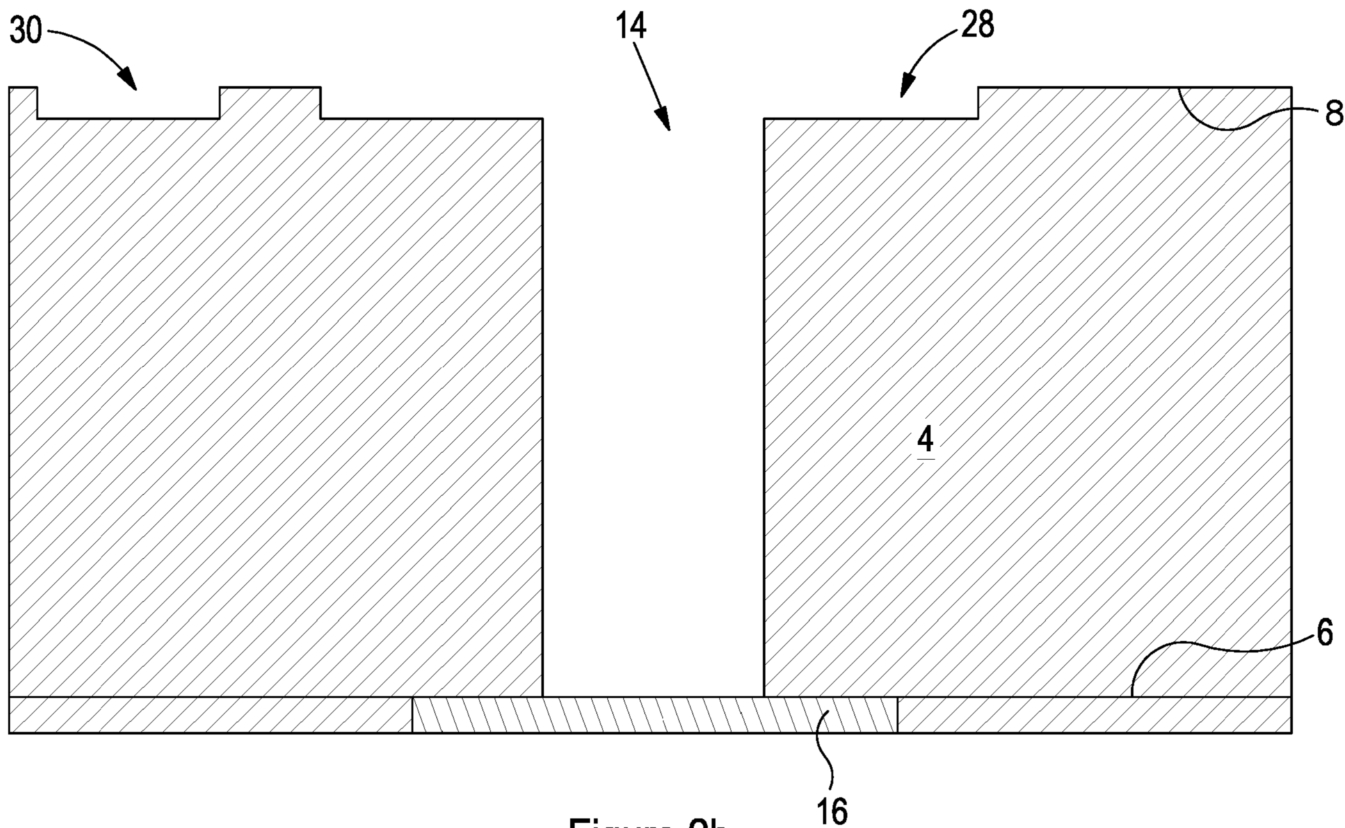

Figure 2b

21 10 19

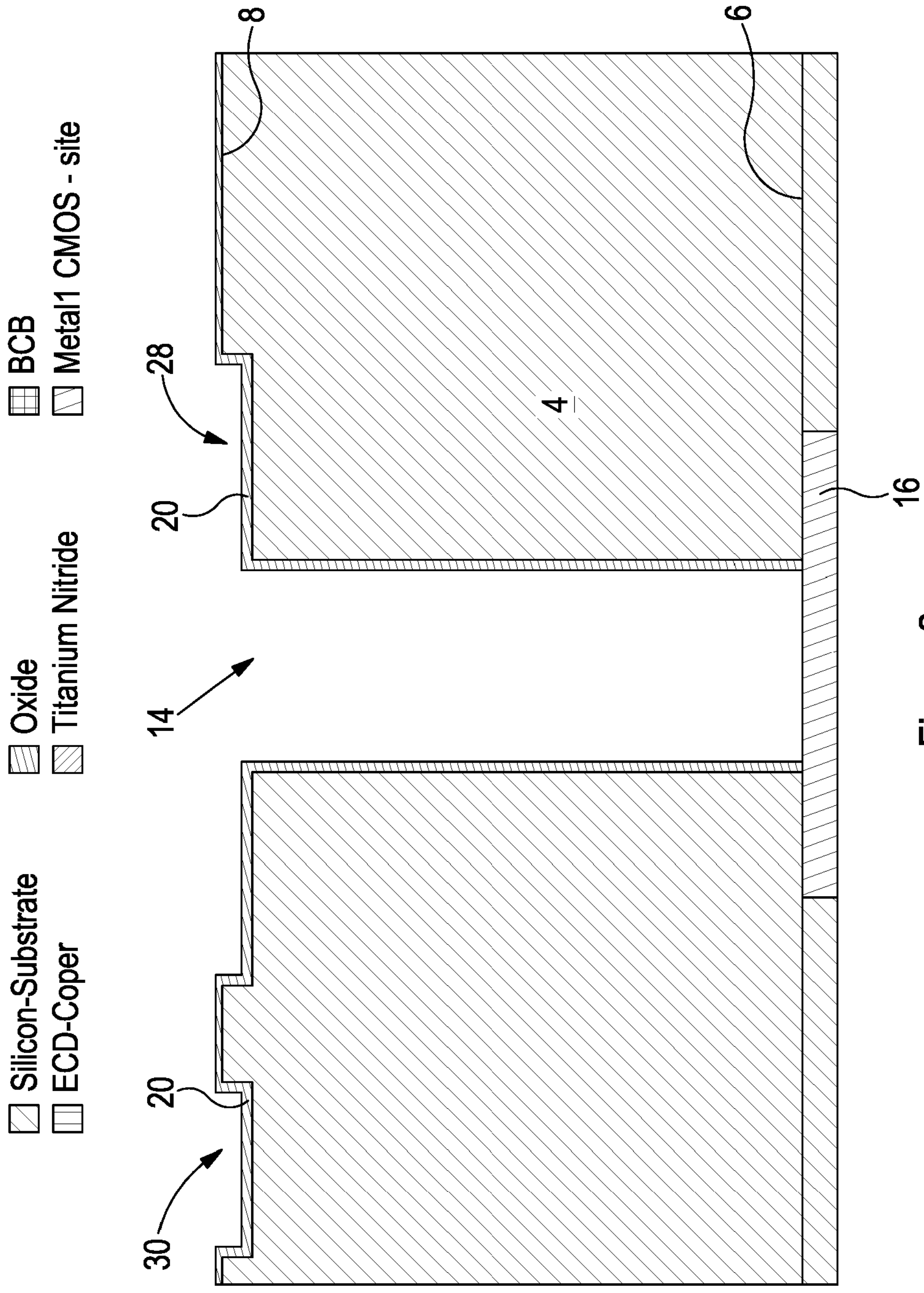

Figure 2c

21 10 19

Silicon-Substrate
ECD-Coper
Oxide
Titanium Nitride
BCB
Metal1 CMOS - site

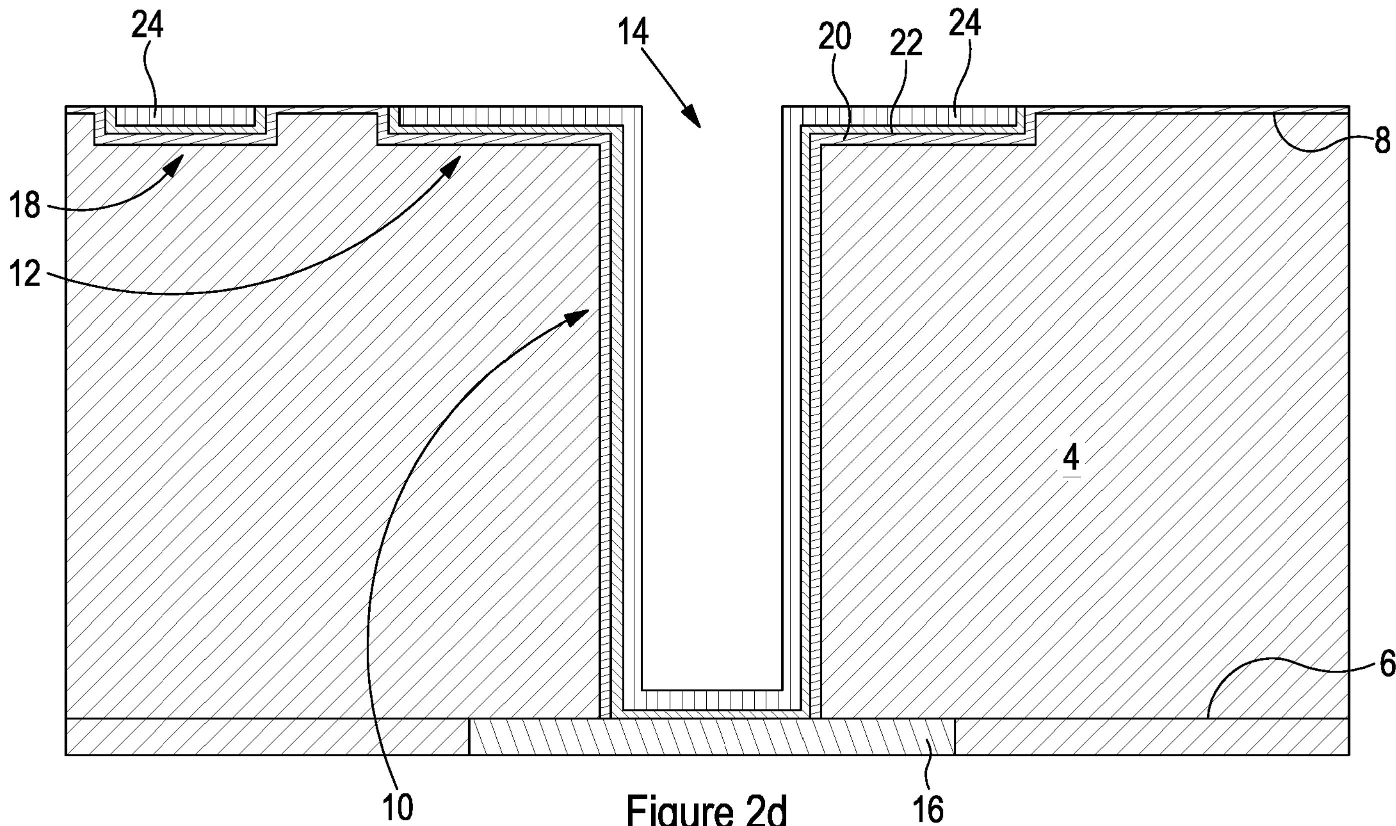

Figure 2d

21 10 19

Protection Layer
BCB
Metal1 CMOS - site
Silicon-Substrate
ECD-Coper
Oxide
Titanium Nitride

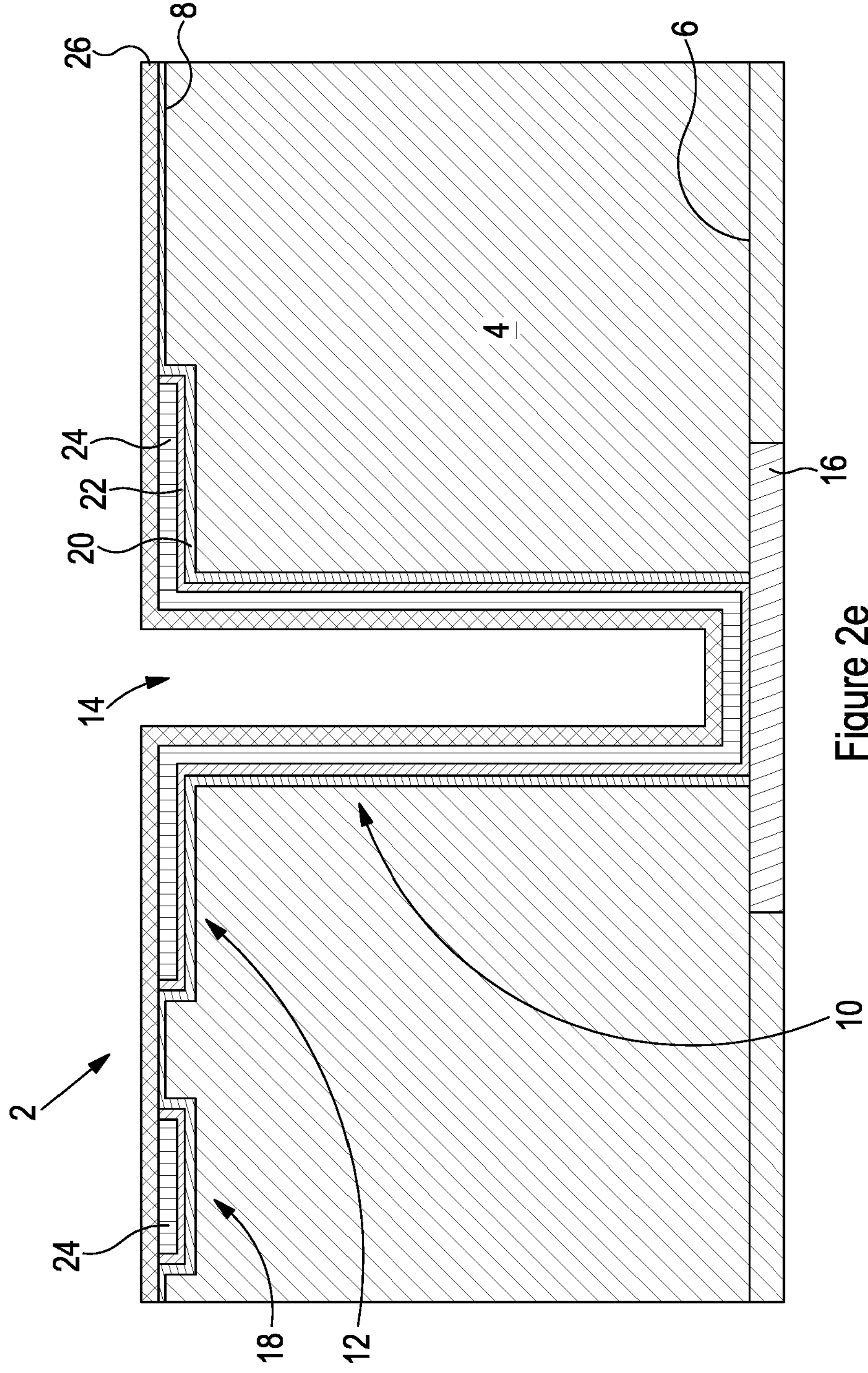

Figure 2e

Through Silicon Via and Redistribution Layer

Technical field

The invention relates to through silicon vias (TSVs) and redistribution layers (RDLs) in semiconductor devices such as complementary metal oxide semiconductor (CMOS) and/or Micro Electrical Mechanical Systems (MEMS) devices.

Background

Through Silicon Vias (TSVs) can be used to provide connections to a CMOS device from the back of the wafer, which enables 3D connection structures. To make a TSV, a hole through the silicon substrate is formed and conformal deposited with copper. A copper redistribution layer (RDL) contains metal line and bond pad structures which enables connectivity (e.g. solder bumping) and functionality.

A technical problem associated with this process is the exposed copper of the TSV and RDL on the wafer surface. During etch back (wet-etch) of the wafer surface an over-etching is required to avoid copper residues between the metal lines, which could otherwise create shorts. The over-etching significantly influences the shape of the metal lines (shrinking), which can negatively affect device performance.

US2011/05840 describes an improved TSV and RDL connection structure formed using a dual damascene type process flow. Using this process, the RDL copper is embedded in an oxide layer on the back of the wafer. Chemical mechanical polishing (CMP) is then used instead to remove excess copper and provide a flat wafer surface.

Summary

Aspects of the present invention provide a semiconductor device and a method of forming a semiconductor device as set out in the accompanying claims.

Preferred embodiments of the invention will now be described, by way of example only, with reference to the accompanying drawings.

Brief description of drawings

Figure 1 shows a schematic diagram of a cross section of a CMOS device having a RDL and a TSV embedded in a silicon substrate;

Figure 2a shows a step of a method of forming a semiconductor device having improved functionality and connectivity, in which RIE (reactive-ion etch) trenches have been formed in the substrate for the RDL and subsequent TSV;

5 Figure 2b shows a subsequent step of the method of forming a CMOS device, in which a hole for the TSV has been etched through the substrate;

Figure 2c shows a subsequent step of the method of forming a CMOS device, in which an oxide layer has been deposited and structured;

10

Figure 2d shows a subsequent step of the method of forming a CMOS device, in which a barrier layer and a copper layer have been deposited; and

Figure 2e shows a final step of a method of forming a CMOS device, in which a
15 protection layer has been provided over the RDL and TSV copper.

Detailed description

Embodiments of the invention provide a semiconductor device such as a complementary metal oxide semiconductor (CMOS) device and/or a Micro Electrical
20 Mechanical Systems (MEMS) device (e.g. an image sensor, a microprocessor, a microcontroller, a pressure sensor, an IR sensor etc. made in a CMOS/MEMS process) comprising a through silicon via (TSV) and a redistribution layer (RDL) that are embedded in the silicon substrate of the device. The semiconductor device may comprise a plurality of such TSVs that are formed using a damascene type process. In
25 contrast to known technologies, the embodiments described herein bury the RDL in the bulk silicon.

By embedding the RDL (e.g. metal pads and metal lines) and TSV in the substrate (instead of in a dielectric layer on the substrate) they are protected from subsequent
30 process steps and in particular from a subsequent wet etch. A wet etch can be used to remove superfluous copper between metal lines and pads in the RDL. In known RDL formation processes, this wet etch tends to shrink the metal lines, which can negatively affect device performance (e.g. due to increased or non-consistent resistance). By providing the RDL and the connection pad of the TSV in trenches formed directly in the
35 silicon substrate, the metal lines suffer less shrinkage/damage by the wet etch.

Embedding the RDL in the silicon substrate can also provide a more planar/smooth outer surface, which can provide better quality films and prevent blistering on the substrate.

5 Before turning to the figures, we first describe the semiconductor device of the figures in general terms, without referring to reference numerals. The semiconductor device described herein comprises a metal layer, which may be referred to as the first metal layer or Metal 1 (n.b. not labelled 1 in the figures). The semiconductor device may comprise a plurality of metal layers formed in the CMOS/MEMS back end of line 10 (BEOL) process, wherein Metal 1 is the first (lowermost) metal layer (followed by Metal 2, Metal 3 etc.). The metal layer can connect to doped regions on the front surface of the silicon substrate to form transistors, diodes and other semiconductor structures of the semiconductor device. The TSV extends from a back surface of the silicon substrate, through the front surface and to the metal layer, to allow connections from 15 the back of the silicon substrate to the metal layer. The TSV has a connection pad (also referred to as “metal pad” or “redistribution pad”) on the back surface of the silicon substrate. This connection pad of the TSV is also embedded in the silicon substrate and may be considered a part of the RDL.

20 The TSV comprises a hole with a deposited layer of copper on the sidewalls and the bottom of the hole. Preferably, the TSV is not bulk filled with copper, which can save costs and process time due to the large aspect ratio of the TSV. Metal lines and pads of the RDL may be filled in the same step as the layer of copper is provided in the TSV, for example using electrochemical deposition (ECD). The TSV and RDL may comprise 25 a barrier layer (e.g. titanium nitride) coating the walls of said hole and said trenches and separating said copper layer from said silicon substrate.

The semiconductor device may further comprise a protection layer covering said RDL. The protection layer may comprise one or more passivation layers (e.g. oxide and/or 30 silicon nitride). The protection layer can provide environmental protection to the RDL and TSV as well as electrical isolation. The final copper encapsulation can be done with a Chemical Vapour Deposition (CVD) or other coating process to form the protection layer.

Embodiments of a method of forming a CMOS device are also described herein. Both the RDL and TSV are provided directly in the silicon substrate using a damascene type process. The method comprises providing the silicon substrate having a front surface and a back surface and forming the metal layer on the front surface. The method further comprises, forming the TSV extending through the silicon substrate from the back surface to the front surface, wherein the TSV is connected at one end to the metal layer, and forming the RDL, wherein the RDL is embedded in the silicon substrate.

The step of forming the TSV may comprise etching a trench in said silicon substrate for forming the connection pad of the TSV. Preferably, a reactive ion etch (RIE) is used. RIE is a type of dry etching which has different characteristics than wet etching. A RIE etch can have the advantage of providing a very anisotropic etch of the substrate. The RDL trenches for metal lines and pads can be etched using RIE in a first process step. A hole can then be etched (e.g. using RIE) through the silicon substrate to said metal layer (e.g. Metal 1). The hole typically extends through the centre of the trench formed for the connection pad of the TSV.

The method may further comprise depositing a copper layer in the trench for the connection pad and in the hole to form the TSV, wherein the copper layer does not completely fill the hole. Before the step of depositing the copper layer, a barrier layer may be deposited, which coats the walls of the hole. A copper seed layer can be provided on the barrier layer for the subsequent deposition of the copper layer.

The method may further comprise performing a wet etch to remove excess copper. The wet etch can be used to remove copper on the barrier/seed layer between metal lines and pads of the RDL to prevent shorts.

A protection layer can be provided that covers the RDL and protects the back surface of the substrate including the RDL and TSV. The protection layer can be provided by depositing one or more passivation layers. For example, a silicon nitride layer may be deposited on the back surface.

Figure 1 shows a schematic cross section of a CMOS/MEMS device 2 according to an embodiment. The device 2 comprises a silicon substrate 4 having a front surface 6 and a back surface 8. A TSV 10 extends through the substrate 4 from the back surface 8 to

the front surface 6. The TSV 10 comprises a connection pad 12 at the back surface 8 and a hole 14 extending through the connection pad 12 and to the first metal layer 16 of the CMOS device 2. The device 2 further comprises a metal line 18 (comprising multiple layers, as described below) of a RDL. The metal line 18 is embedded in the
5 substrate 4. Both the TSV 10 (including the connection pad 12) and the metal line 18 comprise an oxide layer 20 adjacent to the silicon substrate 4 (e.g. formed by oxidising the silicon substrate 4), a titanium nitride barrier layer 22 covering said oxide layer 20, and a copper layer 24 being an ECD copper layer. The copper layer 24 fills the metal line 18 of the RDL and the connection pad 12 of the TSV 10, but does not completely
10 fill the hole 14 of the TSV 10. Due to the large aspect ratio of the hole 14, the copper layer 24 only coats the walls of the hole 14. A substantially flat protection layer 26 (e.g. a silicon nitride layer) covers the back surface 8, including the metal line 18 and the TSV 10.

15 Figures 2a to 2d illustrate some steps in a method of forming a CMOS/MEMS device 2, such as the device illustrated in Figure 1. Similar or corresponding features in the figures have been given the same reference numerals for ease of understanding and are not intended to be limiting.

20 Figure 2a shows a cross-section of substrate 4 having a front surface 6 with a first metal layer 16 thereon and a back surface 8. The back surface 8 of the silicon substrate has been etched using RIE to form a trench 28 suitable for the connection pad of the TSV and a trench 30 for a metal line of the RDL. Both trenches 28 and 30 are formed in the same process step using the same mask. The connection pad 12 of
25 the TSV 10 can also be considered a part of the RDL.

Figure 2b shows the hole 14 of the TSV that has been RIE etched through the substrate 4 from the back surface 8, through the front surface 6 and to the first metal layer 16. The hole 14 is etched through the centre of the trench 28 for the connection
30 pad.

Figure 2c shows the oxide layer 20 having been deposited on the silicon substrate 4. The oxide layer 20 is a passivation layer that provides some protection and electrical isolation to the underlying silicon of the substrate 4. The deposited oxide has been

removed from the metal layer 16 at the end of the hole 14 in order to facilitate the electrical connection between the finished TSV and the metal layer 16.

Figure 2d shows the titanium nitride barrier layer 22 deposited on the oxide layer 20 and ECD copper layer 24 deposited on the barrier layer to form TSV 10 and metal line 18 of the RDL. An etch back (wet etch) of the barrier layer 22 and seed layer (not shown) has been done to remove the barrier layer and seed layer in between the connection pad 12 and metal line 18, as well as in between other metal lines and pads of the RDL (not shown). In a normal damascene process it is known to use CMP after metal deposition to smooth the surface. Using a wet etch instead of CMP has the advantage of being readily available as an already/standard existing process step (e.g. in CMOS and MEMS processes), and therefore does not require the wafer to be moved to a different manufacturing process. The RIE etched trenches in the substrate 4 provide sufficient protection of the ECD copper for performing the wet etch. After the wet etch, the back surface 8 of the silicon substrate, including exposed ECD copper layer 24 and exposed oxide layer 20, are relatively flat and have a surface roughness in the range of 1 μm to 1.5 μm, which can make any potential dry film post processing more reliable.

Figure 2e shows the finished CMOS/MEMS device 2 with RDL metal line 18 and TSV 10 after providing a protection layer 28 by depositing a passivation layer stack 26 on the back surface 8 of the substrate 4.

While specific embodiments of the invention have been described above, it will be appreciated that the invention may be practiced otherwise than as described in the specific embodiments. The descriptions above are intended to be illustrative, not limiting. It will be apparent to one skilled in the art that modifications may be made to the embodiments as described without departing from the scope of the claims set out below.

Each feature disclosed or illustrated in the present specification may be incorporated in the invention, whether alone or in any appropriate combination with any other feature disclosed or illustrated herein.

CLAIMS:

1. A semiconductor device comprising:

a silicon substrate having a front surface and a back surface;

a plurality of metal layers comprising a first metal layer located on said front surface and connected to doped regions on the front surface of the silicon substrate to form semiconductor structures of the semiconductor device;

a through silicon via (TSV) extending through said silicon substrate from said back surface to said front surface, wherein said TSV is directly connected at one end to said first metal layer; and

a redistribution layer (RDL) connected to another end of said TSV, wherein said RDL is embedded in said back surface of said silicon substrate.

2. A semiconductor device according to claim 1, wherein said TSV comprises a hole and a layer of copper, and wherein said layer of copper does not completely fill said hole.

3. A semiconductor device according to claim 1 or 2, wherein said TSV comprises a layer stack comprising at least an isolation layer and a barrier layer coating the walls of said hole and separating said copper layer from said silicon substrate.

4. A semiconductor device according to claim 1, 2 or 3, further comprising a protection layer covering copper in said RDL and TSV.

5. A semiconductor device according to claim 4, wherein said protection layer comprises at least one passivation layer.

6. A semiconductor device according to any preceding claim, wherein said semiconductor device is a complementary metal oxide semiconductor (CMOS) device and/or a Micro Electrical Mechanical Systems (MEMS) device.

7. A method of forming a semiconductor device, the method comprising:

providing a silicon substrate having a front surface and a back surface;

11 07 22

forming a plurality of metal layers comprising a first metal layer on said front surface and connected to doped regions on the front surface of the silicon substrate to form semiconductor structures of the semiconductor device;

forming a through silicon via (TSV) extending through said silicon substrate from the back surface to the front surface, wherein said TSV is directly connected at one end to said first metal layer; and

forming a redistribution layer (RDL) connected to another end of said TSV, wherein said RDL is embedded in said back surface of said silicon substrate.

8. A method according to claim 7, wherein said step of forming the TSV comprises:

etching a trench in said silicon substrate for forming a connection pad of said TSV;

etching a hole through said silicon substrate to said first metal layer;

depositing a copper layer in said trench and in said hole to form said TSV, wherein said copper layer does not completely fill said hole.

9. A method according to claim 8, wherein said step of forming said TSV further comprises, before said step of depositing said copper layer, providing a layer stack comprising at least an isolation layer and a barrier layer coating the walls of said hole.

10. A method according to claim 8 or 9, wherein said step of depositing copper comprises performing electrochemical deposition (ECD).

11. A method according to any one of claims 7 to 10, wherein said step of forming said RDL comprises:

etching one more trenches in said silicon substrate for forming metal lines and/or metal pads of said RDL; and

filling said trenches with copper.

12. A method according to any one of claims 7 to 11, further comprising performing a wet etch to remove excess copper.

13. A method according to any one of claims 7 to 12, further comprising providing a protection layer covering copper in said RDL and TSV.

11 07 22

14. A method according to claim 13, wherein said step of providing a protection layer comprises depositing at least one passivation layer.

5 15. A method according to any one of claims 7 to 14, wherein said first metal layer is in a backend stack of said semiconductor device.

16. A method according to any one of claims 7 to 15, forming a semiconductor device comprises forming a complementary metal oxide semiconductor (CMOS) device

10 and/or a Micro Electrical Mechanical Systems (MEMS) device.

11 07 22