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(54) Timing correction circuit for data communication apparatus

(57) A timing correction circuit maintains proper sample timing in a data modem. A main channel equaliser provides an in-phase error component EX_n and a quadrature phase error component EY_n. These components are fed to a correlator, together with signals $\dot{X}_{EQn}$ and $\dot{Y}_{EQn}$, which represent equalised signals derived from a second channel equaliser operating on the derivative of the main channel signal. The correlator output is used to derive a correction signal for the clock generator 73. The arrangement is such that the second channel equaliser requires fewer coefficients than the main channel equaliser, while clock correction need be performed only once every other band, whereby the number of calculations required to implement the timing correction is reduced.

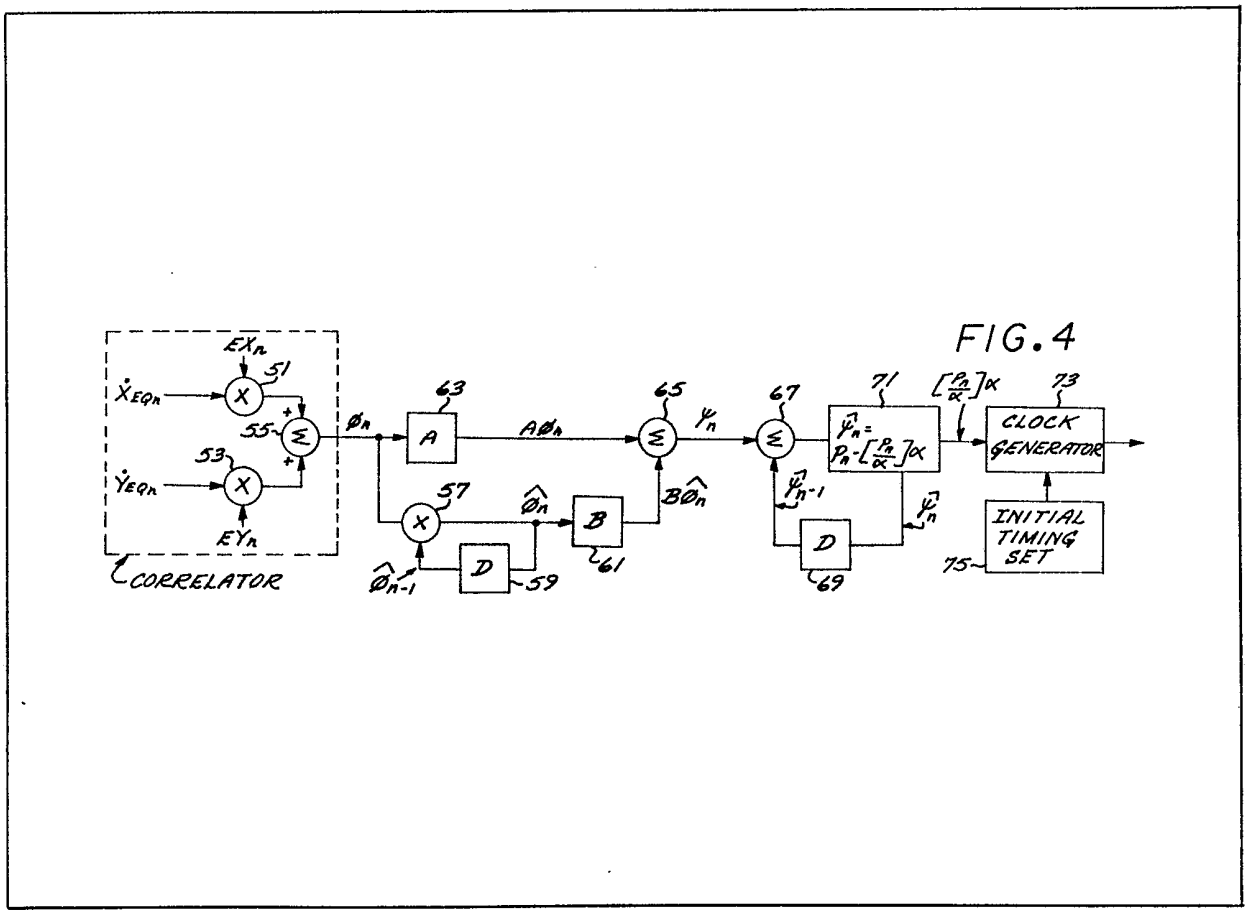

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FIG. 1

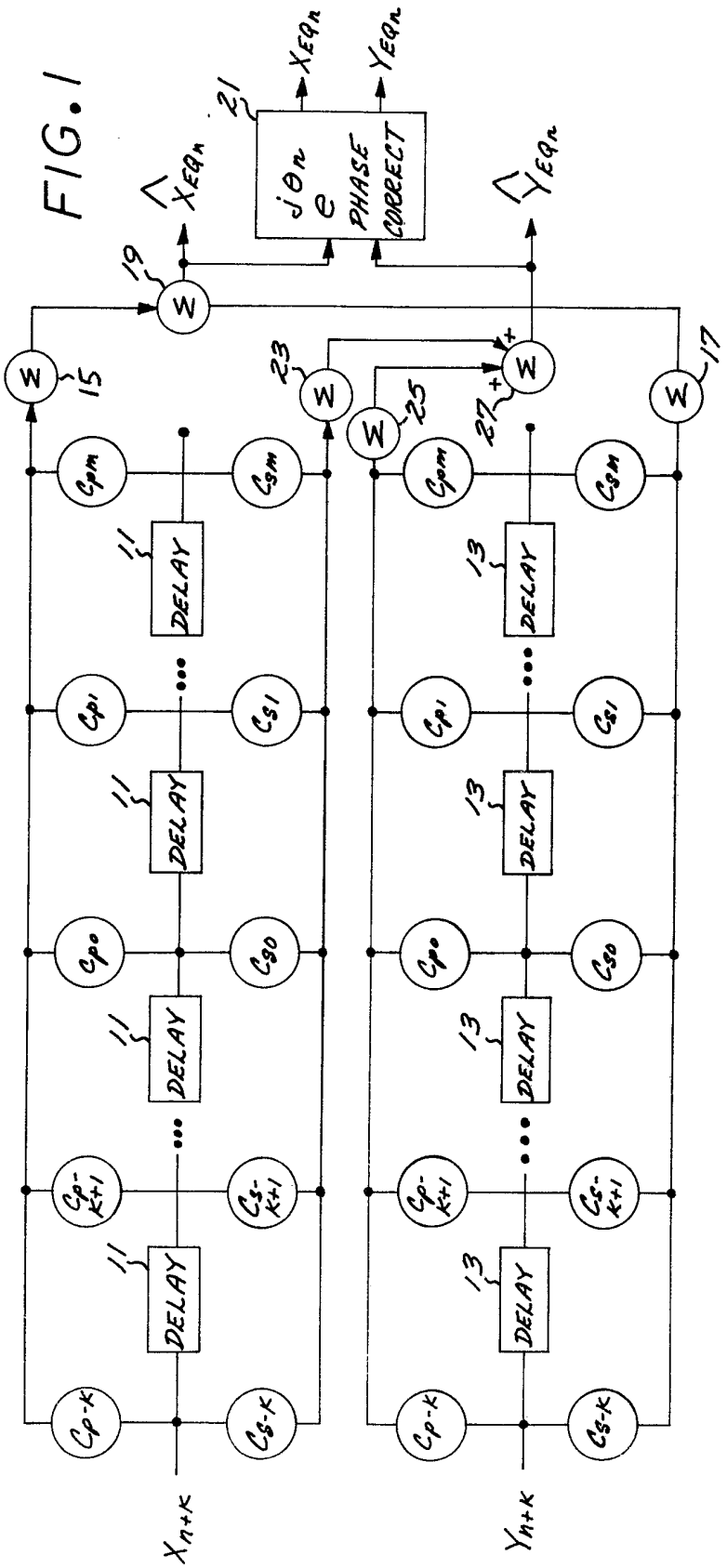

DELAY
DECISION
PHASE CORRECT
X_{EQn}
Y_{EQn}
X_{n+K}
Y_{n+K}

FIG. 2

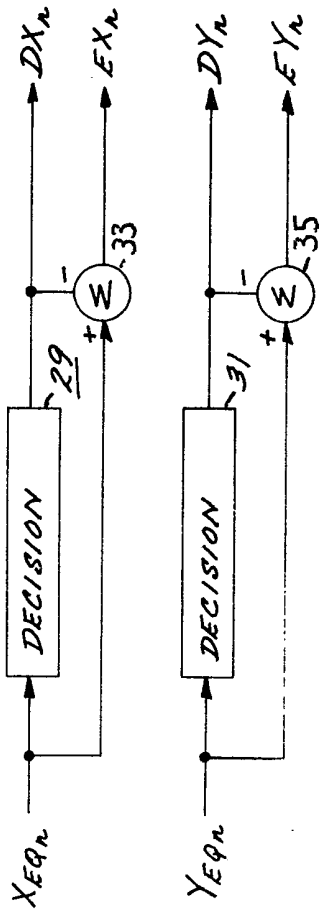

DX_n
EX_n
DY_n
EY_n
DECISION
X_{EQn}
Y_{EQn}

FIG. 3

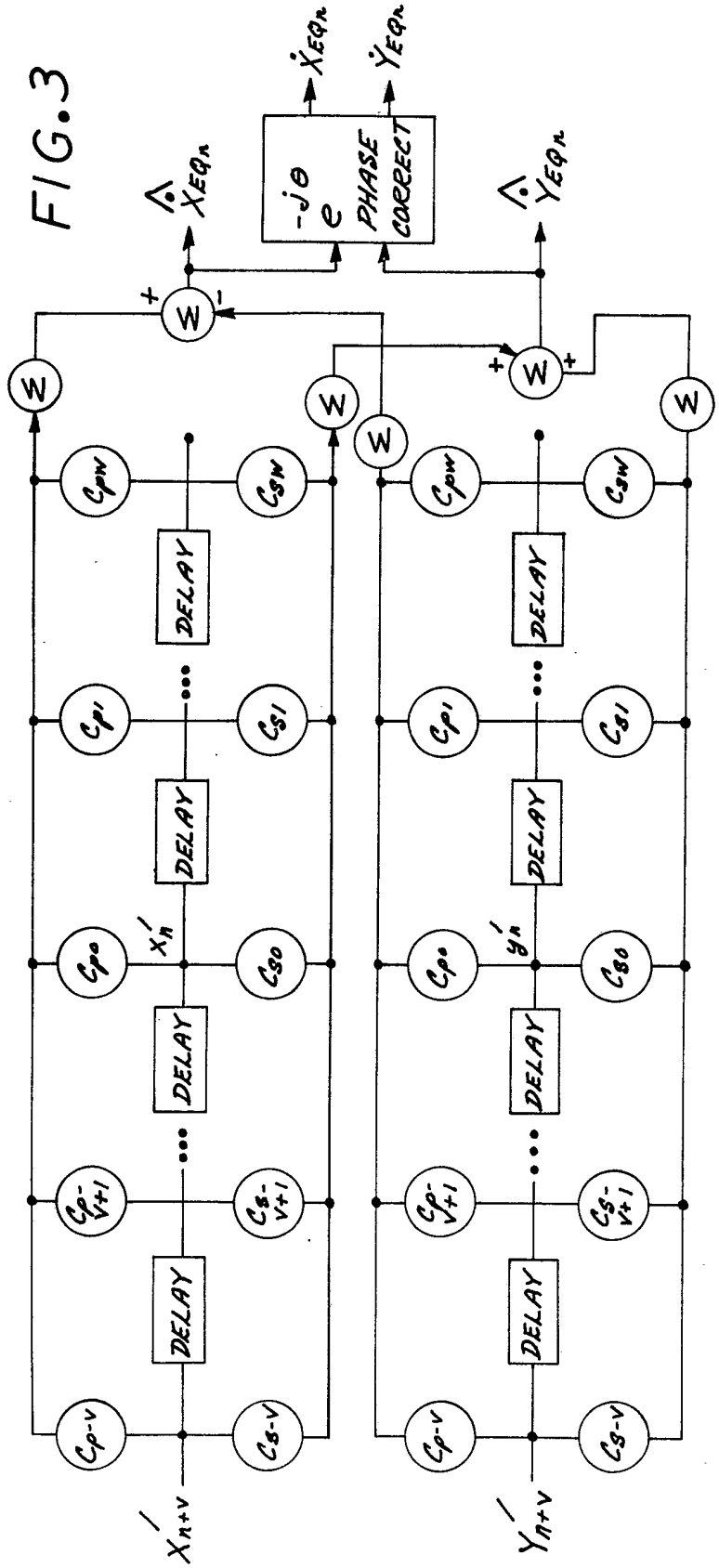
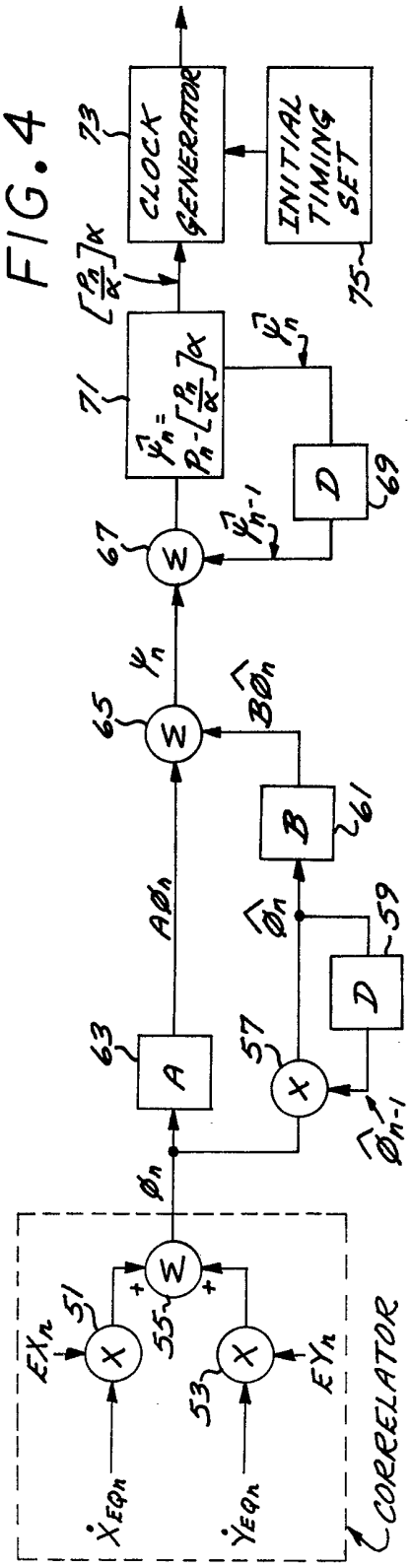

DELAY
PHASE CORRECT
-jθ
e

FIG. 4


CLOCK GENERATOR
INITIAL TIMING SET
CORRELATOR
A
B
D

SPECIFICATION

Timing correction circuit for data communication apparatus

This invention relates to data communication apparatus and, more particularly, to an improved circuit for adjusting the timing of a sampling clock typically used to recover data in the receiver of a data modem. Precise adjustment of the sampling clock is essential to optimum recovery of data.

It has been suggested to derive a clock correction signal by correlating so-called main channel error signals and derivative channel signals. The derivative channel signal is derived by differentiating the main channel (received) signal. According to this suggestion, the derivative channel signals are determined every baud interval and are equalized by a second identical to the equalizer employed to equalize the main channel signal. Furthermore, the technique assumes that the sampling clock has already been set to near the correct sampling point. While theoretically interesting, this prior technique has not appeared practically implementatable because of the complexity involved, such as in providing a second equalizer identical to that utilized to equalize the received signal. The prior technique proves particularly undesirable in modems employing microprocessor techniques because of the excessive number of operations required, which waste valuable microprocessor computation power.

The present invention is defined in the appended claims, to which reference should now be made.

The invention will be described in more detail, by way of example, with reference to the drawings, in which:

Figures 1 and 2 illustrate a main channel equaliser and are based on a known main channel equaliser; and

Figures 3 and 4 illustrate the second channel equaliser in a preferred embodiment of the invention.

In the preferred embodiment of the invention, a main channel equalizer illustrated in Figure 1 and Figure 2 is employed to generate main channel error signals EX_n and EY_n. The main channel equalizer structure of Figure 1 and Figure 2 is well known in the art, and is illustrated in brief schematic form.

Input samples X_{n+K} and Y_{n+K} of the main channel received signal, having a phase quadrature relationship, are employed. Initially it is necessary to set the sampling point near the appropriate point in order to enable proper operation of the preferred embodiment. Such initial setting of the sampling clock may be achieved by known envelope recovery methods or by the preferred technique disclosed in our U.K. Patent application No. 79.13018, entitled Adaptive Equalizer, (publication No. 2022376). Once the timing of the sampling clock has been initially set, the preferred embodiment will proceed to precisely locate the sampling time in order to optimise data recovery.

The equalizer of Figure 1 includes an in-phase channel for the X_{n+K} samples, and a quadrature phase channel for the Y_{n+K} samples. The samples X_{n+K} are stored in delay elements 11 and the samples Y_{n+K} are stored in delay elements 13. The in-phase channel samples X_{n+K} are multiplied by respective constants $CP_{-K} \ldots CP_m$ and summed in a summer 15. The samples Y_{n+K} are also multiplied by respective constants $CP_{-K} \ldots CP_m$ and summed in a summer 17. The outputs of the two summers 15 and 17 are summed by a summer 19 to provide the signal $\hat{X}_{EQ_n}$. The output of the summer 19 $\hat{X}_{EQ_n}$ is fed to a phase correction circuit 21. Similarly, the samples X_{n+K} are multiplied by respective constants $CS_{-K} \ldots CS_m$ and the resulting products are summed in a summer 23. The samples Y_{n+K} are multiplied by respective constants $CP_{-K} \ldots CP_m$ and the resulting products are summed in a summer 25. The respective outputs of the two summers 23, 25 are summed by a summer 27 to produce the signal $\hat{Y}_{EQ_n}$. This signal $\hat{Y}_{EQ_n}$ is then fed to the phase correcting circuit 21. The output X_{EQ_n}, Y_{EQ_n} of the phase correcting circuits are the equalized main channel signal components:

$$X_{EQ_n} = X_{EQ_n} \text{ COS } \theta_n + Y_{EQ_n} \text{ SIN } \theta_n$$

$$Y_{EQ_n} = Y_{EQ_n} \text{ COS } \theta_n - X_{EQ_n} \text{ SIN } \theta_n$$

where θ_n represents the necessary phase angle correction.

The phase corrected equalized main channel signals X_{EQ_n} and Y_{EQ_n} are then fed to respective decision circuits 29, 31 (Fig. 2). Each decision element 29, 31 decides the correct value of the output data signal DX_n, DY_n from the respective raw outputs X_{EQ_n}, Y_{EQ_n} of the equalizer. The data signal values DX_n, DY_n are then fed to the respective summers 33, 35 from which the main channel in-phase error component EX_n and the main channel quadrature phase error component EY_n are derived.

As known in the prior art, the equalizer constants CP_{-K} and CS_{-K}, etc., are adjusted according to some algorithm in order to produce equalized output signals to remedy the effects of intersymbol interference. Such algorithms are well known in the art and will not be discussed further herein.

Figure 3 discloses the second channel equalizer of the preferred embodiment which in the preferred embodiment is a derivative channel equalizer. Generation of the input signal X'_{n+v}, Y'_{n+v} to the derivative channel equalizer is very well known. For example, if X_n and Y_n are the sampled in-phase and quadrature phase baseband signals, then X'_n and Y'_n are the corresponding sampled derivatives of these baseband signals.

These samples are then fed to the respective delay elements of the equalizer, shown in Figure 3, which differs in structure from the equalizer of Figure 1 in the sole but significant respect that the number of taps and tap constants $CP_{-V} \ldots CP_W$ and $CS_{-V} \ldots CS_W$ in Figure 3 is less than the number of taps required by the equalizer of Figure 1 to equalize the main channel received signal. The values of the tap constants CP, CS for corresponding taps of Figure 1 and Figure 3 are the same. By using fewer taps, i.e., $V \leq K$, $W < M$ or $V < K$, $W \leq M$, the derivative signals $\dot{X}_{EQ_n}$ and $\dot{Y}_{EQ_n}$, are not as precisely calculated and are typically in error to an extent not tolerable in the main channel received signal. However, we have appreciated that high accuracy is not required in these signals, whereas high accuracy is required in the output data DX_n and DY_n. As a particular example, in a modem constructed according to the preferred embodiment, main tap to derivative tap numbers of 23 to 17, 30 to 19 and 39 to 26 were found to provide accurate operation.

Moreover, it has also been found unnecessary to determine the signal $\hat{X}_{EQ_n}$ and $\hat{Y}_{EQ_n}$ every baud. In the preferred embodiment these values and hence the values of $\hat{X}_{EQ_n}$ and $\hat{Y}_{EQ_n}$ are calculated once every other baud only, using a subset of the tap constants determined for the main channel equalizer of Figure 1.

The correlation and phase lock structure employed to utilize these approximately-calculated derivative signals $\hat{X}_{EQ_n}$ and $\hat{Y}_{EQ_n}$ is illustrated in Figure 4. The derivative signals $\hat{X}_{EQ_n}$ and $\hat{Y}_{EQ_n}$ are multiplied together with the respective error components of the main channel EX_n and EY_n in the respective multipliers 51, 53. The respective products $EX_n \hat{X}_{EQ_n}$ and $EY_n \hat{Y}_{EQ_n}$ are then summed in a summer 55 to produce a signal ϕ_n representative of the clock error.

The output ϕ_n of the correlator is then applied to a second order loop filter. The second order loop filter includes summers 57, 65 a delay element 59, and a constant multipliers 61, 63. The output of summer 57 is denoted $\hat{\phi}_n$ and is delayed by the delay element 59 whose output is fed back as one input to the summer 57. The summer 57 sums ϕ_n with the delayed value $\hat{\phi}_{n-1}$ provided by the delay element to provide $\hat{\phi}_n$. The multiplier 61 multiplies $\hat{\phi}_n$ by a loop constant B. A multiplier 63 also multiplies $\hat{\phi}_n$ by a loop constant A to produce $A\hat{\phi}_n$. The loop constants A and B are chosen according to well-known phase lock loop design considerations. A summer 65 then sums $A\hat{\phi}_n$ and $B\hat{\phi}_n$ and produces an output ψ_n. The elements 57, 59 and 61 cooperate to provide a second order loop characteristic and eliminate frequency offset between transmitter and receiver clocks.

Another summer 67 forms an output $P_n = \phi_n + \hat{\phi}_{n-1}$ by summing one input ϕ_n with the output $\hat{\phi}_{n-1}$ of a delay element 69. The output P_n is fed to a decision block 71 where

$$\left[\frac{P_n}{\alpha}\right]$$

is determined. The constant α is the smallest adjustment increment or decrement that can be made to the sample clock phase with the given hardware comprising a clock generator 73, and

$$\left[\frac{P_n}{\alpha}\right]$$

represents the integer portion of P_n divided by α. Thus,

$$\left[\frac{P_n}{\alpha}\right] \cdot \alpha$$

provides an integer number of increments or decrements for sample timing correction.

The remainder or non-integer portion is determined by the quantity

$$\hat{\psi}_n = P_n - \left[\frac{P_n}{\alpha}\right] \cdot \alpha.$$

This remainder portion ψ_n is stored in the delay element 69 and combined with the next input to the summer 67 in order to provide more accurate sample-time adjustments.

As may be appreciated, since equalized derivative values $\hat{X}_{EQ_n}$ and $\hat{Y}_{EQ_n}$ are provided only once every other baud, the circuitry of Figure 4 need only operate on a once per every other baud timing basis. Thus, the subscripts "n" as used in Figure 4 indicate the value of the corresponding variable during one particular alternate baud period.

The preferred embodiment just described is admirably suited for a microprocessor modem environment where computation power is at a premium. By utilizing fewer taps, the number of multiplications and summations necessary to calculate $\hat{X}_{EQ_n}$ and $\hat{Y}_{EQ_n}$ are significantly reduced. By further limiting the calculations to once every other baud, the number of calculations is effectively cut in half. As a consequence of the preferred embodiment, the number of calculations required to implement Figure 4 is also cut in half. All of these savings are made at no significant sacrifice to the ultimate accuracy of the timing correction provided.

It is seen from the above that the number of operations necessary to perform sampling clock

correcting functions is dramatically reduced by the discovery that it is not necessary to completely equalize the second channel signal, and that the equalized second signal need not be determined every baud interval. Furthermore, the system employs an initial phase estimate based on the signal envelope to initially estimate the positioning of the sampling clock and establishes that such an estimate is sufficient to enable employment of the precise adjustment technique employed. This initial estimate provides very important in that otherwise very poor system performance may result. Employment of a second order phase lock loop to compensate for frequency offset provides a further improvement.

CLAIMS

1. Data communication apparatus having a main channel for receiving a main channel line signal, means for generating and initially approximately timing a sampling signal for sampling the line signal and responsive to a correction signal for adjusting the phase of the sampling signal, means for producing a second channel signal, and apparatus for precisely adjusting the timing of the sampling signal and which comprises:

means for equalizing the main channel signal and employing a plurality of adjustable multiplying coefficients to produce an error signal indicative of the difference between the actual and desired equalizer output;

means for equalizing the second channel signal to produce an equalized second channel signal; and

means for correlating the equalized second channel signal with the error signal to derive a correction signal for correcting the timing phase of the sampling signal.

2. Apparatus according to claim 1, wherein the correlating means comprises:

means for deriving a phase error signal by correlating the second channel signal and the said error signal;

means for removing frequency offset from the phase error signal to produce a frequency adjusted phase error signal; and

means for determining the adjusted phase error signal the number of increments of timing phase correction to be made.

3. Apparatus according to claim 1 or 2, wherein the means for equalizing the second channel employs a number of multiplying coefficients less than the said plurality.

4. Apparatus according to claim 1, 2 or 3, wherein the means for equalizing the second channel signal operates less than once per baud period to generate said equalized second signal.

5. Apparatus according to any preceding claim, wherein the said error signal includes first and second components, and wherein the equalized second channel signal includes first and second components.

6. Apparatus according to claim 5, wherein the correlating means includes means (1) for multiplying the first component of the error signal by the first component of the equalized second channel signal to form a first product, (ii) for multiplying the second component of the error signal by the second component of the equalized second channel signal to form a second product, and (iii) for summing the first and second products to form a phase adjustment signal.

7. Apparatus according to claim 6, further including:

means for second order filtering the phase adjustment signal to produce a corrected signal, and

means for dividing the corrected signal by a clock correction increment to determine a precise adjustment increment for the sampling clock.

8. Apparatus according to claim 7, wherein the second order filtering means comprises:

a first summer;

means for multiplying the phase adjustment signal by a constant to provide a first input to the first summer;

a second summer having an output and receiving the phase adjustment signal as sone input and a delayed version of the output as a second input; and

means for multiplying the output by a second constant to provide a second output to said first summer.

9. Apparatus according to claim 7 or 8, wherein the dividing means further includes means for delaying the remainder of the dividing and adding the delayed remainder to the corrected signal.

10. Apparatus according to any preceding claim, wherein the second channel signal is a derivative channel signal.

11. Data communication apparatus substantially as herein described with reference to the drawings.

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