(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
29 March 2012 (29.03.2012)

WIPO | PCT

(10) International Publication Number
WO 2012/039120 A4

(51) International Patent Classification:
H05K 1/02 (2006.01) *H01L 25/065* (2006.01)
H05K 1/16 (2006.01) *H01L 23/66* (2006.01)

(21) International Application Number:
PCT/JP2011/005246

(22) International Filing Date:
16 September 2011 (16.09.2011)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
2010-214397 24 September 2010 (24.09.2010) JP

(71) Applicant *(for all designated States except US)*: **CANON KABUSHIKI KAISHA** [JP/JP]; 30-2, Shimomaruko 3-chome, Ohta-ku, Tokyo, 1468501 (JP).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **MIYAZAKI, Toyohide** [JP/JP]; C/O CANON KABUSHIKI KAISHA, 30-2, Shimomaruko 3-chome, Ohta-ku, Tokyo, 1468501 (JP). **KOYAMA, Kenji** [JP/JP]; C/O CANON KABUSHIKI KAISHA, 30-2, Shimomaruko 3-chome, Ohta-ku, Tokyo, 1468501 (JP).

(74) Agents: **ABE, Takuma** et al.; C/O CANON KABUSHIKI KAISHA, 30-2, Shimomaruko 3-chome, Ohta-ku, Tokyo, 1468501 (JP).

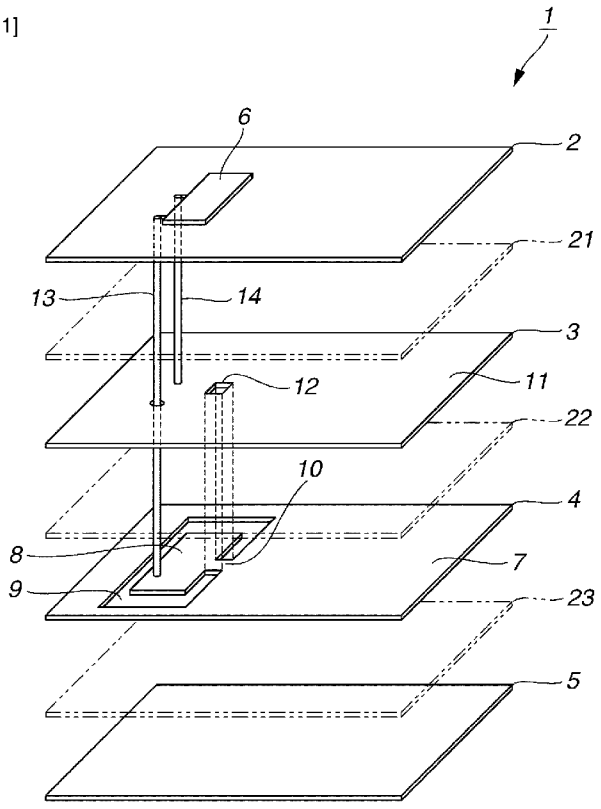
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ,

[Continued on next page]

(54) Title: PRINTED CIRCUIT BOARD

[Fig. 1]



(57) Abstract: A multi- layer printed circuit board (1) includes an embedded capacitor substrate composed of a power source conductor layer (4) and a ground conductor layer (3), the layers being disposed close to each other. The power source conductor layer has a first power source plane (8) to supply power to a circuit element, and a second power source plane (7) that is separated from the first power source plane by a gap (9) and functions as a main power source. The first power source plane is partially connected to the second power source plane by a connecting line (10). The ground conductor layer has an opening (12) at a position overlapping with a projected image when the connecting line is projected on the ground conductor layer. This structure suppresses propagation of the noise caused at the circuit element and reduces radiation noise in the printed circuit board.

WO 2012/039120 A4

TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

— *with amended claims (Art. 19(1))*

(88) Date of publication of the international search report: 18 May 2012

Date of publication of the amended claims: 2 August 2012

AMENDED CLAIMS
received by the International Bureau on
27 April 2012 (27.04.2012)

[Claim 1](Amended) A printed circuit board, wherein
a power source conductor layer;
a ground conductor layer; and
a signal wiring layer having a circuit element thereon;
are multilayered with dielectric layers interposed therebetween, the printed circuit board, comprising;
a first power source plane provided in the power source conductor layer to supply a power source potential to the circuit element, the first power source plane being connected to a power source terminal of the circuit element through a via;
a second power source plane provided in the power source conductor layer separated from the first power source plane by a gap;
a connecting line provided in the power source conductor layer, connecting the first power source plane to the second power source plane; and
a ground plane provided in the ground conductor layer, the ground plane being connected to a ground terminal of the circuit element through a via,
wherein a dielectric layer among the dielectric layers interposed between the power source conductor layer and the ground conductor layer has a thickness equal to or less than 100 micrometer, and
wherein the ground plane has an opening at a portion covering a projected image when the connecting line is projected onto the ground conductor layer.

[Claim 2] The printed circuit board according to claim 1, wherein the opening has a size equal to or larger than the projected image when the connecting line is projected onto the ground conductor layer.

[Claim 3](Amended) The printed circuit board according to claim 1,
wherein a ratio of the length of the opening to the length of the connecting line is equal to or more than 1 and a ratio of the width of the opening to the width of the connecting line is equal to or more than 1.2.