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(74) Agent: WOLFF, BREGMAN AND GOLLER; P.O. Box
1352, 91013 Jerusalem (IL).

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(71) Applicant (for all designated States except US): MEM-ORIGHT MEMORITECH (SHENZHEN) CO., LTD.
[CN/CN]; 3rd Floor, Building W2A, High-tech Industrial Valley, Nan Shan District, Shenzhen (CN).

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(71) Applicant (for MW only): TOPPER, Jonathan [IL/IL];
11/8 Hama'apilim Street, Jerusalem 92545 (IL).

(72) Inventor; and

(75) Inventor/Applicant (for US only): HUANG, He
[CN/CN]; 3rd Floor Building W2A, High Tech Industrial Valley, Nan Shan District, Shenzhen (CN).

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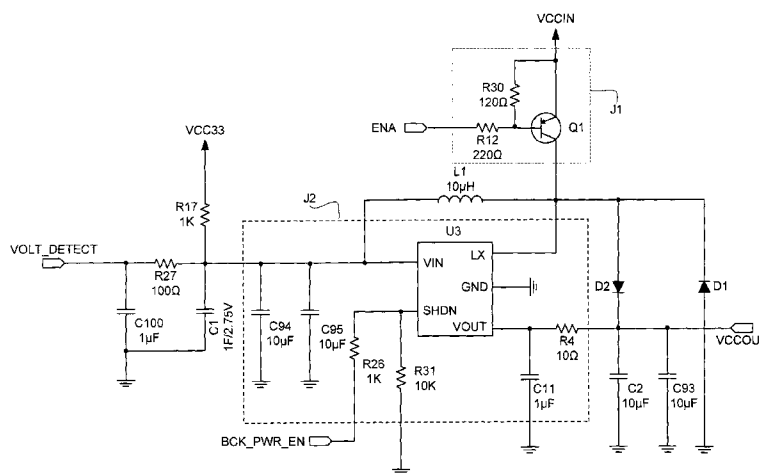


FIG. 3

(57) Abstract: A power failure protection circuit (10) for a non-volatile semiconductor storage device includes an energy storage unit (C1) that serves as a backup power supply for the storage device for providing backup electrical energy for the storage device when a power failure occurs. A main control unit (12) is responsive to normal operation of the device for controlling an external power input to charge the energy storage unit, dynamically detecting a status of the energy storage unit and using the status to ensure sufficient backup electrical energy for the energy storage unit. The main control unit (12) is responsive to an abnormality of the power supply for discharging the energy storage unit for providing power to the semiconductor storage device.

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POWER FAILURE PROTECTION METHOD AND CIRCUIT FOR NON-VOLATILE SEMICONDUCTOR STORAGE DEVICE

BACKGROUND OF THE INVENTION

Field of Invention

The present invention relates to a protection method and circuit for preventing unexpected power failure. More particularly, the present invention relates to a protection method and circuit for a non-volatile semiconductor storage device for preventing an
5 unexpected power failure.

Related Art

It is well-known that with the rapid development of semiconductor processes and technology, non-volatile semiconductor storage devices, especially flash memory devices (for example, U-disks, various flash memory cards, MP3 and MP4 players, as well as
10 newly-developed solid state devices), have become popular among consumers. Meanwhile, as the firmware and structures of those devices become increasingly complicated, the read/write of data is usually accomplished by means of files instead of direct operations on the address of a storage unit. When the data is operated by means of file read/write, during the operation of the device, the data is usually buffered in a volatile storage device, such as
15 SDRAM. Thus, once an unexpected power failure occurs, the data will be permanently lost. If the lost data includes the firmware of the device or system information such as the map table of the data address, the device will be fatally damaged. A power failure protection design for flash memory devices can ensure the certainty of the operating status of the device and the completeness of the recorded data when an unexpected power failure of the
20 flash memory device occurs. Thus, the in-situ data and device status information may be recovered in a timely fashion after the power supply of the device is restored, thereby preventing the loss of data and/or confusion of the main control unit (MCU). In saying this, flash memory devices operate at lower power consumption and occupy little space, so complicated power failure protection circuits are not suitable for flash memory devices.

Therefore, a power failure protection circuit with a simple configuration and low cost is needed to solve the problems caused by unexpected power failures of flash memory devices.

Many of these issues have been addressed in the prior art. Thus, for example, 5 US Patent No. 6,856,556 (Hajeczek) entitled "*Storage subsystem with embedded circuit for protecting against anomalies in power signal from host*" discloses a storage subsystem, such as a flash memory card, which includes a charge pump that receives a power signal from a host system, and generates a regulated power signal that is provided to the storage subsystem's controller. When the power signal from the host is interrupted, the charge 10 pump additionally acts as a backup power supply such that the storage subsystem can continue to operate temporarily. The storage subsystem also includes a voltage detection circuit that monitors the power signal from the host system to detect anomalies therein. The voltage detection circuit responds to detection of an anomaly by asserting a busy signal to block the host system from performing write operations to the storage subsystem. By 15 asserting the busy signal, the voltage detection circuit substantially ensures that the backup, regulated power provided by the charge pump will be sufficient for the controller to complete all outstanding operations.

US Patent No. 7,269,755 (Moshayedi *et al.*) entitled "*Solid-state memory device with protection against power failure*" discloses a data preservation system for flash 20 memory systems with a host system. The flash memory system receives a host system power supply and energizes an auxiliary energy store therewith and communicates with the host system via an interface bus, wherein, upon loss of the host system power supply, the flash memory system actively isolates the connection to the host system power supply and isolates the interface bus and employs the supplemental energy store to continue write 25 operations to flash memory.

The above patents are typical of backup power supplies that store energy from a host system in a backup reservoir and take the stored energy from the backup reservoir in the event of a malfunction in the host's power supply. Typically the backup reservoir is connected directly to the voltage output of the host's power supply since this avoids the

need for an invasive connection to the internal circuitry of the host. But it means that the backup reservoir, typically a storage capacitor, will be fully charged to the output voltage of the host power supply. Any fluctuation in the voltage of the host power supply will also affect the voltage of the backup reservoir. As a result, a gradual drop in the voltage of the host power supply that is not sufficiently large to isolate the host power supply and initiate immediate actuation of the backup supply, may mean that there is insufficient voltage in the backup supply if the voltage of the host power supply subsequently drops to a level that initiates actuation of the backup supply.

Yet a further potential drawback of known systems is the need to provide a control signal to the host power supply. For example, in US Patent No. 6,856,556, the backup power supply has a controller that feeds a ready/busy signal to the host system. The need to provide such a connection is invasive and precludes a completely standalone solution that can be wholly integrated with the memory device and sold as an independent protected unit for direct connection to a host system.

It would therefore be desirable to provide a backup supply that overcomes these drawbacks.

SUMMARY OF THE INVENTION

Accordingly, the present invention is directed to a power failure protection method and circuit advantageous in stable performance and easy-to-operate and adapted to a non-volatile semiconductor storage device. A large-capacity capacitor is used as an energy storage and power supply component to supply power to the device for a certain period of time in a situation that the power supply of the device is abnormal, so as to enable the device to save processing data and relevant device status information securely.

In accordance with a first aspect, the invention provides a method for protecting a non-volatile semiconductor storage device during a power failure of a power supply, said method comprising:

during normal operation of the device, controlling an external power input to charge an energy storage unit, dynamically detecting a status of the energy storage unit and using said status to ensure sufficient backup electrical energy for the energy storage unit; and

upon detecting an abnormality of the power supply, discharging the energy storage unit for providing power to the semiconductor storage device.

In accordance with a second aspect, the invention provides a power failure protection circuit for a non-volatile semiconductor storage device, said power failure protection circuit comprising:

an energy storage unit serving as a backup power supply for the storage device for providing backup electrical energy for the storage device when a power failure occurs; and

a main control unit responsive to normal operation of the device for controlling an external power input to charge the energy storage unit, dynamically detecting a status of the energy storage unit and using said status to ensure sufficient backup electrical energy for the energy storage unit; and being responsive to an abnormality of the power supply for discharging the energy storage unit for providing power to the semiconductor storage device.

Preferably, when the device works normally, the main control unit controls the energy storage unit whereby the main control unit dynamically detects the electrical energy of the energy storage unit, so as to control the external power input to charge the energy storage unit when the electrical energy of the energy storage unit is insufficient and control the external power input to stop charging the energy storage unit after the energy storage unit is fully charged.

The main control unit dynamically detects whether or not the power supply of the storage device is abnormal independently of the host power supply.

In some embodiments, during normal operation, the main control unit selects the external power input to supply power, and during an abnormal operation, the main control unit selects the energy storage unit to supply power.

In some embodiments, when a charge/discharge voltage of the energy storage unit does not match a supply voltage of the storage device, a charge/discharge control circuit adjusting the charge/discharge voltage of the energy storage unit, so as to achieve the match between the charge/discharge voltage and the supply voltage.

5 Typically, the energy storage device is a capacitor.

The non-volatile semiconductor storage device may be a flash memory device.

Preferably, the external power input charges the energy storage capacitor through a buck charge control circuit. The buck charge control circuit includes a charge control switch, an inductor connected in series between the energy storage capacitor and the charge control switch, and a freewheeling diode connected in anti-parallel to the inductor and the energy storage capacitor.

Preferably, the energy storage capacitor provides a backup power supply for the storage device through a boost discharge control circuit. The boost discharge control circuit includes a serially-connected diode, an inductor and an energy storage capacitor shared by the charge control loop, a discharge control switch connected in parallel between two ends of the inductor and the energy storage capacitor, and a decoupling capacitor with one end connected to an output end of the discharge loop and the other end grounded.

Thus, in summary, the invention employs a large-capacity capacitor as an energy storage and power supply component, for effectively solving the problems caused by an abnormal power supply of the non-volatile semiconductor storage device, thereby enabling the device to save processing data and device status information when the power supply is abnormal. The charge status of the energy storage unit is dynamically detected, and the charge to the energy storage unit is stopped after the energy storage unit is fully charged, thereby extending the service life of the energy storage unit. In addition, a charge/discharge voltage adjusting circuit is further used to achieve a better match of the voltage between an external power input and an energy storage capacitor and the voltage between the energy storage capacitor and the device power supply output.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram showing the functionality of a power failure protection circuit according to the present invention;

FIG. 2 is a schematic diagram illustrating principles of a power failure protection circuit according to an embodiment of the present invention;

FIG. 3 is a circuit diagram of a power failure protection circuit according to an embodiment of the present invention;

FIGS. 4 and 5 are block diagrams showing respectively connectivity to the circuit shown in FIG. 3 of the main control unit and the power supply select circuit shown in FIG. 1; and

FIG. 6 is a schematic diagram illustrating processes of a power failure protection method according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

The applications of a flash memory device serving as a non-volatile semiconductor storage device are illustrated in detail below with reference to the accompanying drawings, where identical components that appear in more than one figure or that share similar functionality will be referenced by identical reference symbols.

Referring to the circuit principles of FIG. 1, the power failure protection circuit 10 provided by the present invention includes an external power input 11, an MCU 12, a charge control circuit 13, an energy storage unit 14, a discharge control circuit 15, a power supply select circuit 16, and a device power supply output 17. In this embodiment, a large-capacity capacitor is used as the energy storage unit. When the flash memory device works normally, the MCU 12 controls the external power input 11 to charge the energy storage unit 14 through the charge control circuit 13, and controls the external power input 11 to stop charging the energy storage unit 14 after it is fully charged. At the same time, the MCU 12 dynamically detects the voltage of the energy storage unit 14, so as to ensure sufficient backup electrical energy for the energy storage unit regardless of the voltage of the host power supply, and initiates charging the energy storage unit when the electrical

energy of the energy storage unit drops below a certain threshold so as to ensure that there is always sufficient charge in the energy storage unit to complete the data transfer to the non-volatile semiconductor storage device in the event of a power failure in the host. The MCU further dynamically detects whether the power supply of the storage unit is abnormal or not. In this context, the voltage of the energy storage unit is considered “abnormal” when it is too low for the semiconductor storage device to operate. When the power supply of the storage device is abnormal, or an unexpected power failure of the storage device occurs whereby the supply voltage of the storage device is too low to sustain a normal operation of the memory device, the MCU controls the power supply select circuit 16, which isolates the host power supply and connects the energy storage unit 14 via the discharge control circuit 15. The discharge control circuit 15 feeds current from the energy storage unit 14 to the power supply 17 such that the output of the energy storage unit provides a protection power supply for the semiconductor storage device through the discharge control circuit and the device power supply output.

The charge/discharge control circuit controls the charge/discharge of the energy storage unit 14. It will be understood that while these are shown in Fig. 1 as two separate functional units, they can also be realized by a shared module. When the charge/discharge voltage of the energy storage unit does not match the supply voltage of the storage device, the charge/discharge control circuit 15 is further used to achieve the match between the charge/discharge voltage of the energy storage unit and the supply voltage of the storage device. Thus, when active, the charge control circuit 13 ensures that the charging current to the energy storage unit 14 is the same as the discharge current thus maintaining constant voltage across the energy storage unit 14. Additionally, the discharge control circuit 15 matches the voltage of the host power supply when discharging to provide suitable voltage to the controller and DRAM, flash array. The embodiment that a charge voltage of the energy storage unit is lower than the supply voltage of the storage device is illustrated hereinafter.

FIG. 2 is a schematic circuit diagram illustrating the principles of a power failure protection circuit according to an embodiment of the present invention. In this embodiment,

the charge control circuit 13 is based on a buck converter, and the discharge control circuit is based on a boost converter. In FIG. 2, VCCIN is the input power supply that is fed via a charge enable switch J1 to the charge control circuit 13 comprising a first diode D1, whose anode is connected to GND and whose cathode is connected via an inductor L1 to one end of a first capacitor C1, whose other end is connected to GND. The capacitor C1 serves as the energy storage unit 14 whose voltage is constantly monitored via a VOLT_DETECT pin of the MCU 12 for feeding back the charge status of the energy storage unit 14 constituted by the capacitor C1 to the MCU, so as to determine whether or not to disable the charge.

Upon detecting an unexpected power failure of the device occurs, the MCU 12 enables the device power supply through the power supply select circuit 16. This is done by disabling the charge control circuit 13 by opening the charge enable switch J1 and repetitively opening and closing a discharge enable switch J2. When the discharge enable switch J2 is closed, the energy storage capacitor C1 discharges and the inductor L1 stores electrical energy. When the discharge enable switch J2 is open, the energy storage capacitor C1 and the inductor L1 discharge via the switch J2 through a second rectifier diode D2 to the output VCCOUT of the power supply select circuit 16. The voltage of VCCOUT is the sum of the voltages across L1 and C1. A second capacitor C2 is connected between the output VCCOUT of the power supply select circuit 16 and GND and serves to decouple the output of the boost discharge control circuit.

When the host system is powered up, the MCU 12 closes the charge enable switch J1 so that C1 becomes fully charged via the inductor L1. During the charging cycle, the charge enable switch J1 is closed and opened repetitively until C1 is fully charged. In the steady state when C1 is fully charged, the MCU 12 opens the switch J1 so that prior to a power failure C1 remains fully charged. The charging voltage of C1 will be lower than the host power supply voltage. For example, in an embodiment of the invention reduced to practice, the charging voltage of C1 was 2.7V, while the host power supply voltage was 5V. If the MCU 12 detect a drop in voltage across C1 (due to leakage, for example), it will again intermittently close and open J1 so that the charging process is refreshed.

In steady state, when the charge enable switch J1 is open, the capacitor C1 serves to decouple the host power supply voltage VCCIN so that no current flows through the inductor L1 and the voltage across the capacitor C1 is less than VCCIN. When the charge enable switch J1 is now closed, the host power supply charges the capacitor C1, and when
5 the switch J1 is opened, the host power supply stops charging the capacitor C1. By repetitively closing and opening the enable switch J1, there is a constant change of voltage across the capacitor C1, thus ensuring that during the charging process the capacitor C1 is fully charged. The inductor L1 stores energy during the charge/discharge process. The diode D1 serves to maintain a continuous current. During the charge process, the MCU 12
10 opens the discharge enable switch J2 and intermittently closes and opens the charge enable switch J1, and during the discharge process, the MCU intermittently closes and opens the discharge enable switch J2. The rectifier diode D2 prevents a reverse current flow after the current is boosted.

The charge process operates as follows. When, prior to charging the capacitor C1,
15 the charge enable switch J1 is closed and the discharge enable switch J2 is opened, the diode D1 is not conducting, and J1, L1, feed current which charges C1 through the buck converter. When the charge enable switch J1 is opened, the inductor L1 releases electrical energy to generate a clockwise current, which flows through the capacitor C1 and the diode D1, for storing energy in the capacitor C1. Afterwards, the voltage of the capacitor rises to
20 reach the level of the host power supply through the repeated ON/OFF of the capacitor C1. For so long as the VOLT_DETECT feeds back that the voltage of the capacitor C1 has not reached the threshold, the power supply continues charging the energy storage capacitor C1. When the VOLT_DETECT pin feeds back that the voltage of the capacitor C1 has reached
25 the threshold, the MCU opens J1 to stop charging the energy storage capacitor C1. At this point, the voltage at the non-grounded terminal of C1 is higher than GND, so that the diode D1 is reverse biased, thus preventing current from flowing through D1 when J1 is opened.

The discharge process is as follows. When the charge enable switch J1 is opened and the discharge enable switch J2 is closed, L1, D2, and C1 supply power externally through the boost converter. At the same time, part of the energy across the capacitor C1 is

also fed to the inductor L1 via the diode D1, which is reverse-biased during the discharge process, when the discharge enable switch J2 is closed. When both the charge enable switch J1 and the discharge enable switch J2 are opened, the capacitor C1 can only discharge via the reverse-biased diode D1 through the inductor L1, such that the voltage of VCCOUT is the sum of the respective voltages across capacitor C1 and the inductor L1 both of which store energy during the charging process. As the discharge enable switch J2 is intermittently closed and then opened, the current flowing through the inductor L1 changes. This induces an increased voltage across the inductor L1, whose magnitude depends on the rate of change of the inductor current. Consequently, when the discharge enable switch J2 is closed, the net voltage fed to the output VCCOUT of the power supply select circuit 16 is the sum of the voltages across the inductor L1 and the capacitor C1. The discharge enable switch J2 is repeatedly closed and opened until the MCU 12 finishes saving the desired content or the capacitor C1 is fully discharged. When the host power supply fails, the MCU 12 saves any pending data in a buffer memory whose contents are transferred to the flash chip. All this can easily be accomplished in 1 second and suitable design of the circuit shown in Fig. 2 and switching rate of the charge disable switch J2 ensures that sufficient charge is maintained across the capacitor C1 to achieve this.

FIG. 3 shows a circuit implementation based on the approach of FIG. 2 and which ensures that the above design *desiderata* are achieved. The charge power supply VCCIN is shown in the upper part of the figure, and the discharge power supply VCCOUT is shown in the lower right part of the figure. Capacitors C94, C95, C11, C2, C93, resistors R26, R31, R4, and a DC/DC Boost Regulator U3 such as the SP6641A/B manufactured by Sipex Corporation of California, USA form the discharge enable switch J2. It will be understood that the discharge enable switch J2 serves as the power supply select circuit 16 shown in Fig. 1, since when it is open the host power supply provides power to the non-volatile storage device, while when it is closed, backup power is provided by the energy storage unit. ENA is the voltage supply enable pin, which is activated by the MCU 12 to turn on/off the charge circuit. BCK_PWR_EN is the discharge enable pin, which is activated by the MCU 12 when the power failure of the device occurs so as to enable the energy storage

capacitor C1 to supply power. Resistors R12, R30 and a triode Q1 operate as the charge enable switch J1 shown in Fig. 3. Q1 is turned off to stop charging the capacitor C1 when the voltage on ENA is at a high level, and Q1 is turned on to start charging the capacitor C1 when the voltage on ENA is at a low level. A resistor R27 and a capacitor C100 form a
5 filter circuit, mainly used for filtering and providing the over-current protection during the voltage detection process.

FIGS. 4 and 5 are block diagrams showing respectively connectivity to the circuit shown in FIG. 3 of the MCU 12 and the power supply select circuit 16 shown in FIG. 1. Thus, the charge power supply VCCIN and the VOLT_DETECT pin are fed to respective
10 inputs of the MCU 12, which feeds respective charge and discharge signals to the charge enable switch J1 and the discharge enable switch J2. The MCU 12 also feeds a power select signal to the power supply select circuit 16. Likewise, the host power supply VCCIN and the backup voltage VCCOUT of the energy storage unit 14 are fed to respective inputs of the power supply select circuit 16 as well as the power select signal from the MCU 12. An
15 output of the power supply select circuit 16 is fed to the power supply 17 shown in FIG. 1. The MCU 12 includes a pulse width modulator (PWM) module that is controlled by a processor and generates pulses corresponding to the charge enable signal J1 and the discharge enable signal J2. The frequencies of the pulse enable signals are determined by the circuit design. The power supply select circuit 16 is responsive to the power select
20 signal produced by the MCU 12 for selectably switching VCCIN or VCCOUT to the power supply 17.

FIG. 6 shows the operating processes of the circuit in the above embodiment. When the device is powered on normally, the MCU 12 intermittently activates the power supply charge enable pin in a pulse mode at a predetermined frequency, so as to charge the energy
25 storage capacitor C1. Then, the MCU periodically queries the capacitor detection pin. If the voltage value does not meet the threshold, the energy storage capacitor C1 is continuously charged, and if the voltage value meets the threshold, the power supply charge enable pin is deactivated to stop charging the capacitor. Thereafter, the MCU controls the discharge enable pin according to the status of the external power supply. If the power supply of the

device becomes abnormal, the MCU intermittently activates the discharge enable pin in a pulse mode at a frequency determined by the inductor L1, so as to discharge the energy storage capacitor C1. Meanwhile, the boost circuit provides a supply voltage to the storage device for a certain period of time, such that the MCU has enough time to save processing data and relevant device status information so as to ensure the recovery of the *in situ* data and device status when the power supply is normally provided again. If the operation ends normally without the unexpected power failure, the MCU enters a system ended state, and the processing data and device status information are saved normally. In such case, the protection circuit does not need to supply power.

10 It will be appreciated that though the present invention has been described with reference to the above embodiments, they are not intended to limit the present invention, and other methods and circuits can be used to implement the present invention.

15 It will also be understood that the power failure protection apparatus provided by the present invention is not only applicable to a semiconductor storage device, but also to other electronic products affected by unexpected power failure, so as to prevent damages caused by unexpected power failure.

CLAIMS

1. A method for protecting a non-volatile semiconductor storage device during a power failure of a power supply, said method comprising:
during normal operation of the device, controlling an external power input to charge
5 an energy storage unit, dynamically detecting a status of the energy storage unit and using said status to ensure sufficient backup electrical energy for the energy storage unit; and
upon detecting an abnormality of the power supply, discharging the energy storage unit for providing power to the semiconductor storage device.
2. The method according to claim 1, wherein the status of the energy storage unit is
10 indicative of electrical energy stored in the energy storage unit and using said status to ensure sufficient backup electrical energy for the energy storage unit includes charging the energy storage unit when the electrical energy of the energy storage unit is insufficient and controlling the external power input to stop charging the energy storage unit after the energy storage unit is fully charged.
- 15 3. The method according to claim 1 or 2, further comprising dynamically detecting whether or not the power supply is abnormal.
4. The method according to claim 3, further comprising selecting the external power input to supply power during normal operation of the device, and selecting the energy storage unit to supply power during an abnormal operation.
- 20 5. The method according to any one of claims 1 to 4, wherein ensure sufficient backup electrical energy for the energy storage unit comprises adjusting a charge/discharge rate of the energy storage unit so as to ensure that the energy storage unit charges at a rate that is no less than the rate of discharge.
6. The method according to claim 5, wherein adjusting a charge/discharge rate of the
25 energy storage unit includes intermittently storing energy in an inductor and discharging said energy to the energy storage unit.

7. The method according to any one of claims 1 to 6, wherein the energy storage unit is a capacitor.
8. The method according to any one of claims 1 to 7, wherein the non-volatile semiconductor storage device is a flash memory.
- 5 9. A power failure protection circuit (10) for a non-volatile semiconductor storage device, said power failure protection circuit comprising:
- an energy storage unit (C1) serving as a backup power supply for the storage device for providing backup electrical energy for the storage device when a power failure occurs; and
- 10 a main control unit (12) responsive to normal operation of the device for controlling an external power input to charge the energy storage unit, dynamically detecting a status of the energy storage unit and using said status to ensure sufficient backup electrical energy for the energy storage unit; and being responsive to an abnormality of the power supply for discharging the energy storage unit for providing power to the semiconductor storage
- 15 device.
10. The power failure protection circuit according to claim 9, further comprising:
- a power supply select circuit (16, J2) for selecting the external power supply to provide power to the storage device when the external power supply works normally, and selecting the energy storage unit to supply power to the storage device when the operation
- 20 of the external power supply is abnormal.
11. The power failure protection circuit according to claim 9 or 10, further comprising a charge/discharge control circuit (J1, L1, C1, D1, J2, D2, C2) for controlling the charge/discharge of the energy storage unit.
12. The power failure protection circuit according to claim 11, wherein the
- 25 charge/discharge control circuit is adapted to achieve a match between a charge/discharge voltage of the energy storage unit and a supply voltage of the storage device.

13. The power failure protection circuit according to any one of claims 9 to 12, wherein the energy storage unit includes a capacitor (C1).
14. The power failure protection circuit according to claim 13, including a buck converter for feeding power from the external power input to said capacitor (C1), said buck
5 converter comprising a charge enable switch (J1, R12, R30, Q1), an inductor (L1) connected in series between the capacitor (C1) and the charge enable switch (J1), and a freewheeling diode (D1) connected in anti-parallel to the inductor and the capacitor (C1).
15. The power failure protection circuit according to claim 14, wherein the energy
10 storage capacitor provides a backup power supply for the storage device through a boost discharge control circuit that comprises a diode (D2), an inductor (L1) and an energy storage capacitor (C1), a discharge enable switch (J2) connected across the inductor and the energy storage capacitor, and a decoupling capacitor (C2) connected between an output of the power failure protection circuit and GND.

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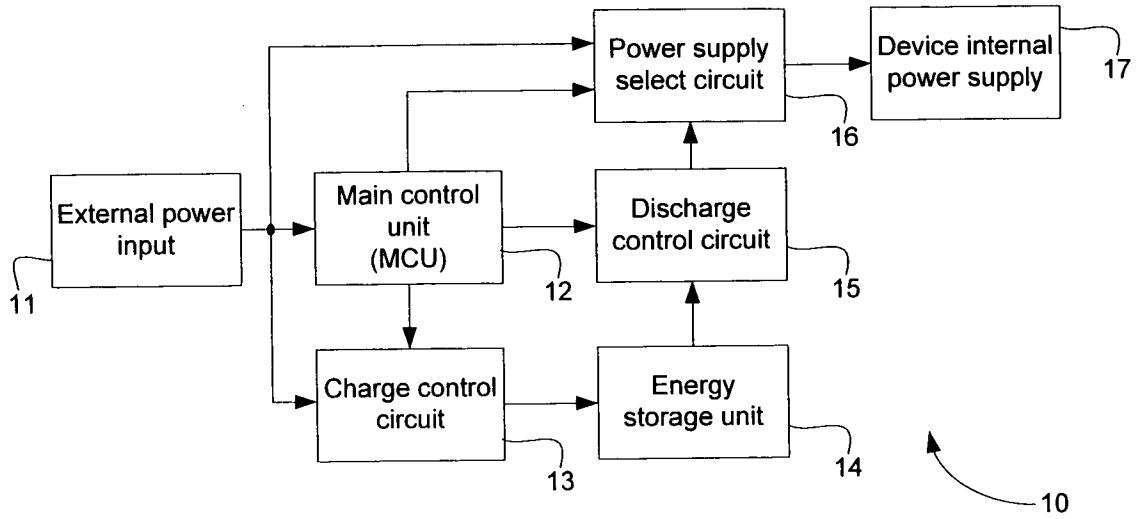


FIG. 1

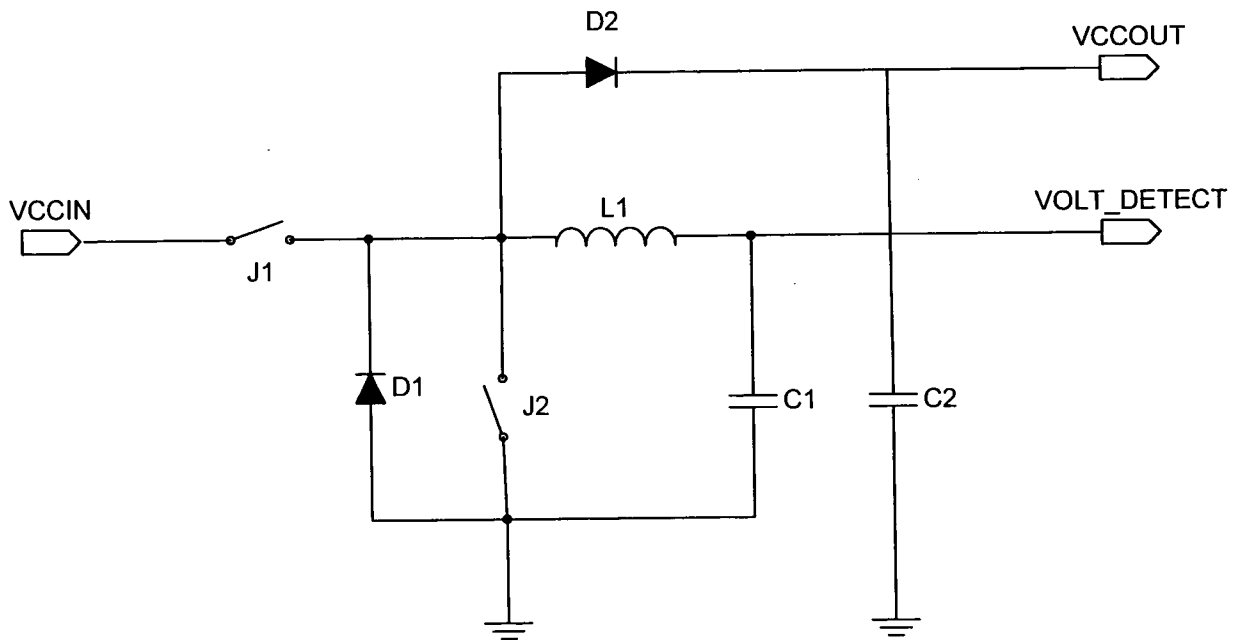


FIG. 2

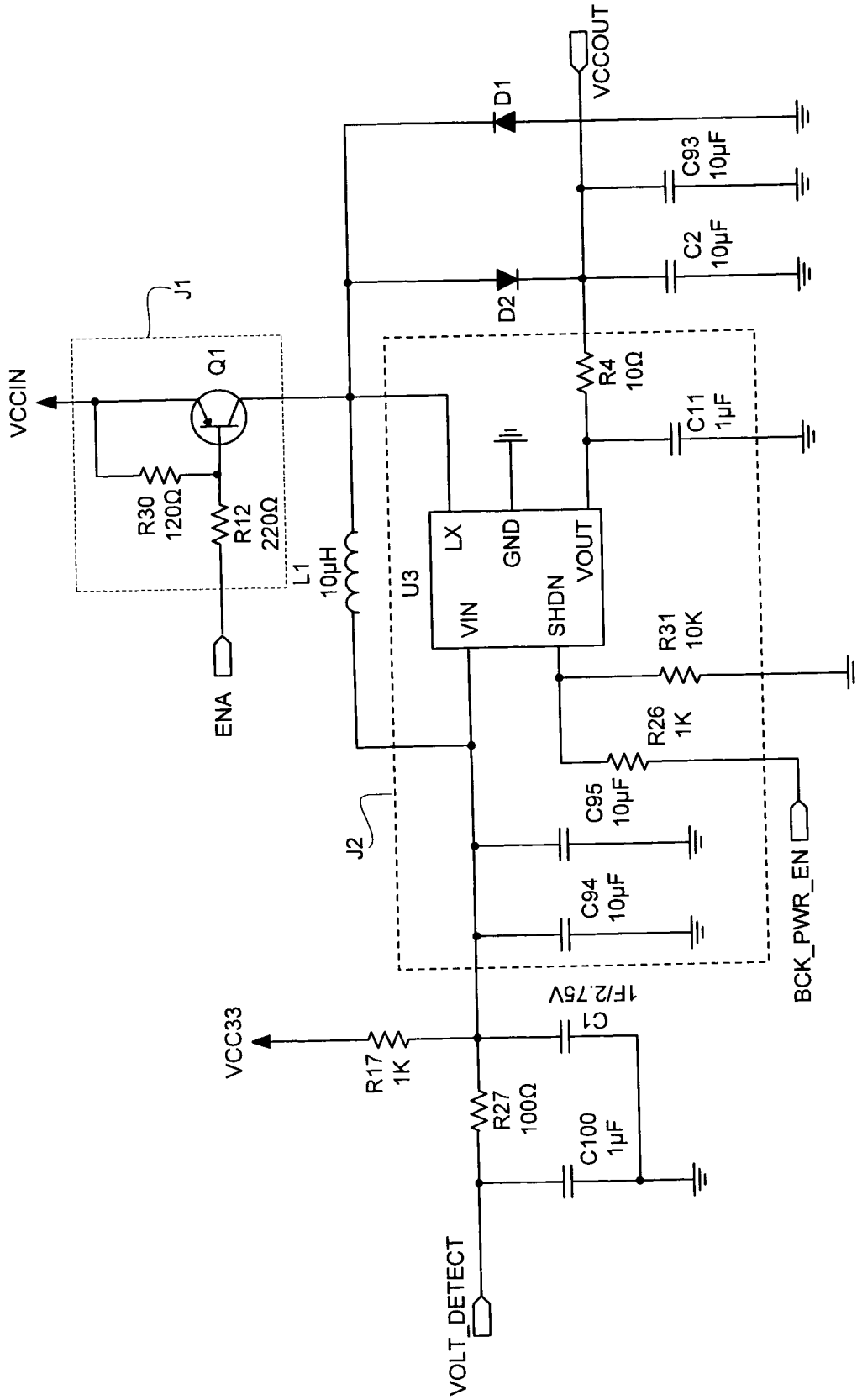


FIG. 3

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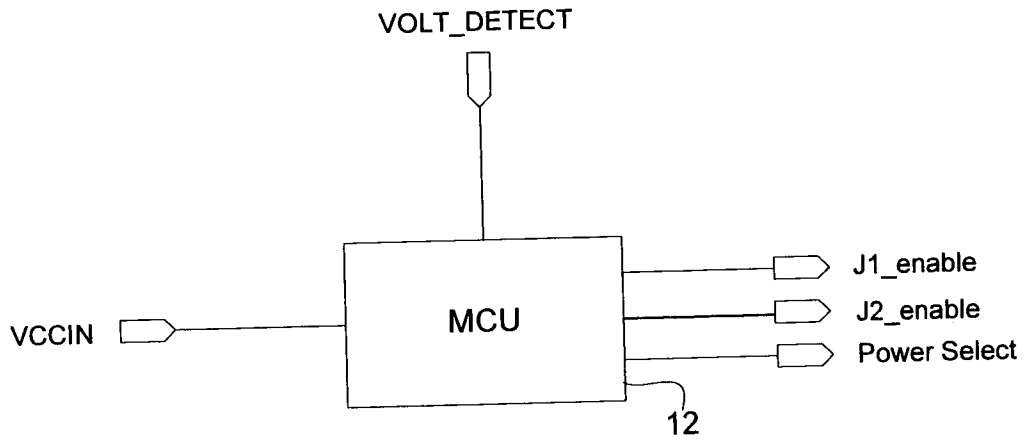


FIG. 4

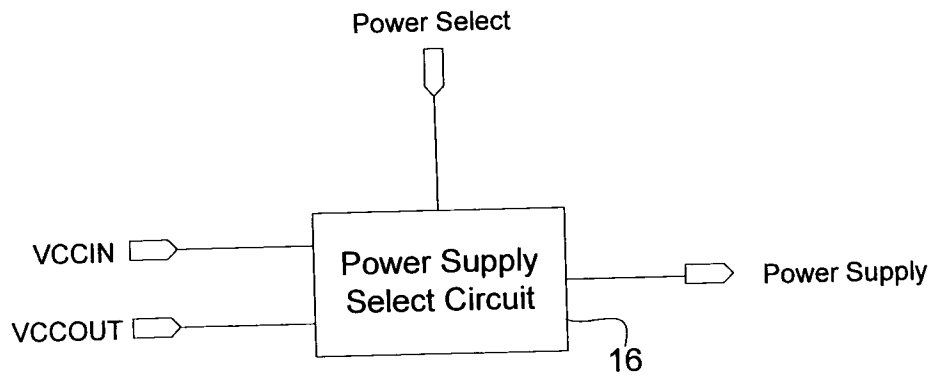


FIG. 5

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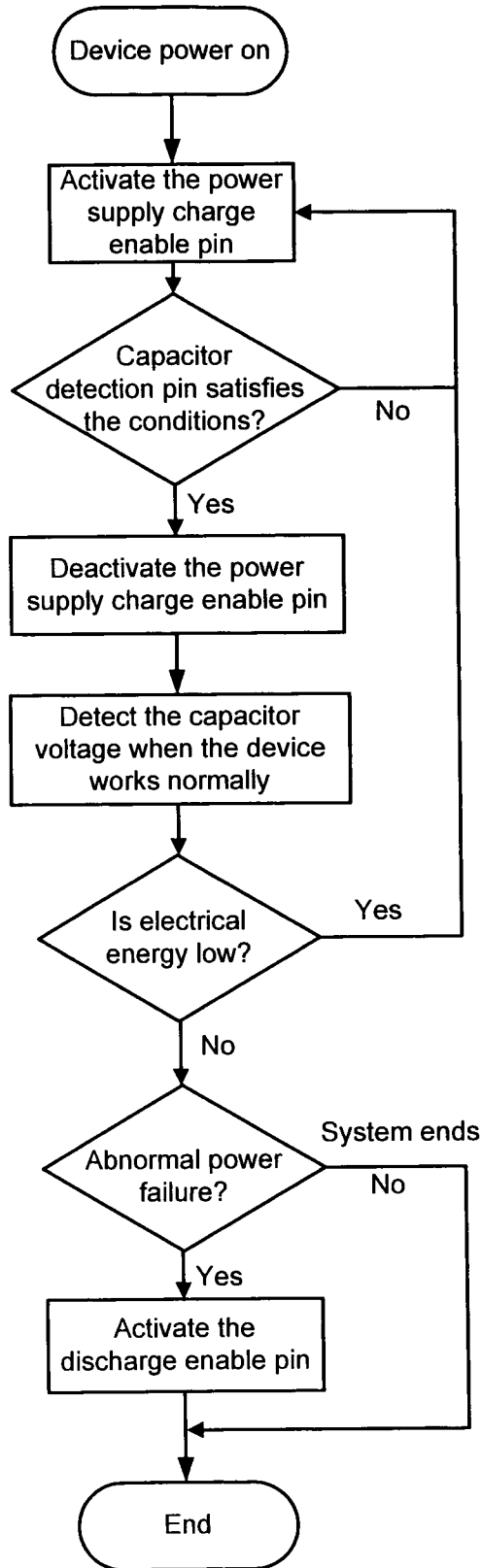


FIG. 6

INTERNATIONAL SEARCH REPORT

International application No
PCT/IL2008/000989

A. CLASSIFICATION OF SUBJECT MATTER INV. G11C16/22		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols) G11C		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practical, search terms used) EPO-Internal, WPI Data		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2004/001359 A1 (OTT WILLIAM E [US]) 1 January 2004 (2004-01-01)	1-5,7-13
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A document defining the general state of the art which is not considered to be of particular relevance	*T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention	
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P document published prior to the international filing date but later than the priority date claimed		
Date of the actual completion of the international search <p style="text-align: center;">3 November 2008</p>	Date of mailing of the international search report <p style="text-align: center;">12/11/2008</p>	
Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Authorized officer <p style="text-align: center;">Gärtner, Wolfgang</p>	

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