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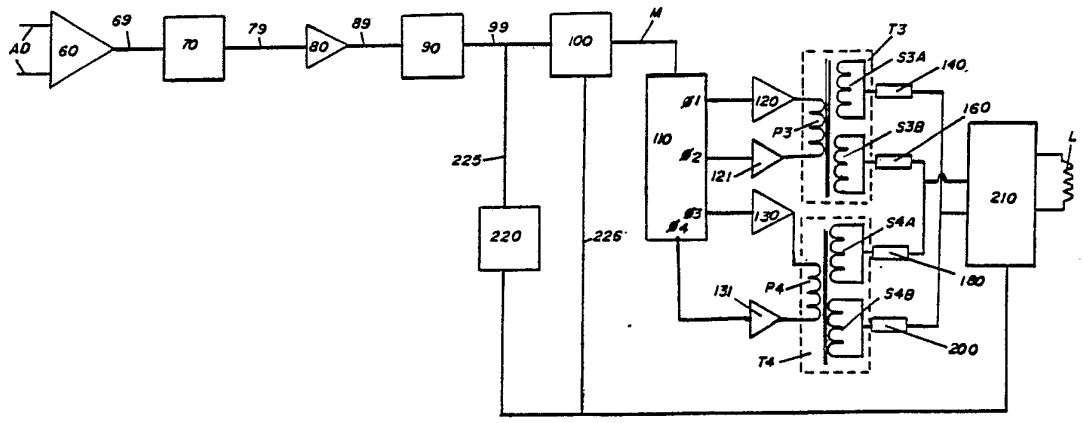

(57) Abstract

A power supply and audio amplifier system including an audio amplifier system adapted to receive an audio signal which is supplied to an attenuator (70) which receives the signal and selectively attenuates the signal which is then supplied to a buffer (80) and filter circuit (90) to condition the signal. The attenuated, filtered signal is then supplied to a modulator (100) where it is converted to a square wave signal having a pulse width which is a function of the level of the audio signal. The square wave pulse signal is then supplied to a push-pull converter (110) to generate an alternating current signal which is supplied to the primary coil (P3, P4) of a transformer (T3, T4) and an amplified output signal is supplied to a load (L) from the secondary (S3, S4) of the transformer. The load characteristics are analyzed and a loading signal is supplied to a clipper circuit (220) which prevents the output from exceeding selected load limits.

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DESCRIPTION

AUDIO AMPLIFIER SYSTEM

TECHNICAL FIELD

The present invention relates to signal amplification systems and power supply systems and more particularly to low signal distortion amplifiers and power supply systems particularly useful in connection with such amplifier systems, as well as other purposes.

Various amplifier and power supply systems are known and have been used in the art for many years in connection with audio systems and for other purposes.

In general power supply arrangements for audio systems, and particularly for audio amplifier systems, must be operable over a wide range of audio frequencies with least signal distortion possible in response to frequency change.

BACKGROUND ART

Various prior art amplifier arrangments are known to provide acceptable audio frequency response but, in general, the cost of such systems has been found to increase directly in proportion to efficiency. Also amplifier systems for providing quality audio can be quite expensive.

Further no prior art system is known to provide an inexpensive power supply arrangement and an inexpensive amplifier arrangment to receive an audio signal and provide substantially distortion free response over a wide range of audio frequencies and at high loading with very high efficiency.

Moreover, no prior art arrangement is known where the amplifier operating characteristics are responsive to the instantaneous load on the output of the system in order to avoid overloading the system input and where signal distortion which inherently occurs in the event of changing load in prior art amplification systems is substantically reduced.

Moreover, no prior art audio smplifier system is known which provides "push-pull" mode of operation of the type provided by devices within the scope of the present invention.

Also, no prior art power supply is known which anticipates devices in accordance with the present invention which utilize MOSFET (metal oxide silicon

field effect transistors) to provide a high efficiency power supply based on generation of a square wave signal of selected frequency where the square wave signal is then used to convert a direct current supply to alternating current in a transformer where the secondary voltage is closely controlled over a wide range of current range.

In general, no prior art amplifier or power supply system is known which yields the efficiencies and the characteristics of devices within the scope of the present invention utilizing.

DISCLOSURE OF THE INVENTION

The present invention provides new, useful, and particularly inexpensive, but effective, arrangements for power supply and audio amplifier systems.

More particularly, the present invention provides audio systems which can accommodate change in loading of the system yet maintain quality of response and avoid the adverse characteristics of various prior art arrangements under similar changes by providing a system which limits the power which can be supplied by the unit but is substantially unaffected by loading on the system so long as the permitted power levels are not exceeded.

Additionally, a power supply can be provided for use with audio systems of the present invention which is economical to fabricate and which utilizes dual transistor switches which allows enhanced speed of operation yet minimize power loss through destructive heat generation and leads to improved overall efficiency of the power supply.

Additionally, multiple voltage outputs can be provided from secondary windings of a transformer associated with the power supply where a change in power consumption at one of the outputs does not necessarily cause a change in the power available at other outputs.

More particularly the present invention provides a power supply and audio amplifier system including an audio amplifier system adapted to receive an audio signal which is supplied to an attenuator which receive the signal and selectively attenuate the signal which is then supplied to a buffer and filter circuit to condition the signal. The attenuated, filtered, signal is then supplied to a modulator where it is converted to a square wave signal having a pulse width a function of the level of the audio signal. The square wave pulse signal is then supplied to push-pull converter to generate an alternating current signal which is supplied to the primary coil of a transformer an amplified output signal is supplied to a load from the secondary of the transformer. The load characteristics are analyzed and a loading signal is supplied to an input clipper circuit which prevents the output from exceeding selected load limits.

A power supply system is provided including a pulse signal generator to operate transistor devices to supply square wave current pulse through an inductive coil at a rate determined by a clock where such current is supplied as a square wave and where the square wave pulses drive first and second transformers which operate first and second switches to gate supply power to the primary coil of a transformer in push-pull relation in response to the pulsed output signal from

the pulse signal generator arrangement to improve efficiency and reduce losses in the conversion. Devices within the scope of the present invention further provide filter arrangements to allow wide variation in output loading without substantially affecting audio characteristics of an associated audio amplifier.

Examples of arrangements within the scope of the present invention are illustrated in the accompanying Figures which will be understood are by way of illustration and not by way of limitations and that various other arrangements also within the scope of the present invention will occur to those skilled in the art upon reading the disclosure set forth hereinafter.

BRIEF DESCRIPTION OF THE DRAWINGS

Examples within the scope of the present invention are illustrated in the accompanying drawings wherein:

Figure 1 is a schematic illustration of an example of a power supply within the scope of the present invention;

Figure 2 is a flow illustration of an audio amplifier system also within the scope of the present invention;

Figure 3A-3C present a more detailed schematic of the amplifier system shown in Figure 2; and

Figure 4 is a graphic illustration of a signal generated in accordance with one feature of the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

Figure 1 illustrates a power supply useful in devices within the scope of the present invention as well as other applications. A direct current voltage source VDC for example a 120 VAC rectified supply is provided across input terminals 41, 42. A current sensing fuse 21 and a temperature sensitive fuse 22 are provided in terminals 41 and 42 along with a filtering capacitor C11. Terminals 41, 42 are connected through transistors Q41, Q42 gated by series transformer windings L2A, L2B so that as the transistors Q41, Q42 are gated current flows through the transistors to the primary coil P1 of a transformer T1. Windings L2A, L2B are operated directly in response to operation of pulse width modulator 40, for example part number 3524 which supplies a pulsed output 43 to drive the base of transistors Q43, Q44 and supply current to winding 61 which is a primary coil for secondary coils L2A, L2B by means of core 44. Pulsing current to coil L1 is supplied through a coupling capacitor C2 and transistors Q43, Q44 are provided to regulate the duty cycle of the primary coil L1.

The resistor capacitor network R,-C, provides a damping network while the capacitor C2 provides a current blocking arangement. Diodes D, D_2 are clamping diodes and capacitor C_3 provides bypass capacitor.

Clamping diodes D3, D4 are provided, as shown, across the base emitter B-E of transistors Q43, Q44 to allow internal transistors in modulator 40 to drive the rising edge of a pulse and Q43 and Q44 to drive the falling edge of the pulse which is inherently slow in a modulator at a relatively low switching rate to avoid the inefficiencies commonly encountered in the operation of similar prior art devices. A control circuit 44 is provided which is unique in that it provides three things not available with a pulse width modulator:

1.) It provides voltage regulations to pulse regulator 40 as set by zener diode Z1.

2.) It provides a soft start by controling modulator 40 during turn on at a rate fixed by capacitor C53.

3.) It provides under voltage protection by shuting off modulator 40 till the input voltage reaches the characteristic voltage of zener diode Z1.

The particular configuration shown permits low speed operation and enhances efficiency. Further, it has been found that the normal filtering requirements of prior art devices similar to devices in accordance with the present invention reduce in direct proportion to frequency but it has been found that with a square wave output of the type supplied to coil L1 in accordance with the present invention practically no

filtering is needed at the low frequency operating point.

Since modulator 40 operates in a push-pull mode current flow is generated through the primary P1 of transformer T1 at the rate set by the pulse width modulator 40 which provides an inexpensive means of setting dead time between the on-off cycles of transistors Q41, Q42 so that a square wave output of desired characteristics is generated through the primary P1 of transformer T1 as opposed to for example an inverter transformer used in the prior art which drives with no dead time. It has been found the the square wave function with very small, (less than 1%) dead time generated in the supply to the primary unexpectedly greatly increases the efficiency of the system and reduces losses. The pulse width modulator 40 is driven in response to clock pulses provided by means of input 68 from a clock (described hereinafter) to an opto- coupler OP41 provided to isolate pulse width modulator 40 where the isolated clock pulses are provided at input 47 is a 5 voltage supply voltage. The coil P1 is the primary frequency determing element of pulse width modulator 40, and the pulses from input 68 to modulator 40 syncronize.

The tap 49 from the primary P1 of transformer T1 provides current limiting input to modulator 40 where resistor R2 is low impedance current sensing resistor

so the voltage generated across resistor R2 is reduced by the R3/R4 divider and supplied to pulse modulator 40 for current sensing and limiting.

Referring now to the output of the device, another feature in accordance with the present invention is illustrated where a higher voltage output from the secondary S1, is provided through a rectifier circuit RCT1 as shown to terminals 51, 52 and is also supplied through a zener diode D6, which limits the overall voltage from the device by way of an opto isolator OP42 where the output 52 from collector of the transistor of isolator OP42 is connected to pulse with modulator 40 to control the output pulse width in response to the output voltage. This control system is a standard way of regulating the power supply but designs within the scope of the present invention do not use it except for over voltage protection, not regulation. This is significant for two reasons:

1.) Useing such arrangements for regulations causes extreme amounts of audio noise which degrade the performance of the amplifier: and of such an arrangement for regulation causes the modulator 40 to put out P.W.M. which is not a square wave.

The logic output of the and gate of isolator OP41 is connected through lead 48 to capacitor C48 to the pulse width modulator 40 as previously described. The output drives the modulator 40 to sychronize operation

of modulator 40 with the clock input 68 from the clock system described hereinafter. A resistor R48 is provided in the output 51 to act as a pullup while capacitor c48 is provided as a differentiating capacitor to generate samll spikes.

It has been found in accordance with one feature of the present invention that precise output voltage control with varying load can be achieved principally because the drive to the primary of the transformer is a square wave. It has further been unexpectedly found that the output voltages at terminals 53-54 generated by secondary S2 and supplied through a standard rectifier circuit RC2T with voltage regulators VR1, VR2 are regulated, with very little loss in the regulators because of the close control of the input voltage 54, 55.

Figure 2 is a flow chart illustration of an example of an amplifier device within the scope of the present invention to provide a general understanding of one example of a device within the scope of the present invention.

A more detailed description of one example of a device within the scope of the present invention is shown in Figures 3A-3C. In Figure 2 an audio signal AD is provided to an amplifier circuit 60 which provides an amplified audio signal 69. Signal 69 is supplied to a digital attenuator 70 which attenuates the signal,

for example, in a binary mode, that is 1dB, 2dB, 4, 8, 16, 32. etc. up to 63dB in 1dB steps. The attenuated output signal 79 is supplied to a buffer 80 which then supplies a buffered signal 89 to a high pass, low pass filter combination 90, (which can be a multiple order filter) to supply a filtered attenuated signal 99 of selected characteristics.

Signal 99 is supplied to modulator 100 which converts the alternating signal to a pulse width modulated signal M which is reflective of the characteristics of the output signal 226 from the device as described hereinafter. The output M from modulator 100 is then supplied to a gating system 110 which generates a 4 phase output Q1, Q2, Q3, Q4, then to drivers 120, 121, 130, 131 to generate signals 129, 139 which is utilized to drive the primary coils P3, P4 of transformers T3 and T4 . The secondary coils 53A, 53B, 54A, 54B are connected in a 4 phase mode operated at a rate determined by the characteristics of output drivers 140, 160, 180, 200 to supply alternating power to a load L. A feedback signal 226 is supplied from filter circuit 210 to modulator 100 to indicate loading on the circuit. Signal 226 is also supplied to a clipper circuit 220 which supplies an output signal 225 to the filter output 99 to override or clip the audio signal in the event the signal indicates a load exceeding a selected load limit as well as an input

signal exceeding a selected input level, as described hereinafter.

Referring now to Figure 3A which illustrates example of an attenuator and amplifier system useful within the scope of the present invention an amplifier A60 is connected in a differential mode to input AD through coupling capacitors C21, C22 and adjusting resistors R21, R22 to supply a signal 23 to a signal attenuation switch network 24. The switch network consists of a number of solid state switches SW1-SW6, SW1B-SW6B cooperatively connected to switches SW1A-SW6A which in the example are manual switches to operate the solid state switches SW1-SW6 by means of inverting buffers B1-B6 but it will be understood that other means such as programmable controllers can also be used.

Resistor ladders (R1A-R6A), (R1B-R6B) (R1C-R6C) are provided and sized so that binary attenuation is provided by appropriate adjustment of the switch SW1A-SW6A positions to attenuate the signal in a binary format. That is, switch SW1A introduces a one dB change in characteristics while switch SW2A introduces a change of 2 dB, switch SW3A introduces a change of 4 dB and so on until switch SW6A introduce a change of 32 dB so that by proper selection of the switches any decibel(dB) attenuation between 0 and 63 can be

provided to supply a selectively attenuated signal 31 at the output.

Attenuated signal 31 is supplied through a network terminating resistor R31 to signal buffer circuit including an operational amplifier A2 with negative feedback loop having a resistor R32. The buffered signal 32 is then supplied through a series of high-pass low-pass amplifier systems as shown where RC pairs R3(A-E); R5(A-E) and C3(A-E); C5(A-E)are provided along with operational amplifiers A3-A5 each with a feedback loops respectively to define three high pass-low pass filter networks. The signal 33 from amp A5 is supplied to a final filter including an amplifier A6 and resistors R33, R6A and capacitors C6E, C6A, C6B, C6E in feedback loops provided so that overall an eight order low pass filter and a seventh order high pass filter is provided.

It has been found that by the use of only four operational amplifiers a multistage filter arrangement can be provided which would require the use of many more operational amplifiers in conventional practice.

Thus, a filtered attenuated audio signal J is provided from the filter network.

Figure 3A-36 also illustrate another feature of the present invention namely a clipping circuit operated by signal 225 from an LC filter 210 in the load output as shown in Figure 2 and 3C which operates

the clipping circuit 220 to supply the signal 225 in direct response to the load. As shown in Figure 3C clipping circuit power is supplied from a power tap S4 where an input voltage, for example plus 150 volts is supplied from the output of a terminal of the power supply previously described. A voltage regulator RF3 is provided to supply an output signal 226 which is filtered by means of a RC filter R15-C15 to the base of a transistor Q221 which drives an opto isolator OP220A in responce to signal from R16 having its collector supplied by voltage source S4. The emitter 72 of opto isolator OP220 is then supplied to an adjusting circuit including an op-amp A7 to operate as a DC bias eliminator to adjust the signal to keep the transistor of opto coupler OP220 at "0" volts, while still passing audio in a linear manner.

The emitter 72 of the opto coupler OP220 provides an adjusted AC signal 225 directly proportional to the current through the load L and in response to the signal 226 received from filter 210.

It has been found that the cost of the circuit of an equivalent type described above would be greatly in excess of the cost of the arrangment shown.

The signal 225 is directly proportional to the current through the load and is supplied through adjusting potentiometer P3 to op-amps A8, A9, of Figure 3A connected as a full wave rectifier to generate

rectified signal 74 indicative of the loading which is supplied op-amp A9 which supplies a signal F which is indicative of loading on the unit.

A signal present indicator is also provided by means of amplifier A10 which gates transistor Q11 in the preence of a load signal to turn on light emitting diode LED 11.

The signal F from the output of the amplifier A11 is supplied to an amplifier A15 having an output AF to be supplied to the base of a transistor Q20.

A potentiometer P223 is provided to adjust a voltage reference VR 220 to adjust the operational amplifier A11 which determines the level at which the current to load L is to be clipped as described hereinafter where the signal 74, 75 is provided to one input of operational amplifier A11 connected as differential amplifier having its second input from voltage reference VR 220 for example a part No. LN317 adjusted by means of a potentiometer P223 to adjust the reference signal to adjust output F from the operational amplifier A11. Potentiometer P223 sets the voltage clipping level and the signal F is supplied to an amplifier A13 to supply an inverted signal -F to an amplifier A14 and the signal F is supplied to amplifier A15. The op-amps A14, A15 are operated in voltage bias mode across the audio signal J where the reference for the inverting amplifiers is supplied from audio signal

J through resistors R71, R72 with clamping diodes D5-D8, provided as shown. The adjusted reference voltage -AF is supplied to adjust the signal J while the signal AF is supplied to the emitter of a transistor Q3 having its collector supplied from a voltage source S6 through a light emitting diode LED 2 and the transistor base operated by the audio signal J. Output signal -AF is then connected to the audio channel signal to provide signal which is the combined effect of the audio signal and reference signal F. If the combined signal is in excess of the voltage necessary to gate the signal J is then increased to clip power as described hereinafter. Diodes D5, D7 block the reference signals F, -F from the audio signal unless the audio exceeds the value of F or -F then they conduct the output of op-amps A15, A13 to clip the audio at the value of reference F or -F. The transistor Q20 is in series with diode D7 and is turned on any time D7 is conducting.

In the arrangement shown if the audio channel voltage exceeds J selected limits the appropriate diode clamps the audio channel voltage at the reference before it can exceed the permissible band and limits the load current as described hereinafter as shown in Figure 3B. The signal J is supplied to the inputs of op-amps A16 and A17 which supply inverted and balanced outputs K and L as inputs to op-amps A18, A19 connected

as integrators. The integrators are clocked by means of a pair of exclusive "OR" gates OR1, OR2 so signals M and N are provided at the outputs. The input to the integrators A18, A19 is further modified by negative feedback 274, 276 from load L as shown in Figure 2. The feedback loops for op-amps A18, A19 including resistors R48, R47 and capacitors C25, C27 assist in converting the audio signal to a pulse width modified signal shown in Figure 4. It has been found that the arrangment shown creates generally flat audio response signals M, N to supplied the input of comparator A20 to generate a signal "0".

Under all normal operating conditions signal F is fixed at a setting which will clip the audio at a selected input level. If the maximum load current is exceeded the signal 74 will exceed this reference F and only then will it cause signal F to reduce and in turn reduce the input clipping level.

The signal O is applied to "OR" gates OR3, OR4 where the second input of "OR" gate OR3 is grounded and the second input of "OR" gates OR4, OR5 is from a voltage reference S8. The second input to "OR" gates OR5, OR6 is from a clock CL101 which includes OR gates OR7, or OR8 driven by a timer T1 with appropriate adjustment. The outputs from the "OR" gate, starting with "OR" gate OR110 are as follows where "OR" means exclusive "OR" Gates:

ORGATE	OUTPUT
OR6	Clock
OR5	Not Clock
OR4	Not Data
OR3	Data

This arrangement of using exclusive "OR" gates to invert a signal provides an output signal that is the exact compliment of the inverted signal, without any time delay or phase shift between outputs, as there would be if an inverter were used.

Thus it can be seen that the outputs are sequenced directly with each other. Each of the outputs is connected to a corresponding Nand Gate N1-N4. A delay is built into the switching of NAND Gate 1 and 4 by means of the inherent capacitance of the gate and the use of resistors R85, R86 which define an RC time constant. Gates N1 through N5 are provided and the connection is as shown so, for example, the "OR" gate OR6 is connected to NAND Gate N4 and N2 So, NAND Gate N4 is clocked by "OR" gate OR6 and receives data from "OR" gate OR4 while NAND Gate 2 receives its data from "OR" gate OR3. Likewise NAND Gate N2 receives clock data from "OR" gate OR6 and its data from "OR" gate OR3. Inverting buffers B1-B4 are provided as shown to supply the outputs signals as shown to the bases of transistors Q13-Q20.

It can be developed that the output from the buffers B1-B4 drive the Mosfets Q13-Q20 which are paired to be connected to the primaries P2-P3 of transformers T4 and T5 so that the buffers cycle on and off to the primary coils. That is the current from primary P2 is slightly delayed to prevent overlap with the signal from primary 1 which is operated by the outputs from buffers B1, B2. Operation of the units is cycled in order to provide the push-pull characteristics necessary to operate secondaries S1-S4 of transformer T4-T5 provided to be operated by the primary P2, P3 as shown. Appropriate rectifiers circuits are F1-F4 associated with the secondaries 51-54 to operate "OR" gates OR9-OR12 and the outputs 161-164; 171-174; 181-184; and 191-194 to operate drive circuits DR1-DR4 utilizing quad OR gates OR13-OR24 as shown which in turn operate MOSFETS Q21-Q28 which, respectively operate MOSFETS Q29-Q32 where the MOSFETS (Q21, Q22), (Q23, Q24), (Q25, Q26) and (Q27,Q28) are tied together and the MOSFETS 29-Q32 are tied together as are MOSFETS Q30, Q31 to supply AC power to load L, through a filter 210 for example a notch filter as known in the art.

It will be understood that the foregoing is but one arrangement within the scope of the present invention and that various other arrangements also within the scope of the present invention will occur to

those skilled in the art upon reading the disclosure set forth hereinafter.

CLAIMS OF THE INVENTION

The invention claimed is:

CLAIM 1

The audio amplifier system including attenuator means to receive an audio signal and selectively attenuate said signal; modulator means to convert said attenuated signal to square wave signal having a pulse width as a function of the level of the audio signal; Push-pull converter means to receive said square wave signal and to generate alternating current signal means; Transformer means to receive said alternating current signal and provide amplified output signal in response thereto to load means.

CLAIM 2

The invention of Claim 1 including clipper means to sense the amplified output signal into to adust said input audio signal in response to selected values of said output signals.

CLAIM 3

The invention of Claim 1 including buffer means to receive said attenuated signal and selectively condition said signal and supply said signal to said modulator means.

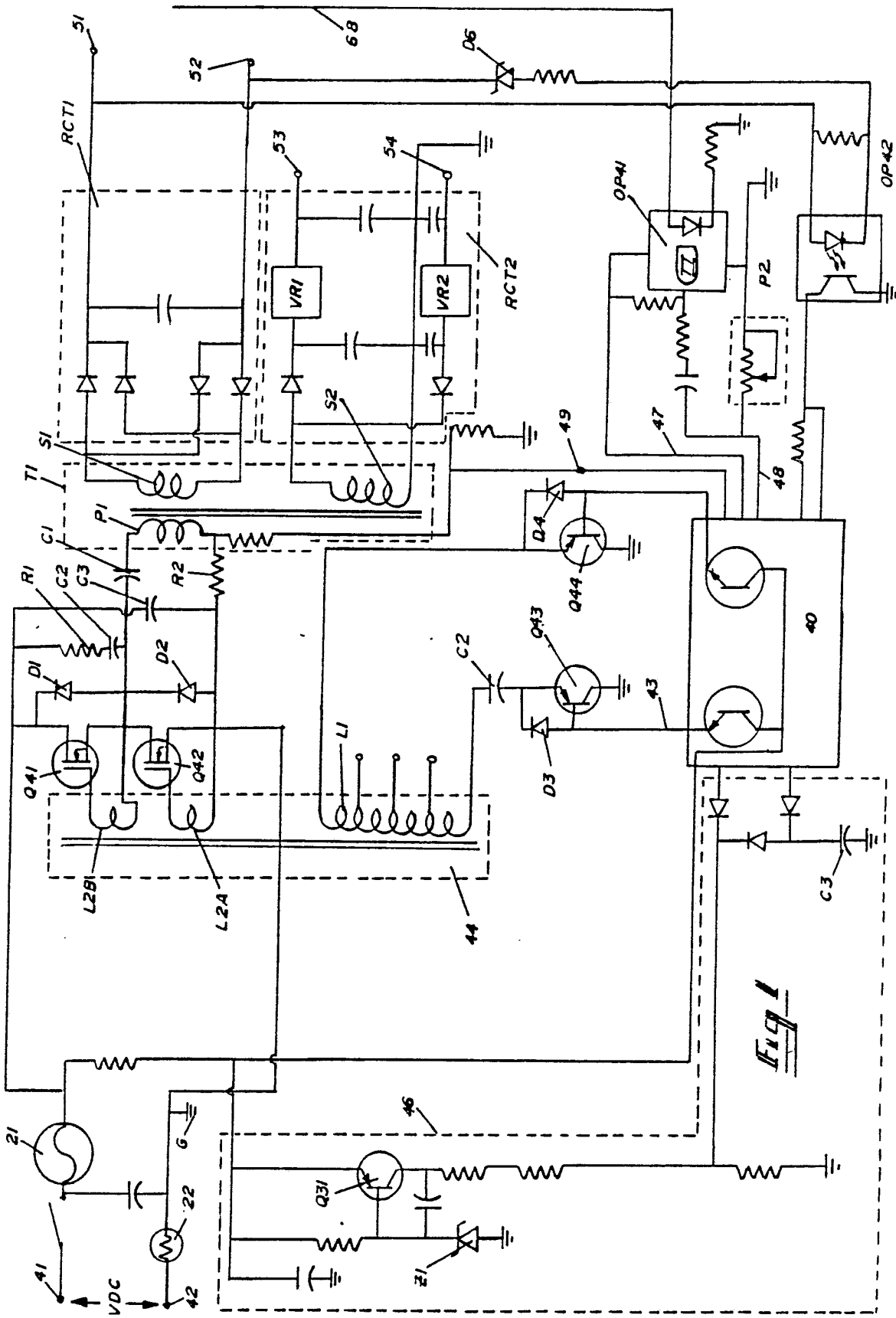
51
52
68
D6
RCT1
53
54
VR1
VR2
RCT2
OP41
OP42
P2
S2
S1
T1
49
47
48
P1
C1
R1
C2
C3
R2
D1
D2
D4
Q44
Q43
40
C2
43
D3
Q41
Q42
L1
L2B
L2A
44
C3
46
21
G
22
Q31
Z1
41
VDC
42

Fig 1

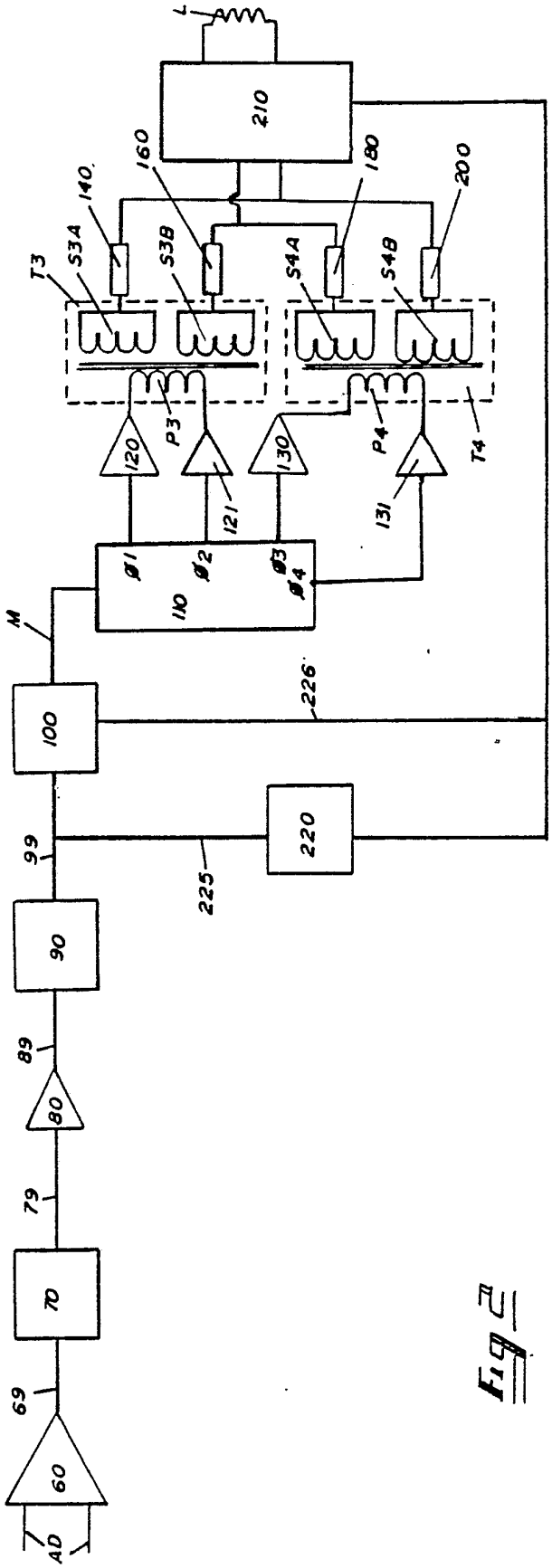
L
210
160
180
200
140
S34
S38
S44
S48
T3
P3
P4
T4
120
130
121
131
Ø1
Ø2
Ø3
Ø4
110
M
226
100
220
99
225
90
89
80
79
70
69
60
40

Fig 2

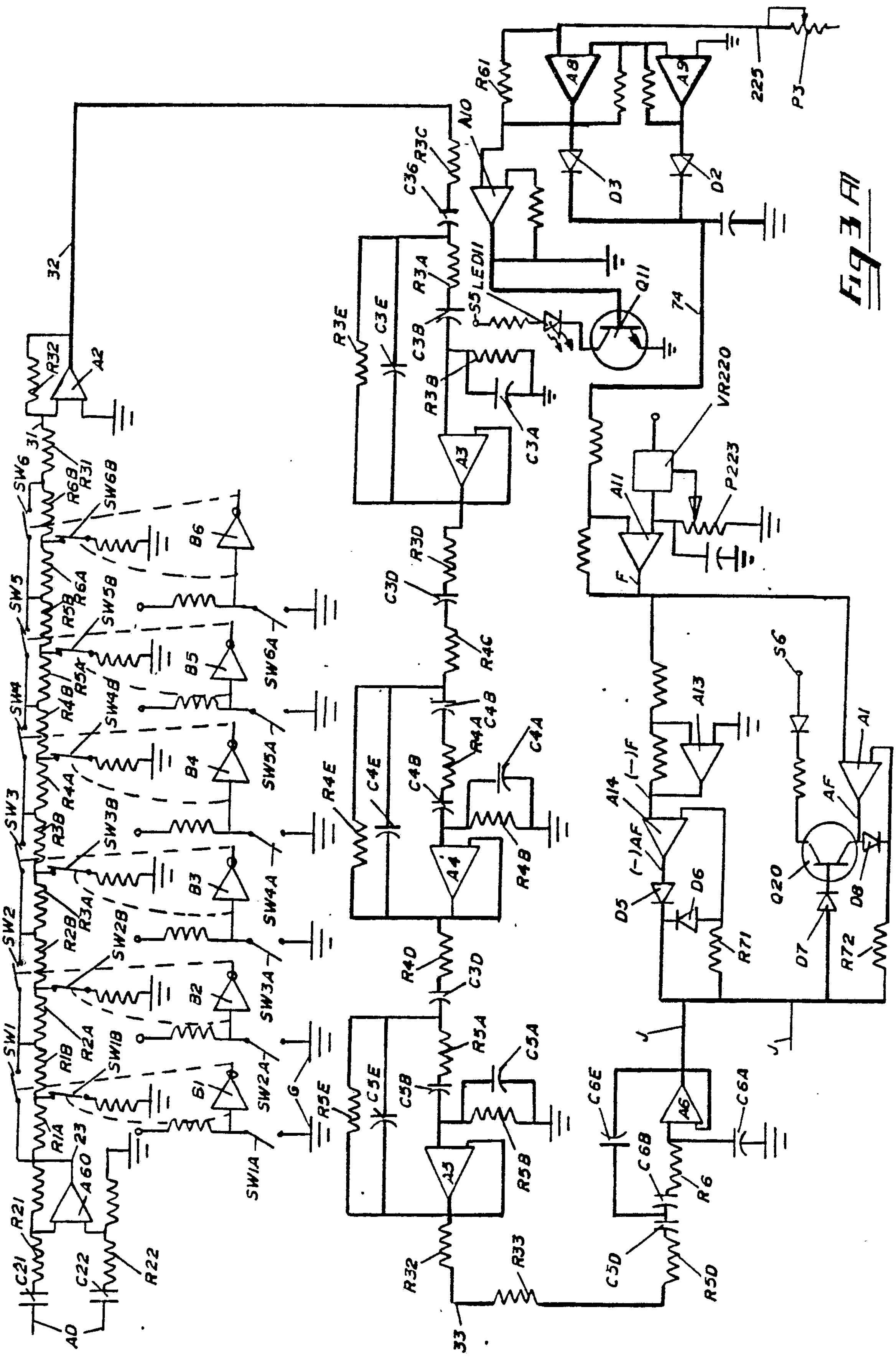
R21
C21
C22
R22
AD
A60
23
R1A
R1B
R2A
R2B
R3A
R3B
R4A
R4B
R5A
R5B
R6A
R6B
R31
31
R32
A2
32
SW1
SW2
SW3
SW4
SW5
SW6
SW1A
SW2A
SW3A
SW4A
SW5A
SW6A
SW1B
SW2B
SW3B
SW4B
SW5B
SW6B
B1
B2
B3
B4
B5
B6
G
R5E
C5E
C5B
C5A
A5
R5B
R4D
C3D
R4E
C4E
C4B
C4A
R4A
A4
R4B
R4C
R3D
A3
R3E
C3E
C3B
R3A
R3B
C3A
C36
R3C
A10
S5
LED11
Q11
74
R61
A8
A9
D3
D2
225
P3
VR220
P223
A11
F
A13
(−)F
A14
(−)AF
D5
D6
R71
S6
AF
A1
Q20
D7
D8
R72
J
C6E
C6A
A6
C6B
R6
C5D
R5D
R32
R33
33

Fig 3A

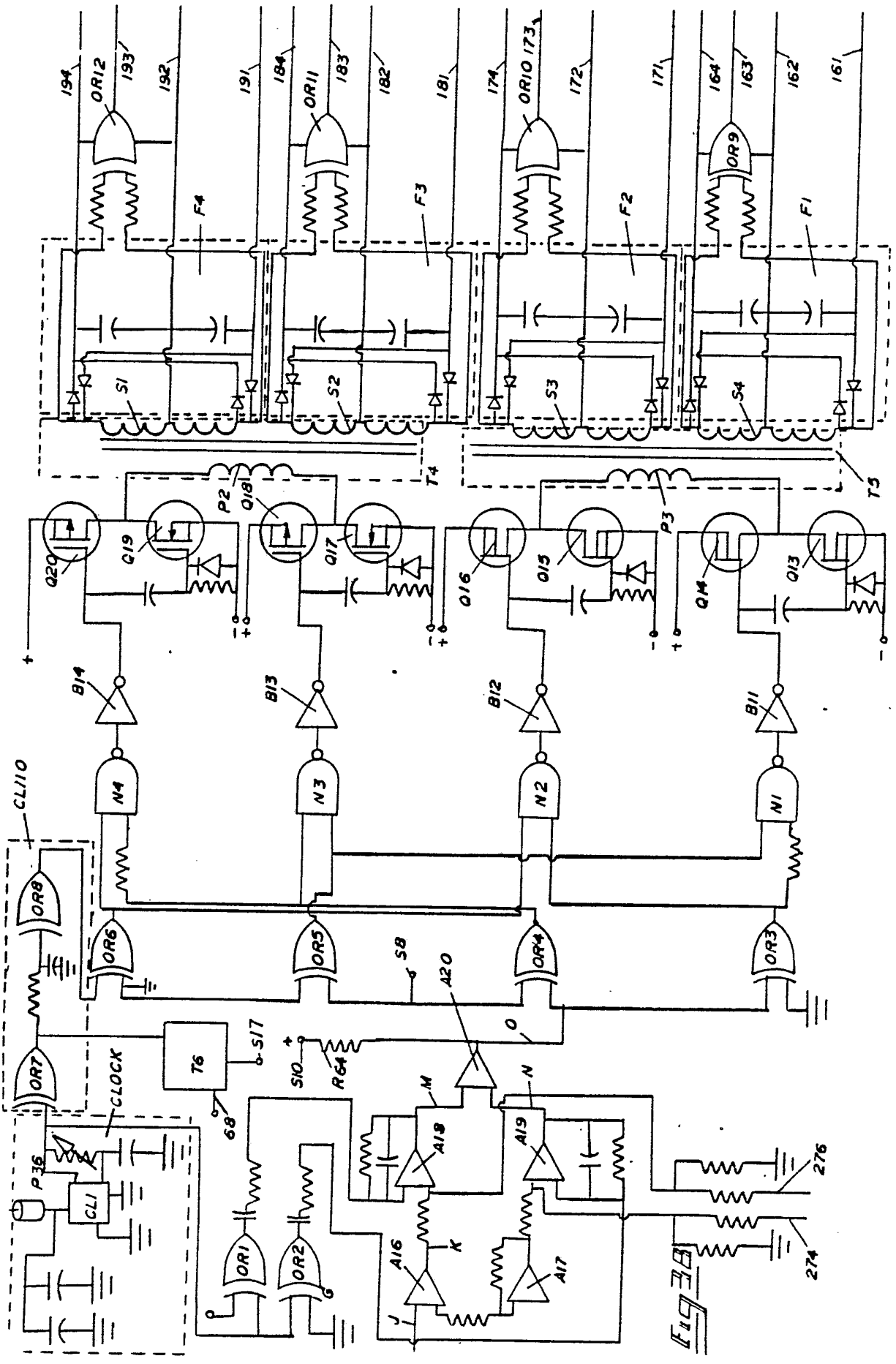
194
OR12
193
192
191
184
OR11
183
182
181
174
OR10 173
172
171
164
163
162
161
OR9
F4
F3
F2
F1
S1
S2
S3
S4
T4
T5
P2
Q18
P3
Q20
Q19
Q17
Q16
Q15
Q14
Q13
B14
B13
B12
B11
N4
N3
N2
N1
CL110
OR8
OR6
OR5
S8
A20
OR4
OR3
O
OR7
T6
S17
S10
R64
CLOCK
68
M
N
A18
A19
276
P36
CL1
OR1
OR2
A16
K
A17
J
274

Fig 3B

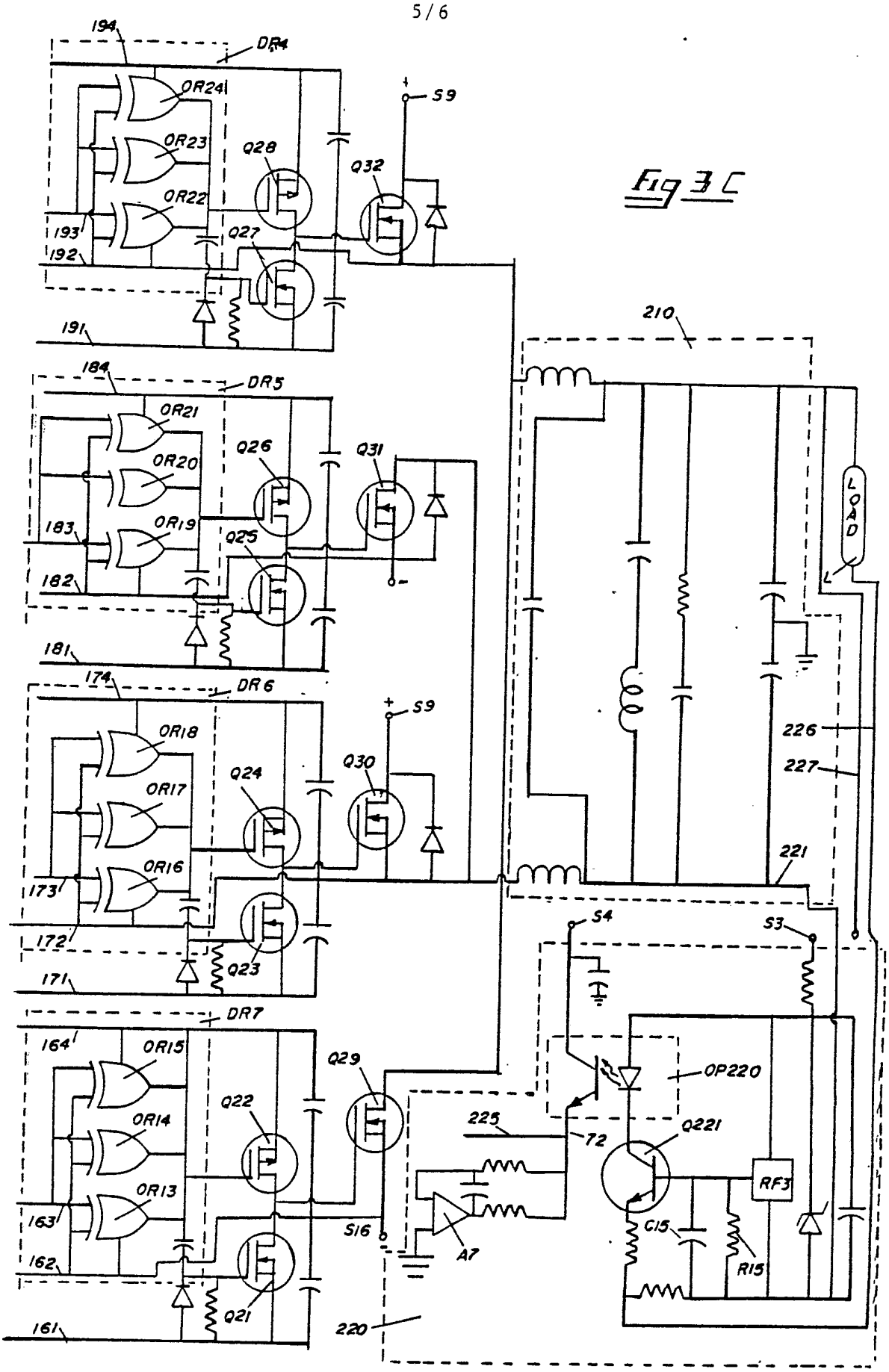
194
DR4
OR24
OR23
OR22
193
192
191
Q28
Q27
Q32
S9
184
DR5
OR21
OR20
OR19
183
182
181
Q26
Q25
Q31
174
DR6
OR18
OR17
OR16
173
172
171
Q24
Q23
Q30
S9
164
DR7
OR15
OR14
OR13
163
162
161
Q22
Q21
Q29
S16
210
LOAD
226
227
221
S4
S3
OP220
Q221
225
72
RF3
C15
R15
A7
220

Fig 3C

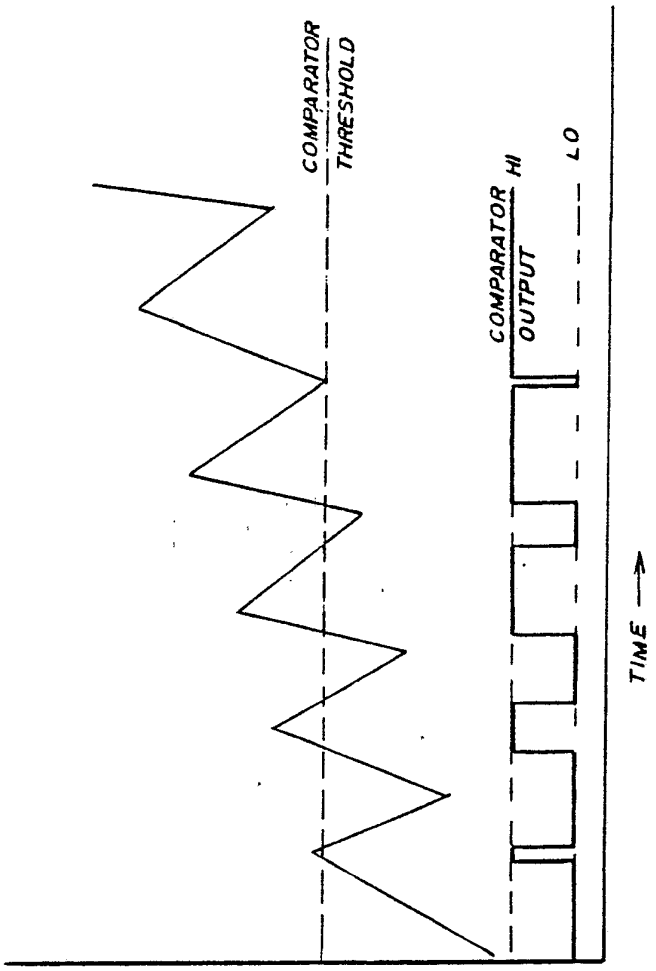

Fig 4

INTERNATIONAL SEARCH REPORT

International Application No PCT/US86/01494

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all)[3]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC(4): H03F 3/38

U.S. CL.: 381/120; 330/10

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
U.S.	381/120, 28; 330/10, 207A, 251

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
A	US,A, 4,201,886 (Nagel) 06 May 1980. See the entire document	1-3
A	US,A, 4,209,781 (Puel) 24 June 1980. See the entire document	1-3
A	US,A, 4,360,707 (Joseph) 23 November 1982. See entire document	1
A	US,A, 4,041,408 (Trotnick, Jr.) 09 August 1977. See entire document.	1
A	JP,A, 58-133044 (Matsushita Denki Sangyo) 08 August 1983. See entire document	1-3
A	JP,A, 58-133043 (Matsushita Denki Sangyo) 08 August 1983. See entire document	1-3
A	US,A, 4,390,849 (Miskin) 28 June 1983. See entire document.	1-3
A	US,A, 4,476,436 (Koizumi) 09 October 1984. See entire document.	1-3

* Special categories of cited documents: [15]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
26 September 1986	03 OCT 1986
International Searching Authority [1]	**Signature of Authorized Officer [20]**
ISA/US	L.C.Schroeder

FURTHER INFORMATION CONTINUED FROM THE SECOND SHEET

A	US,A, 4,504,793 (Yokoyama) 12 March 1985. See entire document.	1-3
A	US,A, 4,531,096 (Yokoyama) 23 July 1985. See entire document.	1-3
A	US,A, 4,554,512 (Aiello) 19 November 1985. See entire document.	1-3
A	US,A, 4,573,018 (Mirow) 25 February 1986. See entire document.	1-3

V. ☐ OBSERVATIONS WHERE CERTAIN CLAIMS WERE FOUND UNSEARCHABLE [10]

This international search report has not been established in respect of certain claims under Article 17(2) (a) for the following reasons:

1. ☐ Claim numbers ..... , because they relate to subject matter [12] not required to be searched by this Authority, namely:

2. ☐ Claim numbers ..... , because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out [13], specifically:

VI. ☐ OBSERVATIONS WHERE UNITY OF INVENTION IS LACKING [11]

This International Searching Authority found multiple inventions in this international application as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims of the international application.

2. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims of the international application for which fees were paid, specifically claims:

3. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claim numbers:

4. ☐ As all searchable claims could be searched without effort justifying an additional fee, the International Searching Authority did not invite payment of any additional fee.

Remark on Protest

☐ The additional search fees were accompanied by applicant's protest.

☐ No protest accompanied the payment of additional search fees.