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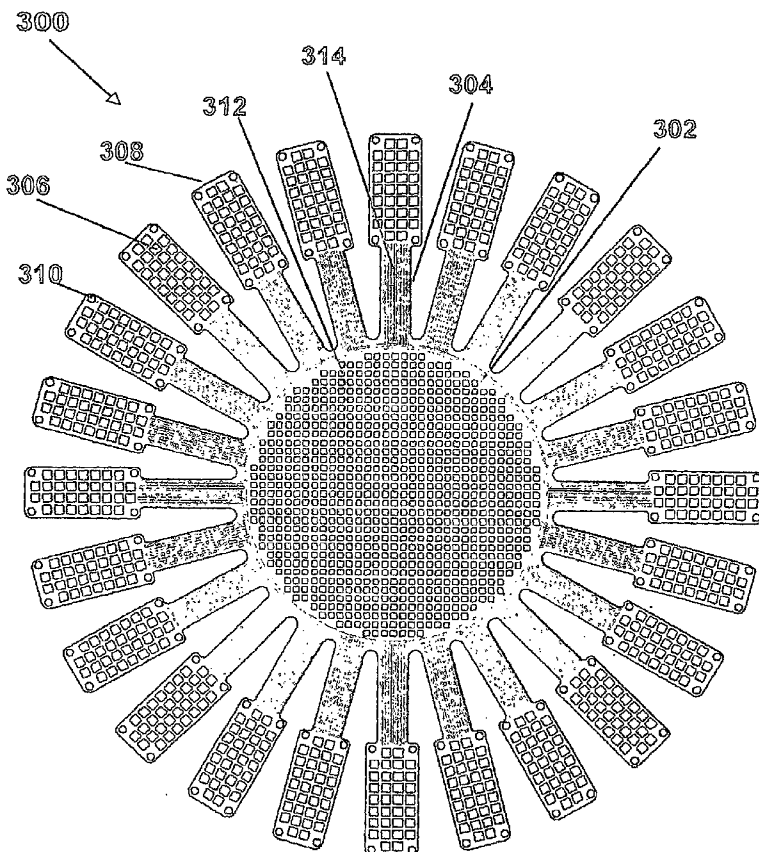
(54) Title: METHOD AND APPARATUS FOR FIXED-FORM MULTI-PLANAR EXTENSION OF ELECTRICAL CONDUCTORS BEYOND THE MARGINS OF A SUBSTRATE



(57) Abstract: An apparatus, suitable for coupling a pads of integrated circuits on wafer to the pogo pins of a pogo tower in a test system without the need of a probe card, includes a body having a first surface and a second surface, the body having a substantially circular central portion, and a plurality of bendable arms extending outwardly from the central portion, each bendable arm having a connector tab disposed at the distal end thereof; a first plurality of contact terminals disposed on the second surface of the central portion of the body, the first plurality of contact terminals arranged in pattern to match the layout of pads on a wafer to be contacted; at least one contact terminal disposed on the first surface of the plurality of connector tabs; and a plurality of electrically conductive pathways disposed in the body such that each of the first plurality of contact terminals is electrically connected to a corresponding one of the contact terminals on the first surface of the connector tabs.

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METHOD AND APPARATUS FOR FIXED-FORM MULTI-PLANAR EXTENSION OF ELECTRICAL CONDUCTORS BEYOND THE MARGINS OF A SUBSTRATE

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Field of the Invention

The present invention relates generally to semiconductor test equipment, and more particularly relates to methods and apparatus for routing electrical conductors to and from integrated circuits, microelectromechanical devices (MEMs), or similar
10 structures in a test environment.

Background

Advances in semiconductor manufacturing technology have resulted in, among other things, reducing the cost of sophisticated electronics to the extent that integrated
15 circuits have become ubiquitous in the modern environment.

As is well-known, integrated circuits are typically manufactured in batches, and these batches usually contain a plurality of semiconductor wafers within and upon which integrated circuits are formed through a variety of semiconductor manufacturing steps, including, for example, depositing, masking, patterning, implanting, etching, and so on.

20 Completed wafers are tested to determine which die, or integrated circuits, on the wafer are capable of operating according to predetermined specifications. In this way, integrated circuits that cannot perform as desired are not packaged, or otherwise incorporated into finished products.

It is common to manufacture integrated circuits on roughly circular semiconductor
25 substrates, or wafers. Further, it is common to form such integrated circuits so that conductive regions disposed on, or close to, the uppermost layers of the integrated circuits are available to act as terminals for connection to various electrical elements disposed in, or on, the lower layers of those integrated circuits. In testing, these conductive regions are commonly contacted with a probe card.

30 The maintenance of probe tip accuracy, good signal integrity, and overall dimensional accuracy severely strains even the best of these highly developed

fabrication methods because of the multiple component and assembly error budget entries.

What is needed are lower-cost, less-complex apparatus and methods to increase test efficiency.

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Summary of the Invention

Briefly, an apparatus, suitable for coupling a pads of integrated circuits on wafer to the pogo pins of a pogo tower in a test system without the need of a probe card, includes a body having a first surface and a second surface, the body having a

10 substantially circular central portion, and a plurality of bendable arms extending outwardly from the central portion, each bendable arm having a connector tab disposed at the distal end thereof; a first plurality of contact terminals disposed on the second surface of the central portion of the body, the first plurality of contact terminals arranged in pattern to match the layout of pads on a wafer to be contacted; at least one contact

15 terminal disposed on the first surface of the plurality of connector tabs; and a plurality of electrically conductive pathways disposed in the body such that each of the first plurality of contact terminals is electrically connected to a corresponding one of the contact terminals on the first surface of the connector tabs.

20

Brief Description of the Drawings

Fig. 1 is a cross-sectional representation of a common probe card/test head configuration.

Fig. 2 is a cross-sectional representation of a fixed form, multi-planar edge-extended wafer translator, mounted for use within a test assembly.

25 Fig. 3 is a top-view representation of an embodiment of a fixed form, multi-planar edge-extended wafer translator prior to bending.

Fig. 4 is a close-in top view of a section of a fixed form, multi-planar edge-extended wafer translator prior to bending.

Fig. 5 is a three-dimensional representation of an embodiment of a fixed form, multi-planar edge-extended wafer translator bent to conform to a metal reinforcing structure, viewed from above.

Fig. 6 is a sectional three-dimensional representation of an embodiment of a fixed form, multi-planar edge-extended wafer translator bent to conform to a metal reinforcing structure, viewed from below.

Fig. 7 is a cross-sectional representation of a segment of a wafer in contact with a fixed form, multi-planar edge-extended wafer translator, indicating the disposition of wire paths.

Fig. 8 is a cross-sectional representation of an alternative embodiment of a fixed form, multi-planar edge-extended wafer translator.

Detailed Description

Generally, an apparatus provides electrical pathways between pads of unsingulated integrated circuits and pogo pins disposed in a pogo tower of a semiconductor test system without the need of a probe card.

Reference herein to "one embodiment", "an embodiment", or similar formulations, means that a particular feature, structure, operation, or characteristic described in connection with the embodiment, is included in at least one embodiment of the present invention. Thus, the appearances of such phrases or formulations herein are not necessarily all referring to the same embodiment. Furthermore, various particular features, structures, operations, or characteristics may be combined in any suitable manner in one or more embodiments.

Terminology

Reference herein to "circuit boards", unless otherwise noted, is intended to include any type of substrate upon which circuits may be placed. For example, such substrates may be rigid or flexible, ceramic, flex, epoxy, FR4, or any other suitable material.

Pad refers to a metallized region of the surface of an integrated circuit, which is used to form a physical connection terminal for communicating signals to and/or from the integrated circuit.

The expression "wafer translator" refers to an apparatus facilitating the
5 connection of pads (sometimes referred to as terminals, I/O pads, contact pads, bond pads, bonding pads, chip pads, test pads, or similar formulations) of unsingulated integrated circuits, to other electrical components. It will be appreciated that "I/O pads" is a general term, and that the present invention is not limited with regard to whether a particular pad of an integrated circuit is part of an input, output, or input/output circuit. A
10 wafer translator is typically disposed between a wafer and other electrical components, and/or electrical connection pathways. The wafer translator is typically removably attached to the wafer (alternatively the wafer is removably attached to the translator). The wafer translator includes a substrate having two major surfaces, each surface having terminals disposed thereon, and electrical pathways disposed through the
15 substrate to provide for electrical continuity between at least one terminal on a first surface and at least one terminal on a second surface. The wafer-side of the wafer translator has a pattern of terminals that matches the layout of at least a portion of the pads of the integrated circuits on the wafer. The wafer translator, when disposed between a wafer and other electrical components such as an inquiry system interface,
20 makes electrical contact with one or more pads of a plurality of integrated circuits on the wafer, providing an electrical pathway therethrough to the other electrical components. The wafer translator is a structure that is used to achieve electrical connection between one or more electrical terminals that have been fabricated at a first scale, or dimension, and a corresponding set of electrical terminals that have been fabricated at a second
25 scale, or dimension. The wafer translator provides an electrical bridge between the smallest features in one technology (e.g., pins of a probe card) and the largest features in another technology (e.g., bonding pads of an integrated circuit). For convenience, wafer translator is referred to simply as translator where there is no ambiguity as to its intended meaning. In some embodiments a flexible wafer translator offers compliance
30 to the surface of a wafer mounted on a rigid support, while in other embodiments, a wafer offers compliance to a rigid wafer translator. The surface of the translator that is

configured to face the wafer in operation is referred to as the wafer-side of the translator. The surface of the translator that is configured to face away from the wafer is referred to as the inquiry-side of the translator. An alternative expression for inquiry-side is tester-side.

5 The expression "edge extended wafer translator" refers to an embodiment of a translator in which electrical pathways disposed in and/or on the translator lead from terminals, which in use contact the wafer under test, to electrical terminals disposed outside of a circumferential edge of a wafer aligned for connection with, or attached to the edge extended translator.

10 The expression "translated wafer" refers to a wafer that has a wafer translator attached thereto, wherein a predetermined portion of, or all of, the contact pads of the integrated circuits on the wafer are in electrical contact with corresponding electrical connection means disposed on the wafer side of the translator. Typically, the wafer translator is removably attached to the wafer. Removable attachment may be achieved,
15 for example, by means of vacuum, or pressure differential, attachment.

The terms die, chip, integrated circuit, semiconductor device, and microelectronic device are sometimes used interchangeably in this field. The present invention relates to the manufacture and test of chips, integrated circuits, semiconductor devices and microelectronic devices as these terms are commonly understood in the field.

20 Fig. 1 is a cross-sectional representation of a common probe card/test head configuration **100**. Test head pin electronics board **102** with attached pogo pin interface **104** contacts load board **106**. Double ended pogo pins **108** housed in pogo tower **112** contact the lowermost surface of load board **106** and the uppermost surface of probe card **110**. Metal reinforcement, or "spider," **114** attaches probe card **110** to pogo tower
25 **112**. Connector **116** provides electrical contact between probe card **110** and probe points **118**, which are available to contact a device under test (DUT).

Fig. 2 is a cross-sectional representation of an embodiment of a fixed form, multi-planar edge extended wafer translator **200**, connected to pogo tower **112** within a test assembly. Fixed form, multi-planar edge extended wafer translator **200** is bent to
30 conform to the profile of metal reinforcing fixture **208**. Reinforcing fixture **208** brings the

extended edge of fixed form, multi-planar edge extended wafer translator **200** into contact with pogo pins **108**. Wafer **204** is mounted on wafer chuck **206**. The uppermost surface of wafer **204** is brought into contact with probe point array **202**, on the wafer-side of fixed form, multi-planar edge-extended wafer translator **200**, by means of a
5 pressure differential between a space between the wafer and wafer-side of wafer translator **200**, and the atmosphere outside that space. In some embodiments, a gasket **210**. is disposed between wafer translator **200** and wafer **204**. In some embodiments, a groove is provided in wafer translator **200** to receive an O-ring, and the O-ring serves to form a substantially gas-tight seal between the wafer and the wafer translator when the
10 two are pressed into contact.

Fig. 3 is a top-view representation of a fixed form, multi-planar edge-extended wafer translator **300** prior to bending. Bendable connectors **304**, printed with wire paths **314**, provide electrical connections to and from wafer translator **302**, and to and from connector tabs **308**. The bendable connectors may be referred to bendable arms, or
15 flexible arms. Perforations **310** in connector tabs **308** provide for mechanical alignment and attachment to a mounting fixture as pictured in Figs. 1 and 2. A plurality of electrically conductive pads **306** are disposed on connector tabs **308**. A plurality of conductive pads **312** are disposed on the upper surface of translator **302**.

Fig. 4 is a close-in top view of a section of a fixed form, multi-planar edge
20 extended wafer translator in accordance with the present invention. Perforations **310** in connector tabs **308** allow for alignment and attachment to a mounting fixture (as pictured in Figs. 1 and 2). Perforations may also be referred to as holes. A plurality of electrically conductive pads **306** are disposed on the surface of connector tab **308**. In this embodiment, wire paths **314** printed on bendable connectors **304** convey signals
25 between conductive pads **306** and pads disposed on the underside of translator **302** (as pictured in Figs. 1 and 2). A plurality of electrically conductive pads **312** are disposed on the surface of translator **302**, and electrically connected to a plurality of conductive pads on the underside of translator **302** by wire paths disposed within translator **302**.

Fig. 5 is a three-dimensional representation of a fixed form, multi-planar edge
30 extended wafer translator bent to conform to a metal reinforcing structure, viewed from

above. Fig. 5 shows a central portion that acts as a wafer translator **302**, bendable arms **304**, connector tabs **308** and perforations **310**. It is noted that the present invention may be implemented as a central wafer translator with bendable arms attached to the central wafer translator and extending outwardly therefrom, and connector tabs attached to the
5 distal ends of the bendable arms. Alternatively, the present invention may be implemented as a unitary body.

Fig. 6 is a sectional three-dimensional representation of an embodiment of an FFMP translator bent to conform to a metal reinforcing structure, viewed from below. The representation includes a wafer translator **302**, bendable connectors **304**, connector
10 tabs **308** and perforations **310**.

Fig. 7 is a cross-sectional representation of a segment of a wafer **204** in contact with a wafer translator **302**, indicating the disposition of wire paths **722** and **704** in an embodiment of an FFMP translator. In this embodiment, pads **726**, disposed on the underside of translator **302**, are connected to pads **708** on the upper surface of
15 translator **302** by wire paths **722**. Pads **724**, disposed on the underside of translator **302**, contacted by wire paths **704**, which may conduct signals to and from electrically conductive pads disposed beyond the circumferential margin of wafer **114**, as seen in Figs. 2-7.

Fig. 8 is a cross sectional representation of an alternative embodiment of an
20 FFMP translator **800** and mounting fixture **802** in contact with a test head pin electronics board **102** with attached pogo pin interface **104**. In this embodiment, electrically conductive pads **804** disposed on the extended edge of FFMP translator **800** directly contact the pin electronics' pogo pins without an intervening pogo tower.

The edge-extended wafer translator, as illustrated in Figs. 2-7, provides the
25 electrical interface between the translated wafer and a test system (not shown). Such a test system may provide power and signals to the device under test, and may further receive signals from the device under test. Such a system may alternatively serve to plug a wafer full of processors into a computer system; mesh routing may be facilitated by edge-extended wafer translators.

It will be appreciated that the ability to lead contact arrays off the wafer in various configurations allows for a range of alternative embodiments beyond those represented in Figs. 1-7.

In one embodiment, an apparatus includes a body having a first surface and a second surface, the body having a substantially circular central portion, and a plurality of bendable arms extending outwardly from the central portion, each bendable arm having a connector tab disposed at the distal end thereof; a first plurality of contact terminals disposed on the second surface of the central portion of the body, the first plurality of contact terminals arranged in pattern to match the layout of pads on a wafer to be contacted; at least one contact terminal disposed on the first surface of the plurality of connector tabs; and a plurality of electrically conductive pathways disposed in the body such that each of the first plurality of contact terminals is electrically connected to a corresponding one of the contact terminals on the first surface of the connector tabs.

Conclusion

The exemplary methods and apparatus illustrated and described herein find application in the field of integrated circuit test and analysis.

It is to be understood that the present invention is not limited to the embodiments described above, but encompasses any and all embodiments within the scope of the subjoined Claims and their equivalents.

What is claimed is:

1. An apparatus, comprising:

a body having a first surface and a second surface, the body having a substantially circular central portion, and a plurality of bendable arms extending outwardly from the central portion, each bendable arm having a connector tab disposed at the distal end thereof;

a first plurality of contact terminals disposed on the second surface of the central portion of the body, the first plurality of contact terminals arranged in pattern to match the layout of pads on a wafer to be contacted;

at least one contact terminal disposed on the first surface of the plurality of connector tabs; and

a plurality of electrically conductive pathways disposed in the body such that each of the first plurality of contact terminals is electrically connected to a corresponding one of the contact terminals on the first surface of the connector tabs.

2. The apparatus of Claim 1, wherein the connector tabs each have at least one perforation therein.

3. The apparatus of Claim 1, wherein the body is a unitary structure.

4. The apparatus of Claim 1, further comprising a groove for receiving an O-ring on the wafer side of the central portion.

5. The apparatus of Claim 4, further comprising an O-ring disposed in the groove.

Fig. 1

Prior Art

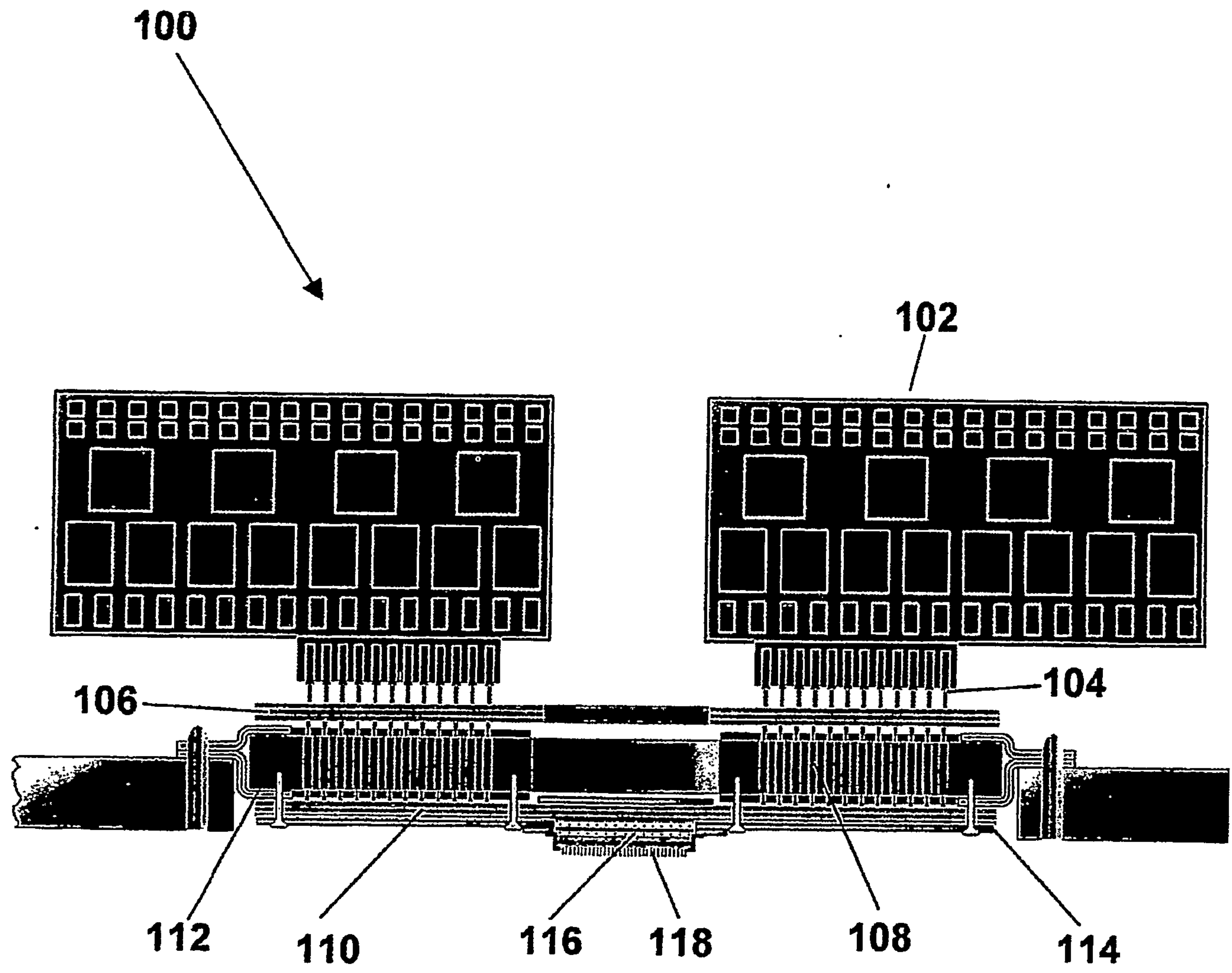


Fig. 2

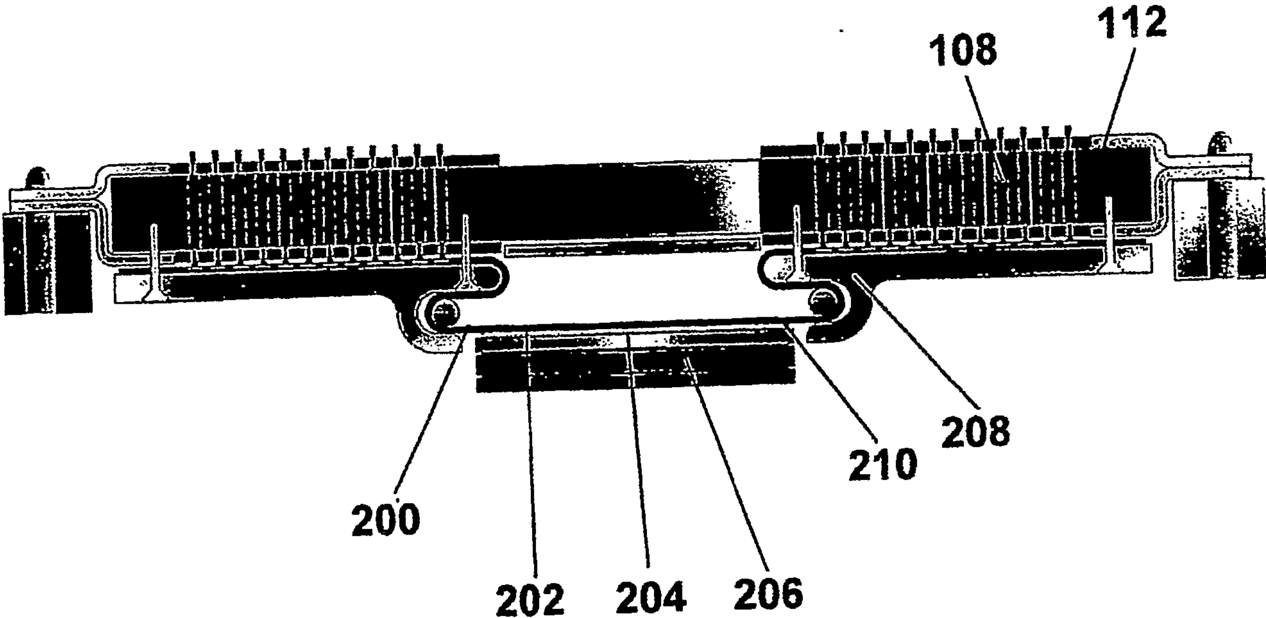


Fig. 3

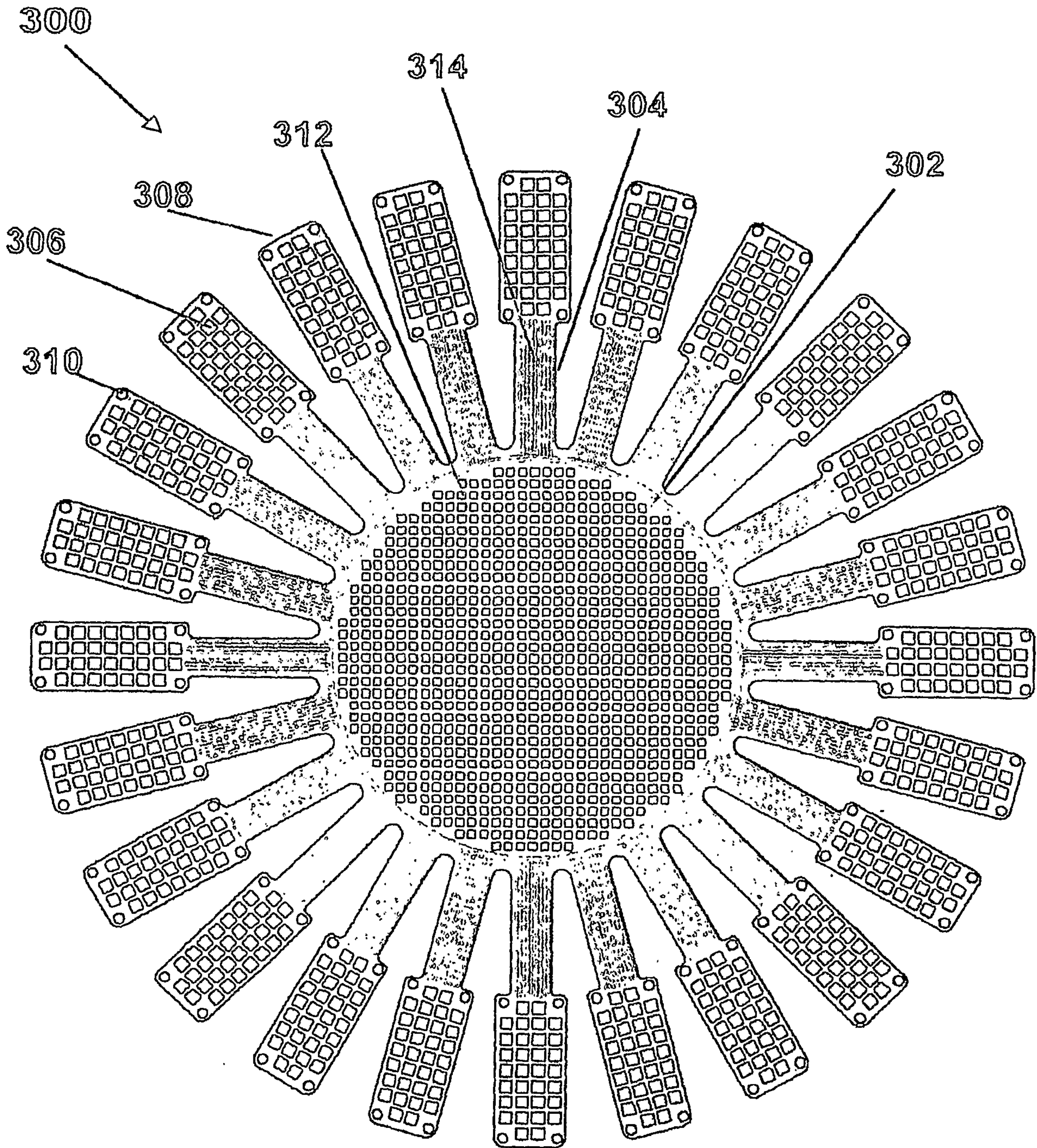


Fig. 4

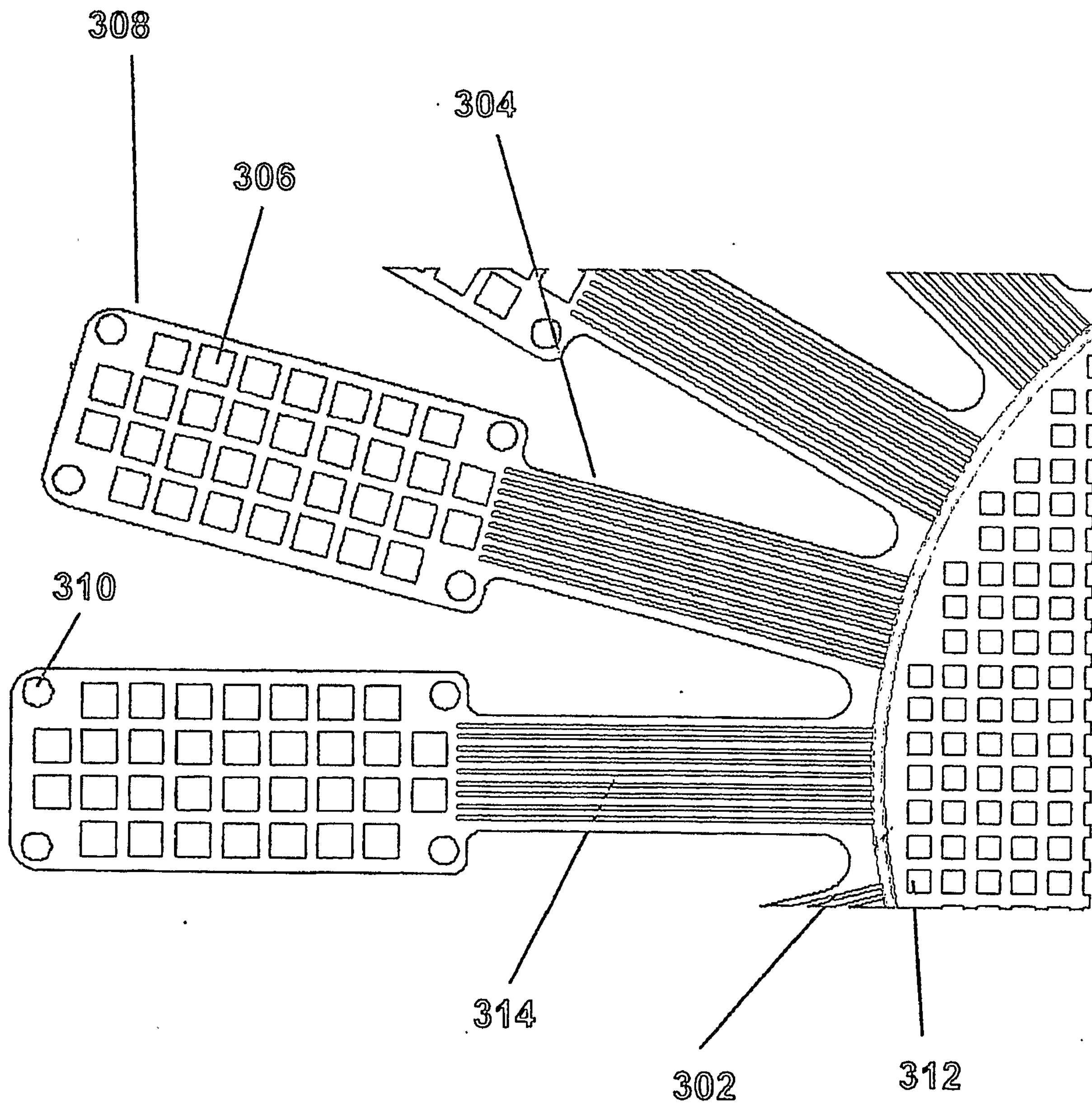


Fig. 5

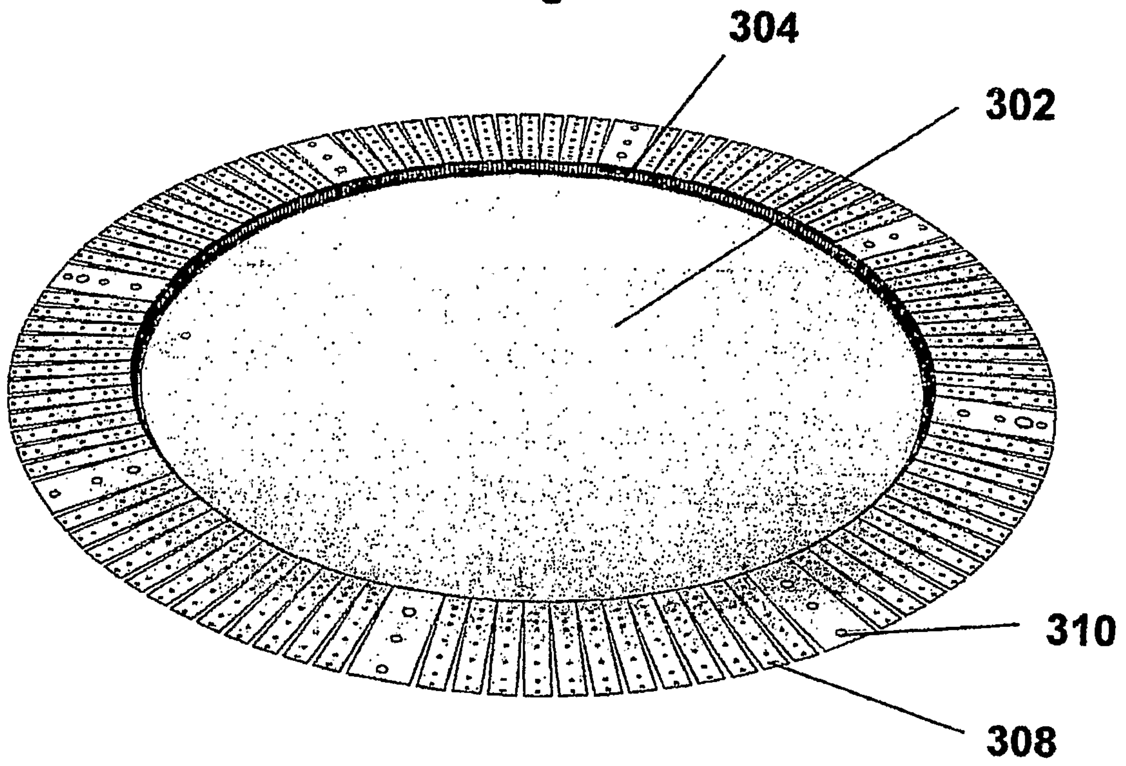


Fig. 6

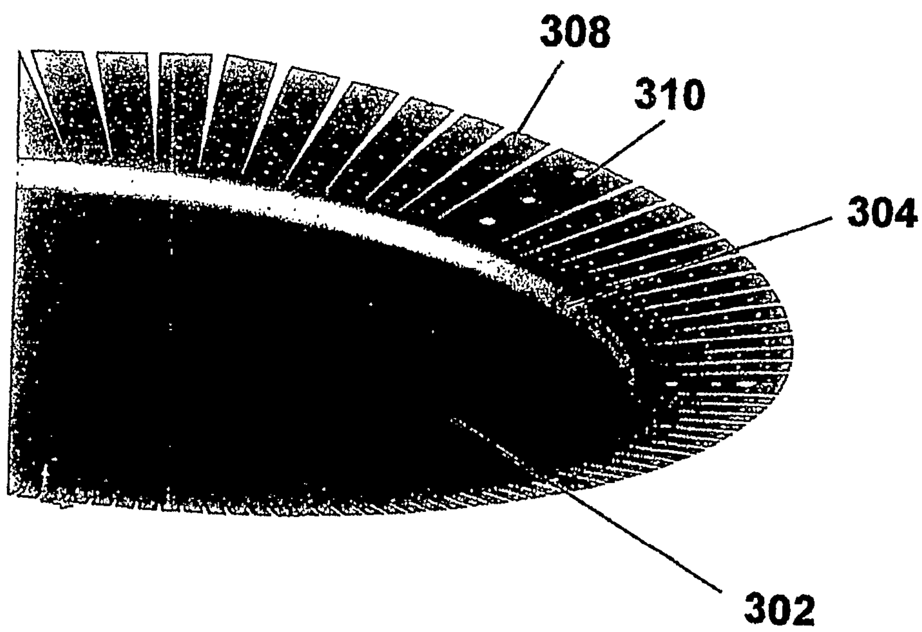
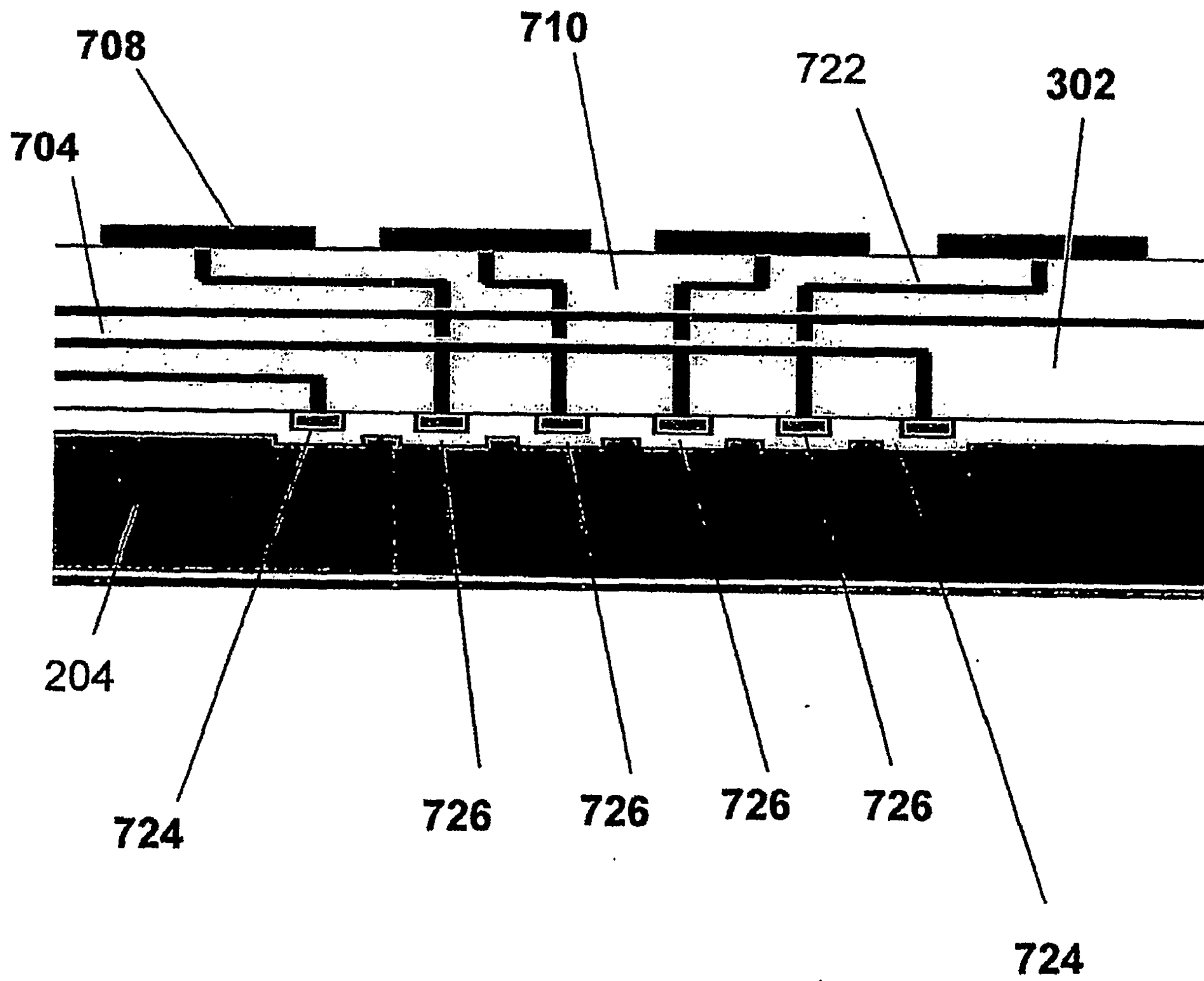


Fig. 7



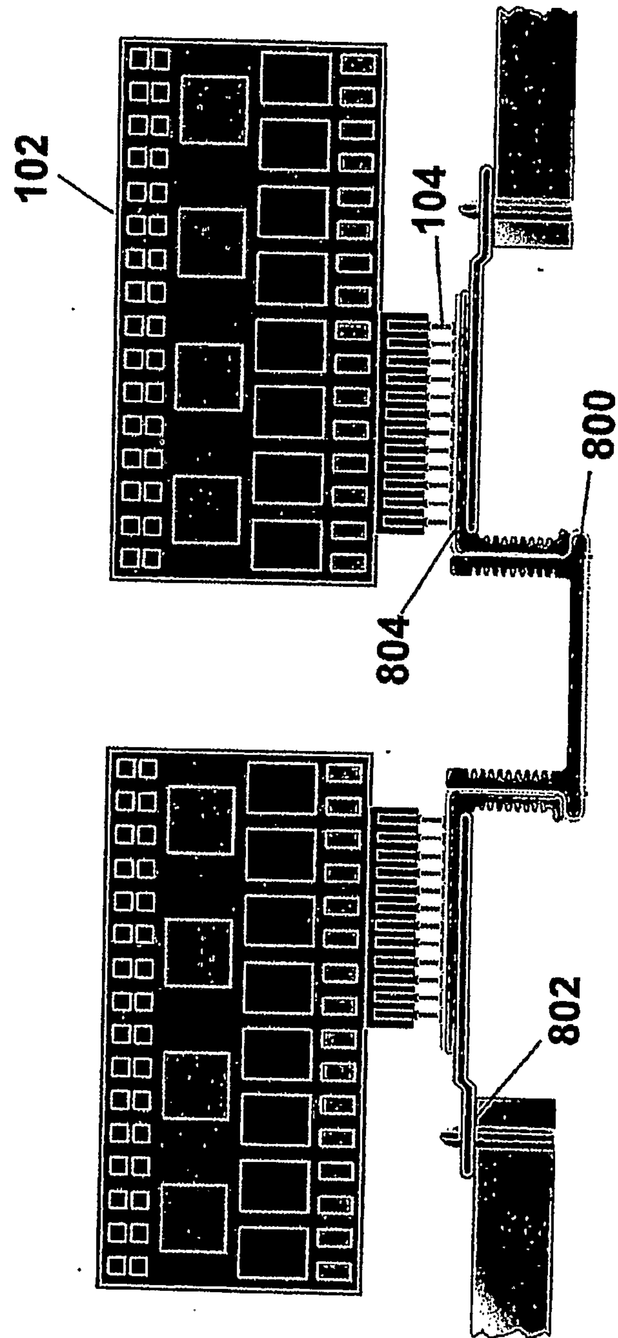


Fig. 8