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(54) **Title**: SEMICONDUCTOR STRUCTURE WITH MULTIPLE TRANSISTORS HAVING VARIOUS THRESHOLD VOLTAGES AND METHOD OF FABRICATION THEREOF

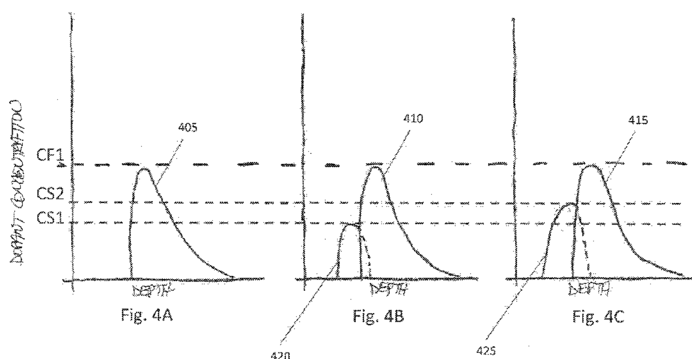


Fig. 4A Fig. 4B Fig. 4C

(57) **Abstract**: A seinxconauctor structure includes first, second, and third transistor elements each having a first screening region concurrently formed therein..A second screening region is formed in the second and third transistor elements such that there is at. least one characteristic of the screening region in the second transistor element that is different than the second screening region in the third transistor element. Different characteristics include doping concentration and depth of implant. In addition, a different characteristic may be achieved by concurrently implanting the second screening region in the second and third transistor element followed by implanting an additional dopant into the second screening region of the third transistor element

SEMICONDUCTOR STRUCTURE WITH MULTIPLE TRANSISTORS HAVING VARIOUS THRESHOLD VOLTAGES AND METHOD OF FABRICATION THEREOF

TECHNICAL FIELD

The following disclosure relates in general to semiconductor devices and processing and more particularly to a semiconductor structure with multiple
5 transistor elements having various threshold voltages and method of fabrication thereof.

BACKGROUND

Many integrated circuit designs use a variety of
10 cells that perform specific functions. Integrated circuits can include logic, memory, controller and other functional blocks. Semiconductor integrated circuits are fabricated in a semiconductor process, often using a CMOS process. Transistors are formed in a semiconductor
15 substrate, and usually involve a sequence of fabrication steps that result in a gate with adjacent source and drain, the source and drain being formed in a channel. A key setting for a transistor is the threshold voltage, which in turn determines the voltage at which a
20 transistor can be switched. Low threshold voltage devices are generally used for high speed circuits, though low threshold voltage devices tend to have higher leakage power. High threshold voltage devices tend to result in slower speeds but are usually implemented when
25 power reduction is desired. It is generally known that variation in threshold voltage from the device specification is undesirable. Threshold voltage can be set by incorporating dopants into the transistor channel,

either by way of direct channel implantation adjacent the gate oxide or by way of pocket or halo implants adjacent the source and drain. Such channel doping or halo implants also have the positive effect of reducing short channel effects especially as the gate length shrinks. Threshold voltage variation can increase with scaling, however, because of random dopant fluctuations in the implanted channel area. The variation problem worsens as critical dimensions shrink because of the greater impact of dopant fluctuations as the volume of the channel becomes smaller. As a result, circuit design has become more limited over time in that circuit designers must account for greater potential variation in the devices with smaller gate dimensions, thus making it impossible to design circuits with the technical freedom needed to build new and improved semiconductor chips. While CMOS technology has improved to allow continued scaling down of critical dimension, the associated and desired scaling down of voltage has not followed.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present disclosure and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, wherein like reference numeral represent like parts, in which:

FIGURE 1 shows an embodiment of a Deeply Depleted Channel (DDC) transistor 100 having an enhanced body coefficient, along with the ability to set threshold voltage Vt with enhanced precision;

FIGUREs 2A-2C illustrate the dopant profiles for exemplary screening regions for three different

transistor device types constructed on a common substrate;

FIGUREs 3A-3C illustrate representative structures of the transistor device types corresponding to the dopant profiles of FIGUREs 2A-2C;

FIGUREs 4A-4C are graphs illustrating an alternative dopant profile for exemplary screening regions for three different transistor device types constructed on a common substrate;

FIGUREs 5A-5C are graphs illustrating still another alternative scheme for setting Vt across three types of transistors;

FIGUREs 6A-6B illustrates the impact of the doses and implant energy used to implant the second screening region dopant on the threshold voltage and the leakage current for a PMOS transistor;

FIGURE 7 illustrates the combined effect of the implant energy and implant dose used to implant the second screening region dopant on the threshold voltage and leakage current for a PMOS transistor;

FIGUREs 8A and 8B illustrate embodiments that advantageously use two different dopant species for the two screening region implants used to form dual screening regions;

FIGURE 9 illustrates a semiconductor wafer supporting multiple die;

FIGURE 10 illustrates one embodiment of a portion of a DDC transistor manufacturing process;

FIGUREs 11A-11D illustrate a dopant profile and corresponding structure for a DDC transistor having dual antipunchthrough (APT) regions with single and dual screening regions respectively;

FIGUREs 12A-12C illustrate threshold voltage as a function of gate length for DDC transistors having single and dual APT regions formed using different implant conditions;

5 FIGURE 13 illustrates the body coefficient for PMOS LVt transistors having single and dual Sb APT regions;

FIGURE 14 illustrates the body coefficient for NMOS LVt transistors having single and dual boron (B) APT regions;

10 FIGUREs 15A-15B illustrate that dual APT regions have an effect on body coefficient for PMOS DDC transistor devices for given screening region conditions;

FIGUREs 16A and 16B illustrate that dual APT regions can provide an enhanced body coefficient for NMOS

15 transistor devices for given screening region conditions.

DETAILED DESCRIPTION

Transistors having improved threshold voltage variation and therefore enabling the scaling of supply

20 voltage are disclosed. Embodiments of structures and fabrication methods allowing for reliable setting of threshold voltage, and with improved mobility, transconductance, drive current, strong body coefficient and reduced junction leakage are provided. More

25 specifically, embodiments of doping profiles to result in different Vt targets for the different transistor device types without the use of pocket or halo implants or channel implantation adjacent the gate oxide are disclosed.

30 FIGURE 1 shows an embodiment of a Deeply Depleted Channel (DDC) transistor 100 having an enhanced body coefficient, along with the ability to set threshold

voltage Vt with enhanced precision. The DDC transistor 100 includes a gate electrode 102, source 104, drain 106, and a gate dielectric 128 positioned over a substantially undoped channel 110. Lightly doped source and drain extensions (SDE) 132, positioned respectively adjacent to source 104 and drain 106, extend toward each other, setting the transistor channel length.

The exemplary DDC transistor 100 is shown as an N-channel transistor having a source 104 and drain 106 made of N-type dopant material, formed upon a substrate such as a P-type doped silicon substrate providing a P-well 114 formed on a substrate 116. In addition, the N-channel DDC transistor in FIGURE 1 includes a highly doped screening region 112 made of P-type dopant material, and a threshold voltage set region 111 made of P-type dopant material. Substantially undoped channel 110 is preferably formed using epitaxially-grown silicon, using a process recipe that is intended to result in undoped crystalline silicon. Although substantially undoped channel 110 may be referred to herein as the "undoped channel", it is understood that a minimum or baseline level of dopants are present due to unavoidable introduction of some foreign material during the otherwise intrinsic epitaxial process. As a general matter, the "undoped channel" preferably has a dopant concentration of less than 5×10^{17} atoms/cm^3 in some portions thereof. However, it is desirable that at least a portion of the channel underlying the gate remains undoped in the final transistor structure and certain process steps are chosen to achieve this configuration. An N-channel DDC transistor is shown in FIGURE 1.

Similarly, a P-channel DDC transistor can be achieved by interchanging N and P regions.

The features of DDC transistor 100 can result in various transistor device types. Such transistor device types include, but are not limited to: P-FETs, N-FETs, FETs tailored for digital or analog circuit applications, high-voltage FETs, high/normal/low frequency FETs, FETs optimized to work at distinct voltages or voltage ranges, low/high power FETs, and low, regular, or high threshold voltage transistors (i.e. low Vt, regular Vt, or high Vt – also referred to as LVt, RVt, or HVt, respectively), etc. Transistor device types are usually distinguished by electrical characteristics (e.g. threshold voltage, mobility, transconductance, linearity, noise, power), which in turn can lend themselves to be suitable for a particular application (e.g., signal processing or data storage). Since a complex integrated circuit such as, for instance, a system on a chip (SoC) may include many different circuit blocks having different transistor device types to achieve the desired circuit performance, it is desirable to use a transistor structure that can be readily fabricated to result in the various transistor device types.

A process for forming a DDC transistor may begin with forming the screening region 112. In certain embodiments, the screening region is formed by providing the substrate having the P-well 114 and implanting screening region dopant material thereon. Other methods may be used to form the screening region such as in-situ doped epitaxial silicon deposition, or epitaxial silicon deposition followed by vertically directed dopant implantation to result in a heavily doped region embedded

a vertical distance downward from gate 102. Preferably, the screening region is positioned such that the top surface of the screening region is located approximately at a distance of Lg/1.5 to Lg/5 below the gate (where Lg
5 is the gate length). The screening region is preferably formed before STI (shallow trench isolation) formation. Boron (B), Indium (I), or other P-type materials may be used for P-type NMOS screening region material, and arsenic (As), antimony (Sb) or phosphorous (P) and other
10 N-type materials can be used for PMOS screening region material. The screening region 112, which is considered heavily doped, has a significant dopant concentration, which may range between about 5×10^{18} to 1×10^{20} dopant atoms/cm^3. Generally, if the screening region 112 dopant
15 level is on the higher end of the range, the screening region 112 can simultaneously function as the threshold voltage setting region.

Though exceptions may apply, as a general matter it is desirable to take measures to inhibit the upward
20 migration of dopants from the screening region, and in any event, controlling the degree to which dopants may migrate upward as a mechanism for controlling the threshold voltage setting is desired. All process steps occurring after the placement of screening region dopants
25 are preferably performed within a limited thermal budget. Moreover, for those dopants that tend to migrate or for flexibility in using a higher temperature in subsequent processes, a germanium (Ge), carbon (C), or other dopant migration resistant layer can be incorporated above the
30 screening region to reduce upward migration of dopants. The dopant migration resistant layer can be formed by way

of ion implantation, in-situ doped epitaxial growth, or other process.

An optional threshold voltage set region 111 is usually positioned above the screening region 112. The threshold voltage set region 111 can be either in contact with, adjacent to, incorporated within, or vertically offset from the screening region. In certain embodiments, the threshold voltage set region 111 is formed by ion implantation into the screening region 112, delta doping, controlled in-situ deposition, or by atomic layer deposition. In alternative embodiments, the threshold voltage set region 111 can be formed by way of controlled outdiffusion of dopant material from the screening region 112 into an undoped epitaxial layer using a predetermined thermal cycling recipe. Preferably, the threshold voltage set region 111 is formed before the undoped epitaxial layer is formed, though exceptions may apply. The threshold voltage is designed by targeting a dopant concentration and thickness of the threshold voltage set region 111 suitable to achieve the threshold voltage desired for the device. Note that if the screening region 112 concentration is sufficiently high, then the screening region 112 can function as the threshold voltage setting region and a separate threshold voltage setting region is not needed. Preferably, the threshold voltage set region 111 is fabricated to be a defined distance below gate dielectric 128, leaving a substantially undoped channel layer directly adjacent to the gate dielectric 128. The dopant concentration for the threshold voltage set region 111 depends on the desired threshold voltage for the device, taking into account the location of the threshold

voltage set region 111 relative to the gate. Preferably, the threshold voltage set region 111 has a dopant concentration between about 1 x 10^{18} dopant atoms/cm^3 and about 1 x 10^{19} dopant atoms per cm^3. Alternatively, the threshold voltage set region 111 can be designed to have a dopant concentration that is approximately one third to one half of the concentration of dopants in the screening region 112.

The final layer of the channel is formed preferably by way of a blanket epitaxial silicon deposition, although selective epitaxial deposition may be used. The channel 110 is structured above the screening region 112 and threshold voltage set region 111, having a selected thickness tailored to the electrical specifications of the device. The thickness of the substantially undoped channel 110 usually ranges from approximately 5-25 nm with a thicker undoped channel 110 usually used for a lower Vt device. To achieve the desired undoped channel 110 thickness, a thermal cycle may be used to cause an outdiffusion of dopants from the screening region 112 into a portion of the epitaxial layer to result in a threshold voltage setting region 111 for a given undoped channel region 110 thickness. To control the degree of outdiffusion of dopants across a variety of device types, migration resistant layers of C, Ge, or the like can be utilized in selected devices. By achieving a thickness of the threshold voltage region by way of the ion implantation, in-situ epitaxial growth or other methods such as thermal cycle to effect a controlled diffusion a distance upward into the channel, different thicknesses of channel 110 may be achieved. Still further methods for establishing different thicknesses of channel 110 may

include selective epitaxial growth or a selective etch back with or without a blanket epitaxial growth or other thickness reduction. Isolation structures are preferably formed after the channel 110 is formed, but isolation may also be formed beforehand, particularly if selective epitaxy is used to form the channel 110.

The transistor 100 is completed by forming a gate electrode 102 which may be a polysilicon gate or a metal gate stack, as well as SDE 132, spacers 130, and source 104 and drain 106 structures using conventional fabrication methods, with the caveat that the thermal budget be maintained within a selected constraint to avoid unwanted migration of dopants from the previously formed screening region 112 and threshold voltage setting region 111. Note that versions of transistor 100 can be implemented in any process node using a variety of transistor structural schemes including, in the more advanced nodes, using techniques to apply stress or strain in the channel. In conventional field effect transistors (FETs), the threshold voltage can be set by directly implanting a "threshold voltage implant" into the channel, raising the threshold voltage to an acceptable level that reduces transistor off-state leakage while still allowing speedy transistor switching. The threshold voltage implant generally results in dopants permeating through the entire channel region. Alternatively, the threshold voltage (V_t) in conventional FETs can also be set by a technique variously known as "halo" implants, high angle implants, or pocket implants. Such implants create a localized, graded dopant distribution near a transistor source and drain that extends a distance into the channel. Both halo implants

and channel implants introduce dopants into the channel, resulting in random fluctuations of dopants in the channel which in turn can affect the actual threshold voltage for the device. Such conventional threshold voltage setting methods result in undesirable threshold voltage variability between transistors and within transistor arrays. Additionally, such conventional threshold voltage setting methods decrease mobility and channel transconductance for the device.

The screening region 112 creates a strong body coefficient amenable for receiving a body bias. A body tap 126 to the screening region 112 of the DDC transistor can be formed in order to provide further control of threshold voltage. The applied bias can be either reverse or forward biased, and can result in significant changes to threshold voltage. Bias can be static or dynamic, and can be applied to isolated transistors, or to groups of transistors that share a common well. Biasing can be static to set threshold voltage at a fixed set point or dynamic to adjust to changes in transistor operating conditions or requirements. Various suitable biasing techniques are disclosed in U.S. Patent No. 8,273,617, the entirety of which is herein incorporated by reference.

Further examples of transistor structure and manufacture suitable for use in DDC transistors are disclosed in U.S. Patent Application Serial No. 12/895,785 filed September 30, 2010 titled "Advanced Transistors with Threshold Voltage Set Dopant Structures" by Lucian Shifren, et al., U.S. Patent No. 8,421,162, U.S. Patent Application Serial No. 12/971,884 filed on December 17, 2010 titled "Low Power Semiconductor

Transistor Structure and Method of Fabrication Thereof" by Lucian Shifren, et al., and U.S. Patent Application Serial No. 12/971,955 filed on December 17, 2010 titled "Transistor with Threshold Voltage Set Notch and Method of Fabrication Thereof" by Reza Arghavani, et al., the respective contents of which are incorporated by reference herein in their entirety.

Many integrated circuit designs benefit from the availability of a variety, or range of transistor device types that can be included in those integrated circuits. The availability of multiple transistor device types provides engineers with the resources to produce optimized circuit designs, as well as to produce circuit designs that might otherwise be unachievable if limited to a small number of transistor device types. As a practical matter, it is desirable that each integrated circuit on a wafer be able to incorporate all, or any subset of, the range of transistor device types available in an integrated circuit manufacturing process while achieving a limited variation in threshold voltage both locally and globally. It is also desirable to reduce the off-state leakage current and to achieve a limited variation in the off-state leakage current for the range of transistor device types available in the integrated circuit.

Various embodiments described below use a combination of ion implantations to form dual screening regions to achieve different transistor device types. Dual screening regions are advantageously used to provide different transistor device types in terms of threshold voltages while achieving a reduced off-state leakage current. In comparison, a transistor device that uses a

single screening region may have a similar threshold voltage but may have higher junction leakage. With dual screens, each peak screening region dopant concentration may be reduced compared with the case of the dopant concentration of a single screening region for a given threshold voltage. Additionally, dual antipunchthrough (APT) regions are disclosed. Dual APT can provide a specified body coefficient using a lower peak concentration as compared to the peak concentration of a single implant APT region for a substantially similar body coefficient. Dual APT regions also provide the benefit of reducing the off-state leakage current of the different transistor device types, for instance if dual APT regions use a combination of a shallower and deeper APT region implants compared to a mid-energy single APT region implant. Transistors having shallower APT regions (due to lower energy APT region implants) can typically include a lower peak screening region dopant concentration to achieve a target threshold voltage. The advantages of dual APT regions can be obtained whether with single screening regions or dual screening regions.

Typically, the value of the threshold voltage is related to the concentration of dopants in the screening region. For various embodiments described below, the concentration of dopants is illustrated as a function of depth (also referred to as a dopant profile), where the zero depth position typically approximates the position of the gate oxide in the device.

FIGUREs 2A-2C illustrate the dopant profiles for exemplary screening regions for three different transistor device types constructed on a common substrate, in which the doped regions are separated from

the gate by a substantially undoped semiconductor layer (preferably intrinsic silicon having a dopant concentration of less than $5x10^{17}$ atoms/cm^3). A range of Vt's can be achieved thereby, for instance a low
5 threshold voltage (LVt) 205, a regular threshold voltage (RVt) 210, and a high threshold voltage (HVt) 215. The screening region dopant profile for the LVt transistor device type has a peak screening region dopant concentration of CF1 atoms/cm^3, the screening region
10 dopant profile for the RVt transistor device type has a peak screening region dopant concentration of CF2 atoms/cm^3, and the screening region dopant profile for the HVt transistor has a peak screening region dopant concentration of CF3 atoms/cm^3, where $CF1 < CF2 < CF3$.
15 Such dopant concentrations can be achieved by selected doses for the implants. In one embodiment, Sb is implanted at a dose of 1×10^{13} atoms/cm^2, 2×10^{13} atoms/cm^2, and 3×10^{13} atoms/cm^2 to form the screening regions of the LVt, RVt, and HVt transistor device types
20 respectively. Implant energies in the range of 10-50 keV can be used to implant the screening region dopants, where the location of the peak is generally related to the implant energy used. The deeper the peak desired, the higher the selected energy for the implant. In the
25 embodiment of FIGUREs 2A-2C, the screening region dopants for the three transistor device types are implanted using the same implant energy but with different doses resulting in three screening region dopant profiles 205, 210, and 215 having three different peak concentrations,
30 where the peak is located at approximately the same depth relative to the top surface of the substrate.

FIGUREs 3A-3C illustrate representative structures of the transistor device types corresponding to the dopant profiles of FIGUREs 2A-2C, showing in cross-section how screening regions may appear. In FIGURE 3A, there may be a screening region 305 placed a defined depth below gate stack 308 with an undoped channel 307 in the space between screening region 305 and gate stack 308 and having a defined thickness selected to achieve threshold voltage, junction leakage, and other device characteristics. Preferably, the thickness of screening region 305 is about 3 nm to 10 nm in thickness or more, but in any event is preferably less thick than the gate length of gate stack 308. Source and drain pair 306 are on either side of screening region 305 such that screening region 305 extends laterally across and underneath undoped channel 307 and abutting the edges of source and drain pair 306. IN FIGURE 3B, there may be screening region 310 that is more heavily doped than screening region 305, placed a similar depth below gate stack 313 as screening region 305 to its gate stack 308, with undoped channel 307 formed using a blanket epitaxial process so that it forms the same silicon thickness for the undoped channel for all of the devices having screening regions. Screening region 310 has a defined thickness selected to achieve threshold voltage, junction leakage, and other device characteristics. Preferably, the thickness of screening region 310 is about 3 nm to 15 nm in thickness and may be thicker than screening region 305, but in any event is preferably less thick than the gate length of gate stack 308. Source and drain pair 311 are on either side of screening region 310 such that screening region 310 extends laterally across and

underneath undoped channel 307 and abutting the edges of source and drain pair 311. IN FIGURE 3C, there may be screening region 315 that is more heavily doped than screening region 310, placed a similar depth below gate stack 318 as screening region 310 and 305 to their respective gate stacks 313 and 308, with undoped channel 307 forming the space between screening region 315 and gate stack 318. Screening region 315 has a defined thickness selected to achieve threshold voltage, junction leakage, and other device characteristics. Preferably, the thickness of screening region 315 is about 3 nm to 20 nm in thickness and may be thicker than screening regions 310 and 305, but in any event is preferably less thick than the gate length of gate stack 318. Source and drain pair 316 are on either side of screening region 315 such that screening region 315 extends laterally across and underneath undoped channel 307 and abutting the edges of source and drain pair 316. The transistors illustrated in FIGUREs 3A-3C are to demonstrate exemplary schemes for placement of the respective screening regions 305, 310, and 315, though specific implementations may differ depending on a variety of desired characteristics for the devices in the context of the semiconductor fabrication node. For instance, source and drains may be elevated and fabricated using selective epitaxial growth using a silicon, silicon-germanium, or other material to form the source and drain or any other process that imparts a stress in the channel.

Note that it may be desired to locate the screening regions at different depths to achieve different threshold voltage and other characteristics for the device. Screening region depth can be controlled based

on controlling the process settings, for instance higher ion implant energy to drive the ions deeper or lower ion implant energy to maintain a more shallow implanted region. After the screening region dopants are emplaced, the channel is completed by depositing an epitaxial silicon layer on the substrate over the screening region dopants. It follows that, if the screening region dopants are at the approximately same depth below the top surface of the substrate, then to achieve differing Vt's, different implant doses are used to modulate the Vt value. A higher implant dose generally results in a higher concentration of dopants. A lower implant dose generally results in a lesser concentration of dopants. If the screening region dopant implant process uses differing energies, then the Vt values will be modulated based upon the different depths of the screens or, put another way, based upon the different resulting relative thicknesses of the undoped epitaxial layer.

FIGUREs 4A-4C are graphs illustrating an alternative dopant profile for exemplary screening regions for three different transistor device types constructed on a common substrate. Note that the profiles may represent the distribution of dopant material prior to anneal. Post anneal, the profiles may be less distinct. Preferably, the profiles are achieved by way of separate ion implant steps. The common substrate is doped to create different transistor device types, e.g. a low threshold voltage (LVt), a regular threshold voltage (RVt), and a high threshold voltage (HVt) transistor corresponding to FIGUREs 4A-4C respectively. Preferably, the screening region dopant profiles for the three transistor device types illustrated in FIGUREs 4A-4C are obtained by

performing multiple screening region dopant implants. In one embodiment, a first screening region dopant can be implanted for all three devices as shown herein as dopant profiles 405, 410, and 415 for the LVt, RVt, and HVt transistor device types respectively. An additional implant step is performed for the RVt transistor device type to form the second screening region dopant profile 420, such that the combination of the dopant profiles 410 and 420 sets the threshold voltage of the RVt transistor device type. An additional implant step is performed for the HVt transistor device type to form the second screening region dopant profile 425, where the combination of the dopant profiles 415 and 425 sets the threshold voltage of the HVt transistor device type. The advantage of the scheme illustrated in FIGUREs 4A-4C is that a reduced dose implant can be used to achieve a peak concentration in the low end of the screening region range and, if desired, the same dose and energy for the screening region for the LVt device can be used for the RVt and HVt devices. Instead of relying upon a higher peak concentration for the screening region for the RVt and HVt devices, a reduced peak concentration is used, preferably at approximately the same depth within the substrate for each of the devices, and the Vt is achieved by implanting a secondary dopant profile at a location adjacent to but closer to the gate using a dose selected to result in the peak concentration appropriate to set the Vt for the device. As illustrated in FIGUREs 4A-4C, the LVt device does not contain a secondary implant and uses the initial screening region implant at peak concentration CF1, the RVt device includes the screening region implant at peak concentration CF1 and contains a

secondary implant at concentration CS1, and the HVt device includes the screening region implant at peak concentration CF1 and contains a secondary implant at concentration CS2 which is higher than CS1. All peak concentrations of dopants and relative depths within the substrate are determined as part of the device design to achieve the desired Vt while comprehending other design constraints including leakage, drive-current, and other factors understood by those skilled in the art.

FIGUREs 5A-5C are graphs illustrating still another alternative scheme for setting Vt across three types of transistors. The common substrate is doped to create dopant profiles for different transistor device types, e.g. a low threshold voltage (LVt), a regular threshold voltage (RVt), and a high threshold voltage (HVt) transistor. Preferably, a first screening region dopant is implanted for all three transistor device types resulting in first screening region dopant profiles 505, 510, and 515 for the LVt, RVt, and HVt transistor device types respectively. First screening region dopant profiles 505, 510, and 515 are preferably formed to have approximately the same peak concentration, designated as CF, at approximately the same depth within the substrate. An additional screening region dopant implant step is performed for the RVt transistor device type to form the second screening region dopant profile 520 at a peak concentration of CS, where the combination of the dopant profiles 510 and 520 sets the threshold voltage of the RVt transistor device type. An additional screening region dopant implant step is performed for the HVt transistor device type to form the second screening region dopant profile 525, using a reduced energy with

the same or approximately the same dose so that second screening region dopant profile 525 is at peak concentration of approximately CS but offset from the location of screening region dopant profile 515 to be located closer to the gate. Dopant profiles 515 and 525 may be separate from each other but connected by a lesser amount of dopant concentration as shown, namely a valley between the two peaks, or the dopant profiles 515 and 525 may be isolated from each other. In effect, the undoped channel for the device at FIGURE 5C is thinner than for FIGURE 5B and FIGURE 5A. The combination of the dopant profiles 515 and 525 sets the threshold voltage of the HVt transistor device type. The second screening region implant for the RVt and HVt transistor device types can be performed using the same dopant species at a substantially similar dose but using different implant energies, such that the peak dopant concentrations of the second dopant profile is approximately the same, but the peak is positioned at a different depth for the two transistor device types. In alternative embodiments, a combination of different dopant species, different dopant doses, and different implant energies can be used to implant the second dopant to form the screening regions of the different transistor device types. All peak concentrations of dopants and relative depths within the substrate are determined as part of the device design to achieve the desired Vt while comprehending other design constraints including leakage, drive-current, and other factors understood by those skilled in the art.

FIGURE 6A illustrates the impact 600 of the doses used to implant the second screening region dopant on the threshold voltage and the leakage current for a PMOS

transistor. The two graphs 605 and 610 in FIGURE 6A are obtained from TCAD simulations performed for a PMOS DDC transistor having a single implant screening region and dual screening regions respectively. Graph 605 illustrates the leakage current Isub as a function of threshold voltage for a PMOS transistor having only one screening region implant consisting of Sb implanted at 20 keV using doses in the range of 1 x 10^{13} to 2 x 10^{13} atoms/cm^2. Point 605A of graph 605 corresponds to a dose of 1 x 10^{13} atoms/cm^2 and point 605B of the graph 605 corresponds to a dose of 2 x 10^{13} atoms/cm^2. Graph 610 illustrates the leakage current Isub as a function of threshold voltage for a PMOS transistor having dual screening regions, where the first screening region implant is Sb implanted at 20 keV using doses in the range of 1 x 10^{13} to 2 x 10^{13} atoms/cm^2 and the second screening region implant is Sb implanted at 10 keV using doses in the range of 2 x 10^{12} to 5 x 10^{12} atoms/cm^2. Point 610A corresponds to a dose of 2 x 10^{12} atoms/cm^2, point 610B corresponds to a dose of 3 x 10^{12} atoms/cm^2, point 610C corresponds to a dose of 4 x 10^{12} atoms/cm^2, and point 610D corresponds to a dose 5 x 10^{12} atoms/cm^2.

FIGURE 6B illustrates the impact 601 of the implant energy used to implant the second screening region dopant on the threshold voltage and the leakage current for a PMOS transistor. The three graphs 615, 620, and 625 in FIGURE 6B are obtained from TCAD simulations performed for a PMOS DDC transistor having a single screening region and dual screening regions respectively, where different implant energies are used to implant the second screening region dopant. Graph 615 illustrates the leakage current Isub as a function of threshold voltage

for a PMOS transistor having only one screening region implant consisting of Sb implanted at 40 keV using doses in the range of 1×10^{13} to 2×10^{13} atoms/cm^2. Point 615A of graph 615 corresponds to a dose of 1×10^{13} atoms/cm^2 and point 615B of graph 615 corresponds to a dose of 2×10^{13} atoms/cm^2. Graph 620 illustrates the leakage current Isub as a function of threshold voltage for a PMOS transistor having dual screening regions, where the first screening region implant is Sb implanted at 40 keV using doses in the range of 1×10^{13} to 2×10^{13} atoms/cm^2 and the second screening region implant is Sb implanted at 20 keV using doses in the range of 0.5×10^{13} to 1×10^{13} atoms/cm^2. Point 620A corresponds to a dose of 0.5×10^{13} atoms/cm^2, point 620B corresponds to a dose of 0.6×10^{13} atoms/cm^2, and point 620C corresponds to a dose of 1×10^{13} atoms/cm^2. Graph 625 illustrates the leakage current Isub as a function of threshold voltage for a PMOS transistor having dual screening regions, where the first screening region implant is Sb implanted at 40 keV using doses in the range of 1×10^{13} to 2×10^{13} atoms/cm^2 and the second screening region implant is Sb implanted at 10 keV using doses in the range of 0.5×10^{13} to 0.6×10^{13} atoms/cm^2. Point 625A corresponds to a dose of 0.5×10^{13} atoms/cm^2 and point 625B corresponds to a dose of 0.6×10^{13} atoms/cm^2.

FIGURE 7 illustrates the combined effect 700 of the implant energy and implant dose used to implant the second screening region dopant on the threshold voltage and leakage current for a PMOS transistor. FIGURE 7 includes an overlay of graphs 605 and 610 (FIGURE 6A) and graphs 615, 620, and 625 (FIGURE 6B). It is noted that a 200 mV range of threshold voltage, as indicated by the

interval 705, can be obtained at substantially the same leakage by appropriate selection of the first screening region implant and the second screening region implant conditions. It is also noted that the graphs 610 and 625 have substantially similar slope and that both graphs show substantially similar threshold voltage and leakage current for the same second screening region implant dose. Therefore, the implant conditions of the second screening region dopant can have a dominant effect on setting the threshold voltage.

The dual screening regions described above can be formed by implanting either the same dopant species for the first screening region implant or a different dopant species can be used for the second screening region implant, wherein the dopant species are of the same polarity. FIGUREs 8A and 8B illustrate embodiments that advantageously use two different dopant species for the two screening region implants used to form the dual screening regions. FIGURE 8A illustrates an embodiment, where the second dopant species is a heavier molecule than the first dopant species and, therefore, the second dopant species can be implanted using a higher implant energy to form a shallow second implant for the screening region as compared to the implant energy that would be required if the first dopant species were used to form the shallow second implant. In FIGURE 8A, dual screening regions are formed for an NMOS transistor by implanting B to form the first implant and using BF2 to form the second implant. Since BF2 is approximately five times heavier than B, the implant energy used for the BF2 implant can be five times the implant energy that would be used to implant B. This is advantageous because the

high energy implant can be more precisely controlled. FIGURE 8B illustrates an embodiment where the first and second dopant species diffuse at different rates during dopant activation anneal. In FIGURE 8B, dual screening regions are formed for a PMOS transistor by implanting Sb to form the first implant and using As to form the second implant, where the Sb and As implant energies and doses are selected to form the Sb and As doped implants at approximately the same depth. However, during subsequent thermal processing such as activation anneal, As will diffuse more than Sb and, therefore, forms a shallow doped region as illustrated in FIGURE 8B. The use of a second dopant species that diffuses more also permits higher dopant energies to be used to implant the second dopant species.

FIGURE 9 illustrates a semiconductor wafer 942 supporting multiple die such as previously described. In accordance with the present disclosure, each die can support multiple blocks of circuitry, each block having one or more transistor types. Such an arrangement enables the creation of complex system on a chip (SoC), integrated circuits, or similar die that optionally include FETs tailored for analog or digital circuit applications, along with improved transistors such as DDC transistors. For example, four useful blocks in a single die are illustrated as follows. Block 944 outlines a collection of deeply depleted channel (DDC) transistors having low threshold voltage, block 945 outlines a collection of DDC transistors having regular threshold voltage, block 946 outlines a collection of DDC transistors having high threshold voltage, and block 947 outlines a collection of DDC transistors tailored for a

static random access memory cell. As will be appreciated, these transistor types are representative and not intended to limit the transistor device types that can be usefully formed on a die or wafer. Wafer 900
5 includes a substrate 902 (typically silicon) that can be implanted with optional APT regions and required single or dual screening regions 904 and an epitaxial blanket layer 906 formed after implantation of dopants in screening region 904. Wafer 900 can also include an
10 optional threshold voltage set region (not shown in FIGURE 9) positioned between the screening region 904 and the epitaxial blanket layer 906.

FIGURE 10 illustrates one embodiment of a portion of a DDC transistor manufacturing process 1000. A
15 semiconductor wafer is masked at step 1002 with a "zero layer" alignment mask to define dopant implantable well regions. To illustrate one embodiment, it is shown in FIGURE 10 to create PMOS dopant structures followed by NMOS dopant structures, but in implementation the order
20 can be reversed. In FIGURE 10, a deep N-well can be optionally formed at step 1004 in combination with or alternative to a conventional N-well. A first screening region dopant is implanted at step 1006 to form a first highly doped screening region for the LVt, RVt, and HVt
25 PMOS transistor device types. Typically, implant conditions for the first screening region dopant are selected to provide the target threshold voltage for the PMOS LVt transistor device type. At step 1008, the PMOS LVt and HVt devices are masked and an RVt additional
30 screening region dopant is implanted to form dual screening regions for the RVt PMOS transistors. The implant conditions for the additional RVt screening

region dopant are selected such that the combination of the first screening region dopant and the additional RVt screening region dopant provide the target threshold voltage for the PMOS RVt device. At step 1010, the PMOS LVt and RVt devices are masked and an additional HVt screening region dopant is implanted to form dual screening regions for the HVt PMOS transistors. The implant conditions for the additional HVt screening region dopant are selected such that the combination of the first screening region dopant and the additional HVt screening region dopant provide the target threshold voltage for the PMOS HVt device. In alternative embodiments, the additional RVt screening region dopant is implanted as part of the dual screening regions for both the PMOS RVt and HVt devices and both LVt and RVt devices are then masked to allow for a still further HVt screening region implant for the HVt devices only. For this embodiment, the implant condition for the first screening region dopant is selected to provide the target threshold voltage for the PMOS LVt devices, the implant conditions of the additional RVt and the additional HVt dopants are selected such the combination of the first screening region dopant and the additional RVt dopant provides the target threshold voltage for the RVt devices, and the combination of all three screening region dopants (i.e., the first screening region dopant, the additional RVt dopant, and the additional HVt dopant) provides the target threshold voltage for the HVt devices. Other well implants such as the APT region implant can be formed in the N-well before or after implanting the screening region dopants in steps 1006, 1008, and 1010.

After masking the N-well, the P-well is implanted at step 1012. A first screening region dopant is implanted at step 1014 to form a first highly doped screening region for the LVt, RVt, and HVt NMOS transistor device types. Typically, implant conditions for the first screening region dopant are selected to provide the target threshold voltage for the NMOS LVt transistor device type. At step 1016, the NMOS LVt and HVt devices are masked and an additional RVt screening region dopant is implanted to form dual screening regions for the RVt NMOS transistors. The implant conditions for the additional RVt screening region dopant are selected such that the combination of the first screening region dopant and the additional RVt screening region dopant provide the target threshold voltage for the NMOS RVt device. At step 1018, the NMOS LVt and RVt devices are masked and an additional HVt screening region dopant is implanted to form dual screening regions for the HVt NMOS transistors. The implant conditions for the additional HVt screening region dopant are selected such that the combination of the first screening region dopant and the additional HVt screening region provide the target threshold voltage for the NMOS HVt device. In alternative embodiments, the additional RVt screening region dopant is implanted as part of the dual screening regions for both the NMOS RVt and HVt devices and the NMOS LVt and RVt devices are then masked to allow for a still further screening region implant for the NMOS HVt devices only. For this embodiment, the implant condition for the first screening region dopant is selected to provide the target threshold voltage for the NMOS LVt devices, the implant conditions of the additional RVt and the additional HVt dopants are

selected such the combination of the first screening region dopant and the additional RVt dopant provides the target threshold voltage for the NMOS RVt devices, and the combination of all three screening region dopants (i.e., the first screening region dopant, the additional RVt dopant, and the additional HVt dopant) provides the target threshold voltage for the NMOS HVt devices. Other well implants such as the APT region implant can be formed in the P-well before or after implanting the screening region dopants in steps 1014, 1016, and 1018.

Next, at step 1020, a capping silicon epitaxial layer is deposited/grown across the entire substrate using a process that does not include added dopant species so that the resulting channel is substantially undoped and is of a resulting thickness tailored to achieve the multitude of threshold voltages. Typically the epitaxial layer is 100% intrinsic silicon, but silicon germanium or other non-silicon in-situ deposited atoms can also be added to the epitaxial layer either across the substrate or a preselected device location using masks, though preferably the resulting material from the epitaxial growth process is intrinsic in terms of dopant-based polarity. For further adjustment of Vt, a thermal cycling can be used to cause a controlled out-diffusion of some of the screening region dopants. Following epitaxial growth, at step 1022, shallow trench isolation (STI) structures are formed. In steps 1024 and 1026, gate structures, spacers, contacts, stress implants, tensile films, dielectric coatings, and the like are then formed to establish structures for operable transistors. The processes used to form the various structures are generally conventional, though within a

defined thermal cycle and with appropriate adjustments to conventional process recipes to comprehend reduced temperatures from otherwise high-temperature steps. In some devices, optionally, additional channel doping can be done using halo implants and/or traditional channel implants to render such devices conventional as opposed to DDC. It shall further be noted that the exemplary dopant profiles can be achieved using alternative processes. Although the process sequence of doping the screening region followed by forming the epitaxial undoped layer may be preferred, other processes can be used, for instance providing an undoped semiconductor region and then performing ion implantation at selected higher energies to drive the dopants down a depth through the undoped semiconductor region to achieve the exemplary dopant profiles. A further alternative process is to replace ion implantation with in-situ doped epitaxial growth to achieve the doped screening regions followed by deposition of semiconductor material to create the desired dopant profiles having the screening regions embedded a depth below the gate.

FIGURE 11A illustrates a dopant profile 1100 for a DDC transistor having dual APT regions and a single screening region. FIGURE 11B illustrates a structure 1120 with the dual APT regions 1105 and 1110 and the single screening region 1115 underlying an undoped channel 1102. The dopant profile 1100 includes two APT region implants having dopant profiles that form the dual APT regions 1105 and 1110. The dopant profile 1100 also includes a single screening region implant having a dopant profile that form the single screening region 1115. Typically, the peak dopant concentration of the

APT region implant positioned closest to the screening region, i.e. the dopant profile for APT region 1105, is greater than the peak dopant concentration of the APT region implant for APT region 1110 that is positioned deeper in the substrate. However, in alternative embodiments, the peak dopant concentration of the dopant profiles for APT region 1105 and APT region 1110 can be approximately the same. Though shown as adjacent and in contact with one another, APT regions 1105 and 1110 and screening region 1115 may be spaced apart from each other as desired.

FIGURE 11C illustrates a dopant profile 1150 for a DDC transistor having dual APT regions and dual screening regions. FIGURE 11D illustrates a structure 1180 with the dual APT regions 1155 and 1160 and the dual screening regions 1165 and 1170 underlying an undoped channel 1182. The dopant profile 1150 includes two APT region implants having dopant profiles that form the dual APT regions 1155 and 1160. The dopant profile 1150 also includes two screening region implants having a dopant profile that form dual screening regions 1165 and 1170. The dual APT regions 1155 and 1160 can be combined with a single or dual (or triple or more) screening regions, in combinations of varying peak dopant concentrations, in embodiments that are not shown herein. Proper selection of the dual APT region dose and energy condition allows the APT region to perform its primary function of preventing deep punchthrough between the source and drain regions (which would pinch-off the screening region isolating the screening region from the body bias voltage) while minimizing the junction leakage that can be caused by excessive screening region and APT region

implant dose. A single APT region implant controls the pinch-off performance through increased dose at a penalty of higher junction leakage from the increased APT region peak concentration. A wider APT region made from two separately optimized implants can be even more effective at protecting against pinch-off than a single APT region implant and allows the peak concentration for each implant to be lower than the equivalent single APT region implant resulting in overall lower leakage. Though shown as adjacent and in contact with one another, APT regions 1155 and 1160 and screening regions 1165 and 1170 may be spaced apart from each other as desired.

For the dual APT region dopant profiles illustrated in FIGUREs 11A and 11C, the deep APT region implant corresponding to the dopant profiles of APT regions 1110 and 1160 can assist the respective screening regions by controlling the depletion region generated by the operational voltage and, therefore, preventing the respective screening regions from being pinched off by the depletion region. Preventing the pinch off of the screening regions allows the screening regions to be biased by a body bias voltage applied to the transistor body. Typically the peak concentration of the deep APT region implant (i.e. dopant profiles of APT regions 1110 and 1160) is selected based on a predetermined range of body bias voltages to be applied to the DDC transistor such that the selected peak concentration prevents screening region pinch off for the predetermined range of body bias voltages. Typically the peak dopant concentration of the shallow APT region implant (i.e. dopant profiles for APT regions 1105 and 1155) is

selected to be lower than the peak screening region dopant concentration.

One of the advantages of using dual APT regions is that the lower peak dopant concentration in the dual APT region structure as compared to that of a single APT region helps to reduce junction leakage that may otherwise be present in a DDC device. Further, when dual APT regions are used, the device can more readily be designed with a reduced peak concentration screening region, either as a single screening region or dual screening regions, which provides advantages of reduced junction leakage. Having two implanted APT regions more readily allows for a continuum of doping extending from the screening region down through the device to the well. In contrast, a single implanted APT region generally has a tighter Gaussian distribution. The tighter Gaussian distribution makes for a potential pocket of very low-doped area between the screening region and the single APT region. Such a pocket that is very low in dopants essentially separates the screening region from the APT region, rendering the APT region less effective. The dual APT regions can also be combined with diffusion mitigation techniques, for instance Ge preamorphization implants (PAI) with carbon implants. With diffusion mitigation techniques, a selected target APT region dopant profile can be achieved using lower implant doses to form wider implanted region dopant profiles as a starting point, because the implanted APT region dopants are less apt to diffuse and spread during subsequent thermal steps.

FIGUREs 12A-12C illustrate threshold voltage as a function of gate length for DDC transistors having single

and dual APT regions formed using different implant conditions. FIGURE 12A illustrates the changes in threshold voltage as a function of drawn channel length for a transistor having a drawn width of 1 μm at a body bias voltage of 0.3 volts. FIGURE 12B illustrates the difference between the threshold voltage at a body bias voltage of 0 volts and at a body bias voltage of 0.9 volts as a function of drawn channel length for a DDC transistor having a drawn channel width of 1 μm. FIGURE 12C is an expanded version of a portion of the curves illustrated in FIGURE 12B. FIGUREs 12B and 12C provide a measure of the changes in the body coefficient as a function of the drawn channel length. The threshold voltages corresponding to four different APT region implant conditions are illustrated in these figures - (i) single implant APT region formed by implanting Sb at 160 keV using a dose of 0.9×10^{13} atoms/cm^2, (ii) single implant APT region formed by implanting Sb at 130 keV using a dose of 0.9×10^{13} atoms./cm^2, (iii) single implant APT region formed by implanting Sb at 130 keV using a dose of 1.2×10^{13} atoms/cm^2, and (iv) dual APT regions formed by a first implant of Sb at 130 keV using a dose of 0.6×10^{13} atoms/cm^2 and a second implant of Sb at 80 keV using a dose of 1.2×10^{13} atoms/cm^2. It is noted from FIGUREs 12A-12C that the lowest Vt roll-off is obtained for the dual APT regions. FIGUREs 12A-12C show that dual APT regions can result in lower threshold voltage roll-off (Vt roll off).

FIGURE 13 illustrates the body coefficient for PMOS LVt transistors having single and dual Sb APT regions. It is noted that the PMOS transistors having dual APT regions have a higher body coefficient at a body bias

voltage of -0.3 V (labeled Body Factor) as compared to the PMOS transistors having a single implant APT region.

FIGURE 14 illustrates the body coefficient for NMOS LVt transistors having single and dual boron (B) APT regions. It is noted that the NMOS transistors having dual APT regions have a higher body coefficient at a body bias voltage of 0.3 V (labeled Body Factor) as compared to the NMOS transistors having a single implant APT region.

FIGUREs 15A and 15B illustrate that dual APT regions have an effect on body coefficient for NMOS DDC transistor devices for given screening region conditions. FIGUREs 15A and 15B illustrate the median threshold voltage for NMOS transistors of various widths as a function of four different applied body bias voltages - 0 volts, 0.3 volts, 0.6 volts, and 0.9 volts. It is noted that for all channel widths, the NMOS transistors having dual APT regions have a higher body coefficient compared to NMOS transistors with single APT regions as indicated by the threshold voltage response for varying applied body bias voltage. In addition, the threshold voltage of dual APT NMOS transistors varies less in response to the applied body bias voltage for smaller channel widths, indicating an improved narrow-Z effect in the DDC devices having the dual APT regions.

FIGUREs 16A and 16B illustrate that dual APT regions can provide an enhanced body coefficient for PMOS transistor devices for given screening region conditions. FIGUREs 16A and 16B illustrate the median threshold voltage for PMOS transistors of various widths as a function of four different applied body bias voltages - 0 volts, 0.3 volts, 0.6 volts, and 0.9 volts. It is noted

that for all channel widths the PMOS transistors having dual APT regions have a higher body coefficient compared to PMOS transistors with single APT regions as indicated by the threshold voltage response for varying applied body bias voltage. In addition, the threshold voltage of dual APT PMOS transistors varies less in response to the applied body bias voltage for smaller channel widths, indicating an improved narrow-Z effect in the DDC devices having the dual APT regions.

In one embodiment, a target LVt transistor device type having a target threshold voltage of 0.38 V can be achieved using screening region implant dose of 5×10^{12} atoms/cm^2 for a transistor using dual APT regions (where the dual APT regions are formed with a first Sb implant at 80 keV using a dose of 1.2×10^{13} atoms/cm^2 and a second Sb implant at 130 keV using a dose of 1.2×10^{13} atoms/cm^2) as compared to a higher screening region dose of 8×10^{12} atoms/cm^2 for a transistor using a single APT region (where the single APT region is formed with an Sb implant at 130 keV using a dose of 1.2×10^{13} atoms/cm^2). In addition, the body factor of the dual APT LVt transistor is higher compared to that of the single APT LVt transistor, 85 as compared to 60 respectively, where the body factor is measured at a body bias voltage of -0.3 V. In an alternative embodiment, a target SVt transistor device type having a target threshold voltage of 0.46 V can be achieved using a screening region implant dose of 1.2×10^{13} atoms/cm^2 for a transistor using dual APT regions (where the dual APT regions are formed with a first Sb implant at 80 keV using a dose of 1.2×10^{13} atoms/cm^2 and a second Sb implant at 130 keV using a dose of 1.2×10^{13} atoms/cm^2) as compared to a

higher screening region dose of 1.4 x 10^{13} atoms/cm^2 for a transistor using a single APT region (where the single APT region is formed with an Sb implant at 130 keV using a dose of 1.2 x 10^{13} atoms/cm^2). The body factor of the
5 dual APT SVt transistor is also higher compared to that of the single APT SVt transistor, 96 as compared to 85 respectively, where the body factor is measured at a body bias voltage of -0.3 V.

Transistors created according to the foregoing
10 embodiments, structures, and processes can be formed on the die alone or in combination with other transistor types. Transistors formed according to the disclosed structures and processes can have a reduced mismatch arising from scattered or random dopant variations as
15 compared to conventional MOS analog or digital transistors. This is particularly important for transistor circuits that rely on closely matched transistors for optimal operation, including differential matching circuits, analog amplifying circuits, and many
20 digital circuits in widespread use such as SRAM cells. Variation can be even further reduced by adoption of structures such as a screening region, an undoped channel, or a threshold voltage set region as described herein to further effectively increase headroom which the
25 devices have to operate. This allows high-bandwidth electronic devices with improved sensitivity and performance.

In summary, a dual-screen DDC transistor is disclosed. There is provided a transistor device having
30 a gate, a doped source and drain region on either side of the gate and embedded in the substrate, for which the substrate comprises a substantially undoped epitaxial

layer (prior to the formation of the source and drain regions), a first heavily doped region doped with dopants of opposite polarity as the source and drain dopants, the first heavily doped region recessed a vertical distance down from the bottom of the gate at a depth of 1/1.5 to 1/5 times the gate length, and a second heavily doped region adjacent to the first heavily doped region, wherein the second heavily doped region is also of the opposite polarity as the source and drain dopants, the second heavily doped region which may have a higher or lower concentration of dopants than the first heavily doped region and may abut the first heavily doped region. In addition, there may be one or more separately doped regions also of the opposite polarity as the source and drain dopants to serve as anti-punch through. Variations in the location, number of regions, and dopant concentrations allow for a substrate to include multiple transistors with differing threshold voltages.

Although the present disclosure has been described in detail with reference to a particular embodiment, it should be understood that various other changes, substitutions, and alterations may be made hereto without departing from the spirit and scope of the structures and methods disclosed herein. Numerous other changes, substitutions, variations, alterations, and modifications may be ascertained by those skilled in the art and it is intended that the present disclosure encompass all such changes, substitutions, variations, alterations, and modifications as falling within the spirit and scope of the structures and methods disclosed herein. Moreover, the present disclosure is not intended to be limited in any way by any statement in the specification.

WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit having a plurality of transistor devices fabricated on a substrate surface to support a plurality of threshold voltages, the transistor devices each having a gate with a source and a drain on either side of the gate, comprising:

a first transistor device region having a first screening region with a first preselected doping concentration and first thickness and set to be a first predefined depth below the substrate surface;

a second transistor device region having a second screening region with a second doping concentration and second thickness and second depth, wherein the second thickness and second depth are substantially similar to the first screening region but the second doping concentration is higher than the first doping concentration; and

a third transistor device region having a third screening region with a third doping concentration and third thickness and third depth, wherein the third thickness and third depth are substantially similar to the second screening region but the third doping concentration is higher than the second doping concentration;

wherein each of the first, second, and third transistor device regions are covered by a substantially undoped layer to form a channel;

wherein each of the first, second, and third transistor device regions extend laterally across the length of the channel and abut the source and drain;

wherein each of the first, second, and third transistor device regions are located to be below the

surface of the substrate at a distance of at least 1/1.5 times a length of the gate and above the bottom of the source and drain to which each of the transistor device regions abuts.

5

2. The semiconductor structure of Claim 1, wherein the second transistor device region further includes a fourth screening region adjacent to the second screening region to form a dual screening structure.

10

3. The semiconductor structure of Claim 1, wherein the third transistor device region further includes a fifth screening region adjacent to the third screening region to form a dual screening structure.

15

4. The semiconductor structure of Claim 1, wherein each of the first, second, and third transistor device regions each include a first antipunchthrough region underlying each respective screening region.

20

5. The semiconductor structure of Claim 4, wherein at least one of the first, second, and third transistor device regions includes a second antipunchthrough region underlying the first antipunchthrough region.

25

6. The semiconductor structure of Claim 5, wherein the first antipunchthrough region is in contact with the second antipunchthrough region.

7. The semiconductor structure of Claim 5, wherein the first antipunchthrough region is in contact with the first screening region of at least one of the first, second, and third transistor device regions.

5

8. The semiconductor structure of Claim 2, wherein the second screening region is in contact with the fourth screening region.

10 9. The semiconductor structure of Claim 1, wherein the substantially undoped layer comprises a blanket epitaxial layer.

10. The semiconductor structure of Claim 9, wherein

15 at least one of the first, second, and third transistor device regions includes a channel that includes stress in the channel crystalline structure.

11. A method of fabricating a semiconductor

20 structure, comprising:

concurrently implanting in a substrate a first screening region for each of first, second, and third transistor elements;

implanting in the substrate a second screening

25 region for each of the second and third transistor elements, the second screening region in the second transistor element having a different characteristic than the second screening region in the third transistor element.

30

12. The method of Claim 11, wherein the first screening region is in contact with the second screening

region of at least one of the second and third transistor elements.

13. The method of Claim 11, wherein the second
5 screening region is implanted with a higher dopant concentration in the third transistor element than in the second transistor element to provide the different characteristic.

10 14. The method of Claim 11, wherein the second screening region is implanted at a lesser depth in the third transistor element than in the second transistor element to provide the different characteristic.

15 15. The method of Claim 11, wherein the different characteristic is provided by implanting in the substrate an additional dopant into the second screening region of the third transistor element.

20 16. The method of Claim 15, wherein the second screening region is concurrently implanted in the substrate for each of the second and third transistor elements.

25 17. The method of Claim 11, further comprising:

forming a channel layer on the substrate for each of the first, second, and third transistor elements by a blanket epitaxial growth.

18. The method of Claim 11, further comprising:

concurrently implanting a first antipunchthrough region for each of the first, second, and third transistor elements;

5 concurrently implanting a second antipunchthrough region for each of the first, second, and third transistor elements;

wherein the first and second antipunchthrough regions underlie the respective screening regions of the

10 first, second, and third transistor elements.

19. The method of Claim 18, wherein the first antipunchthrough area is formed in contact with the second antipunchthrough area.

15

20. The method of Claim 18, wherein the second antipunchthrough region is formed in contact with the first screening region.

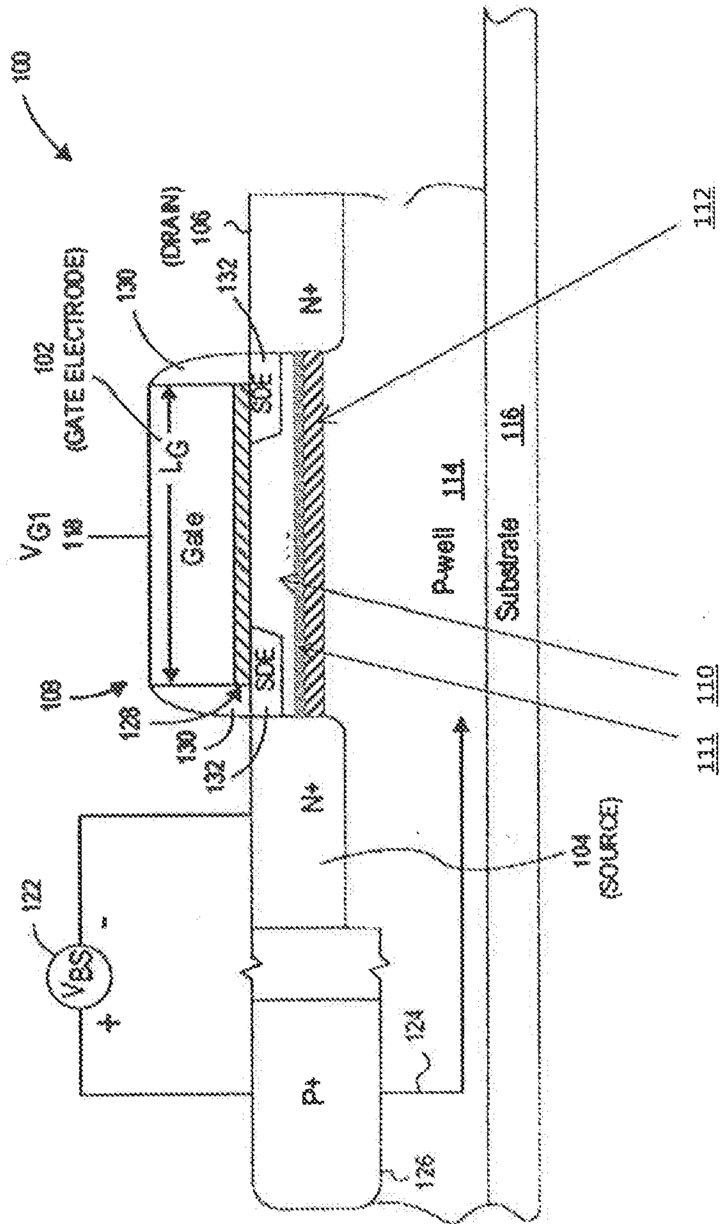


Figure 1

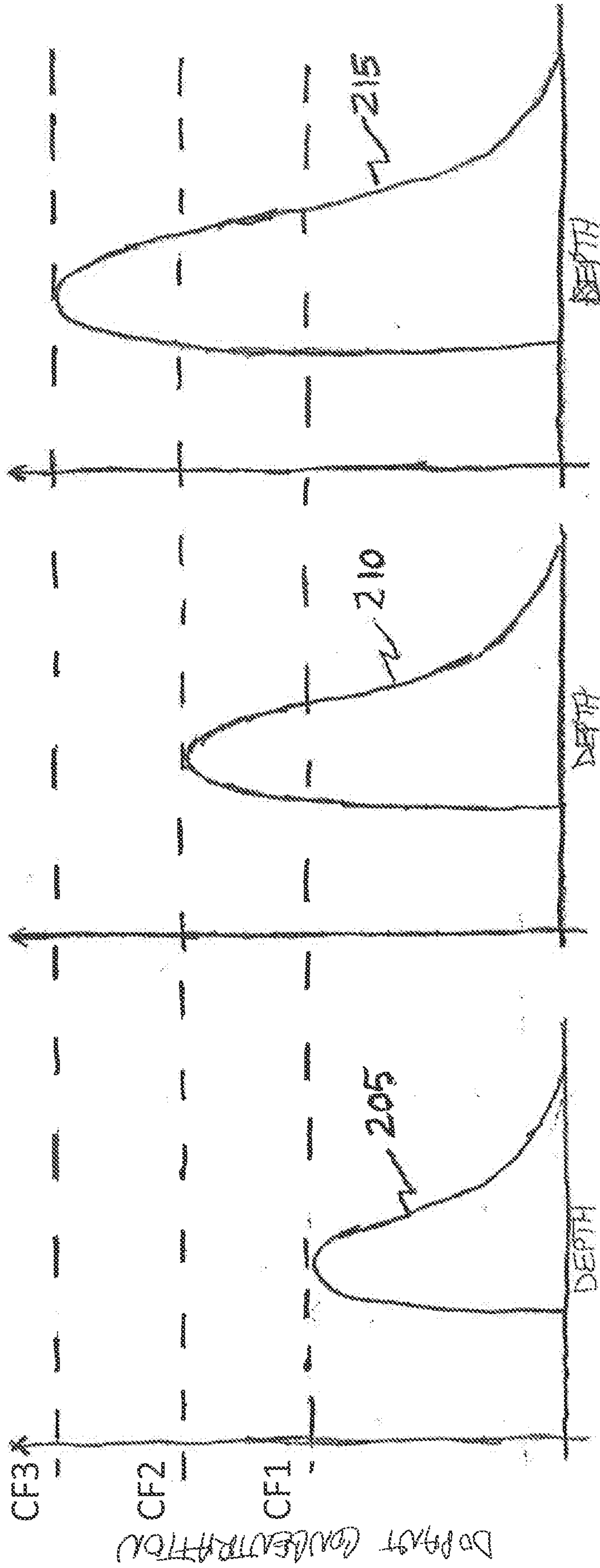


Fig. 2A

Fig. 2B

Fig. 2C

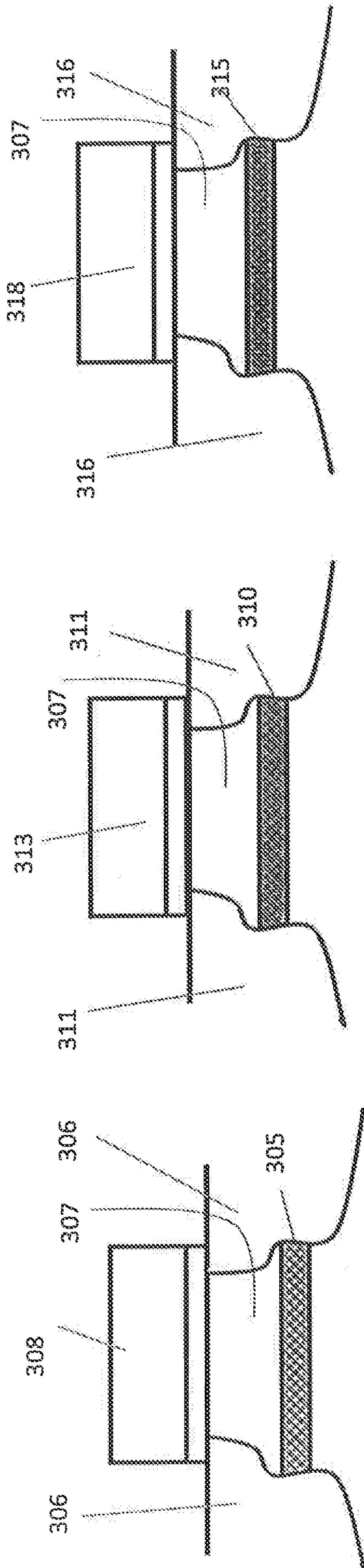
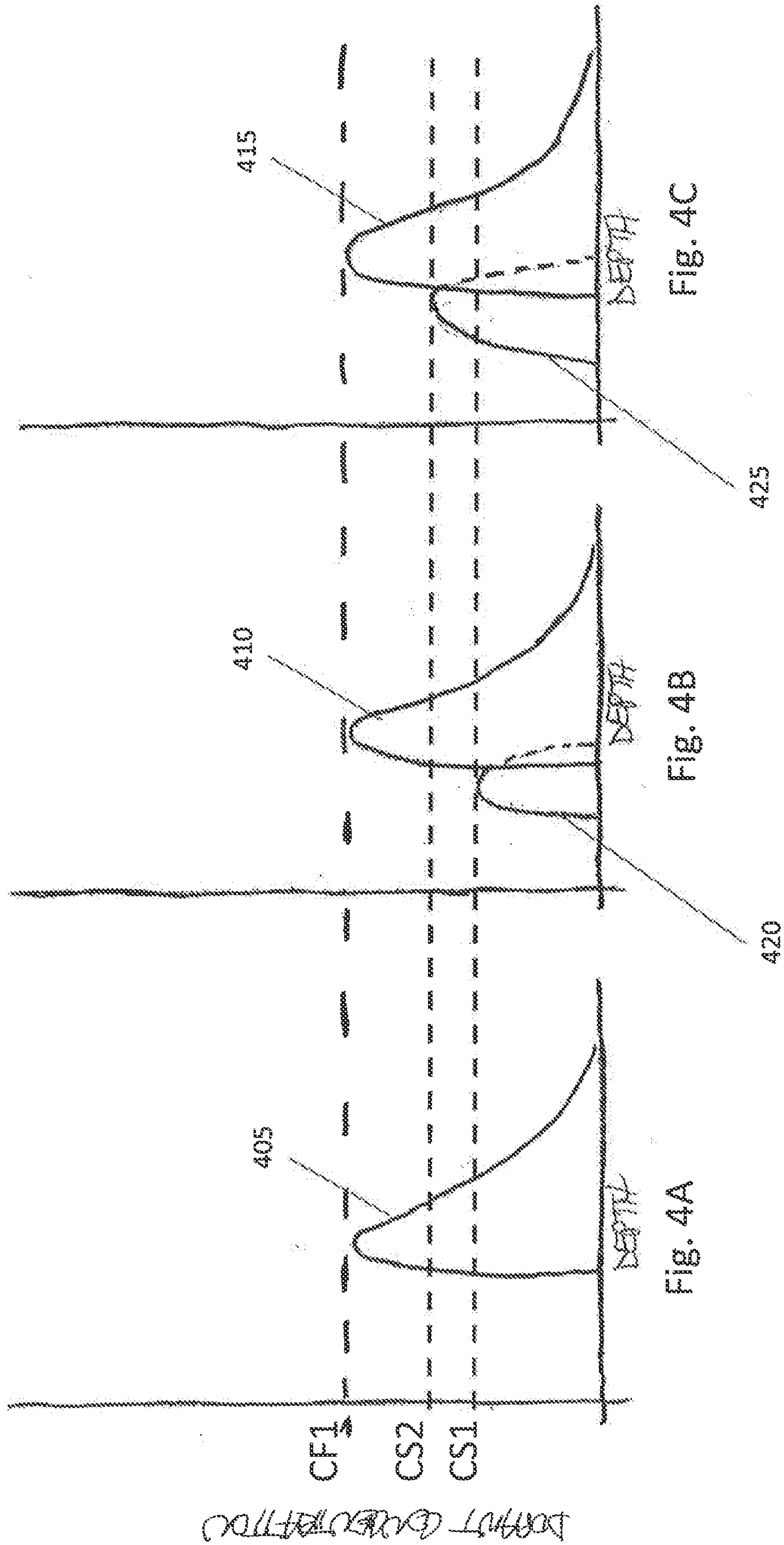


Fig. 3A

Fig. 3B

Fig. 3C


415
425
Fig. 4C
410
420
Fig. 4B
405
Fig. 4A
DEPTH
CF1
CS2
CS1

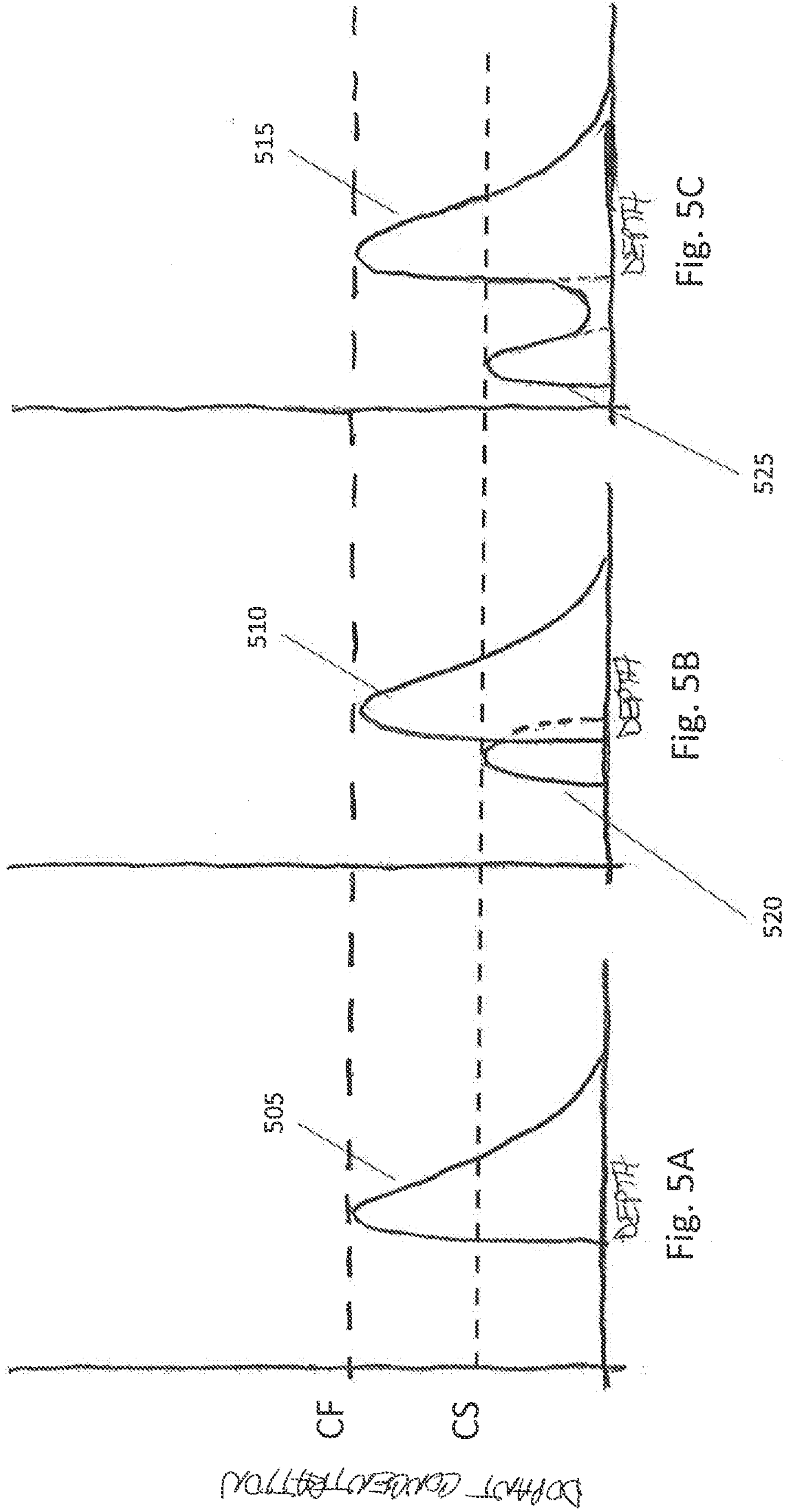


Fig. 5A

Fig. 5B

Fig. 5C

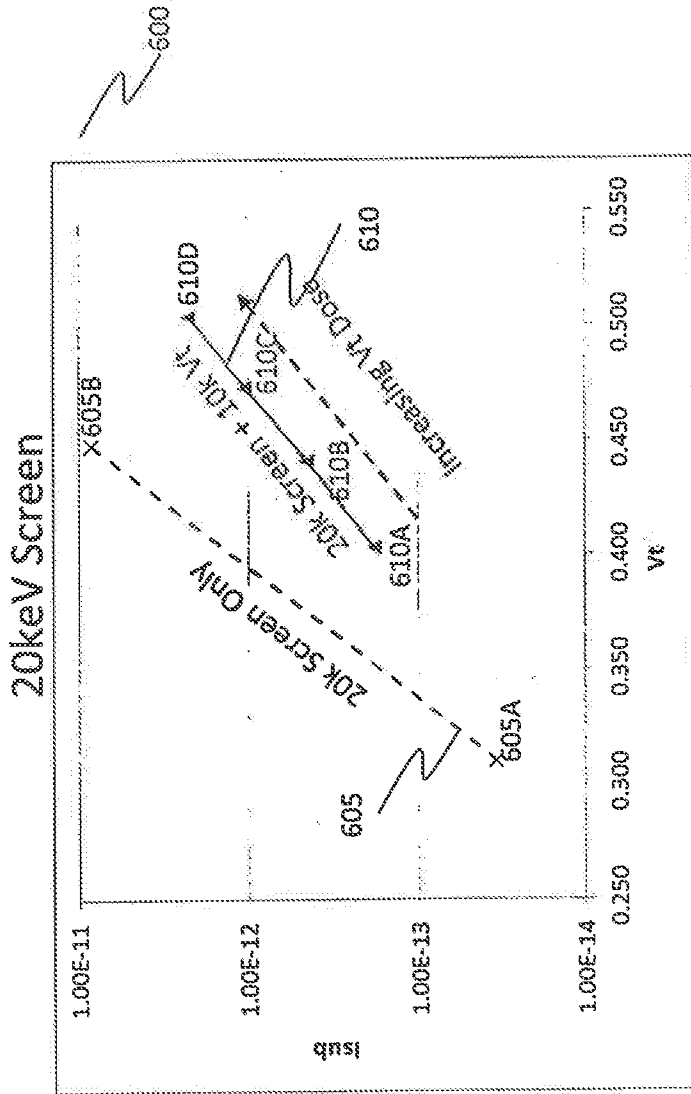


Figure 6A

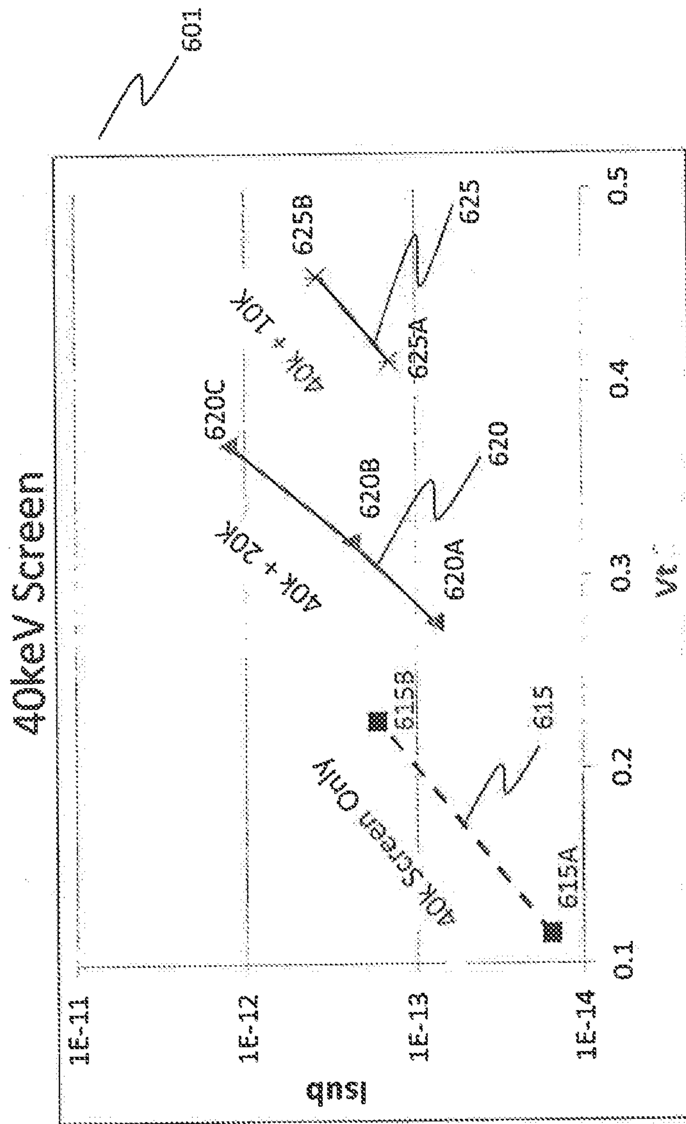


Figure 6B

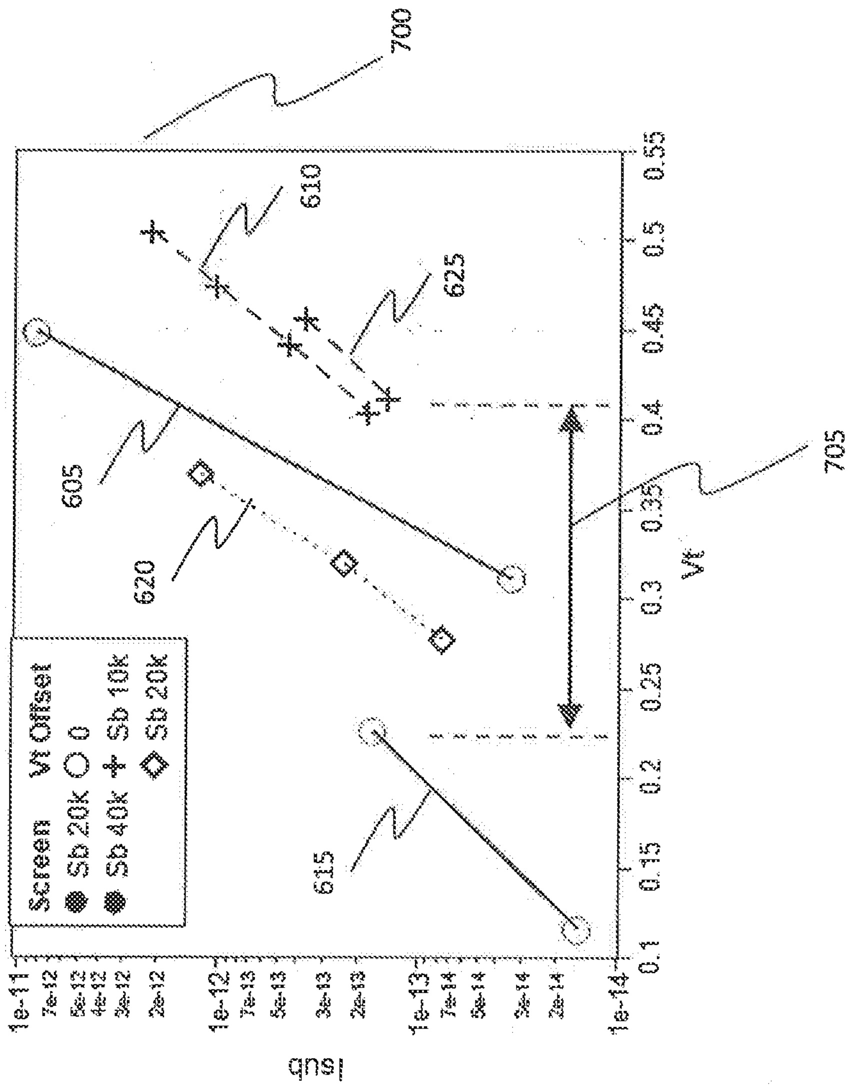


Figure 7

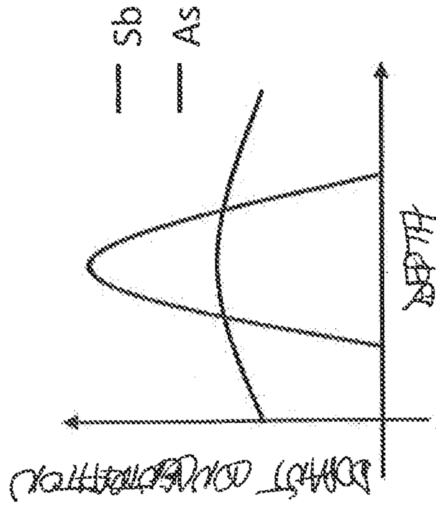


Figure 8B

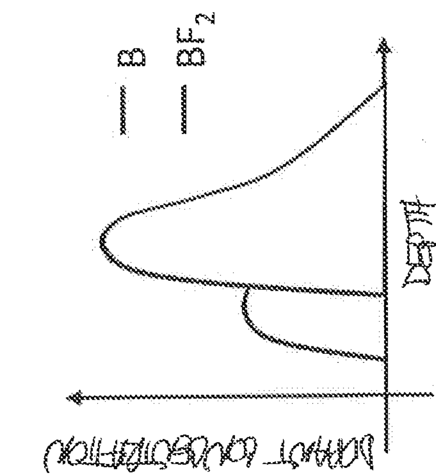
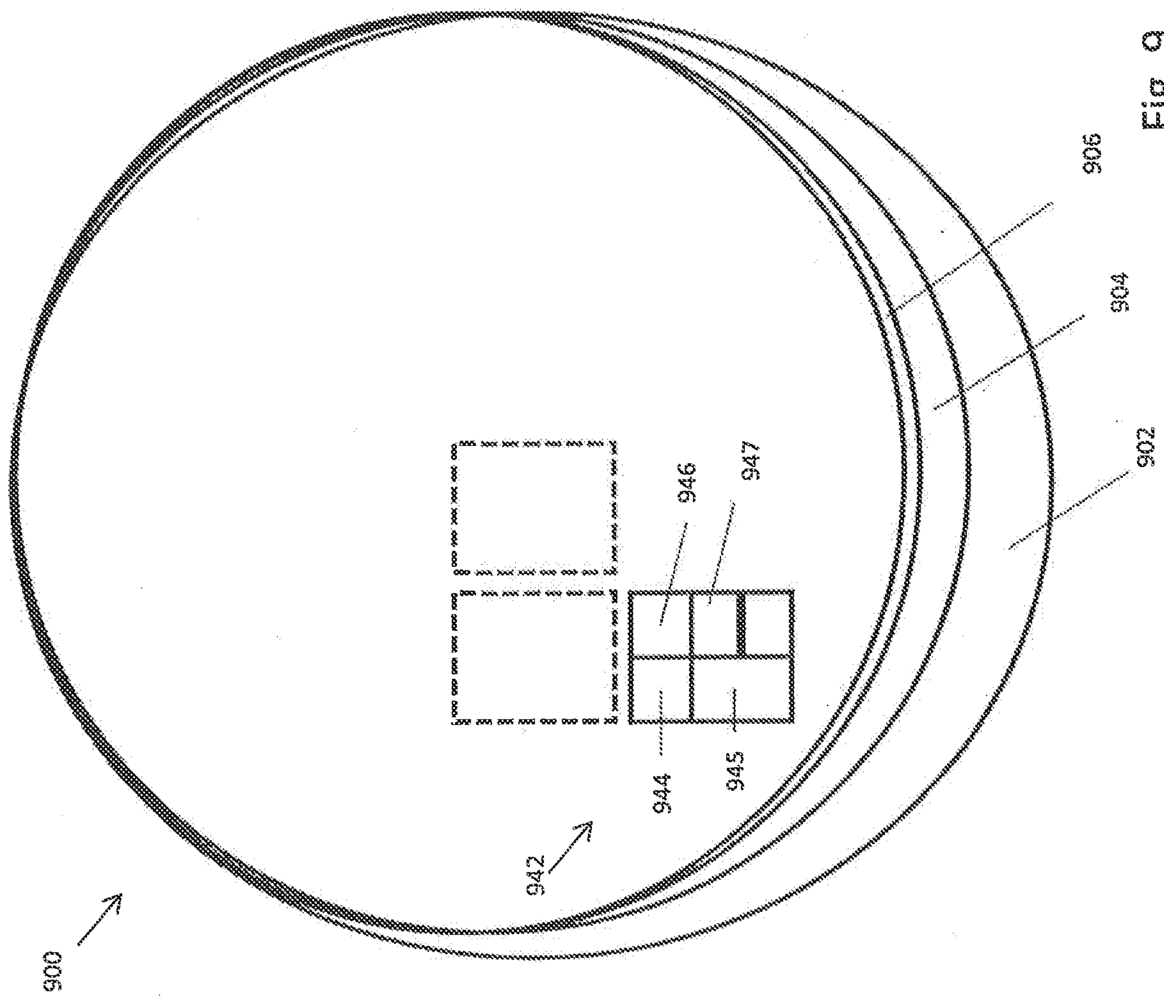


Figure 8A


900
942
944
945
946
947
902
904
906
Fig. 9

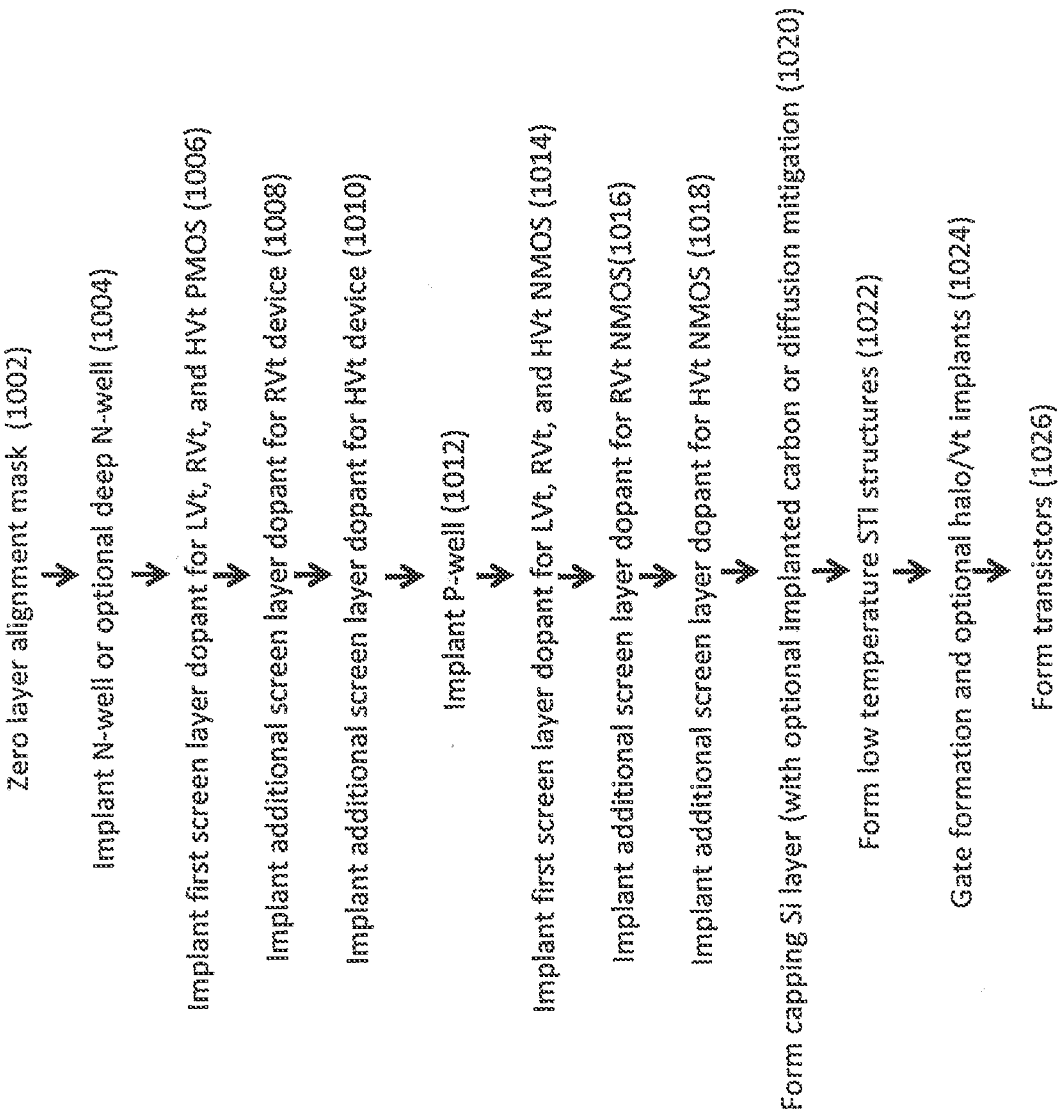


Fig. 10

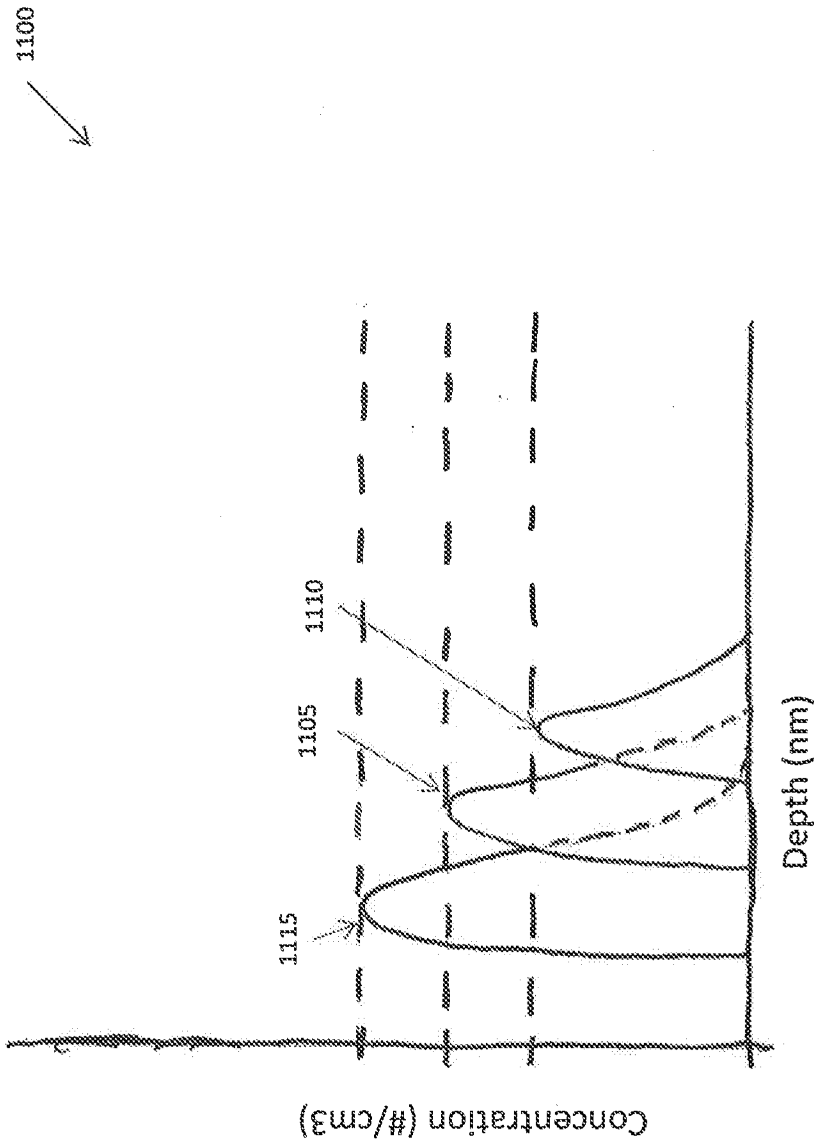


Fig. 11A

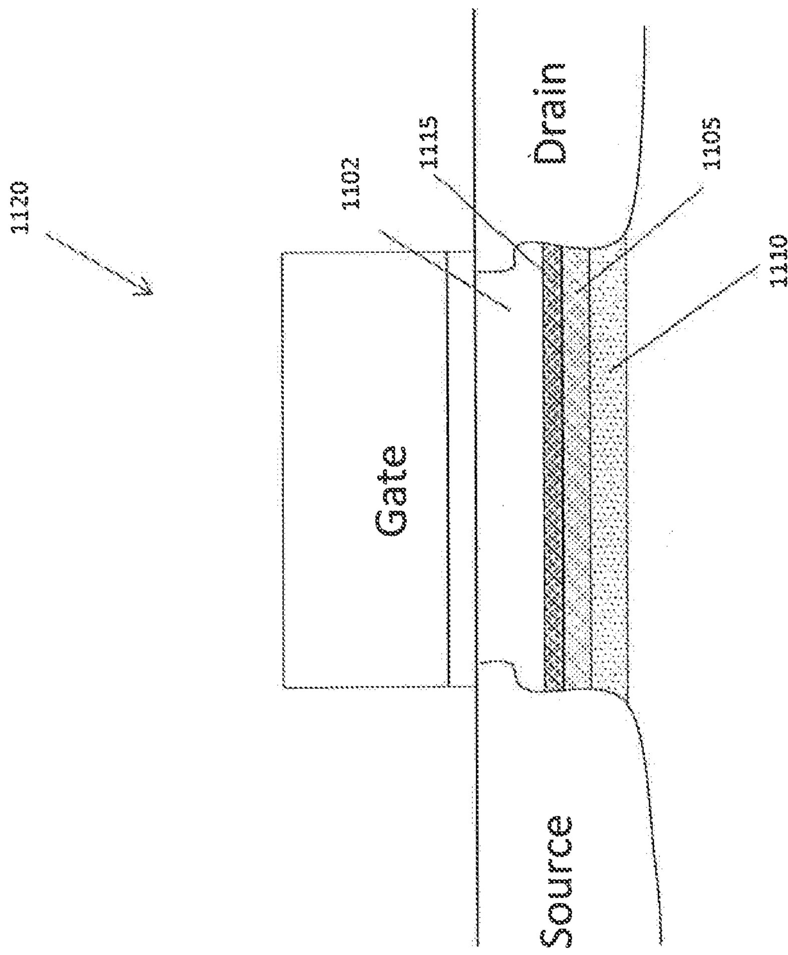


Fig. 11B

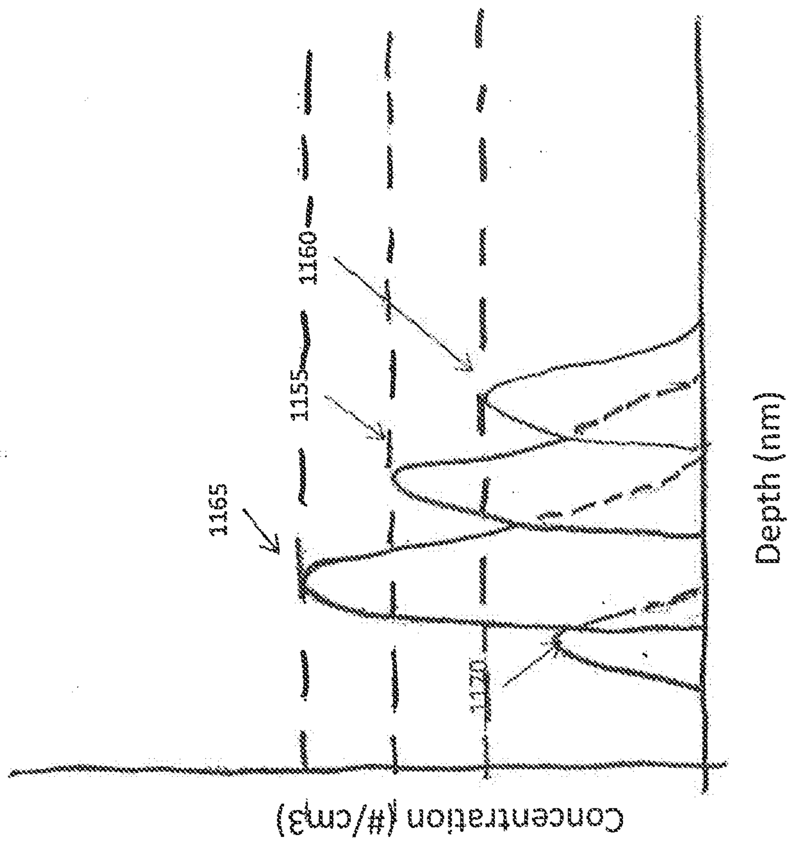


Fig. 11C

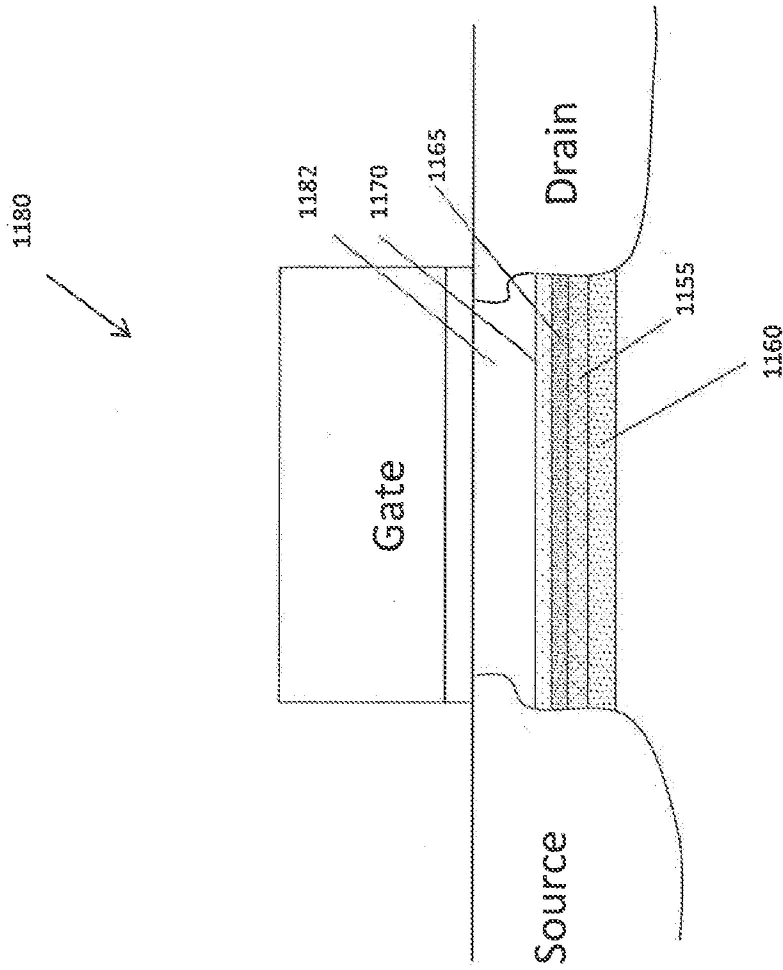


Fig. 11D

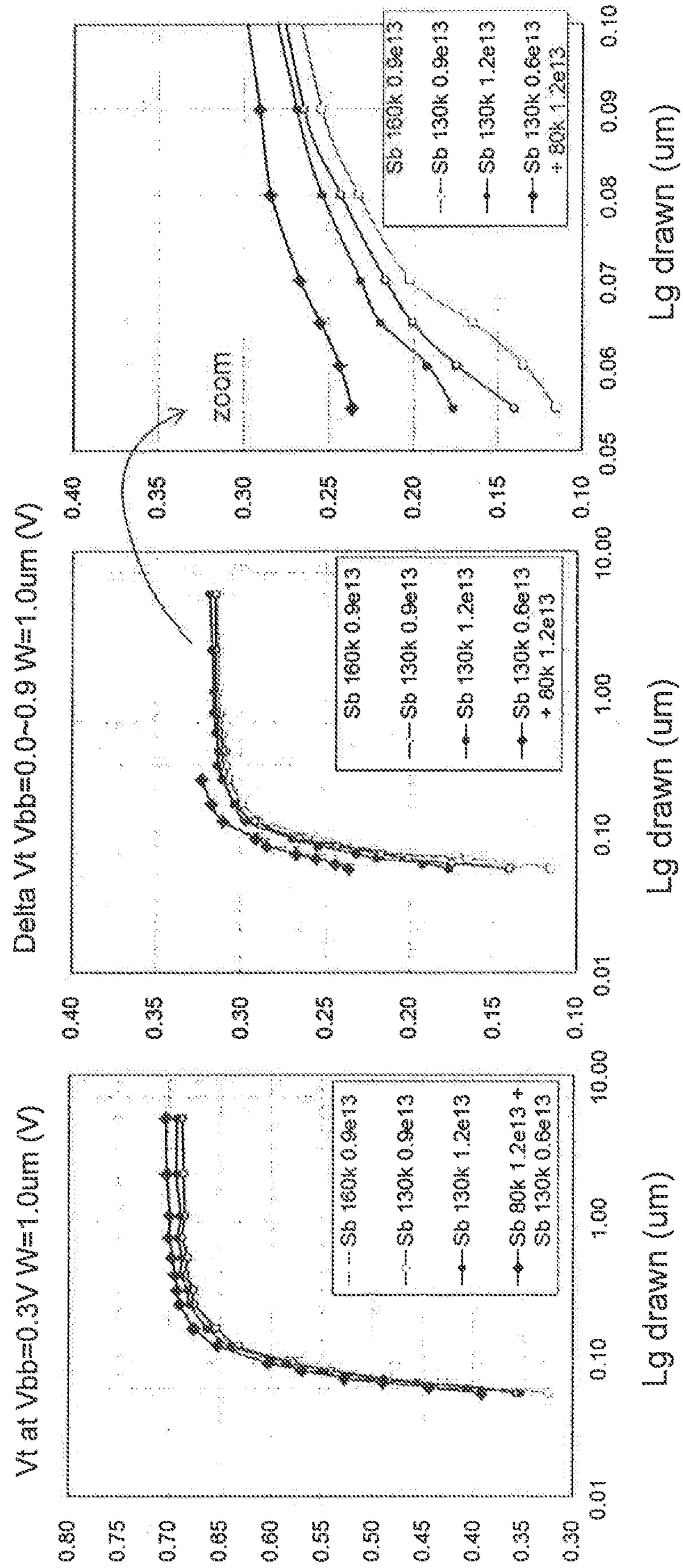


Fig. 12A

Fig. 12B

Fig. 12C

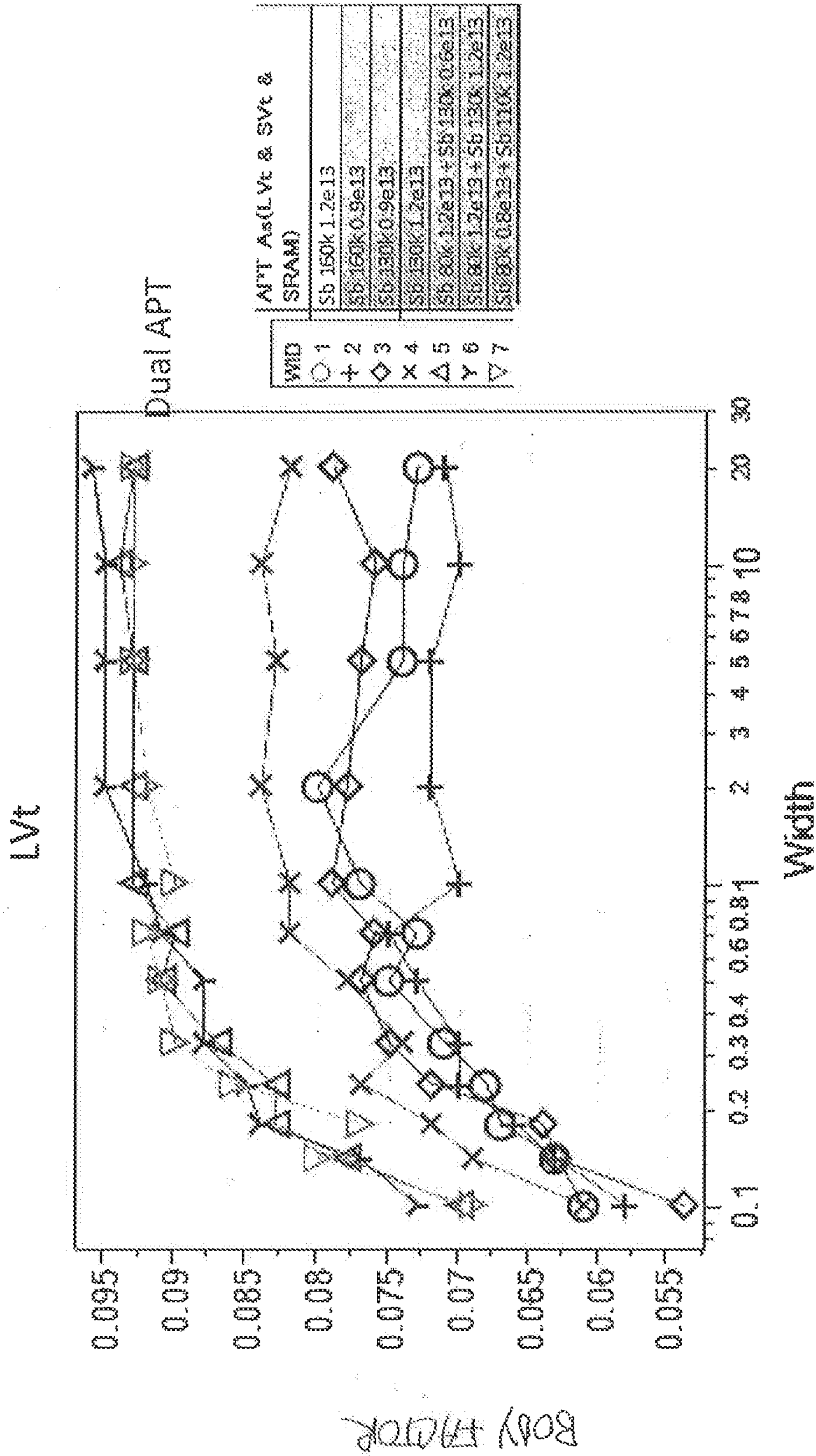


Fig. 13

Capacitance

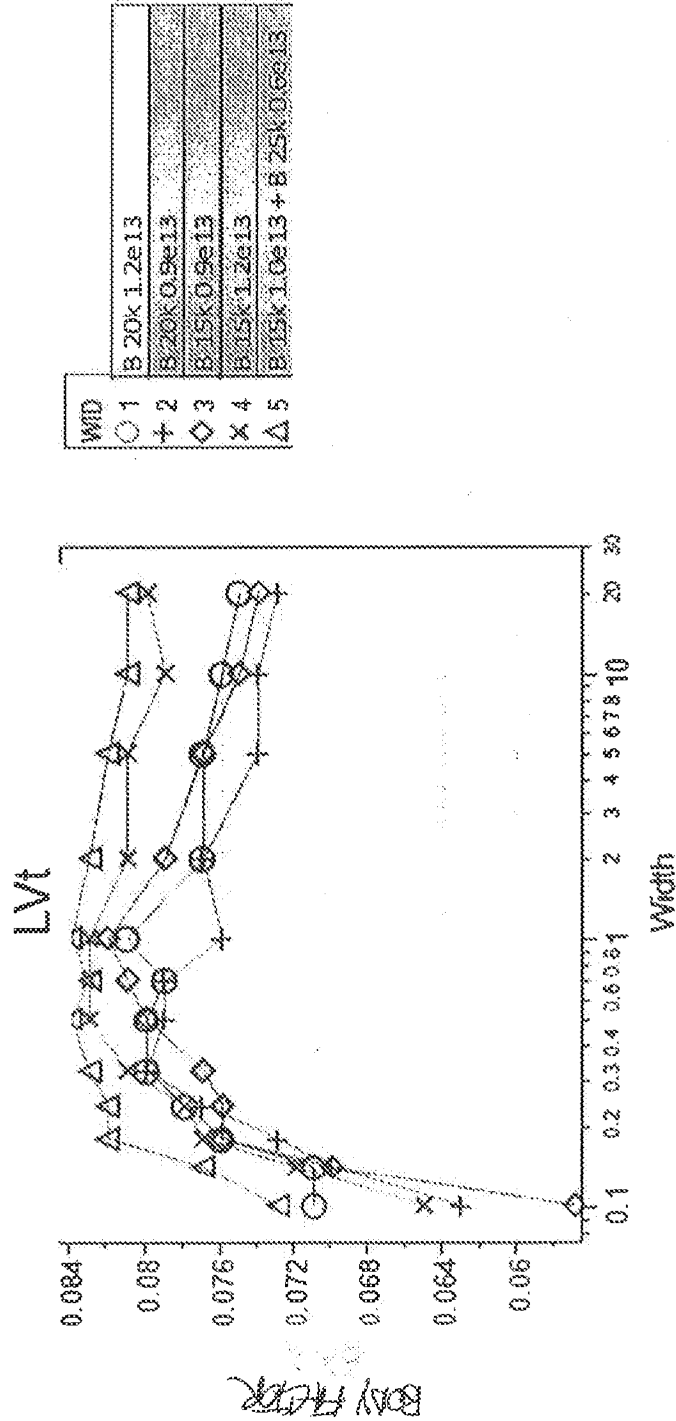


Fig. 14

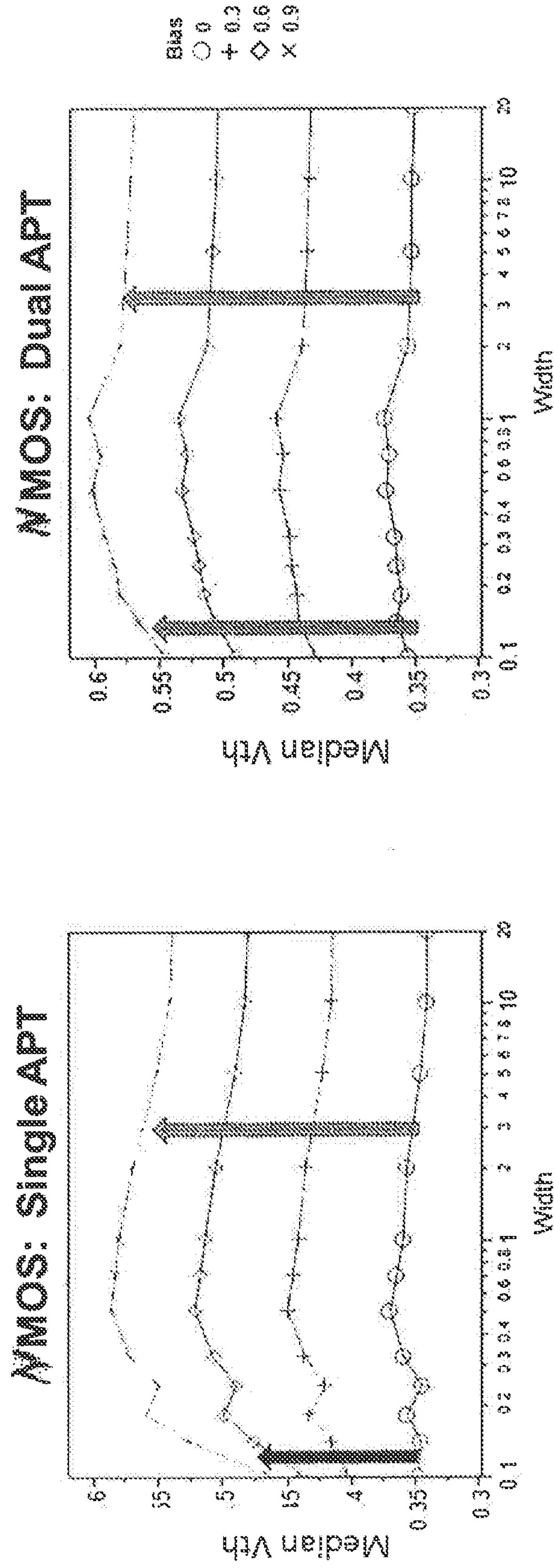


Fig. 15A

Fig. 15B

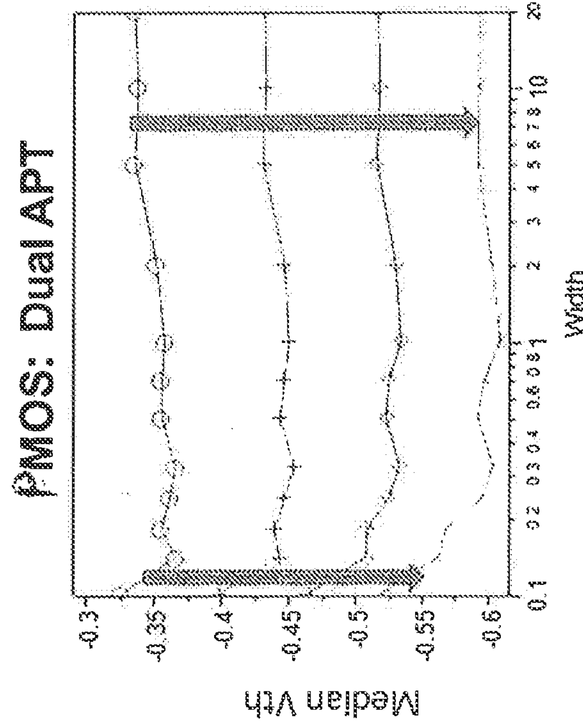


Fig. 16B

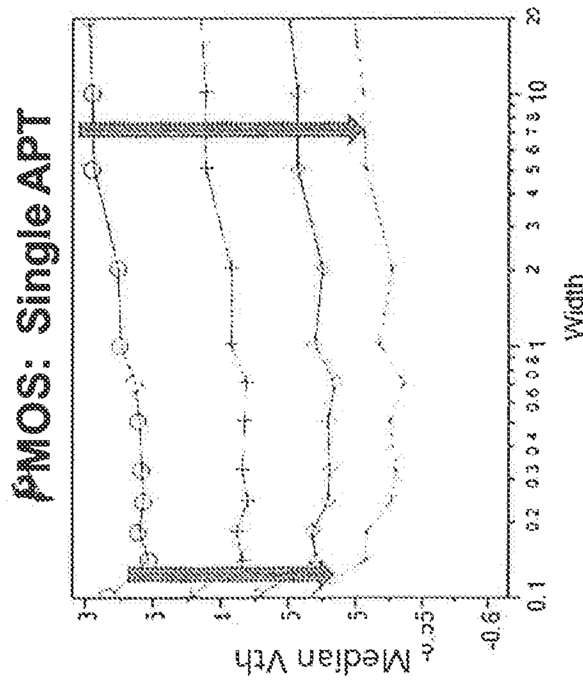


Fig. 16A

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2013/047767

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/8234 H01L27/088
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 342 413 B1 (MASUOKA SADAAKI [JP] ET AL) 29 January 2002 (2002-01-29) figures 2, 3D, 3E	11-16
X	US 2011/248352 A1 (SHIFREN LUCIAN [US] ET AL) 13 October 2011 (2011-10-13) cited in the application	1-9
Y	paragraphs [0028], [0029], [0087]; figures 8,11,12,30	10
X	US 2011/309450 A1 (SHIFREN LUCIAN [US] ET AL) 22 December 2011 (2011-12-22)	11-13,15
Y	paragraph [0039]; figure 6	14
A		16,17

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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Date of the actual completion of the international search	Date of mailing of the international search report
6 September 2013	16/09/2013

Name and mailing address of the ISA/
European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040,
Fax: (+31-70) 340-3016

Authorized officer
Seck, Martin

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	FUJITA K ET AL: "Advanced channel engineering achieving aggressive reduction of V T variation for ultra-low-power applications", ELECTRON DEVICES MEETING (IEDM), 2011 IEEE INTERNATIONAL, IEEE, 5 December 2011 (2011-12-05), pages 32.3.1-32.3.4, XP032096049, DOI: 10.1109/IEDM.2011.6131657 ISBN: 978-1-4577-0506-9 Section "DDC Transistor Structure"; figures 1(b), 2	11-13, 15,17-20
Y	US 2011/074498 A1 (THOMPSON SCOTT E [US] ET AL) 31 March 2011 (2011-03-31) paragraphs [0103] - [0105]	10
Y	US 2011/121404 A1 (SHIFREN LUCIAN [US] ET AL) 26 May 2011 (2011-05-26)	14
A	paragraphs [0020], [0021], [0033]; figures 2,3,6 abstract	4-7, 18-20

3

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2013/047767

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