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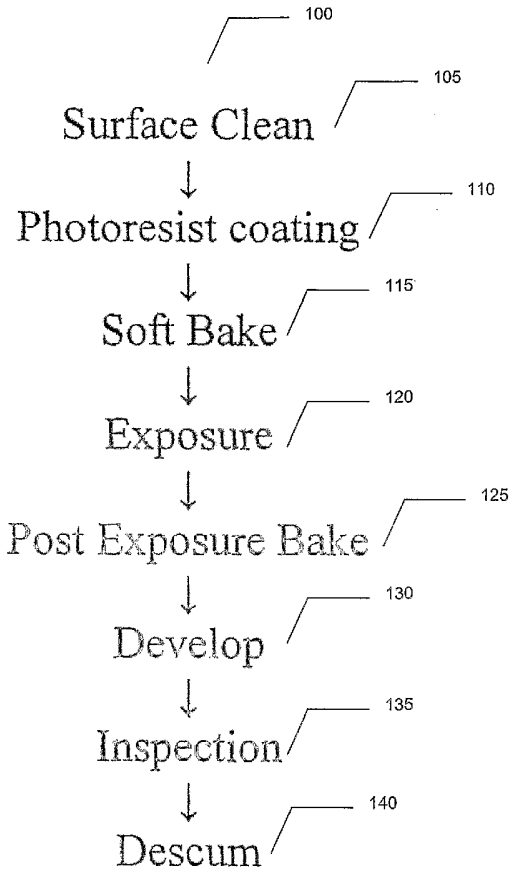
(54) Title: FABRICATION OF PARASCAN TUNABLE DIELECTRIC CHIPS



(57) Abstract: A tunable dielectric chip, and method of manufacture therefore, that comprises a dielectric substrate, the dielectric substrate patterned to a critical dimension, a metallized portion integral to the dielectric substrate, and an encapsulant covering an any portion of the dielectric substrate not covered by the metallized portion. A thin titanium layer can be deposited in between the metallized portion and the dielectric substrate to promote adhesion. The dielectric substrate can be a dielectric thick film. The thickness of the titanium can vary from 200A to 500A and the metallized portion integral to the dielectric substrate in a preferred embodiment is gold and varies in thickness from 3um to several microns depending on the application. Further, in the present preferred embodiment, the encapsulant is a photo/definable encapsulant. The present invention also provides solder pads integral to the metallized portion enabling maximum protection from moisture and other contaminants. The metallized portion discussed above in a preferred embodiment is formed by cleaning the surface of the thick film tunable dielectric, applying a photoresist coating of a thin film metal to the thick film tunable dielectric, applying a photoresist coating of a thin film metal to the thick film tunable dielectric, applying a photoresist coating of a thin film metal to the thick film tunable dielectric, soft baking the thick film tunable dielectric with the thin film metal coated thereon, exposing the thick film tunable dielectric with the thin film metal coated thereon, post exposure baking the thick film tunable dielectric with the thin film metal coated thereon; and developing the thick film tunable dielectric with the thin film metal coated thereon.

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FABRICATION OF PARASCAN TUNABLE DIELECTRIC CHIPS

CROSS-REFERENCE TO RELATED APPLICATION

This application claims priority to US Provisional Patent Application Serial No. 60/445,337, "FABRICATION OF PARASCAN TUNABLE DIELECTRIC CHIPS" filed February 05, 2003, by Chen Zang et al.

BACKGROUND OF THE INVENTION

The present invention generally relates to dielectric chips and more specifically to the fabrication of tunable dielectric chips. Still more particularly the present invention relates to the fabrication of tunable dielectric chips that are made from Paracan tunable dielectrics.

RF microwave devices made of tunable dielectrics (such as Parascan, the trademarked tunable dielectric material invented by Paratek Microwave Corporation, the assignee of the present invention) is typically screen printed on different substrates to form a thick film layer. These dielectric films have average surface roughness between O.4um to 1 um and peak to valley roughness more than 4um. A thin film layer more than 3um is required to pattern on

these rough thick films in order to make tunable RF devices. Typically, in the semiconductor industry, thin film is patterned on a smooth surface such as a polished silicon wafer and the thickness of the film is less than 1 um. Patterning a 3um or thicker thin film on rough dielectrics is a challenge.

Therefore, a strong need in the industry exists to provide the ability to pattern a 3um or thicker thin film on rough dielectrics to enable the fabrication of tunable dielectric chips that are made from Paracan tunable dielectrics.

SUMMARY OF THE INVENTION

The present invention provides a tunable dielectric chip that comprises a dielectric substrate, the dielectric substrate patterned to a critical dimension, a metallized portion integral to the dielectric substrate, and an encapsulant covering any portion of the dielectric substrate not covered by the metallized portion. A thin titanium layer can be deposited in between the metallized portion and the dielectric substrate to promote adhesion. The dielectric substrate can be a dielectric thick film. The thickness of the titanium can vary from 200A to 500A and the metallized portion integral to the dielectric substrate in a preferred embodiment is gold and varies in thickness from 3um to several microns depending on the application. Further, in the present preferred embodiment, the encapsulant is a photo-definable encapsulant. The present invention also provides solder pads integral to the metallized portion enabling maximan protection from moisture and other contaminants.

The metallized portion discussed above in a preferred embodiment is formed by cleaning the surface of the thick film tunable dielectric, applying a photoresist coating of a thin film metal to the thick film tunable dielectric, soft baking the thick film tunable dielectric with the thin film metal coated thereon, exposing the thick film tunable dielectric with the thin film metal coated thereon, post exposure baking the thick film tunable dielectric with the thin film metal coated thereon, and developing the thick film tunable dielectric with the thin film metal coated thereon.

The encapsulant covering any portion of the dielectric substrate not covered by the metallized portion is formed by surface cleaning the thick film tunable dielectric with the thin film metal coated thereon, baking the thick film tunable dielectric with the thin film metal coated thereon, adhesion promoter coating the thick film tunable dielectric with the thin film

metal coated thereon, encapsulent coating the thick film tunable dielectric with the thin film metal coated thereon, creating a thick film tunable dielectric with the thin film metal and encapsulent coated thereon, soft baking the thick film tunable dielectric with the thin film metal and encapsulent coated thereon, exposing the thick film tunable dielectric with the thin film metal and encapsulent coated thereon, pre-develop baking the thick film tunable dielectric with the thin film metal and encapsulent coated thereon, and curing the thick film tunable dielectric with the thin film metal and encapsulent coated thereon.

The solder pads integral to the metallized portion mentioned above in a preferred embodiment are formed by surface cleaning the thick film tunable dielectric with the thin film metal and encapsulent coated thereon, photoresist coating the thick film tunable dielectric with the thin film metal and encapsulent coated thereon, soft baking the thick film tunable dielectric with the thin film metal and encapsulent coated thereon, exposing the thick film tunable dielectric with the thin film metal and encapsulent coated thereon, post exposure baking the thick film tunable dielectric with the thin film metal and encapsulent coated thereon, developing the thick film tunable dielectric with the thin film metal and encapsulent coated thereon, inspecting the thick film tunable dielectric with the thin film metal and encapsulent coated thereon, descumming the thick film tunable dielectric with the thin film metal and encapsulent coated thereon, metalizing at least one solder pad on the thick film tunable dielectric with the thin film metal and encapsulent coated thereon thereby creating a thick film tunable dielectric with the thin film metal, encapsulent coating and at least one metal solder pad thereon, acetone immersing the thick film tunable dielectric with the thin film metal, encapsulent coating and at least one metal solder pad thereon, remover liftoff of the thick film tunable dielectric with the thin film metal, encapsulent coating and at least one metal solder pad thereon, inspecting the thick film tunable dielectric with the thin

film metal, encapsulent coating and metal at least one solder pad thereon, and final cleaning of the thick film tunable dielectric with the thin film metal, encapsulent coating and at least one metal solder pad thereon.

The present invention also provides for a method of fabricating tunable dielectric chips, comprising the steps of defining a critical dimension on the dielectric via patterning and metallization, and encapsulating a critical area on the critical dimension in order to protect the critical area from moisture and other contaminations. To elaborate on the first step of defining a critical dimension on the dielectric via patterning and metallization, this step can include the following sub-steps of cleaning the surface of a thick film tunable dielectric, applying a photoresist coating of a thin film metal to the thick film tunable dielectric, soft baking the thick film tunable dielectric with the thin film metal coated thereon, exposing the thick film tunable dielectric with the thin film metal coated thereon, post exposure baking the thick film tunable dielectric with the thin film metal coated thereon, developing the thick film tunable dielectric with the thin film metal coated thereon, inspecting the thick film tunable dielectric with the thin film metal coated thereon, and descumming the thick film tunable dielectric with the thin film metal coated thereon.

To elaborate on the second step of encapsulating a critical area on the critical dimension in order to protect the critical area from moisture and other contaminations, this step can include the following sub-steps of surface cleaning the thick film tunable dielectric with the thin film metal coated thereon, baking the thick film tunable dielectric with the thin film metal coated thereon, adhesion promoter coating the thick film tunable dielectric with the thin film metal coated thereon, encapsulent coating the thick film tunable dielectric with the thin film metal coated thereon, creating a thick film tunable dielectric with the thin film metal and encapsulent coated thereon, soft baking the thick film tunable dielectric with

the thin film metal and encapsulent coated thereon, exposing the thick film tunable dielectric with the thin film metal and encapsulent coated thereon, pre-develop baking the thick film tunable dielectric with the thin film metal and encapsulent coated thereon, curing the thick film tunable dielectric with the thin film metal and encapsulent coated thereon, and descumming the thick film tunable dielectric with the thin film metal and encapsulent coated thereon.

The present method can further include the step of metallizing at least one solder pad on the tunable dielectric chip. This metallizing at least one solder pad step can include the following sub-steps of surface cleaning the thick film tunable dielectric with the thin film metal and encapsulent coated thereon, photoresist coating the thick film tunable dielectric with the thin film metal and encapsulent coated thereon, soft baking the thick film tunable dielectric with the thin film metal and encapsulent coated thereon, exposing the thick film tunable dielectric with the thin film metal and encapsulent coated thereon, post exposure baking the thick film tunable dielectric with the thin film metal and encapsulent coated thereon, developing the thick film tunable dielectric with the thin film metal and encapsulent coated thereon, inspecting the thick film tunable dielectric with the thin film metal and encapsulent coated thereon, descumming the thick film tunable dielectric with the thin film metal and encapsulent coated thereon, metallizing at least one solder pad on the thick film tunable dielectric with the thin film metal and encapsulent coated thereon thereby creating a thick film tunable dielectric with the thin film metal, encapsulent coating and at least one metal solder pad thereon, acetone immersing the thick film tunable dielectric with the thin film metal, encapsulent coating and at least one metal solder pad thereon, remover liftoff of the thick film tunable dielectric with the thin film metal, encapsulent coating and at least one metal solder pad thereon, inspecting the thick film tunable dielectric with the thin

film metal, encapsulent coating and metal at least one solder pad thereon, and final cleaning of the thick film tunable dielectric with the thin film metal, encapsulent coating and at least one metal solder pad thereon.

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BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows the process flow for gap defining (step 1);

FIG. 2 shows process flow for encapsulation (step2);

FIG. 3 shows the process flow for the optional solder pad creation (step3);

FIG. 4 illustrates the schematic of finished step one;

FIG. 5 depicts the schematic of finished step two; and

FIG. 6 shows the schematic of finished step three.

DESCRIPTION OF THE PREFERRED EMBODIMENT

The applicant of the present invention has successfully developed and describes herein a technique that patterns thin film metals on thick film dielectrics which make Parascan® RF tunable devices a success.

To provide Fabrication of Parascan® tunable dielectric chips of the present invention requires three major steps. The first step is to define critical dimension (CD) on the dielectric via patterning and metallization. The second step is encapsulation in order to protect the critical area from moisture and other contaminations. The third step is creation of a solder pad. This step is optional depending on the design.

Typically, gold metallization is used for step one, due to its high conductivity as well as good corrosion resistance. However, it is understood that other metals can also be used instead of gold provided they have similar properties as gold. A thin titanium layer is deposited in between the gold and a dielectric thick film to promote adhesion. Thickness of the gold varies from 3um to several microns depending on the application of the devices. Titanium thickness can vary from 200A to 500A. A preferred embodiment of the present invention has a typical thickness of 350 A. Metal CD size for the devices starts from 4um and varies with designs. Encapsulation is conducted after step one, starting from substrate cleaning and baking. A temperature as high as 450°C is required for the baking for two purposes: bake out moisture and remove any residual photoresist that is trapped in the dielectric films. A photo-definable encapsulant is used in this case. The areas that require protection are patterned with encapsulation materials followed by curing.

After the encapsulation, the whole crystal fabrication process can be considered finished unless special solder pads are required. The process for creating solder pads is similar to step one, except the metallization metal used for this step must be compatible with the soldering material. Typically, copper is selected as the material for solder pad with a flash of gold on top for protection. Again, however, this is one preferred embodiment of the present invention and it is anticipated that other metals can be used for this step in alternate embodiments.

Turning now to the figures, FIGS 1-3 are flow charts for each step described above. FIG. 1, shown generally at 100, depicts the process flow for gap defining (step 1). The first step in the process is to prepare the surface by surface cleaning 105. Next, at 110, a photoresist is applied and soft baked at 115. The next step is exposure at 120 and then a post-exposure bake at 125. Developing takes place at 130 with an inspection following at 135. The final step is then to descum at step 140.

FIG. 2 shows process flow for encapsulation (step2). This is shown generally as 200, with the first step being surface cleaning, 205. Next is baking at 210, followed by adhesion promoter coating 215 and encapsulent coating 220. Soft baking takes place at 225 followed by exposure at 230. The step of pre-develop baking takes place at 235 and subsequenty at 240 the process includes developing and curing at 245. The final step is then to descum at step 250.

Turning now to FIG. 3, which includes the flow for the optional solder pad creation (step3). The flow is shown generally as 300, with the first step in the flow again starting with a surface cleaning at 305. Next is a photo resist coating at 310 and soft baking at 315. Exposure occurs at 320, followed by a post exposure bake at 325. Developing occurs at 330, with an inspection following at 335. Descum occurs at 340 with the metallization step

following at 345. An acetone immersion happens at 350 with a remover liftoff occurring shortly thereafter at 355. An inspection once again occurs at 360 with a final cleaning taking place next at 365.

FIG. 4 illustrates a depiction of finished step one, shown generally as 400, which includes defining the critical dimension (CD) on the dielectric 420 via patterning and metallization of metals 410 and 415 . The second step, shown as 500 of FIG. 5, is encapsulation 505 above metals 410 and 415 and above dielectric 420 in order to protect the critical area 510 from moisture and other contaminations.

In FIG 6, at 600 is the third step of creation of the optional solder pads 610 and 615. Solder pads 610 and 615 can be placed adjacent to the ecapsulation portion 505 and above metals 410 and 415 which are above dielectric 420. This provides for maximan protection from moisture and other contaminants. Again, this step is optional depending on the design.

While various embodiments of the present invention have been described above, it should be understood that they have been presented by way of example, and not limitation. It will be apparent to persons skilled in the relevant art that various changes in form and detail can be made therein without departing from the spirit and scope of the invention.

The present invention has been described above with the aid of functional building blocks illustrating the performance of specified functions and relationships thereof. The boundaries of these functional building blocks have been arbitrarily defined herein for the convenience of the description. Alternate boundaries can be defined so long as the specified functions and relationships thereof are appropriately performed. Any such alternate boundaries are thus within the scope and spirit of the claimed invention. Thus, the breadth and scope of the present invention should not be limited by any of the above-described

exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.

What is claimed is:

1. A tunable dielectric chip, comprising:

a dielectric substrate;

said dielectric substrate patterned to a critical dimension;

a metallized portion integral to said dielectric substrate; and

an encapsulant covering an any portion of said dielectric substrate not covered by said metallized portion.

2. The tunable dielectric chip of claim 1, wherein a thin titanium layer is deposited in between the metallized portion and said dielectric substrate to promote adhesion.

3. The tunable dielectric chip of claim 1, wherein said dielectric substrate is a dielectric thick film.

4. The tunable dielectric chip of claim 1, wherein said encapsulant is a photo-definable encapsulant.

5. The tunable dielectric chip of claim 1, further comprising solder pads integral to said metallized portion enabling maximan protection from moisture and other contaminants.

6. The tunable dielectric chip of claim 2, wherein the thickness of said Titanium varies from 200A to 500A.

7. The tunable dielectric chip of claim 1, wherein said metallized portion integral to said dielectric substrate varies in thickness from 3um to several microns depending on the application.

8. The tunable dielectric chip of claim 7, wherein said metallized portion integral to said dielectric substrate is gold.

9. The tunable dielectric chip of claim 1, wherein said tunable dielectric chip has a typical thickness of 350 A.

10. The tunable dielectric chip of claim 9, wherein the metal critical dimension size starts from 4um.

11. A method of fabricating tunable dielectric chips, comprising the steps of:

(a) defining a critical dimension on the dielectric via patterning and metallization; and

(b) encapsulating a critical area on said critical dimension in order to protect the critical area from moisture and other contaminations

12. The method of fabricating tunable dielectric chips of claim 11, wherein step (a), comprises the steps of:

cleaning the surface of a thick film tunable dielectric;

applying a photoresist coating of a thin film metal to said thick film tunable dielectric;

soft baking said thick film tunable dielectric with the thin film metal coated thereon;

exposing said thick film tunable dielectric with the thin film metal coated thereon;

post exposure baking said thick film tunable dielectric with the thin film metal coated thereon; and

developing said thick film tunable dielectric with the thin film metal coated thereon.

13. The method of fabricating tunable dielectric chips of claim 12, wherein step (a) further comprises the steps of:

inspecting said thick film tunable dielectric with the thin film metal coated thereon; and

descumming said thick film tunable dielectric with the thin film metal coated thereon.

14. The method of fabricating tunable dielectric chips of claim 12, wherein step (b), comprises the steps of:

surface cleaning said thick film tunable dielectric with the thin film metal coated thereon;

baking said thick film tunable dielectric with the thin film metal coated thereon;

adhesion promoter coating said thick film tunable dielectric with the thin film metal coated thereon;

encapsulent coating said thick film tunable dielectric with the thin film metal coated thereon, creating a thick film tunable dielectric with the thin film metal and encapsulent coated thereon;

soft baking said thick film tunable dielectric with the thin film metal and encapsulent coated thereon;

exposing said thick film tunable dielectric with the thin film metal and encapsulent coated thereon;

pre-develop baking said thick film tunable dielectric with the thin film metal and encapsulent coated thereon; and

curing said thick film tunable dielectric with the thin film metal and encapsulent coated thereon.

15. The method of fabricating tunable dielectric chips of claim 14, wherein step (b) further comprises the step of descumming said thick film tunable dielectric with the thin film metal and encapsulent coated thereon.

16. The method of fabricating tunable dielectric chips of claim 14, further comprising the step of:

(c) metallizing at least one solder pad on said tunable dielectric chip.

17. The method of fabricating tunable dielectric chips of claim 16, wherein step (c), comprises the steps of:

surface cleaning said thick film tunable dielectric with the thin film metal and encapsulent coated thereon;

photoresist coating said thick film tunable dielectric with the thin film metal and encapsulent coated thereon;

soft baking said thick film tunable dielectric with the thin film metal and encapsulent coated thereon;

exposing said thick film tunable dielectric with the thin film metal and encapsulent coated thereon;

post exposure baking said thick film tunable dielectric with the thin film metal and encapsulent coated thereon;

developing said thick film tunable dielectric with the thin film metal and encapsulent coated thereon;

inspecting said thick film tunable dielectric with the thin film metal and encapsulent coated thereon;

descumming said thick film tunable dielectric with the thin film metal and encapsulent coated thereon;

metalizing at least one solder pad on said thick film tunable dielectric with the thin film metal and encapsulent coated thereon thereby creating a thick film tunable dielectric with the thin film metal, encapsulent coating and at least one metal solder pad thereon;

acetone immersing said thick film tunable dielectric with the thin film metal, encapsulent coating and at least one metal solder pad thereon;

remover liftoff of said thick film tunable dielectric with the thin film metal, encapsulent coating and at least one metal solder pad thereon;

inspecting said thick film tunable dielectric with the thin film metal, encapsulent coating and metal at least one solder pad thereon; and

final cleaning of said thick film tunable dielectric with the thin film metal, encapsulent coating and at least one metal solder pad thereon.

18. A tunable dielectric chip, comprising:

a thick film dielectric;

said thick film dielectric patterned to a critical dimension;

a metallized portion integral to said thick film dielectric, said metalized portion formed by:

cleaning the surface of said thick film tunable dielectric;

applying a photoresist coating of a thin film metal to said thick film tunable dielectric;

soft baking said thick film tunable dielectric with the thin film metal coated thereon;

exposing said thick film tunable dielectric with the thin film metal coated thereon;

post exposure baking said thick film tunable dielectric with the thin film metal coated thereon; and

developing said thick film tunable dielectric with the thin film metal coated thereon;

and

an encapsulant covering an any portion of said dielectric substrate not covered by said metallized portion, said encapsulant formed by:

surface cleaning said thick film tunable dielectric with the thin film metal coated thereon;

baking said thick film tunable dielectric with the thin film metal coated thereon;

adhesion promoter coating said thick film tunable dielectric with the thin film metal coated thereon;

encapsulent coating said thick film tunable dielectric with the thin film metal coated thereon, creating a thick film tunable dielectric with the thin film metal and encapsulent coated thereon;

soft baking said thick film tunable dielectric with the thin film metal and encapsulent coated thereon;

exposing said thick film tunable dielectric with the thin film metal and encapsulent coated thereon;

pre-develop baking said thick film tunable dielectric with the thin film metal and encapsulent coated thereon; and

curing said thick film tunable dielectric with the thin film metal and encapsulent coated thereon.

19. The tunable dielectric chip of claim 18, further comprising solder pads integral to said metallized portion, said solder pads formed by:

surface cleaning said thick film tunable dielectric with the thin film metal and encapsulent coated thereon;

photoresist coating said thick film tunable dielectric with the thin film metal and encapsulent coated thereon;

soft baking said thick film tunable dielectric with the thin film metal and encapsulent coated thereon;

exposing said thick film tunable dielectric with the thin film metal and encapsulent coated thereon;

post exposure baking said thick film tunable dielectric with the thin film metal and encapsulent coated thereon;

developing said thick film tunable dielectric with the thin film metal and encapsulent coated thereon;

inspecting said thick film tunable dielectric with the thin film metal and encapsulent coated thereon;

descumming said thick film tunable dielectric with the thin film metal and encapsulent coated thereon;

metalizing at least one solder pad on said thick film tunable dielectric with the thin film metal and encapsulent coated thereon thereby creating a thick film tunable dielectric with the thin film metal, encapsulent coating and at least one metal solder pad thereon;

acetone immersing said thick film tunable dielectric with the thin film metal, encapsulent coating and at least one metal solder pad thereon;

remover liftoff of said thick film tunable dielectric with the thin film metal, encapsulent coating and at least one metal solder pad thereon;

inspecting said thick film tunable dielectric with the thin film metal, encapsulent coating and metal at least one solder pad thereon; and

final cleaning of said thick film tunable dielectric with the thin film metal, encapsulent coating and at least one metal solder pad thereon.

20. The tunable dielectric chip of claim 19, wherein a thin titanium layer is deposited in between the metallized portion and said dielectric substrate to promote adhesion.

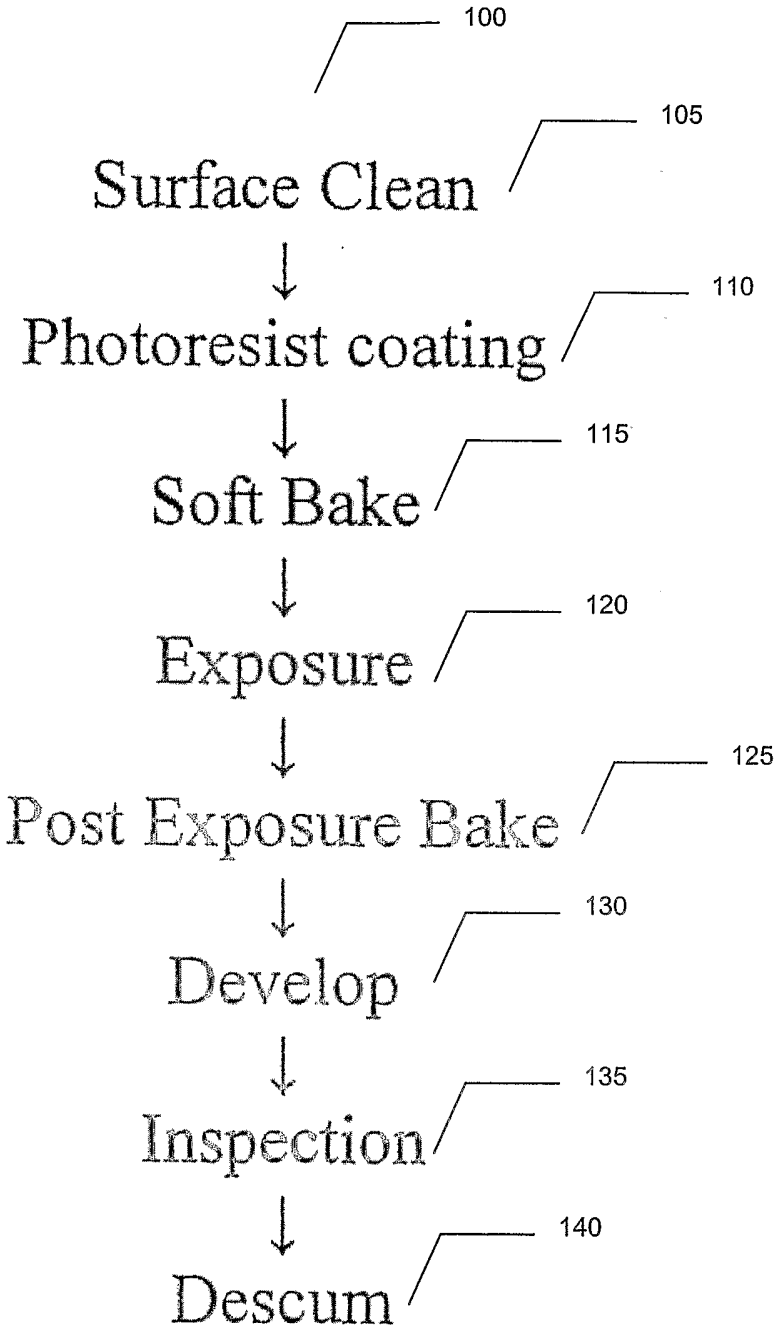

100
105
Surface Clean
110
Photoresist coating
115
Soft Bake
120
Exposure
125
Post Exposure Bake
130
Develop
135
Inspection
140
Descum

FIG. 1

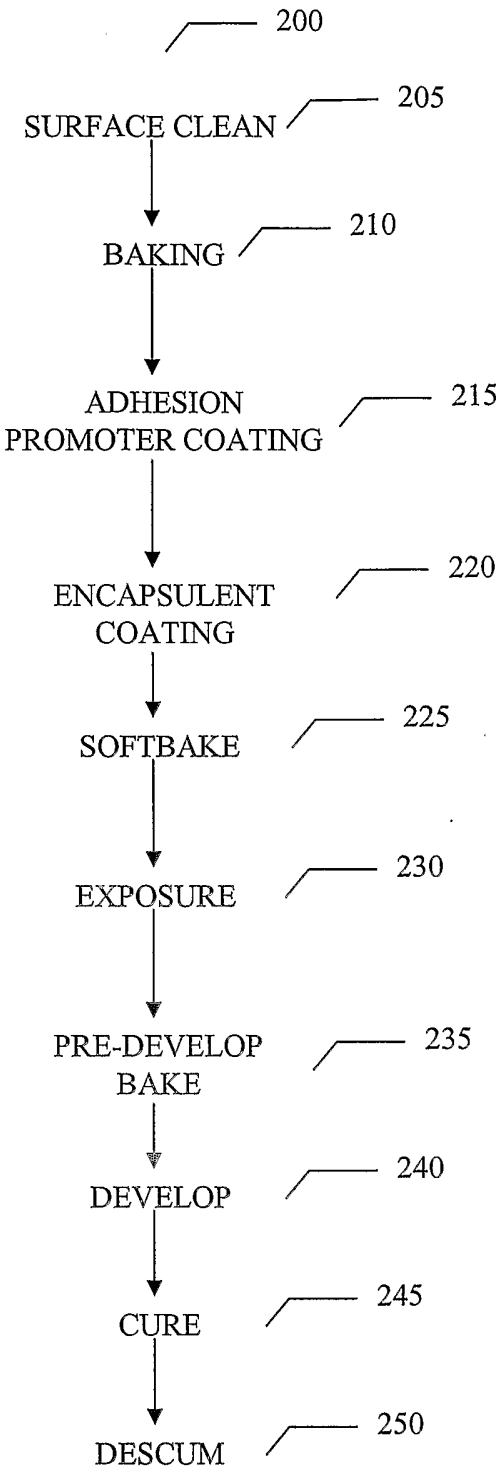
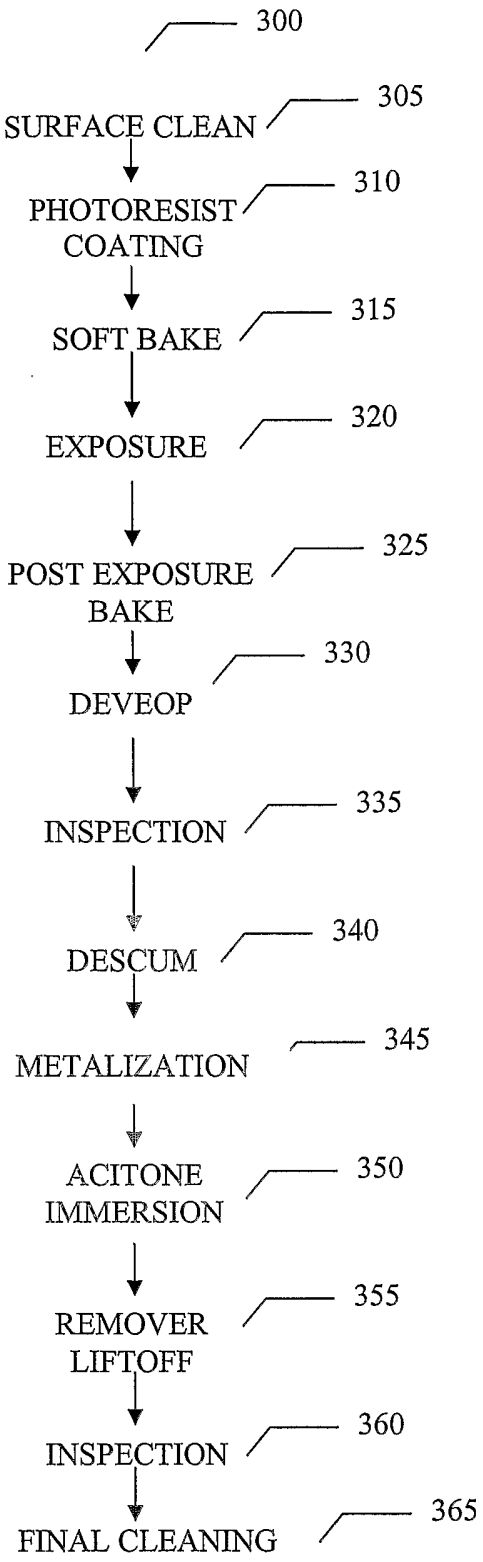

200
SURFACE CLEAN
205
BAKING
210
ADHESION PROMOTER COATING
215
ENCAPSULENT COATING
220
SOFTBAKE
225
EXPOSURE
230
PRE-DEVELOP BAKE
235
DEVELOP
240
CURE
245
DESCUM
250

FIG. 2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SURFACE CLEAN
305
PHOTORESIST COATING
310
SOFT BAKE
315
EXPOSURE
320
POST EXPOSURE BAKE
325
DEVEOP
330
INSPECTION
335
DESCUM
340
METALIZATION
345
ACITONE IMMERSION
350
REMOVER LIFTOFF
355
INSPECTION
360
FINAL CLEANING
365

FIG. 3

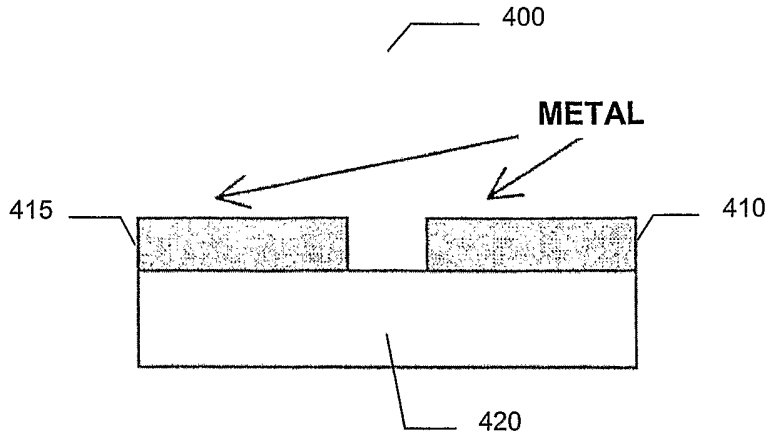

FIG. 4

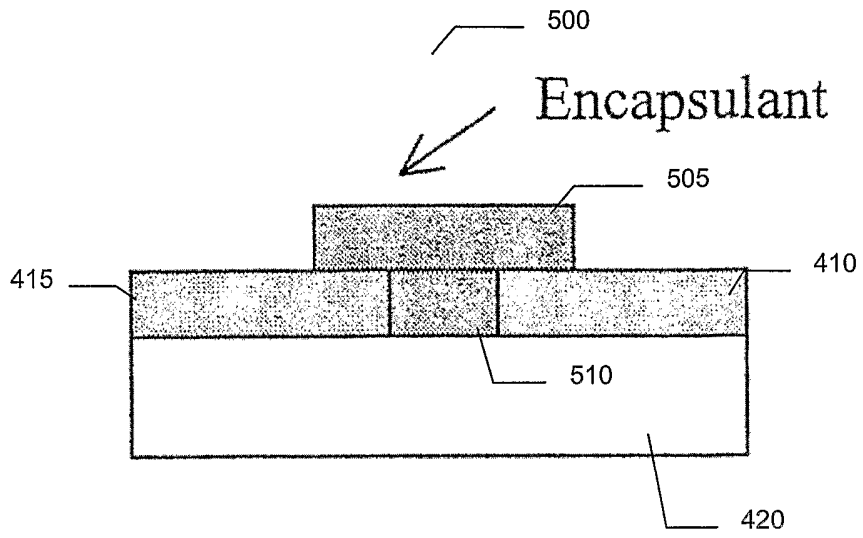

FIG. 5

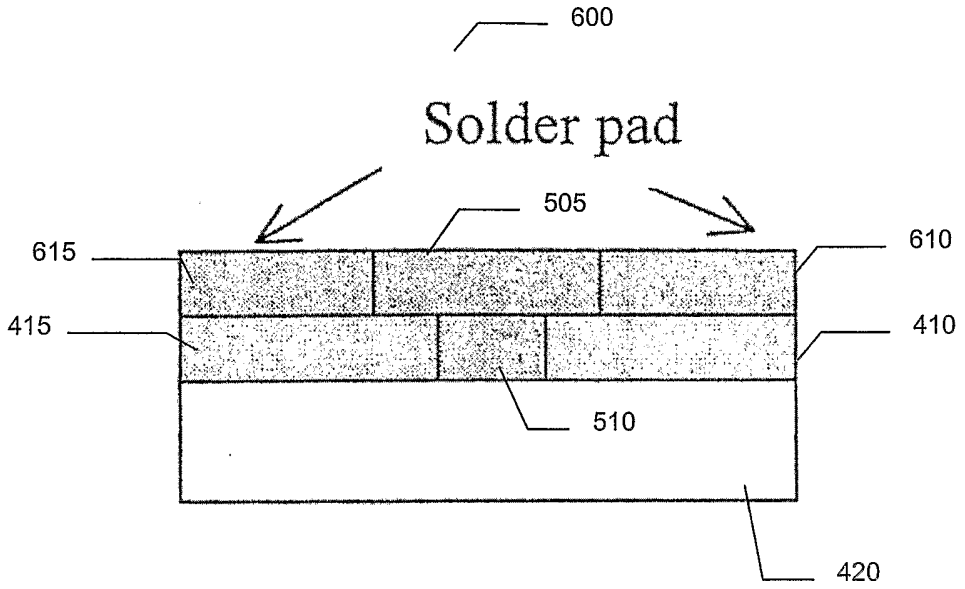

FIG. 6