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(54) THIN FILM TRANSISTORS AND METHODS OF FORMING THIN FILM TRANSISTORS

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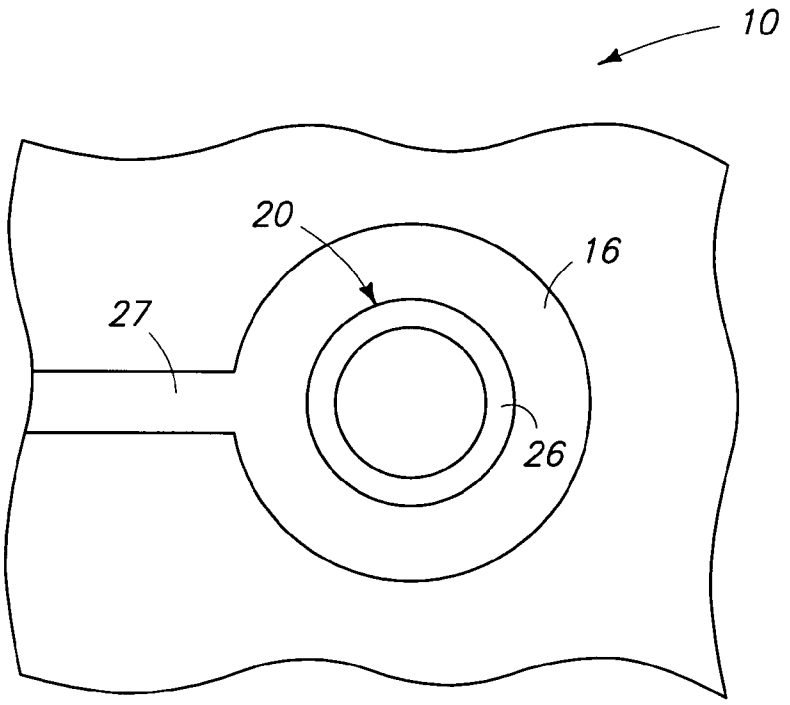
(57) **ABSTRACT**

A method of forming a thin film transistor over a substrate is provided whereby at least one of the source region or the drain region is conductively doped while preventing conductivity doping of the channel region without any masking of the channel region occurring by any separate masking layer. A method includes, a) providing a substrate having a node to which electrical connection is to be made; b) providing a first electrically insulative dielectric layer over the substrate; c) providing an electrically conductive gate layer over the first dielectric layer; d) providing a second electrically insulative dielectric layer over the electrically conductive gate layer; e) providing a contact opening through the second dielectric layer, the electrically conductive gate layer and the first dielectric layer; the contact opening defining projecting sidewalls; f) providing a gate dielectric layer within the contact opening laterally inward of the projecting sidewalls; g) providing a layer of semiconductive material over the second dielectric layer and within the contact opening against the gate dielectric layer and in electrical communication with the node; the semiconductive material within the contact opening defining an elongated and outwardly extending channel region the electrical conductance of which can be modulated by means of the adjacent electrically conductive gate and gate dielectric layers; and h) conductively doping the semiconductive material layer lying outwardly of the contact opening to form one of a source region or a drain region of a thin film transistor. Thin film transistor constructions are also disclosed.



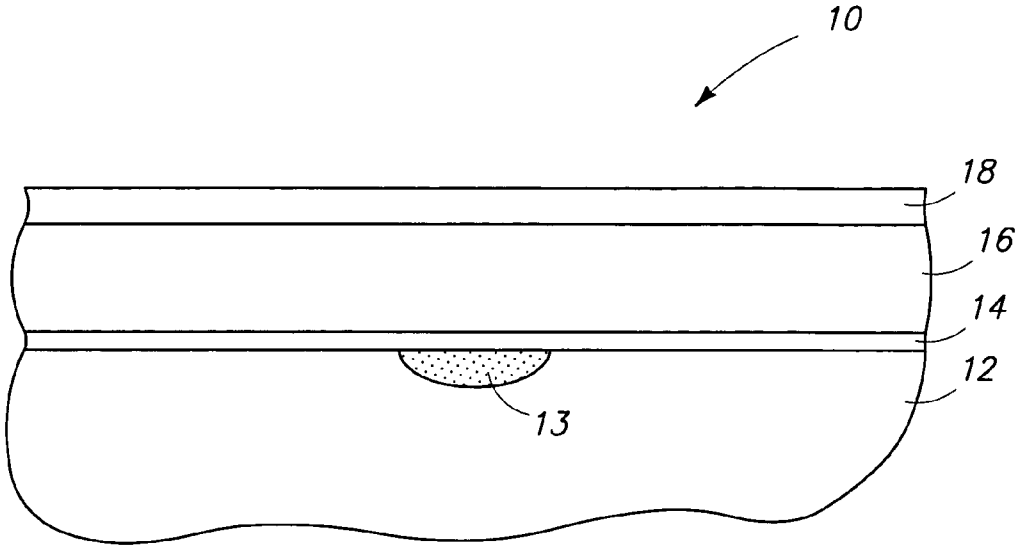


Fig. 1

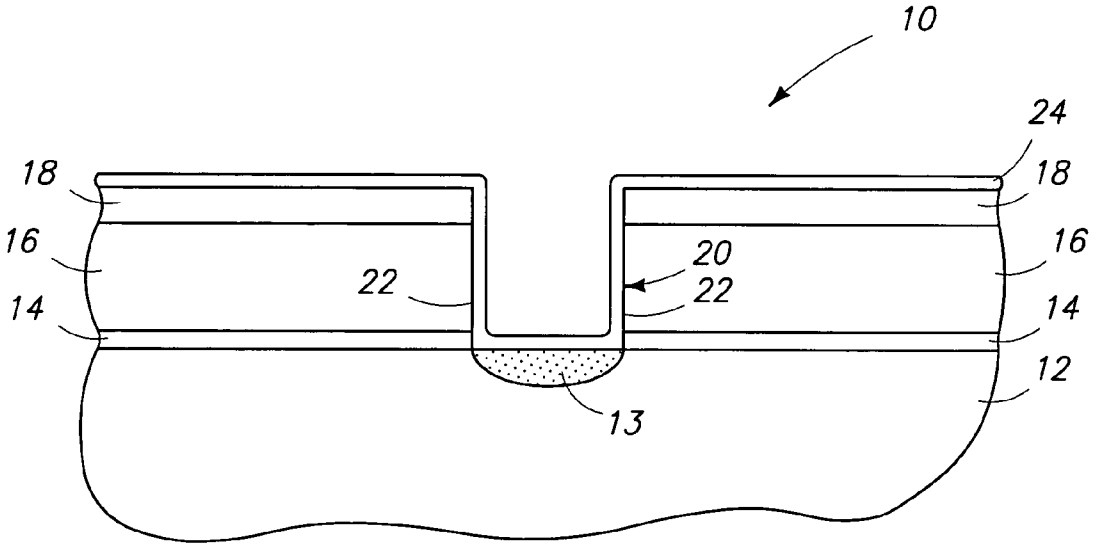


Fig. 2

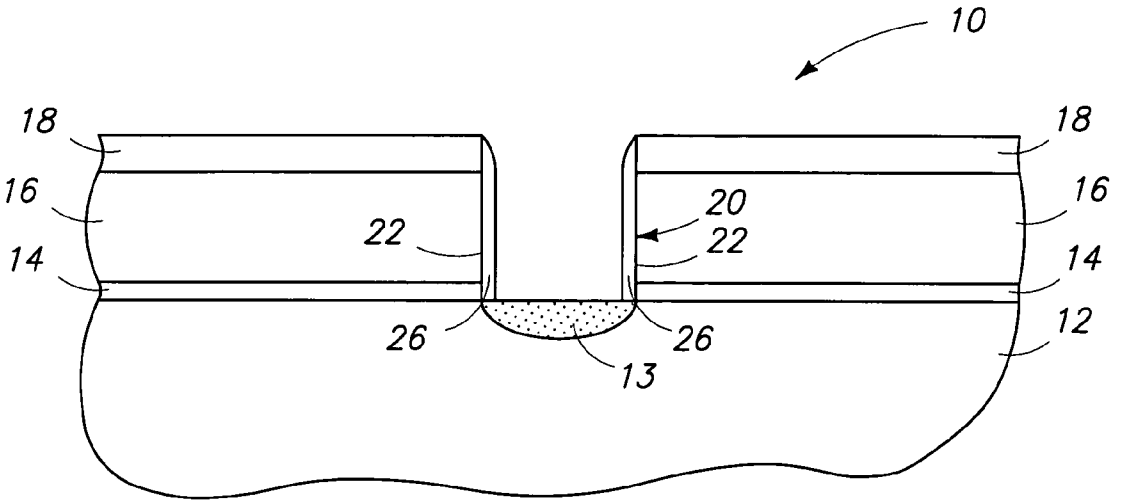


Fig 3

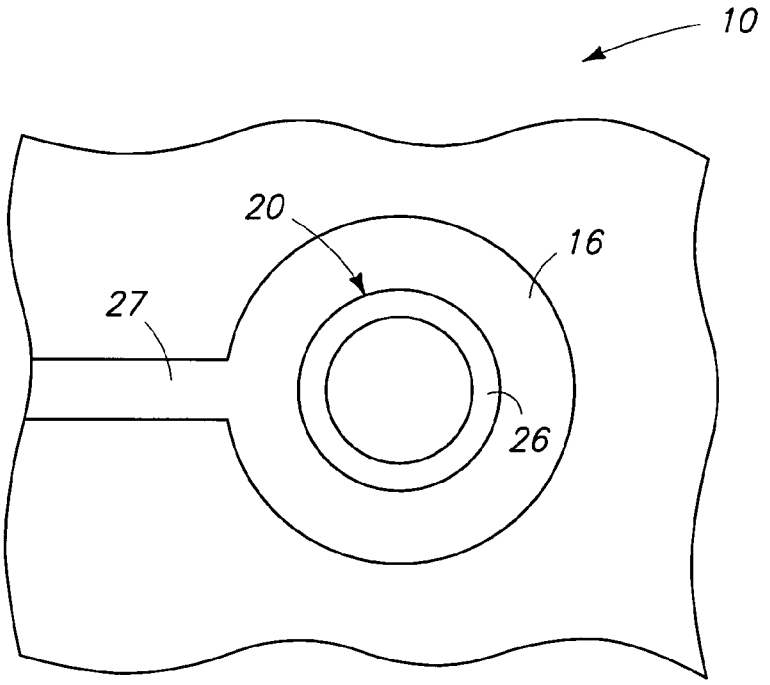
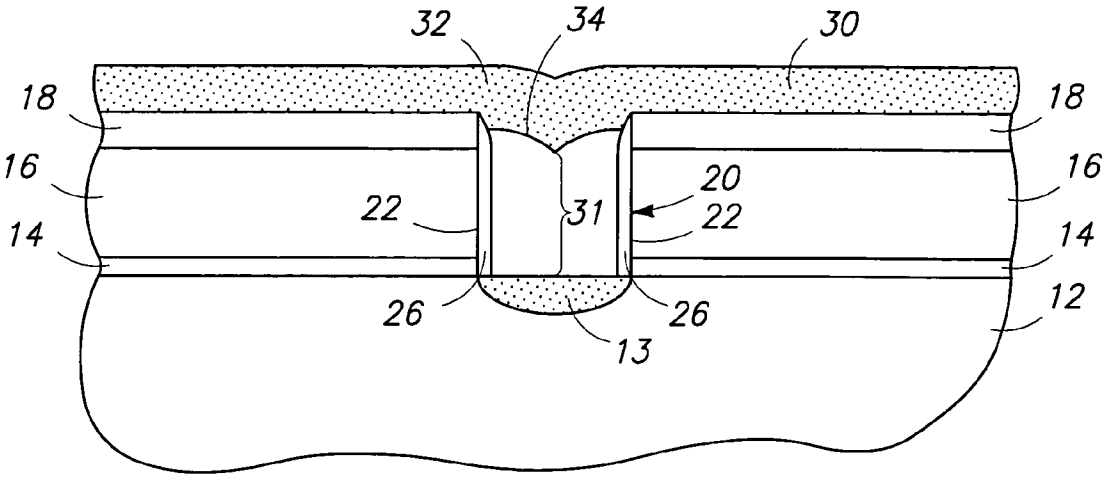


Fig 4


32
34
30
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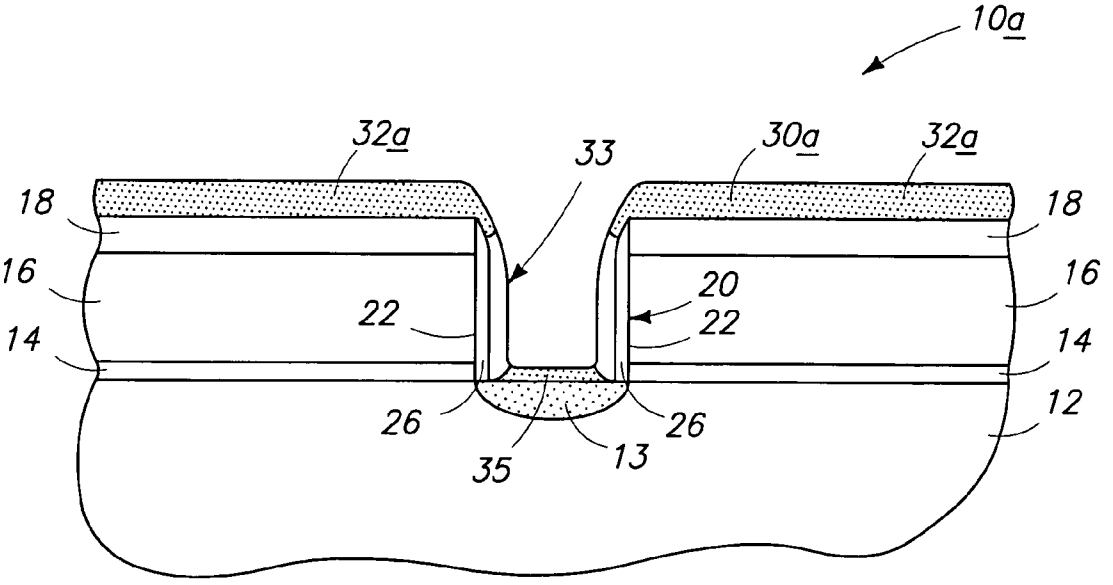
18
16
16
20
22
31
22
14
14
26
26
12
13

Fig 5


10a
32a
33
30a
32a
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18
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16
20
22
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14
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26
26
12
35
13

Fig 6

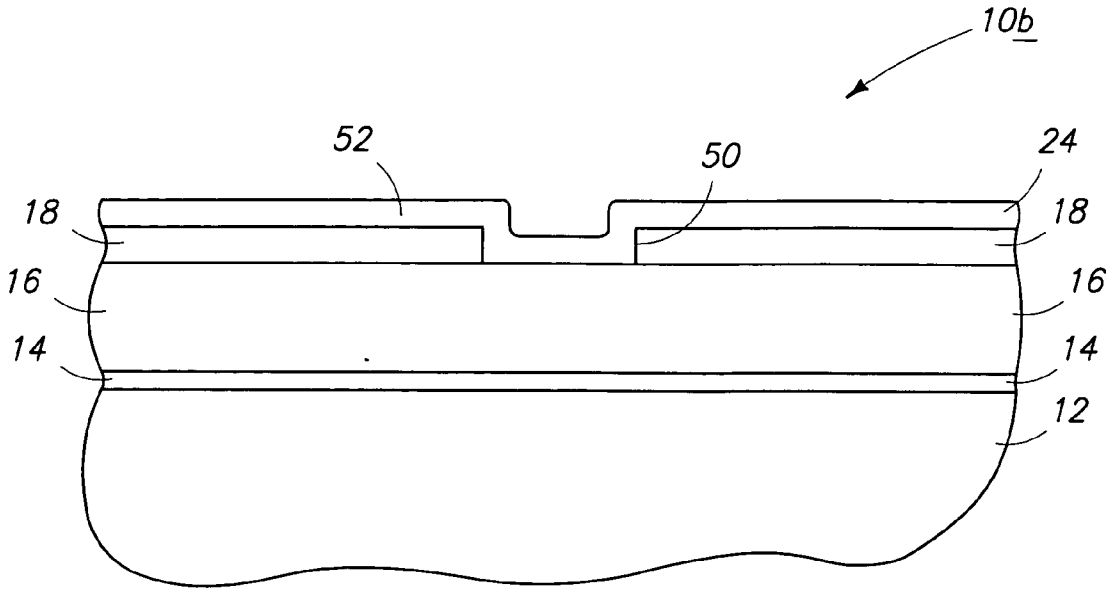

Fig. 7

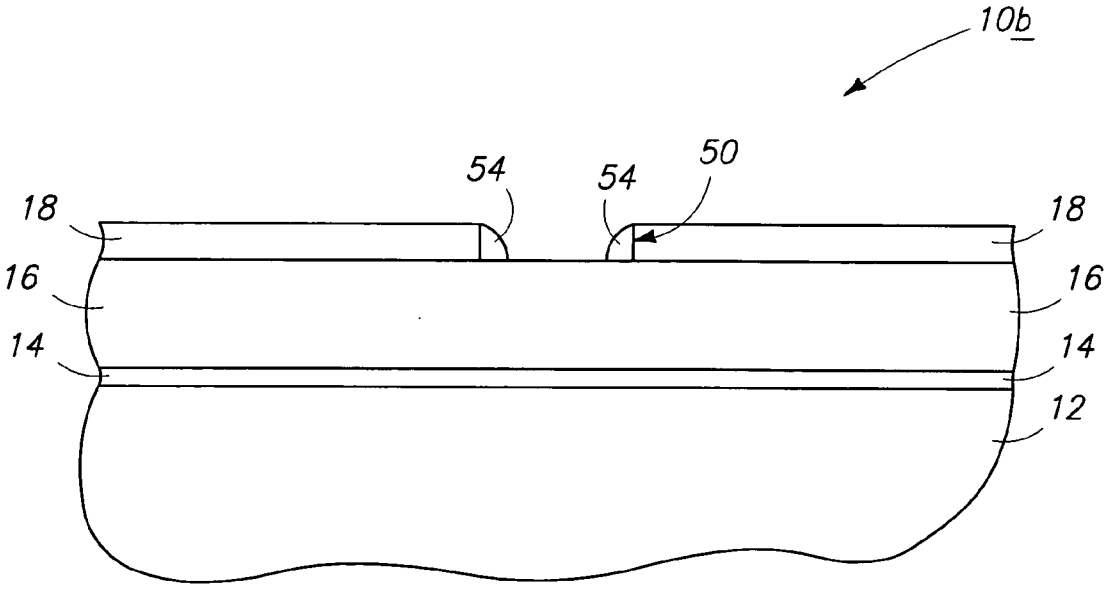

Fig. 8

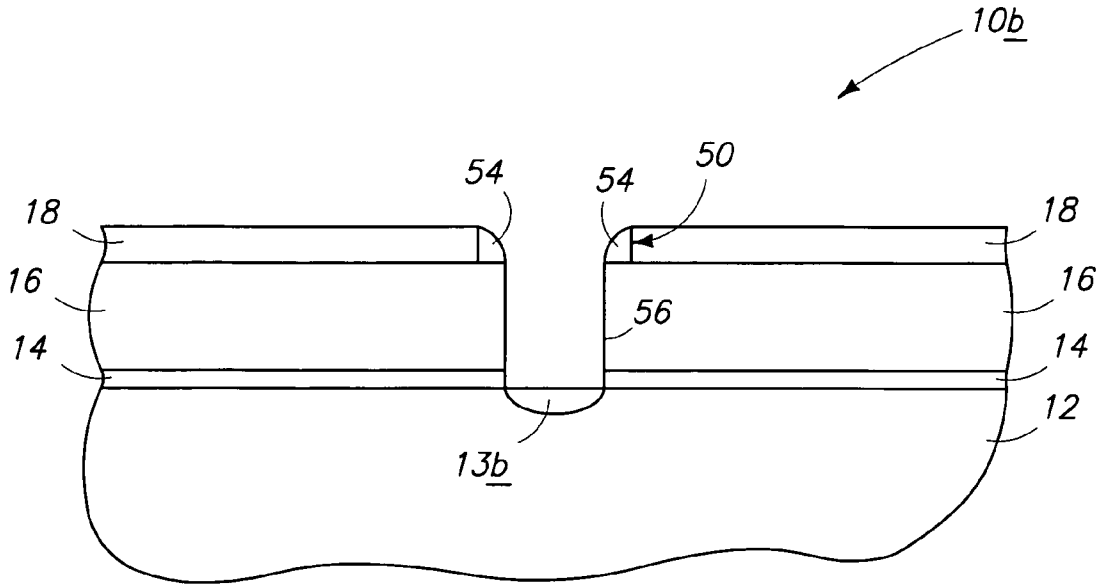
10b
54
54
50
18
18
16
16
56
14
14
12
13b

FIG 9

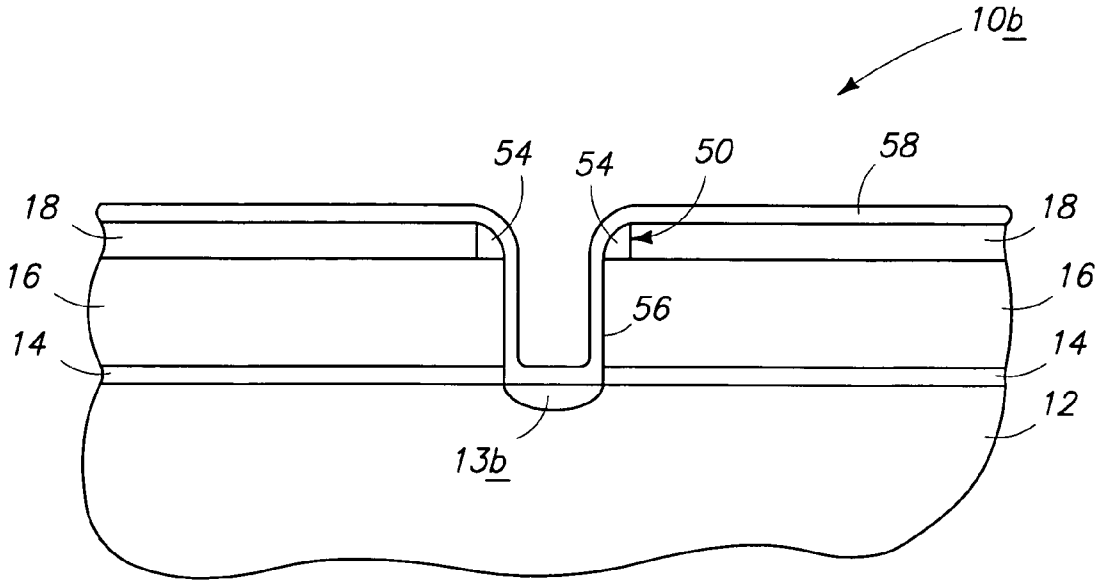
10b
54
54
50
58
18
18
16
16
56
14
14
12
13b

FIG 10

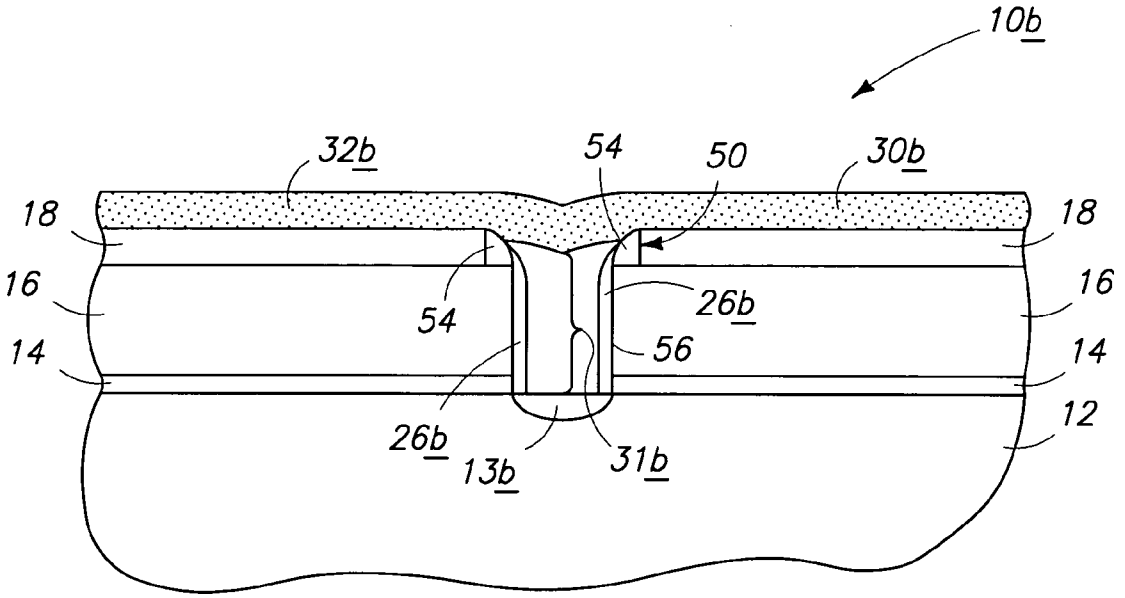

FIG. 11

THIN FILM TRANSISTORS AND METHODS OF FORMING THIN FILM TRANSISTORS

PATENT RIGHTS STATEMENT

[0001] This invention was made with Government support under Contract No. MDA972-92-C-0054 awarded by Advanced Research Projects Agency (ARPA). The Government has certain rights in this invention.

TECHNICAL FIELD

[0002] This invention relates specifically to thin film transistor technology.

BACKGROUND OF THE INVENTION

[0003] As circuit density continues to increase, there is a corresponding drive to produce smaller and smaller field effect transistors. Field effect transistors have typically been formed by providing active areas within a bulk substrate material or within a complementary conductivity type well formed within a bulk substrate. One additional technique finding greater application in achieving reduced transistor size is to form field effect transistors with thin films, which is commonly referred to as "thin film transistor" (TFT) technology. These transistors are formed using thin layers which constitute all or a part of the resultant source and drain regions, as opposed to providing both regions within a bulk semiconductor substrate.

[0004] Specifically, typical prior art TFT's are formed from a thin film of semiconductive material (typically polysilicon). A central channel region of the thin film is masked by a separate layer, while opposing adjacent source/drain regions are doped with an appropriate p or n type conductivity enhancing impurity. A gate insulator and gate are provided either above or below the thin film channel region, thus providing a field effect transistor having active and channel regions formed within a thin film as opposed to a bulk substrate.

[0005] It would be desirable to improve upon methods of forming thin film transistors and in improving thin film transistor constructions.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

[0007] **FIG. 1** is a diagrammatic sectional view of a semiconductor wafer fragment at one processing step in accordance with the invention.

[0008] **FIG. 2** is a view of the **FIG. 1** wafer fragment at a processing step subsequent to that shown by **FIG. 1**.

[0009] **FIG. 3** is a view of the **FIG. 1** wafer fragment at a processing step subsequent to that shown by **FIG. 2**.

[0010] **FIG. 4** is one example of a possible top view of **FIG. 3**.

[0011] **FIG. 5** is a view of the **FIG. 1** wafer fragment at a processing step subsequent to that shown by **FIG. 3**.

[0012] **FIG. 6** is a diagrammatic sectional view of an alternate embodiment wafer fragment in accordance with the invention.

[0013] **FIG. 7** is a diagrammatic sectional view of yet another alternate embodiment wafer fragment at one processing step in accordance with the invention.

[0014] **FIG. 8** is a view of the **FIG. 7** wafer fragment at a processing step subsequent to that shown by **FIG. 7**.

[0015] **FIG. 9** is a view of the **FIG. 7** wafer fragment at a processing step subsequent to that shown by **FIG. 8**.

[0016] **FIG. 10** is a view of the **FIG. 7** wafer fragment at a processing step subsequent to that shown by **FIG. 9**.

[0017] **FIG. 11** is a view of the **FIG. 7** wafer fragment at a processing step subsequent to that shown by **FIG. 10**.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0018] This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section-8).

[0019] In accordance with one aspect of the invention, a method of forming a thin film transistor over a substrate comprises the following steps:

[0020] providing a layer of semiconductive material from which a channel region and at least one of a source region or a drain region of a thin film transistor are to be formed; and

[0021] conductively doping the at least one of the source region or the drain region of the semiconductive material layer while preventing conductivity doping of the channel region of the semiconductive material layer, such doping being conducted without any masking of the channel region by any separate masking layer.

[0022] In accordance with another aspect of the invention, a method of forming a thin film transistor comprises the following steps:

[0023] providing a substrate having a node to which electrical connection is to be made;

[0024] providing a first electrically insulative dielectric layer over the substrate;

[0025] providing an electrically conductive gate layer over the first dielectric layer;

[0026] providing a second electrically insulative dielectric layer over the electrically conductive gate layer;

[0027] providing a contact opening through the second dielectric layer, the electrically conductive gate layer and the first dielectric layer; the contact opening defining projecting sidewalls;

[0028] providing a gate dielectric layer within the contact opening laterally inward of the contact opening sidewalls;

[0029] providing a layer of semiconductive material over the second dielectric layer and within the contact opening against the gate dielectric layer and in electrical communication with the node; the semiconductive material within the contact opening defining an elongated and outwardly extending channel region the electrical conductance of which can be modulated by means of the adjacent electrically conductive gate and gate dielectric layers; and

[0030] conductively doping the semiconductive material layer lying outwardly of the contact opening to form one of a source region or a drain region of a thin film transistor.

[0031] In accordance with still another aspect of the invention, a thin film transistor comprises:

[0032] a thin film transistor layer having a source region, a channel region and a drain region; the thin film channel region comprising an annulus; and

[0033] a gate in proximity to the thin film channel annulus, the gate comprising an annulus which surrounds the thin film channel annulus.

[0034] These and other aspects of the invention will be more readily appreciated from the following description with proceeds with reference to the accompanying drawings.

[0035] Referring to **FIG. 1**, a semiconductor wafer fragment in process is indicated generally with reference numeral **10**. Such comprises a bulk substrate **12** of lightly doped p or n type monocrystalline silicon, having a diffusion region **13** provided therein. A first electrically insulative dielectric layer **14** (typical SiO_2) is provided over bulk substrate **12**. An example and preferred thickness range for layer **12** is from 50 Angstroms to 2000 Angstroms, with 100 Angstroms being more preferred. An electrically conductive layer **16** is provided over first dielectric layer **14**. Layer **16** will ultimately comprise the conductive gate of the thin film transistor, and preferably comprises a heavily doped (greater than 1×10^{20} ion/cm^3) layer of polysilicon. An example and preferred thickness range is from 3000 Angstroms to 10,000 Angstroms, with 8000 Angstroms being more preferred. A second electrically insulative dielectric layer **18** is provided over electrically conductive gate layer **16**. Such can be considered as a base layer over which a thin film transistor layer will be provided. An example and preferred material is SiO_2 deposited to a thickness range of from 300 Angstroms to 3000 Angstroms, with 1000 Angstroms being more preferred.

[0036] Referring to **FIG. 2**, a contact opening **20** is provided through second dielectric layer **18**, electrically conductive gate layer **16**, and first dielectric layer **14** to outwardly expose diffusion region **13**. Alternately, diffusion region **13** could be provided after forming contact opening **20**. One method of doing this is by using ion implantation through contact opening **20**, thereby making diffusion regions **13** self-aligned to contact opening **20**. Contact opening **20** defines projecting sidewalls **22** which in the preferred embodiment are provided to be substantially perpendicular relative to the expanse of bulk substrate **12**. A dielectric layer **24**, which will serve as gate dielectric layer, is deposited over second dielectric layer **18** and within contact opening **20** to a thickness which less than completely fills contact opening **20**. An example diameter for contact opening **20** is 3500 Angstroms, with an example layer **24** being SiO_2 deposited to a thickness of 200 Angstroms in such instance.

[0037] Referring to **FIG. 3**, gate dielectric layer **24** is anisotropically etched to define a resultant gate dielectric layer **26** within contact opening **20** laterally inward of sidewalls **22**. When anisotropically etching gate dielectric layer **24**, some of second dielectric layer **18** is removed during a desired overetch. If layer **18** is 1000 Angstroms thick and layer **24** is 200 Angstroms thick, a preferred over-etch would be 200 Angstroms, reducing **18** to 800 Angstroms. In the illustrated and preferred embodiment, such gate dielectric layer takes on the shape or appearance of conventional insulative sidewall spacers, and in the depicted embodiment is in the form or shape of a longitudinally elongated annulus. Thus, electrically conductive gate layer **16** also is comprised of an annulus which surrounds contact opening **20**.

[0038] **FIG. 4** illustrates one example of a possible patterned top construction of **FIG. 3**. Such illustrates gate dielectric annulus **26** encircling within contact opening **20**. Electrically conductive gate layer **16** has been patterned to comprise a ring portion and an extension **27**. Regardless, the bulk mass of layer **16** constitutes an annulus which encircles contact opening **20**. The above described process provides but one example of a manner in which a gate dielectric layer is provided within contact opening **20**.

[0039] Referring to **FIG. 5**, a layer **30** of semiconductive material is provided over second dielectric layer **18** and within contact opening **20** against gate dielectric layer **26**, and in electrical communication with diffusion region **13**. In this particular described embodiment, layer **30** is provided to completely fill the remaining open portion of contact opening **20**. Semiconductive material layer **30** constitutes a layer from which a channel region and at least one of a source region or a drain region of a thin film transistor are to be formed. The semiconductive material of layer **30** within contact opening **20** defines an elongated and outwardly extending channel region **31** the electrical conductance of which can be modulated by means of the adjacent electrically conductive gate and gate dielectric layers **16** and **26**, respectively.

[0040] Field effect transistor channel regions typically utilize some minimum conductivity doping, less than the doping concentrations of the source and drain, to provide desired conductance when modulated by the gate. Such can be provided in this example by in situ doping of layer **30** during its deposition. Alternately, an ion implant can be conducted with subsequent processing providing desired diffusion of the dopants.

[0041] The semiconductive material layer **30** is then conductively doped such that its portion lying outwardly of contact opening **20** forms one of a source or a drain region **32** of a thin film transistor. The doping results in an interface **34** being created relative to the outermost portions of layer **30** and that portion within channel region **31**, such that portion **32** constitutes a highly doped electrically conductive region, while channel region **31** constitutes a semiconductive layer capable of being rendered conductive by applying suitable voltage to gate layer **16**. Note that advantageously in accordance with the preferred process, conductive doping of layer **36** is conducted using its thickness to effectively prevent conductivity doping of channel region **31**, with such doping being conducted without other masking of the channel region by any separate masking layer. The effective thickness and doping conditions for the outer portion of layer **30** effectively can be utilized to prevent undesired conductivity enhancing doping of channel region **31**.

[0042] In the above described embodiment; one of doped regions **32** of layer **30** or diffusion region **13** of bulk substrate **12** constitutes a source region of a thin film transistor, while the other of such constitutes a drain region.

Region **31** constitutes a channel region, with gate layer **16** comprising an annulus which encircles thin film channel region **31**. Both of channel region **31** and diffusion region **32** are elongated, with diffusion region **32** being oriented substantially perpendicular relative to channel region **31** and also substantially parallel with bulk substrate **14**. Elongated channel region **31** and gate dielectric annulus **26** are perpendicularly oriented relative to bulk substrate **14**.

[**0043**] If region **13** constitutes the drain region, then the thickness of oxide layer **14'** defines the gate-drain offset dimension of the thin film transistor. As well known to those of skill in the art, a drain offset is a region used in thin film transistors to reduce off current caused by thermionic field emission in the channel region near the drain. If region **32** is the drain, then the thickness of layer **18** defines the offset dimension. The thickness of gate polysilicon layer **16** defines the channel length of the thin film transistor.

[**0044**] An alternate embodiment is shown and described with reference to **FIG. 6**. Like numerals from the first described embodiment are utilized where appropriate, with differences being indicated by the suffix "a" or with different numerals. In the depicted embodiment of wafer fragment **10***a,* semiconductive material **30***a* is provided to only partially fill the remaining portion of contact opening **20**. Such forms an annulus **33** within contact opening **20**, with such annulus being utilized to comprise the channel region of the resultant thin film transistor.

[**0045**] Layer **30***a* can be doped in a single step to form diffusion regions **32***a* and **35**, one of which constitutes a drain region and the other of which constitutes a source region of the resultant thin film transistor. Accordingly, channel annulus **33** is elongated and oriented substantially perpendicularly relative to bulk substrate **12** and diffusion regions **32***a* and **35**. In this described embodiment, gate layer **16** comprises an annulus which surrounds thin film channel annulus **33**. Again, the elongated and substantially vertical nature or orientation of channel region **33** prevents conductivity doping from occurring therein when regions **32***a* and **35** are doped by a highly directional perpendicular ion implantation doping. In this embodiment, diffusion region **13** constitutes a node to which electrical connection of a thin film transistor is to be made, while in the first embodiment example region **13** comprised an inherent part of the thin film transistor. Diffusion region **13** might alternately be provided by out-diffusion of dopant material from region **35** from subsequent heating steps.

[**0046**] Desired minimum doping for the channel region of **FIG. 6** can be provided by in situ doping or by ion implanting, such as angled implanting.

[**0047**] Yet another alternate preferred embodiment is described with reference to **FIGS. 7-11**. Like numerals from the first described embodiment have been utilized where appropriate, with differences being indicated with the suffix "b" or with different numerals. Referring first to **FIG. 7**, second electrically insulative dielectric layer **18** is provided with an initial contact opening **50** therethrough to electrically conductive gate layer **16**. A preliminary electrically insulative layer **52** is provided over second dielectric layer **18** and to within initial contact opening **50**, with such layer less than completely filling contact opening **50**.

[**0048**] Referring to **FIG. 8**, preliminary electrically insulative layer **52** is anisotropically etched to define an insulative annulus spacer **54** within initial contact opening **50**. Such facilitates or enables producing a contact opening inwardly of the spacers which is less than the minimum photolithographic feature size which can be useable to produce the smallest possible initial contact opening **50**. For example, where a minimum available photolithographic width for contact opening **50** were 0.32 micron, the resultant width of the opening after spacer etch can be reduced to 0.1 micron. As examples, if layer **18** is 1500 Angstroms thick and opening **50** is 3200 Angstroms in diameter, layer **52** is preferably provided to a thickness of from 500 Angstroms to 1200 Angstroms, with 1000 Angstroms being most preferred. An anisotropic etch of a 1000 Angstrom thick layer **52** will preferably be conducted as an over-etch of 300 Angstroms, leaving layer **18** 1200 Angstroms thick.

[**0049**] Referring to **FIG. 9**, a secondary contact **56** is etched through electrically conductive gate layer **16** and first dielectric layer **14**. During such etching, insulative annulus spacer **54** and second dielectric layer **18** are used as an etching mask. Diffusion regions **13***b* is provided as shown.

[**0050**] Referring to **FIG. 10**, a secondary electrically insulative layer **58** is provided over second dielectric layer **18** and insulative annulus spacer **54** to within secondary contact opening **56**, with such layer being provided to less than completely fill secondary contact opening **56**.

[**0051**] Referring to **FIG. 11**, secondary electrically insulative layer **58** has been anisotropically etched to define a gate dielectric layer annulus **26***b* within secondary contact opening **56**. A subsequent semiconductive layer **30***b* is provided and doped as shown to provide diffusion region **32***b,* and to provide channel region **31***b.* An example thickness for layer **58** is 200 Angstroms. Anisotropic etching of such a layer preferably includes a 200 Angstrom over-etch, resulting in a final preferred thickness of layer **18** of 1000 Angstroms.

[**0052**] The above described embodiments utilizing an annulus gate essentially enables provision of a channel region which is gated about all sides, thus enabling provision of smaller field effect transistors. Such results in a reduced consumption of substrate area, with such example thin film transistors enabling the required area to be that of the contact and the associated anisotropic spacer-like constructions. Conventional horizontal thin film transistors require additional area for the channel, source and drain regions. Such also provides for improved thin film transistor characteristics, due to gating of the channel region on all sides which provides greater controllable on/off currents.

[**0053**] The above described method and embodiment further reduce overall mask count in semiconductor processing. Since in the preferred embodiment the channel region is substantially vertical, masks are not required to protect the desired channel from the thin film transistor source and drain implants. Depending on implementation, the channel region may even be completely sealed from the surface providing even greater protection, thus eliminating at least two masks.

[**0054**] In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention

into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.

1-35. (canceled)

36. A wafer comprising: a transistor comprising:

a substrate;

a gate provided over the substrate and substantially surrounding an opening;

a first source/drain region;

a second source/drain region;

semiconductive material proximate the gate and comprising a channel intermediate the first and second source/drain regions, wherein at least a portion of the channel is formed within the opening; and

dielectric material formed intermediate the gate and the semiconductive material.

37. The wafer of claim 36, wherein the semiconductive material partially fills the opening within the gate.

38. The wafer of claim 36 further comprising an electrically insulative layer over the substrate and below the gate.

39. The wafer of claim 36, wherein the transistor comprises a thin film transistor.

40. The wafer of claim 36, wherein the dielectric material is formed within the opening, and wherein the dielectric material and the semiconductive material completely fill the opening within the gate.

41. The wafer of claim 36, wherein at least a portion of the first source/drain region is formed above the opening of the gate.

42. The wafer of claim 41, wherein at least a portion of the second source/drain region is formed below the opening of the gate.

43. The wafer of claim 36, wherein the gate laterally surrounds dielectric material.

44. The wafer of claim 36, wherein the dielectric material laterally surrounds the channel formed within the opening.

45. The wafer of claim 36, wherein at least a portion of the first source/drain region is formed within the semiconductive material.

46. The wafer of claim 36, wherein at least a portion of the first source/drain region is formed within the substrate.

47. The wafer of claim 36, wherein the channel is formed elevationally above at least one of the first and second source/drain regions.

48. The wafer of claim 36, wherein the channel comprises an elongated structure extending substantially perpendicularly to an upper surface of the substrate.

49. A wafer comprising: a transistor comprising:

a substrate;

a gate provided over the substrate and substantially surrounding an opening, wherein the opening has a lateral cross-sectional dimension which is less than a minimum photolithographic feature size utilized for fabricating the transistor;

a first source/drain region;

a second source/drain region; and

semiconductive material proximate the gate and comprising a channel intermediate the first and second source/drain regions.

50. The wafer of claim 49, wherein the channel is formed within the opening.

51. The wafer of claim 49, wherein at least a portion of the first source/drain region is formed above the opening of the gate.

52. The wafer of claim 49, wherein the gate laterally surrounds the channel.

53. The wafer of claim 49, wherein the transistor comprises a gate dielectric between the gate and the channel, and wherein the gate dielectric laterally surrounds the channel.

54. The wafer of claim 49, wherein at least a portion of the first source/drain region is formed above the opening, and wherein at least a portion of the second source/drain region is formed below the opening.

55. The wafer of claim 49, wherein the transistor comprises a thin film transistor.

56. The wafer of claim 49 further comprising an electrically insulative layer over the substrate and below the gate.

57. A semiconductor device comprising: a transistor comprising:

a substrate;

a gate provided over the substrate and substantially surrounding an opening;

a first source/drain region comprising at least a portion formed partially below the opening;

a second source/drain region comprising at least a portion formed partially above the opening;

semiconductive material proximate the gate and comprising a channel intermediate the first and second source/drain regions; and

a gate dielectric formed intermediate the gate and the semiconductive material.

58. The semiconductor device of claim 57, wherein the channel is formed within the opening.

59. The semiconductor device of claim 57, wherein the transistor comprises a thin film transistor.

60. A semiconductor device comprising: a transistor comprising:

a substrate;

a gate provided over the substrate and substantially surrounding an opening, wherein the opening has a lateral cross-sectional dimension which is less than a minimum photolithographic feature size utilized for fabricating the transistor;

first and second source/drain regions;

semiconductive material proximate the gate and comprising a channel intermediate the first and second source/drain regions; and

a gate dielectric formed intermediate the gate and the channel.

61. The semiconductor device of claim 60, wherein the channel is formed within the opening.

62. The semiconductor device of claim 60, wherein the transistor comprises a thin film transistor.

63. A transistor comprising:

a substrate;

a gate provided over the substrate and substantially surrounding an opening;

a first source/drain region comprising at least a portion formed partially below the opening;

a second source/drain region comprising at least a portion formed partially above the opening;

semiconductive material proximate the gate and comprising a channel intermediate the first and second source/drain regions; and

a gate dielectric intermediate the gate and the channel.

64. The transistor of claim 63, wherein the channel is formed in the opening and partially fills the opening.

65. The transistor of claim 63 further comprising a thin film transistor.

66. The transistor of claim 63, wherein the gate dielectric and the semiconductive material completely fill the opening within the gate.

67. The transistor of claim 63, wherein the semiconductive material is provided within the opening and over the gate.

68. The transistor of claim 63, wherein the opening is formed through an entirety of the gate.

69. The transistor of claim 63, wherein at least a portion of the first source/drain region is formed within the semiconductive material.

70. The transistor of claim 63, wherein at least a portion of the first source/drain region is formed within the substrate.

71. A transistor comprising:

a substrate;

a gate provided over the substrate and substantially surrounding an opening over the substrate, the opening has a lateral cross-sectional dimension which is less than a minimum photolithographic feature size utilized for fabricating the transistor;

first and second source/drain regions; and

semiconductive material intermediate the first and second source/drain regions and comprising a channel.

72. The transistor of claim 71, wherein at least a portion of at least one of the first and second source/drain regions is formed within the opening.

73. The transistor of claim 71, wherein at least a portion of the semiconductive material is formed within the opening.

74. The transistor of claim 71 further comprising insulative material provided intermediate the gate and the semiconductive material.

75. The transistor of claim 71, wherein at least a portion of at least one of the first and second source/drain regions is formed above the opening of the gate.

76. The transistor of claim 75, wherein at least a portion of at least one of the first and second source/drain regions is formed below the opening of the gate.

77. The transistor of claim 71 further comprising a thin film transistor.

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