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(19)

(54) IMPROVEMENTS IN OR RELATING TO TELECOMMUNICATION EXCHANGES

(71) We, ITT INDUSTRIES LIMITED, a British Company, of 190 Strand, London, WC2R 1DU, England, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:

This invention relates to automatic telecommunication exchanges in which the intelligence is handled in time division multiplex (TDM) manner using pulse code modulation (PCM).

One of the problems which has to be solved in a processor-controlled telecommunication exchange is the provision of signalling to and from the processor, and an object of the invention is to enable such signalling to be conveyed over the same physical path as that used for intelligence, e.g. speech.

According to one aspect of the invention there is provided an automatic telecommunication exchange of the processor-controlled type, in which communication connections are set up in TDM manner using PCM, in which signalling between the interfaces for the peripherals served by the exchange and the exchange control equipment, and also signalling involving access to the processors uses the same physical transmission medium as is used for the communication intelligence, in which the signalling between the said interfaces and the control equipment is conveyed by the use of one of the bit places of each of the PCM code groups used to convey said intelligence and in which the signalling involving processor access uses at least one time position in the PCM/TDM cycle which is reserved for use for processor access.

In the case of a telephone exchange the peripherals referred to in the preceding paragraphs are subscribers' line circuits, multiplex terminals from remote exchanges, multiplex terminals from remote line concentrators, and possibly non-multiplex junctions.

An embodiment of the invention will now be described with reference to the drawings accompanying the Provisioned Specification, in which Fig. 1 is a simplified trunking diagram of a telephone exchange which uses the present invention, while Fig. 2 is a schematic diagram of as much of the control circuitry as is needed to understand the present invention.

The exchange described herein is of the time-space-time (TST) type, without concentration within the exchange, and the operations associated with the various stores used in the TST system follow established practice in many respects, and so will not be described in full. The subscribers' line interfaces and their multiplex terminals follow the principles enuciated in our Patent Application No. 929/75 (Serial No. 1462003).

The exchange uses two 'levels' of processors, one 'level' referred to as the front-end processors being associated with the various groups of lines served by the exchange, while the other, 'level' referred to as back-end processors is associated with inter-group switching. An example of a telephone exchange using processors arranged in this way will be found in our Patent Application No. 40184/76, (Serial No. 1552812.) although the exchange described therein is of the so called 'space-division' type.

The present arrangement, while using the principles of the above-quoted Patent Applications, describes the use of the same physical transmission medium as is used to convey the speech to convey signalling from the line interface or line circuit, to and from the processors. Also described is the use of separate time positions in various stores and bus bars to enable the front-end processors to access their own groups directly via the inter-group switch. Fianlly it will be noted that the front-end processors can access bus bars to the back-end processors.

Referring now to Fig. 1, the non-concentrated subscribers access the switches for their line groups directly, while for subscribers served by a remote concentrator a multiplex highway from the concentrator is terminated at a Mux Terminal. This demultiplexes for connection to inlets to the switches serving the various line groups. Inter-exchange working is digital, again using multiplexes, with connection to the switches via a multiplex terminal.

The switch formation follows established practice in TST arrangements, with auxiliary time positions used through the inter-group switch. The time switches which serve the individual groups of peripherals are formed, in the exchange described, by semiconductor stores which provide cyclic and/or random access. Each line group is served by a set of four such stores T, S, ß in and ß out. Each group is controlled by a pair of front-end processors A and B, and these in turn co-operate with common back-end processors V and W. This duplication is of course desirable in the interests of system security.

The inter-group switch IGS is an assembly of semiconductor gates switching parallel channels, eight per time position, so that serial representation is concentrated into parallel representation for cross-office transmission. For the front-end processors, bus bars P_a, P_b, eight bits parallel, are used to send information to the processor and another eight bits parallel to receive information from the processor.

Signalling is conveyed in the exchange of Figs 1 and 2 by the use of a ninth bit added to the eight information bits used for speech, so that the ninth bits can form parts of characters and be a sub-multiplex of the main information.

However, another possibility which is discussed in more detail later, is to "steal" the least significant bit of the 8-bit code group every n_{th} TDM cycle, so that 'sub-multiplexes' are provided for signalling. In such case the "stolen" bits are assembled into, say, 8-bit words on reception at the processor.

We will now describe the operation of the exchange, as far as it is relevant to the present invention, commencing with the origination of a call.

The first of the time switches to be considered is the T store, e.g. T1, which has eleven columns, of which the ninth column receives the ninth bit marker to indicate that a signal is being received. The tenth and eleventh columns are used to indicate which processor is in use for the call, a 1 bit in column ten indicating that processor A is in use while a 1 bit in column eleven indicates that the group's processor B is in use.

The controls for the T store Fig. 2, include three separate binary counters CC, QZa and QZb which control the select circuitry SC. Cyclic selection of the rows of the store is the normal routine used for selection as the counter CC hunts through its cycle and addresses each row of the store in turn. The other two counters QZa and QZb are queue control counters for the processors A and B respectively, so that the position can be remembered of the last call handled by each of the processors. Two queue control counters are used because when selection digits are being assembled, all digits for the same call should be assembled via the same processors. The use of two queue control counters in this way meets this requirement.

To further clarify the connection to the processors, the output from the ß in switch column circuits is applied in parallel fashion to the inter-group switch, while the input from the line or from a signal assembler is a serial stream at the appropriate rate, which is subjected to serial-parallel conversion into the column circuits for writing into the ß in switch.

When a subscriber lifts his receiver, it loops his line, and this is detected by the appropriate line interface unit, which latter generates a serial signal consisting of eight information words at least one of which has a bit in its ninth bit position: in fact at least *two* ninth bit positions are always used. This serial stream is interrogated at gate G1 and the ninth bit is inserted, as can be seen from the gate control *t*9. The other gate control Pt1 is that for a first of four sub-time slots in each time position - see the inset to Fig 2. Thus a mark has been made in one of the rows of the store T to indicate that a line wishes to have the services of one of the processors.

In due course either front-end processor A or B becomes free. Assume that processor A is the next to become available to deal with the call; the queue controls QZa and QZb indicate by their settings if any calls exist as the ones to be dealt with for next operations by the processor. However, we are now concerned with the immediate writing of some information associated with the incoming signals at this instant, say Ax. This takes place at Pt1 time, marking the output of the cyclic counter CC via gates G2 and G9 into select control SC, and at the same time it causes the select control SC to be enabled so that selection can occur in the T store.

When the ninth bit is detected in the signal stream, this is written to make a mark in the appropriate time position, for instance, Ax of the T store column 9. In reading the contents of the Ax store of T the absence of any mark in the tenth or eleventh columns will be apparent because this is a new entry in the system, so that neither the tenth nor the eleventh elements (actually flip-flops) of the row newly seized are operated at Pt. 2. Hence at Pt. 3, the same cyclic selector can

write into the columns 10 or 11, in this case 10, to identify the processor involved, in this case the A processor.

The calling signal is dealt with then by assembling the signal in the assembled signal character shift register ASC which extracts each ninth bit and assembles an eight bit character at one eighth of the information rate. This is inserted into the serial-to-parallel converter of the ß in store (but at the line rate), and parallel transferred therefrom into the column circuits.

This signal is put into the za time position of ß in because gate G10 (top right hand corner of Fig. 2) opens under the control of the front-end processor A signal and the WS flip-flop at 1. This occurs as WS has moved to 1 to indicate that a full character has been received in the assemble signal character shift register ASC. Thus this signal may now be transferred through the inter-group switch to the processor.

A discriminatory calling signal can be used which indicates, for instance, which party on a shared line is originating the call, so that the processor may take the appropriate action. This signal is sent until acknowledged by the processor so that the processor does not have to interrupt its functions to deal with calling or other conditions. Such a signalling technique is described in the above quoted Application No. 929/75 (Serial No. 1462003). In this case dial tone is returned to the caller after an acknowledgment signal, whereafter the subscriber sends the selection information. This is received a digit at a time and handled in a similar manner to the calling signal except that no acknowledgment is given, the cycle time being such that the processor can deal with the incoming information. Each digit is dealt with separately but the digits are routed to the appropriate processor because of the stored information in the T1 store.

When the full selection data has been received the appropriate processor replaces its address in the T1 store by that of a free time position in the stores S1, ß in and ß out. At the same time the processor enters in the terminating T store, for instance Tn, at the Ay position, the same time position to control Sn ß in and ß out appropriately in the terminating group. Hence the set up now is that, via the incoming line interface and T1 a connection is established through ß in and the inter-group switch to the ß out of the Tn group and out therefrom to the interface of the called party. Thus a one-way connection is established while the return channel is established through the ß in group associated with the n group and via the ß out of the T1 group to the appropriate subscriber line interface. Study of Fig 1 will indicate the writing and read controls involved in such a set up which will be found to be that normally expected in such an arrangement.

The front-end processors may not, of course, be able to achieve the connection without the aid of the back-end processors, but the receipt of selection information, for instance, in the group 1 front-end processor involved, might require the intervention of the back-end processor to direct the connection through to the front-end processor concerned with the terminating group. It will be seen that the appropriate bus-bars and controls are available for such functions.

At this point in the connection the called party is rung by transmission of a signal from the n-group front-end processor involved in controlling this connection, and when the called subscriber responds the ring trip causes the ringing to be removed. The signal sent out to apply ringing is also of the form described previously, the eight-unit code, and return of the ring trip is likewise of a similar type. Hence the same method as before, the combination of the ninth bit, permits the direction of the signals to the appropriate controls as indicated by the za, zb marker.

Conversation proceeds, until one of the subscribers hangs up. When either party clears the clear signal is extended to the responsible front-end processor which then causes the address in the T1 and Tn stores to be removed from this time slot which is then free for further use.

In the case of a subscriber on a concentrator, the call is handled in a similar way to that described above because the signals are transmitted via the multiplex channel right to the concentrator. Hence the concentrator function may take place remotely, the signalling being received at the central processors without any difficulty. It is the function, of course, of the concentrator to connect the appropriate subscriber or to make connection to the appropriate calling subscriber, and thus the switching functions as normally expected in a concentrator would be provided.

To handle junction traffic, the switch may be used as a transit switch or as a switch to terminate a call with calls originating over a junction. There is no difference in the operation as the junction multiplexes are able to carry the signals to and from the controlling processors. The absence of concentration provides for very high traffic capabilities to be handled on these junctions.

In one method of allocating groups there are 200 subscriber terminals, and 54 allocated to concentrators or junctions, giving a total with the two time positions for the processors, of 256 terminals available for use. However, a total of 128 terminals would also be a suitable figure which would reduce the operating frequency to 8 mHz instead of 16 mHz.

It will be seen that the arrangements described provides for serial transfer from line circuits to main store but parallel transfer through the inter-group switch. The desirability of serial transfer from the line interface will be appreciated as it permits a single gate instead of multiple gates and consequent economy.

In the arrangement described above, the signalling channel is provided by the use of an extra bit added to each PCM code group, which increases the bit rate which has to be catered for by 12.5%. and necessitates the provision of extra wiring and information path equipment within the parallel-operating positions of the exchange. This could be inconvenient in some cases, and to avoid the inconveniences, it is possible to use one bit place of the PCM groups as the signalling channel. To minimize interface with the speech being conveyed, the least significant bit place is used and this bit is only used for signalling once in n cycles of the multiplex system. Thus the least significant bit place provides a "within band" signalling channel, with only 1 out of n of these bit places actually used.

When using the so-called bit stealing technique referred to in the preceding paragraph, the gates used to extract the signalling would need to be suitably altered as to their controlling inputs. In addition a counter is provided to count the multiplex cycles and to give an output to define the one cycle out of n used for signalling. Thus to consider some of the gates as examples, we examine the two gates which control the character shift register ASC, Fig 2. The uppermost gate of these two supplies stepping pulses for the register, which occur at sub-slot Pt 2, the other control for the gate being t9, the ninth bit time. When using the "bit stealing" technique described in the preceding paragraph thus t9 control is replaced by a t1 control as this is least significant bit time, plus a control for the counter mentioned in the previous paragraph. This latter control is energised during the nth cycle used for signalling. Similarly the data entry gate for ASC has its t9 control replaced by two controls, in the manner just mentioned.

WHAT WE CLAIM IS:-

1. An automatic telecommunication exchange of the processor-controlled type, in which communication connections are set up -in TDM manner using PCM, in which signalling between the interfaces for the peripherals served by the exchange and the exchange control equipment, and also signalling involving access to the processors uses the same physical transmission medium as is used for the communication intelligence, in which the signalling between the said interfaces and the control equipment is conveyed by the use of one of the bit places of each of the PCM code groups used to convey said intelligence and in which the signalling involving processor access uses at least one time position in the PCM/TDM cycle which is reserved for use for processor access.

2. An exchange as claimed in claim 1, and in which the bit place used for the signalling between the interfaces and the control equipment is provided by the addition of a bit place to each PCM combination additional to the bit places used to convey the communication intelligence.

3. An exchange as claimed in claim 1, and in which the bit place used for the signalling between the interfaces and the control equipment is provided by the use for signalling of the least significant bit place of the PCM combinations, said bit place being used for that purpose on every nth one of the PCM cycles.

4. An exchange as claimed in claim 1, 2 or 3 in which the exchange is of the time-space-time type, in which first processors are used to serve the various groups of peripherals, and in which second processors are used to control the establishment of inter-group connections via the space switching portion of the exchange.

5. An exchange as claimed in claim 4 in which each said group of peripherals is served by two first processors, and in which the infirmation stored in the time switches includes an indication as to which of the two processors is in use for the call.

6. An exchange as claimed in claim 4 or 5, and in which all of the first processors and the second processors have access to a set of bus-bars used for inter-processor communication, so that said inter-processor communication can occur independent of the paths used for conveying said PCM code groups.

7. An exchange as claimed in claim 2 or any claim appendant thereto, in which when the initiation of a call has been detected, the additional bit for the TDM channel in use for the calling subscriber is set to its 1 condition to indicate that line looping has taken place, and in which the detection of such a bit in its 1 condition indicates to the processor that a line is calling and thus requires the services of a said first processor.

8. An exchange as claimed in claim 7, and in which intellegence as to a line's class or nature, (e.g. which party on a party-line) is conveyed as a PCM code group, as is information relating to the wanted line.

9. An automatic telecommunication exchange substantially as described with reference to the drawings accompanying the Provisional Specification.

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1560695 PROVISIONAL SPECIFICATION

2 SHEETS *This drawing is a reproduction of the Original on a reduced scale*

Sheet 1

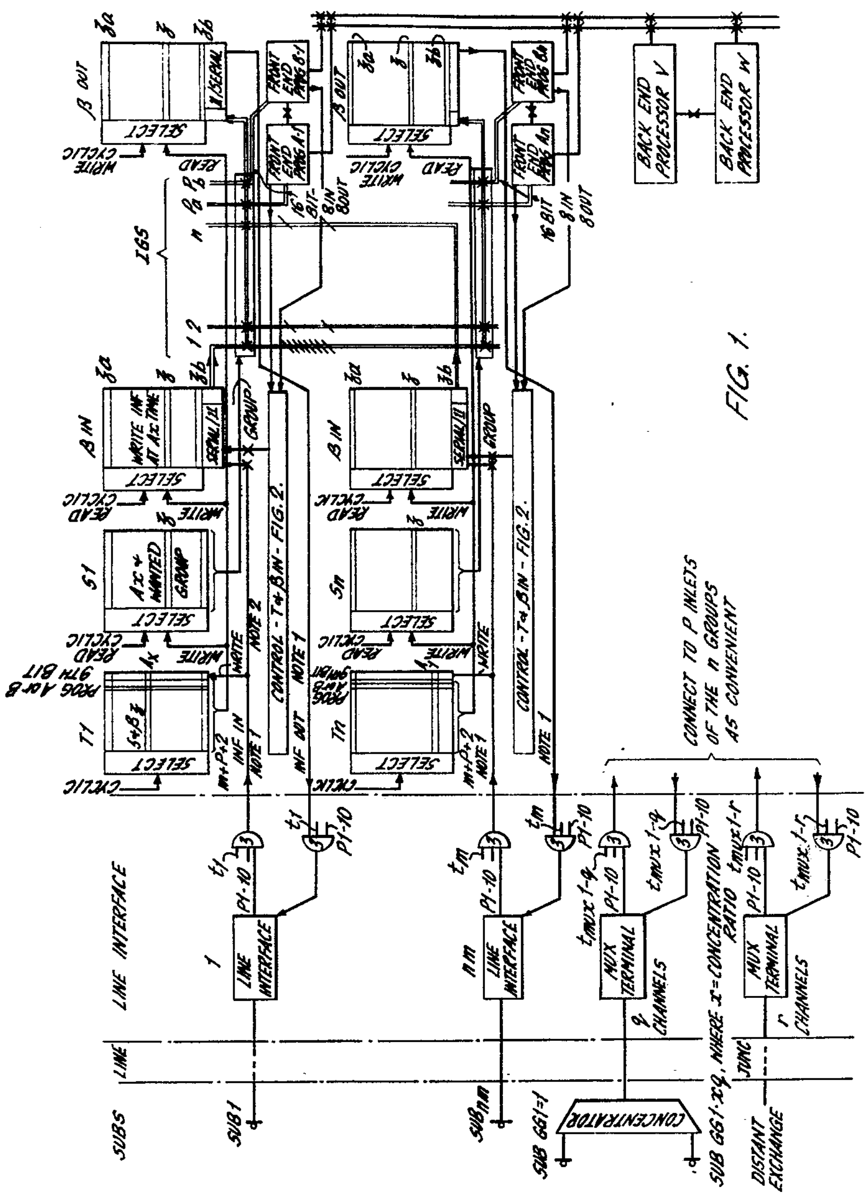

FIG. 1.

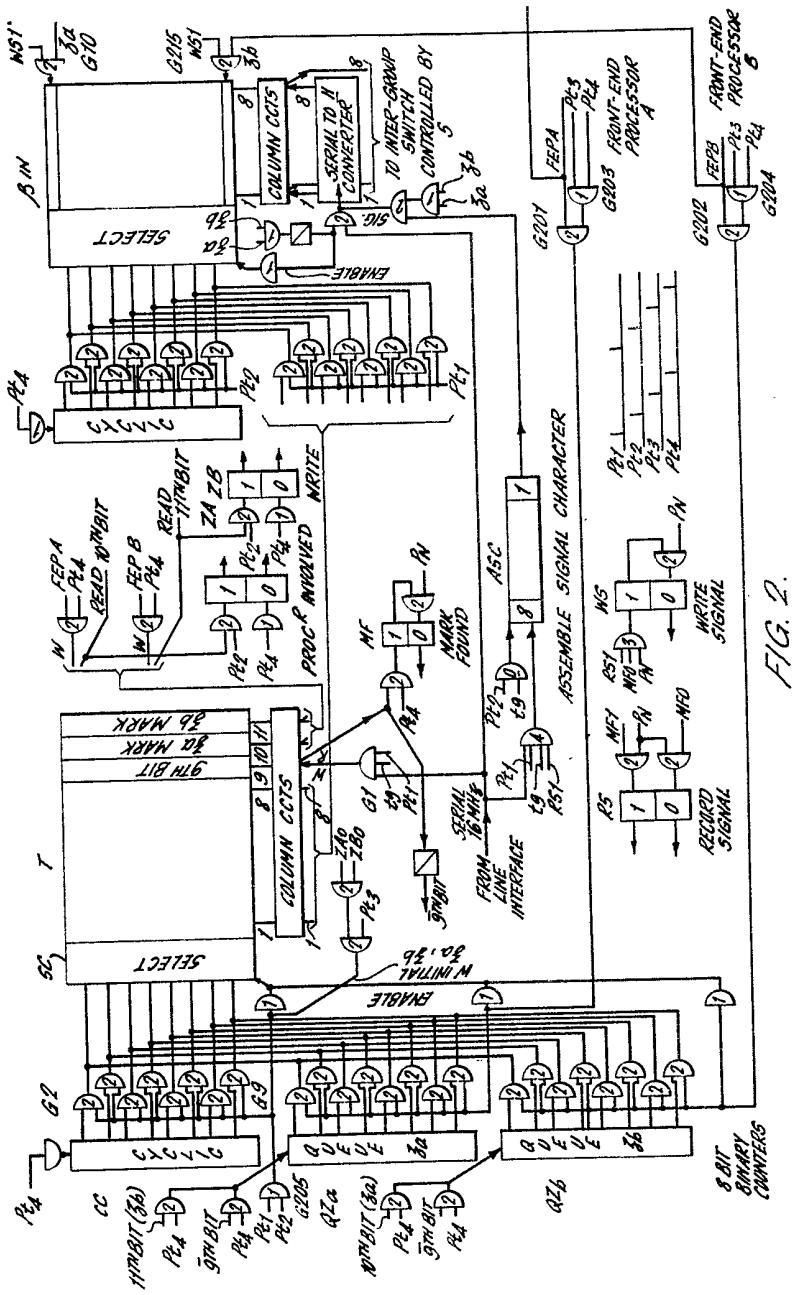
FRONT-END PROCESSOR B
FRONT-END PROCESSOR A
TO INTER-GROUP SWITCH CONTROLLED BY S
SERIAL TO // CONVERTER
COLUMN CCTS
SELECT
ENABLE
ASSEMBLE SIGNAL CHARACTER
MARK FOUND
PROC.P INVOLVED
READ INHIBIT
WRITE INHIBIT
WRITE SIGNAL
RECORD SIGNAL
FROM LINE INTERFACE
8 BIT BINARY COUNTERS

FIG. 2.