

(19) World Intellectual Property Organization  
International Bureau



(43) International Publication Date  
20 February 2003 (20.02.2003)

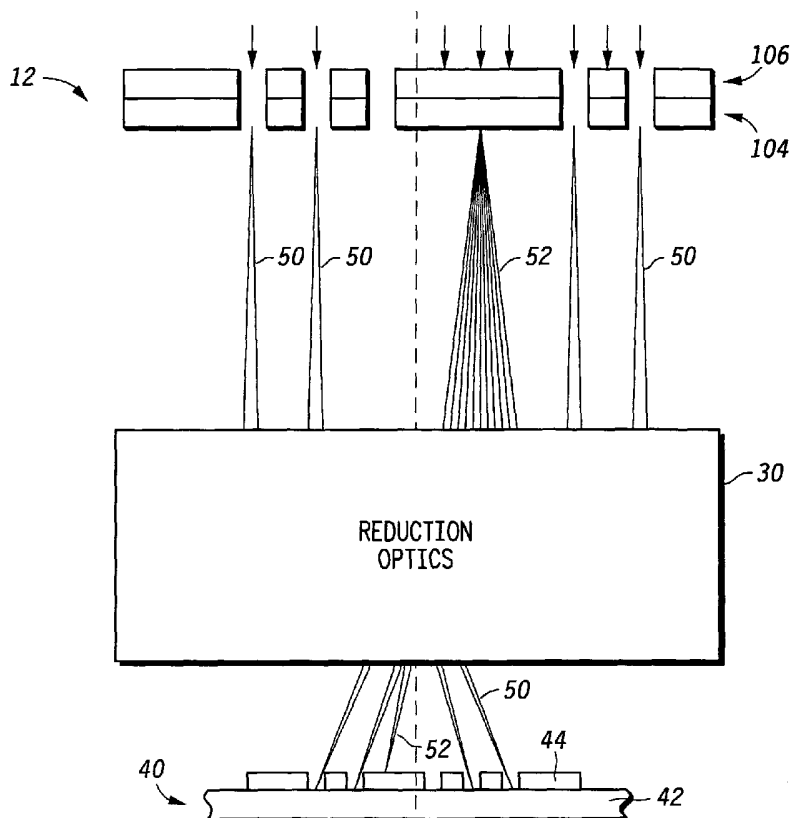
PCT

(10) International Publication Number  
WO 03/015135 A3

- (51) International Patent Classification<sup>7</sup>: **G03F 1/16**
- (21) International Application Number: PCT/US02/24164
- (22) International Filing Date: 23 July 2002 (23.07.2002)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:  
09/927,024 9 August 2001 (09.08.2001) US
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- (81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZM, ZW.
- (84) Designated States (*regional*): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM),

[Continued on next page]

(54) Title: METHOD FOR FABRICATING A THIN-MEMBRANE STENCIL MASK AND METHOD FOR MAKING A SEMI-CONDUCTOR DEVICE USING THE SAME



(57) Abstract: A stencil mask (12 or 12) has both a thin membrane layer (106) and a stress controlled layer (104) for enabling electron and ion projection lithography at very small geometries. The thin membrane layer (106) is within a range of substantially forty to two hundred nanometers and is preferably silicon nitride, and the stress controlled layer is preferably a metal or a metal alloy. Annealing of the stress controlled layer (104) may be performed to obtain a desired stress characteristic. Semiconductors are made using the mask by projecting radiation through the thin membrane stencil mask and reduction optics (30) onto resist (44) formed on a plurality of die, the radiation forming a contrast image on the resist that is subsequently developed. Commercially available lithography equipment is compatible with the thin stencil mask.



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European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

**(88) Date of publication of the international search report:**

24 April 2003

**Published:**

— with international search report

*For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*

INTERNATIONAL SEARCH REPORT

International Application No

PCT/US 02/24164

A. CLASSIFICATION OF SUBJECT MATTER

IPC 7 G03F1/16

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 G03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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X	US 5 500 312 A (HARRIOTT LLOYD R ET AL) 19 March 1996 (1996-03-19) column 5, line 28 - line 55 ---	1,3,6
X	PATENT ABSTRACTS OF JAPAN vol. 1998, no. 05, 30 April 1998 (1998-04-30) & JP 10 010706 A (DAINIPPON PRINTING CO LTD), 16 January 1998 (1998-01-16) abstract ---	1
X	US 5 935 739 A (KALT SAMUEL ET AL) 10 August 1999 (1999-08-10) column 3, line 57 -column 4, line 12; figure 1 --- -/--	1

Further documents are listed in the continuation of box C.

Patent family members are listed in annex.

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Date of the actual completion of the international search

21 January 2003

Date of mailing of the international search report

05/02/2003

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International Application No

PCT/US 02/24164

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