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(12) **United States Design Patent**
Phipps et al.

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(45) **Date of Patent:** **** Aug. 2, 2005**

(54) **CHIP AND LIGHT EMITTING DIODE PANEL HOUSING**

4,763,781 A * 8/1988 Donalson et al. 206/707
5,235,496 A * 8/1993 Chomette et al. 361/764
5,375,709 A * 12/1994 Petro 206/709
6,100,468 A * 8/2000 Niggl et al. 174/52.1

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* cited by examiner

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(**) Term: **14 Years**

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(21) Appl. No.: **29/212,946**

(57) **CLAIM**

(22) Filed: **Sep. 10, 2004**

We claim the ornamental design for a chip and light emitting diode panel housing, as shown and described.

(51) **LOC (8) Cl.** **13-03**

DESCRIPTION

(52) **U.S. Cl.** **D13/184**

(58) **Field of Search** D13/182, 184;
D9/418; 174/50, 52.1; 206/706, 707, 709;
220/4.02; 361/600, 601, 730, 736, 748;
438/107

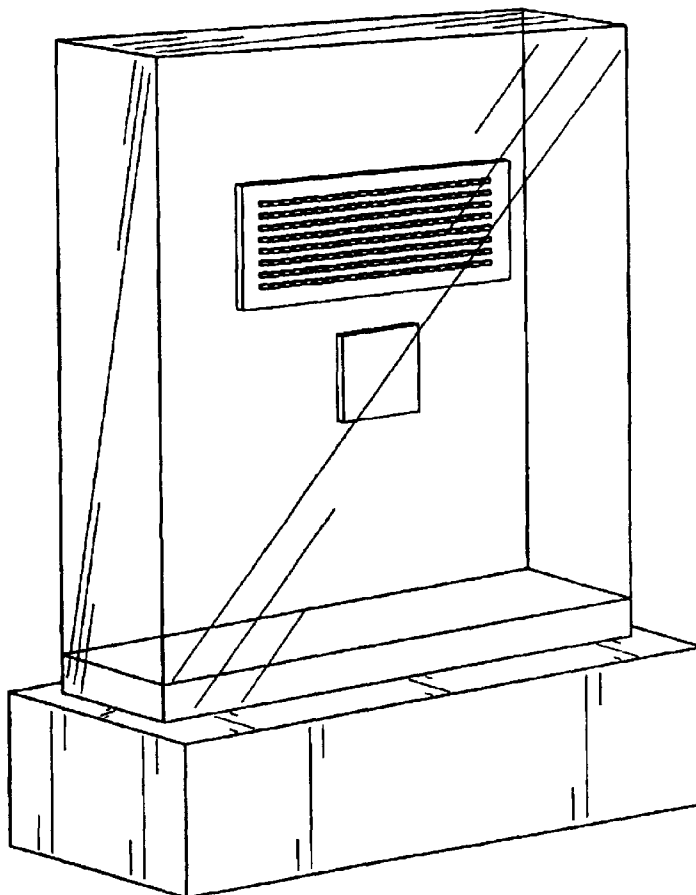
FIG. 1 is a perspective view of a chip and light emitting diode panel housing in accordance with the design; FIG. 2 is a front view of the housing of FIG. 1; FIG. 3 is a back view of the housing of FIG. 1; FIG. 4 is a left view of the housing of FIG. 1; FIG. 5 is a right view of the housing of FIG. 1; FIG. 6 is a top view of the housing of FIG. 1; and, FIG. 7 is a bottom view of the housing of FIG. 1.

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,746,009 A * 5/1988 Liberman 206/723

1 Claim, 7 Drawing Sheets



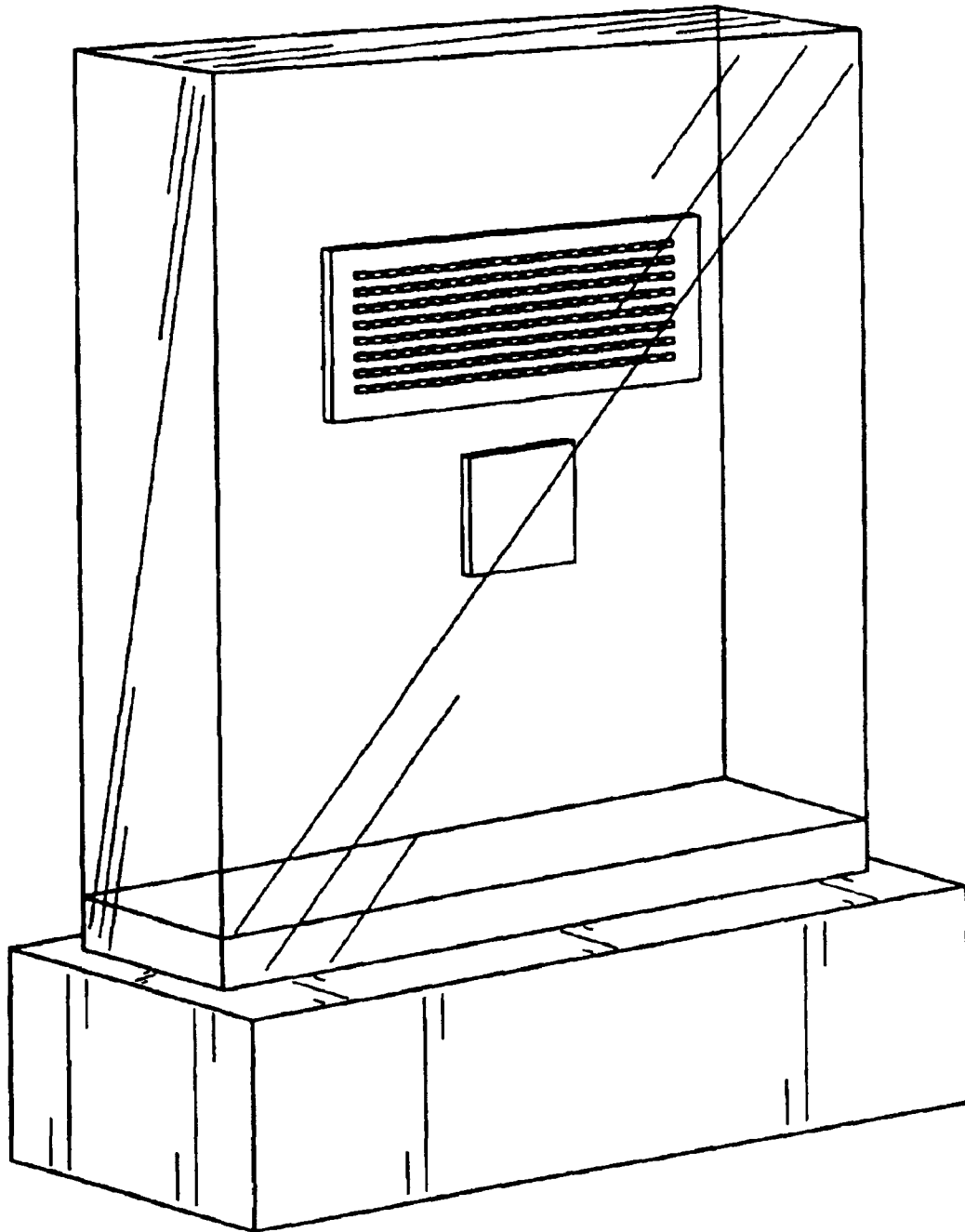


FIG. 1

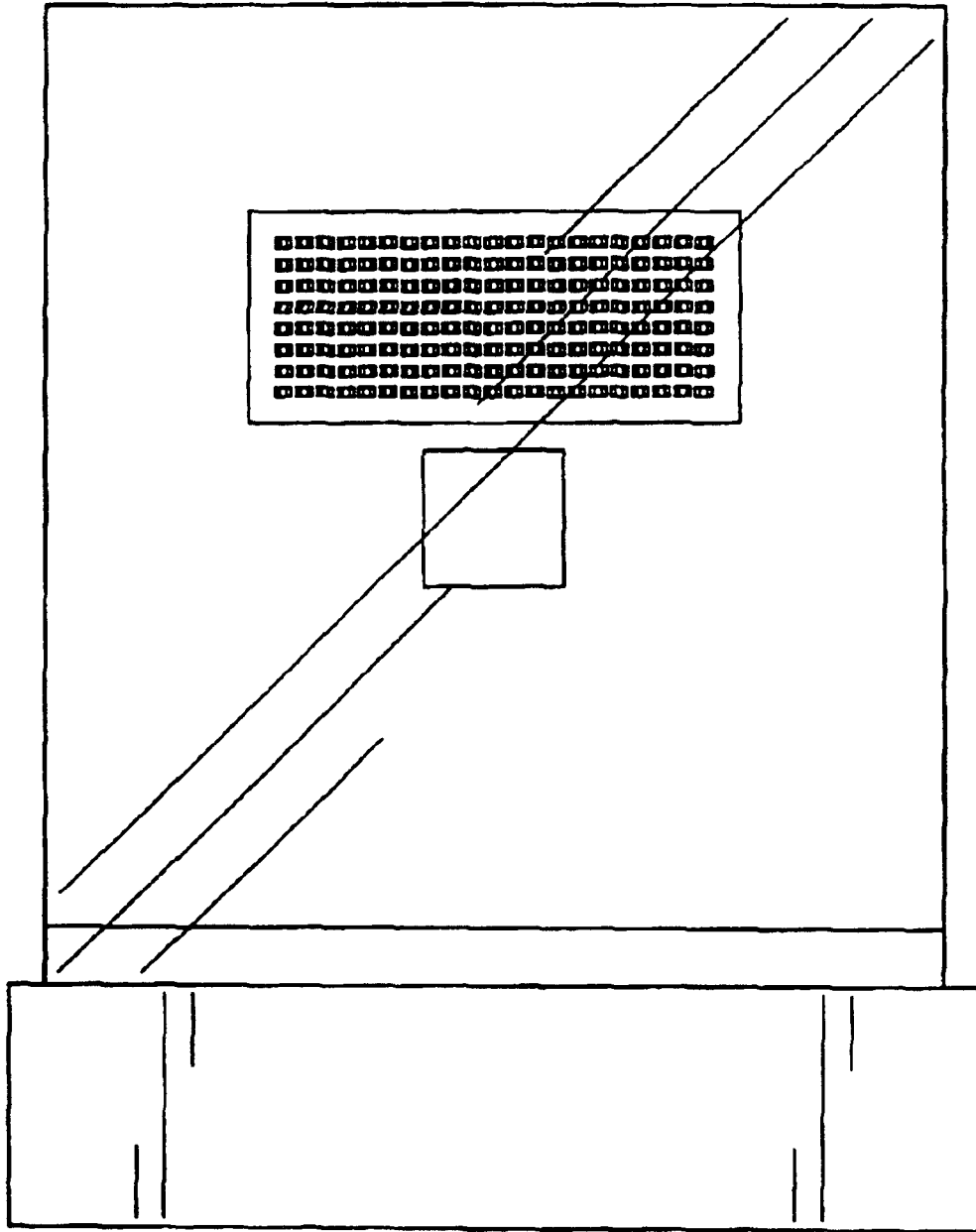


FIG. 2

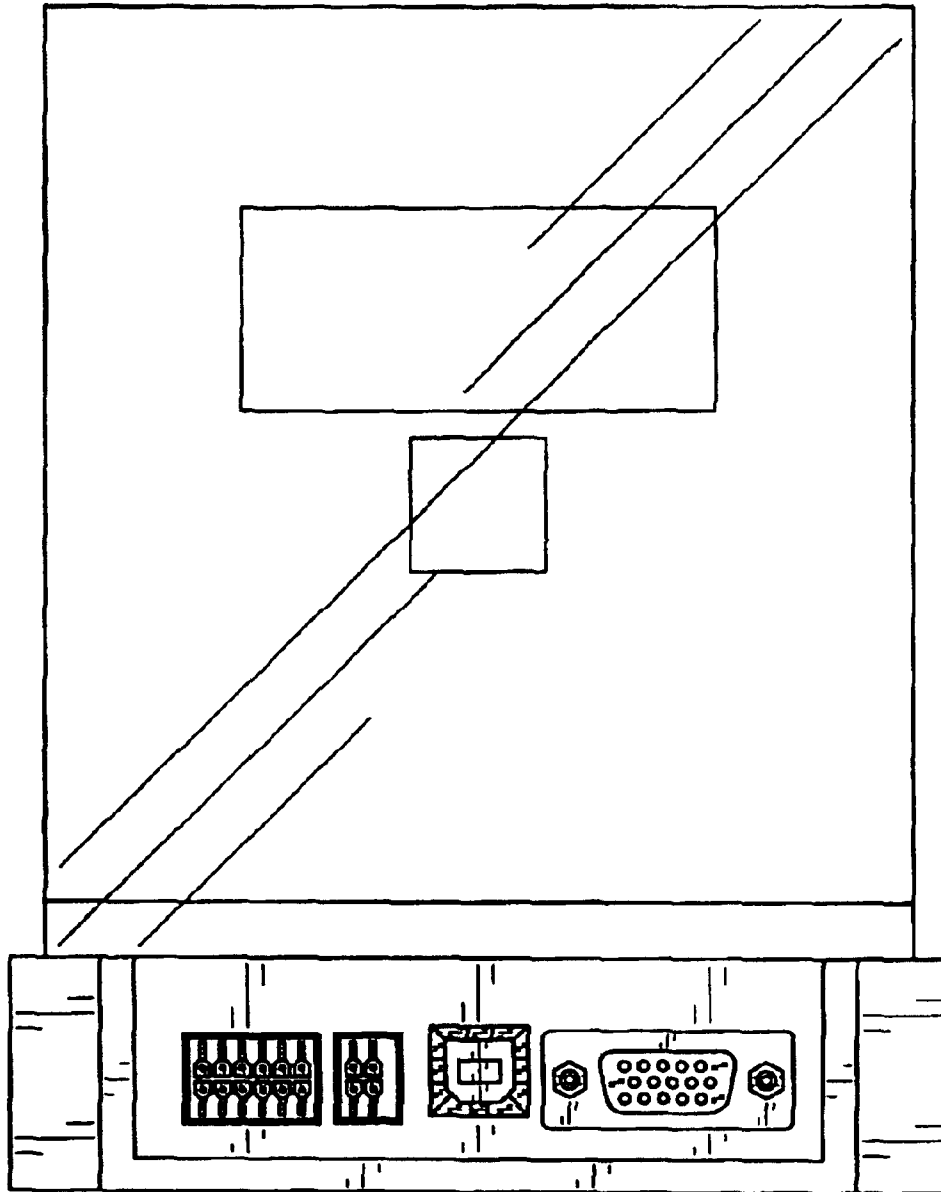


FIG. 3

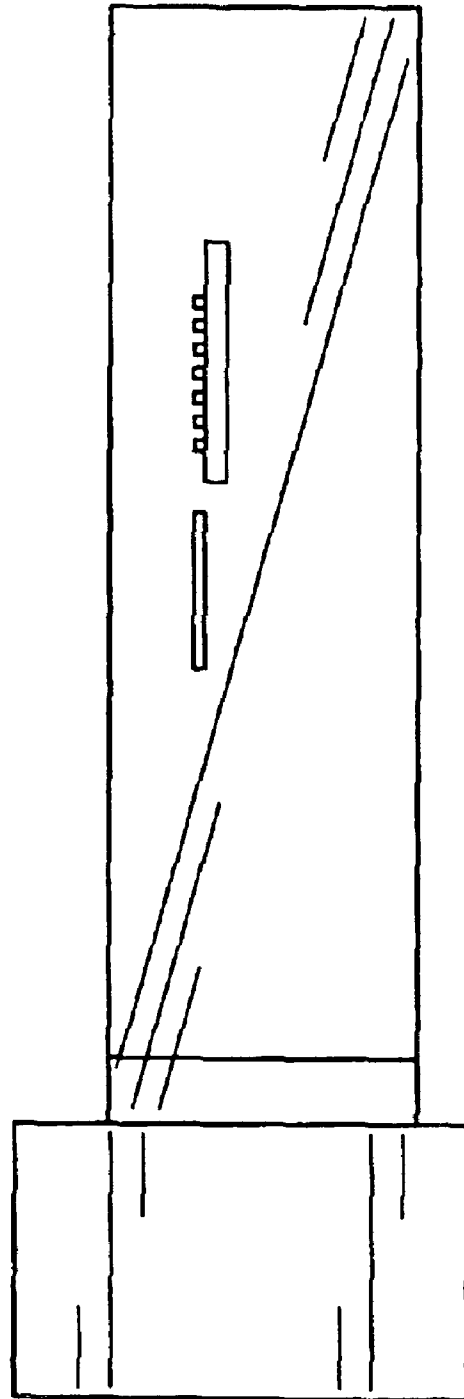


FIG. 4

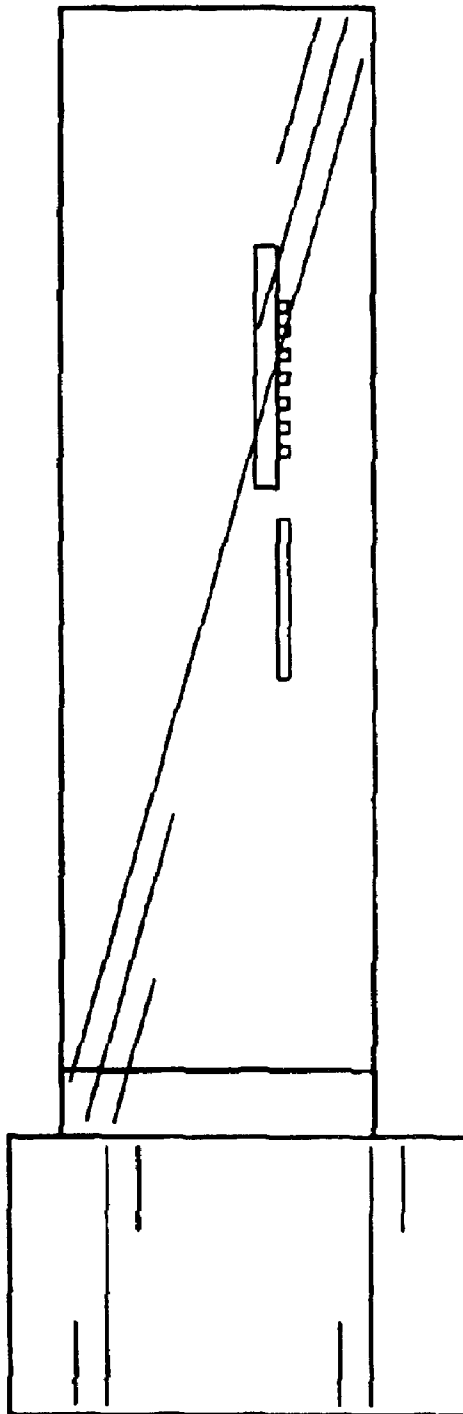


FIG. 5

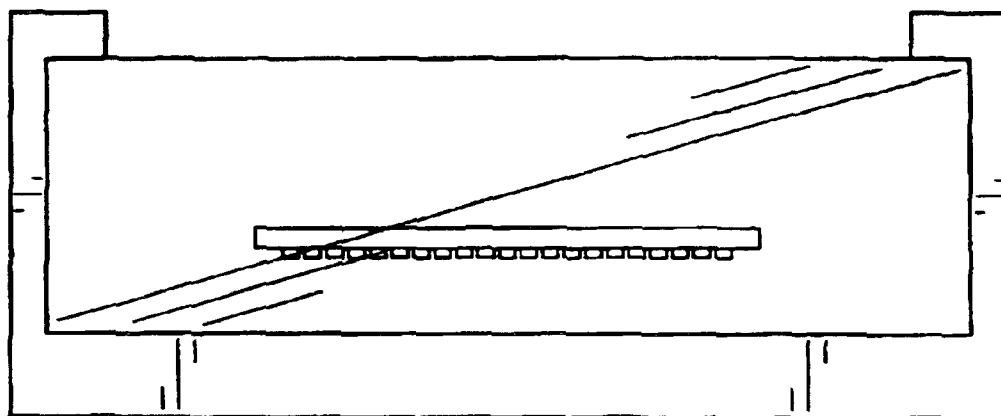


FIG. 6

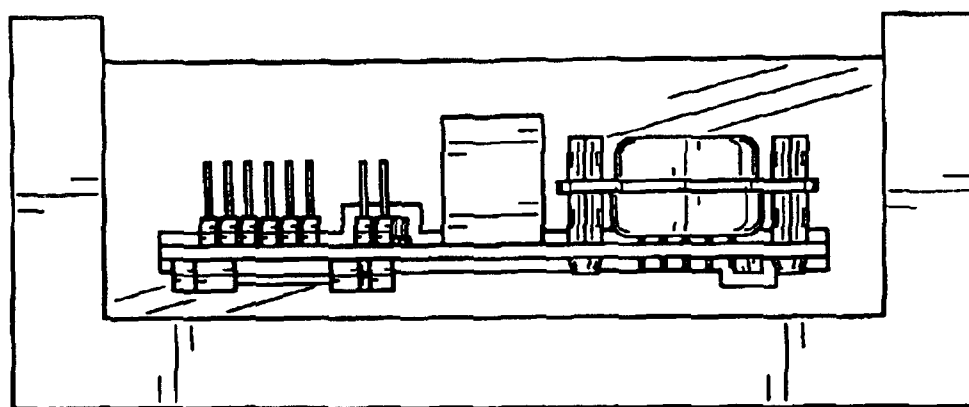


FIG. 7