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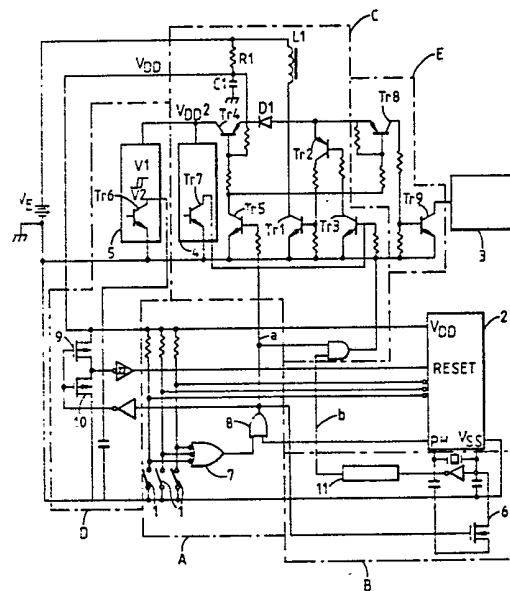
(56) Documents cited  
 GB A 2125975 EP A2 0049462 US 4685023  
 US 4537488

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(54) Power circuit for a camera

(57) A power circuit for a camera comprises a power activation unit (A) containing a release switch group (1) for activating the camera, a step-up unit (C) for stepping up the voltage ( $V_E$ ) of a battery under the control of the power activation unit, and a CPU (2) arranged to be driven by the output ( $V_{DD}$ ) of the step-up unit so as to control the operation of the camera, and which has a reset terminal for stopping operation. A unit (5) detects the output voltage of the step-up unit and generates a detection signal when the output voltage is lower than a predetermined set voltage which corresponds to a limiting operation voltage of the CPU. The detection signal is connected to the reset terminal so as to stop the operation of the CPU when the output of the step-up unit is lower than the limiting operation voltage of the CPU.

Fig.1



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Fig.1

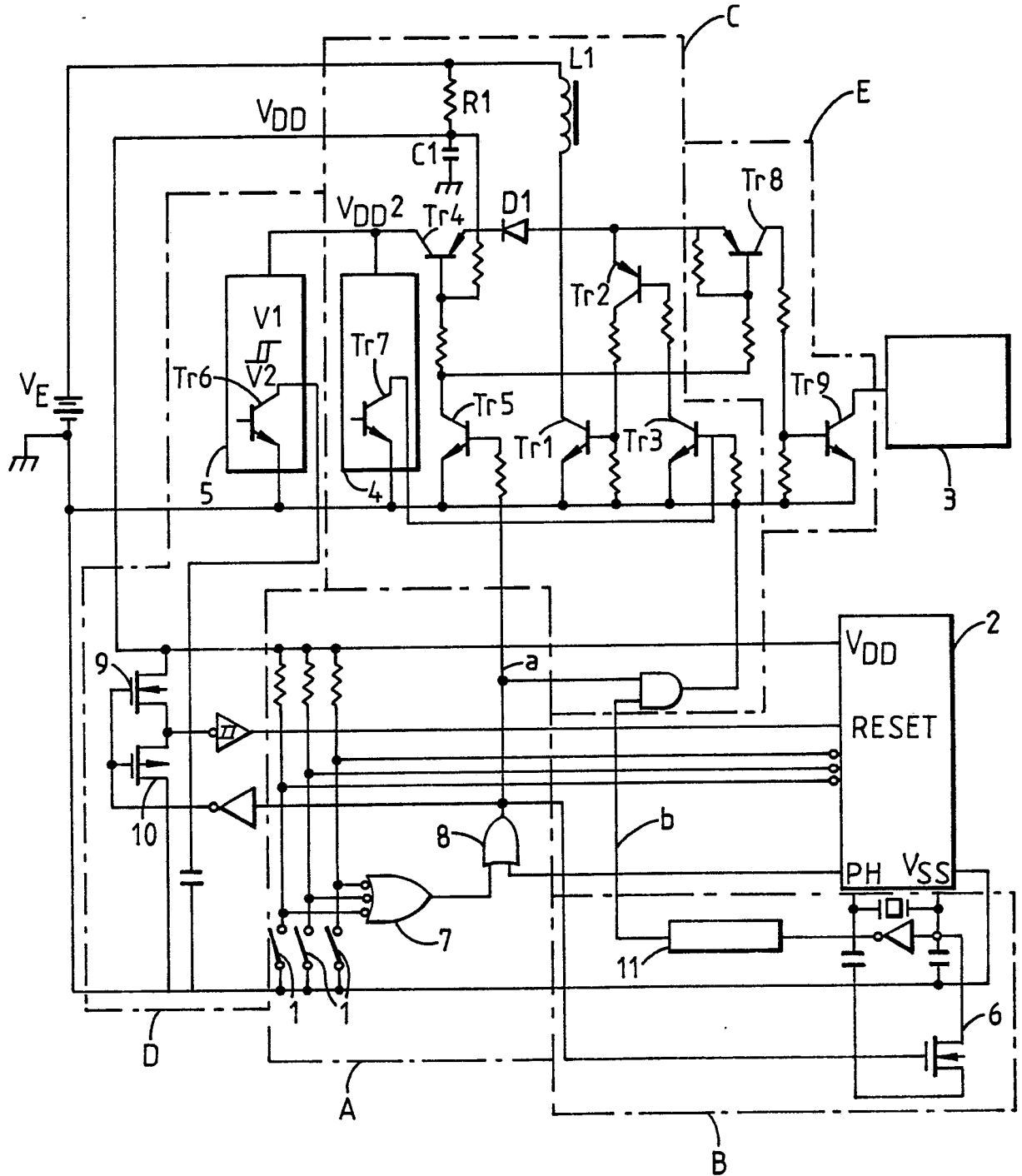


Fig.2

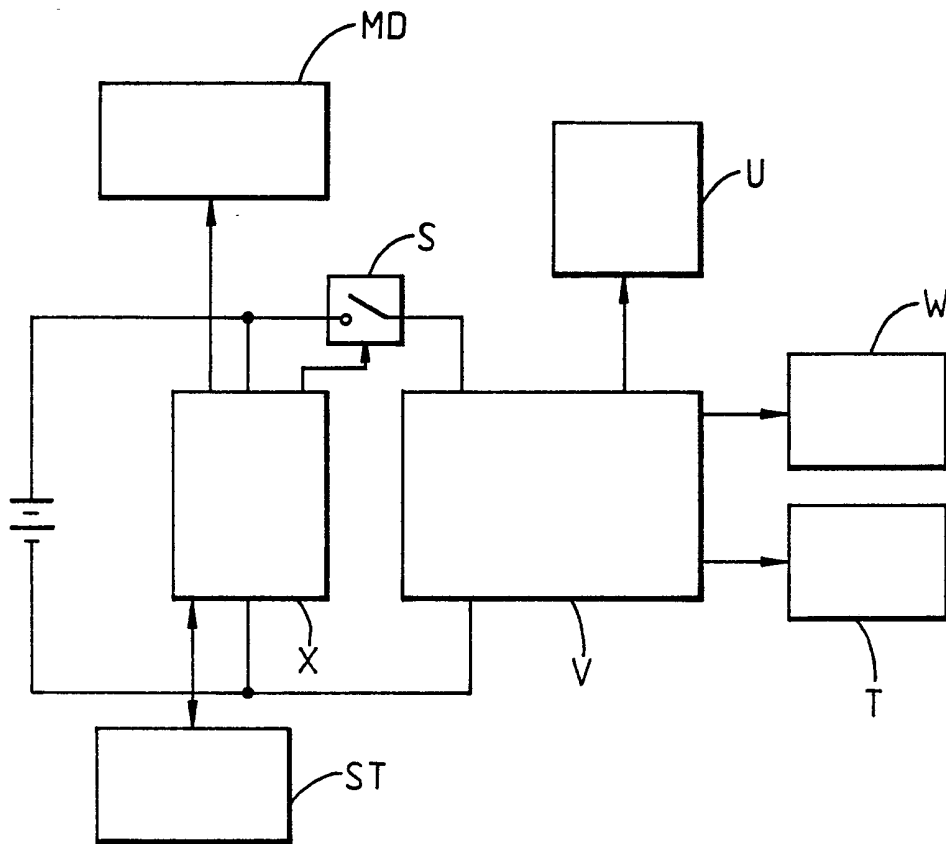


Fig.3

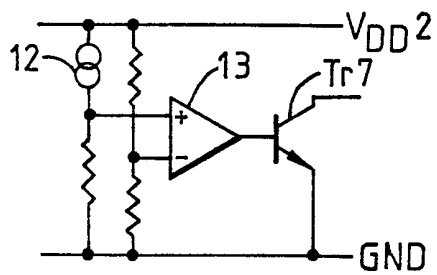
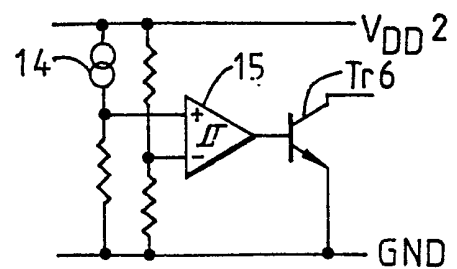


Fig.4



**POWER CIRCUIT FOR A CAMERA**

5           This invention relates to power circuits for  
cameras.

          Over the past few years, electronic circuits have  
been used more and more in cameras, and many operations,  
which had previously depended on the experience and  
10       perception of human operators, are now automatically  
performed by electronic circuits which, for example,  
control exposure time, control automatically camera-to-  
shutter distance, etc. Microcomputers are often used as  
the electronic circuits in view of the degree of freedom  
15       of control and reduction in development time.

          Although a battery is generally used as a power  
source in a camera, the voltage of the battery in a  
camera which has a strobo (flash) unit or an auto-  
loading function for automatically winding on films, can  
20       temporarily vary. In such a camera, the source voltage  
to a microcomputer will also vary, resulting in  
malfunctioning of the microcomputer. It is therefore  
necessary to use a step-up power source as a source of  
voltage for such a microcomputer.

25           However, there is a danger that, if the voltage of  
the step-up power source is not sufficiently high when

the microcomputer starts operation even after the voltage has been stepped up, or if the voltage of the step-up power source is not completely stepped up and falls for some reason during operation of the microcomputer, the operation of the microcomputer becomes unstable, resulting in malfunctioning.

Figure 2 is a block diagram of a conventional power source for a camera. Heretofore, a battery voltage is directly applied to a microcomputer, with no step-up circuit being provided. Therefore, a controller X which can operate at lower voltages is used to supply power to a driver MD which drives a strobo circuit ST and a motor for winding on and rewinding films, and a switch S for supplying power to a microcomputer V, are controlled so that, if the battery voltage drops, the supply of the battery voltage to the microcomputer V is turned off to ensure that the microcomputer cannot be operated. There is, therefore, a disadvantage in that the usable range of battery voltage is extremely limited, and thus vital shutter release time can be lost. In Figure 2, reference letter U represents a shutter, reference letter W an A/F circuit and reference letter T a photometric circuit.

Although the above described problem can be solved by providing a multifunctional controller X, it is

disadvantageous to provide those functions in the microcomputer itself in view of reduction in development time and the degree of freedom to change. To overcome  
5 the problem, it was, therefore, thought that the source voltage of the microcomputer could be maintained at a value above a limiting operation voltage, i.e. the minimum operation voltage, even if the battery voltage falls, by using a step-up circuit. However, the  
10 functions of a step-up circuit are limited, and there is a danger than when, for example, the capacity of the battery is reduced in the last stages of its life or if a film is being wound on or rewound immediately after a strobo has been charged, the step-up source voltage of  
15 the microcomputer will become lower and the minimum operation voltage and the microcomputer will mis-operate.

The present invention seeks to provide a power circuit for a camera using a microcomputer, malfunction  
20 of which is prevented by resetting it when the voltage of a step-up power source is lower than a minimum operation voltage of the microcomputer or becomes lower than the minimum operation voltage of the microcomputer during operation thereof.

25 Although the present invention is primarily directed to any novel integer or step, or combination of

integers or steps, herein disclosed and/or as shown in the accompanying drawings, nevertheless, according to one particular aspect of the present invention to which, 5 however, the invention is in no way restricted, there is provided a power circuit for a camera comprising: a power activation means containing release switch means for activating said camera; a step-up means for starting to step up the voltage of a battery under the control of 10 said power activation means; a CPU arranged to be driven by an output of said step-up means so as to control the operation of said camera and which has a reset terminal for stopping said operation; and a voltage detecting means for detecting the output voltage of said step-up 15 means and for generating a detection signal when said output voltage is lower than a predetermined set voltage, said predetermined set voltage corresponding to a limiting operation voltage of said CPU and said detection signal being connected to said reset terminal 20 so as to stop the operation of said CPU when the output of said step-up means is lower than said limiting operation voltage of said CPU.

The power circuit may include oscillator means the output of which is provided to the step-up means.

25 Preferably said voltage detecting means includes a constant current source and resistor means for

determining said predetermined set voltage and a comparator for generating said detection signal when said output voltage of the step-up means is lower than said predetermined set voltage.

In one embodiment the power circuit includes an inverter, which together with the voltage detecting means, constitutes reset means connected to the reset terminal of the CPU to stop operation thereof.

The step-up means may include a coil.

The invention is illustrated, merely by way of example, in the accompanying drawings, in which:-

Figure 1 is a block diagram of a power circuit according to the present invention for a camera;

Figure 2 is a block diagram of a conventional power circuit for a camera;

Figure 3 is a circuit diagram of a  $V_{DD}$  detecting regulator of the power circuit of Figure 1; and

Figure 4 is a circuit diagram of a  $V_{DD}$  detecting resetter of the power circuit of Figure 1.

Figure 1 is a circuit diagram of a power circuit according to the present invention for a camera. A portion A surrounded by a broken line in Figure 1 denotes a power activation unit which includes a power activation switch group 1, for example, comprising a shutter release switch and a film-rewinding switch. A



CPU 2 determines which switch has activated the power source and performs a given function. For example, if the power source is turned on by the shutter release switch, an exposure is performed and then the film is automatically wound on.

If any one of the switches of the power activation switch group 1 turns on the power source, the output of an OR gate 8, i.e., an output a of the power activation unit A, goes high and a start signal is produced. The power activation cause that produced the output a is also fed to the CPU 2. A PH signal connected to one input terminal of the OR gate 8 is set when a program in the CPU 2 is started, so that the output a of the power activation unit A is maintained high even if the power activation switch group 1 is turned off during the operation of the CPU 2.

A portion B surrounded by a broken line in Figure 1 denotes a standby oscillator in which, when the output a of the power activation unit A goes high, an N-channel FET 6 is turned off so that oscillation is started and is output to the CPU 2. A step-up clock b is also output to a step-up circuit C through a frequency division circuit 11. When the output a of the power activation unit A goes low, the N-channel FET 6 is turned on so that oscillation is stopped and the current

consumed by the standby oscillator B becomes zero.

In a standby state wherein the output a of the power activation unit A is low, all of transistors Tr1, Tr2, Tr3 of the step-up circuit C are turned off. Thus, a step-up power source  $V_{DD}$  is made to be  $V_E$  ( $V_E =$  battery voltage) by a resistor R1, a step-up coil L1, and a diode D1. Since, at the same time, transistors Tr4, Tr5 are both turned off, when  $V_{DD} = V_E$ , the current consumed by the step-up circuit C becomes substantially zero. The resistor R1 is a resistor for increasing the step-up power source  $V_{DD}$  to the battery voltage  $V_E$ .

When the step-up clock b is input to the transistor Tr3, it is amplified by the transistors Tr2, Tr1 so as to switch the step-up coil L1. When the transistor Tr1 is turned on, a current passes through the step-up coil L1, and, when it is turned off, the energy stored in the step-up coil L1 is stored in a capacitor C1 through the diode D1. If the voltage  $V_{DD}$  of the capacitor C1 is above a given value, a transistor Tr7 is turned on and the transistor Tr3 is turned off so that the input of the step-up clock b is blocked. If the voltage  $V_{DD}$  falls below the given value, the transistor Tr7 is turned off so that the step-up clock is input. Therefore, the voltage  $V_{DD}$  is stepped up to a substantially constant voltage.

When the output a of the power activation circuit A goes high, the transistor Tr5, Tr4 are turned on so that the step-up power source  $V_{DD}$  is applied to a  $V_{DD}$  detecting regulator 4 and the step-up clock is input to the transistor Tr3 to start the stepping up. The  $V_{DD}$  detecting regulator 4 controls the step-up clock b input to the base of the transistor Tr3 so as to stabilise the step-up power source  $V_{DD}$  (the transistor Tr7 is turned on or off by the voltage  $V_{DD}$ ).

When the output a of the power activation circuit A goes low, the stepping up is immediately stopped so that the voltage of the step-up power source  $V_{DD}$  gradually becomes closer to the battery voltage  $V_E$ .

A portion D surrounded by a broken line in Figure 1 denotes a reset circuit for controlling the resetting of the CPU 2. A  $V_{DD}$  detecting resetter 5 turns off the transistor Tr6 when the voltage of the step-up power source  $V_{DD}$  becomes higher than a voltage V1, and turns on the transistor Tr6 when the step-up power source  $V_{DD}$  becomes lower than a voltage V2. The voltages V1, V2 are each set at a value slightly higher than the minimum operation voltage of the CPU 2.

When the output a of the power activation unit A is low, the transistor Tr4 is turned off so that the step-up power source  $V_{DD}$  is not applied to the  $V_{DD}$

detecting resetter 5. In addition, the output of an inverter comprising FETs 9,10 goes low so that the CPU 2 is reset. At this point, the current consumed by the reset circuit D becomes substantially zero. When the output a of the power activation unit A goes high, the output of the inverter also goes high, and the voltage of the step-up power source  $V_{DD}$  is immediately applied to the  $V_{DD}$  detecting resetter 5. At this point, if  $V_{DD} < V_1$ , the transistor Tr6 is turned on so that the CPU 2 is kept in the reset state. If  $V_E \geq V_1$  i.e., if  $V_{DD} \geq V_1$ , the reset state is immediately removed. Therefore if the voltage of the step-up power source  $V_{DD}$  is lowered for some reason and becomes less than the voltage  $V_2$  during the operation of the CPU 2, the transistor Tr6 is turned on so that the CPU is reset, thus preventing runaway. Hysteresis is imparted to the  $V_{DD}$  detecting resetter 5 since  $V_1 > V_2$ .

A portion E surrounded by a broken line in Figure 1 denotes a strobo step-up inhibiting signal output unit in which, when the output a of the power activation unit A goes high, transistors Tr8, Tr9 are turned on so as to inhibit strobo step-up and, when the output a goes low, the transistors Tr8, Tr9 turn off so as to release the inhibition of the strobo set-up.

The voltage of the step-up power source  $V_{DD}$  is

always applied to the CPU 2. When the reset is released, the program in the CPU 2 is started, the PH signal is reset so that the output a of the power  
5 activation unit A is kept high, and the CPU 2 checks which of the switches of the power activation switch group 1 activated the power source and performs a given operation.

Even if the power activation switch group 1 is  
10 turned off while the CPU 2 is operating, the operation can continue because the PH signal is set. When the given operation is completed, the PH signal is reset and, if the power activation switch group 1 has been turned off at this point, the CPU is reset. If the  
15 power activation switch group 1 is turned on, the CPU is reset when the power activation switch group 1 is turned off.

When on standby, in which all the switches of the power activation switch group 1 are turned off and no  
20 operation is being performed, the capacitor C1 is charged with the battery voltage  $V_E$  by the step-up coil L1, the diode D1, and the resistor R1, so the output a of the power activation unit A goes low and the N-channel FET 6 is turned on, so that the standby  
25 oscillator B is not operated. In addition, the transistors Tr1, Tr2, Tr3, Tr4, Tr8 are turned off and

the output of the inverter comprising FETs 9,10 in the reset circuit D goes low, so that the current consumed from the battery voltage  $V_E$  becomes substantially zero. This means that, during standby, the battery voltage is applied to the CPU 2.

If one of the switches of the power activation switch group 1 is turned on when the device is on standby, the output a of the power activation unit A goes high and the standby oscillator B starts to oscillate. At the same time, the step-up clock B is applied to the base of the transistor Tr5 so as to start the stepping up, and the transistors Tr2, Tr6 are turned on so as to output a strobo step-up inhibiting signal. The step-up power source  $V_{DD}$  detection is applied to the  $V_{DD}$  detecting resetter 5 and the  $V_{DD}$  detecting regulator 4.

In this state, if the battery voltage is higher than the voltage V1, the reset is removed by the output from the  $V_{DD}$  detecting resetter so that the program is started. Alternatively, if the battery voltage is lower than the voltage V1, the reset state is held by the output from the  $V_{DD}$  detecting resetter 5. Thereafter, when the voltage of the step-up power source  $V_{DD}$  becomes higher than the voltage V1, the reset is removed so that the program is started. When the

program is started, the CPU 2 checks which power activation switch started the power source, and the PH signal from the CPU 2 is set so that the operation  
5 corresponding to the selected switch of the power activation switch group 1 is started. While the CPU 2 is operating, its operation is continued by the PH signal even if the power activation switch group 1 is turned off.

10 When the given operation has been completed, the PH signal is reset, and, if the power activation switch group 1 is not on at this point, the output a of the power activation unit goes low and the CPU 2 is immediately reset so that it is on standby. If the  
15 power activation switch group 1 is on, the CPU is reset when the power activation switch group is turned off, so that it is on standby. While it is on standby, if the battery voltage drops during strobo step-up, immediately after strobo step-up, or immediately after the film has  
20 been wound on, and if the power activation switch group 1 has been turned on, the reset state is maintained until the voltage of the step-up power source  $V_{DD}$  becomes higher than the voltage  $V_1$ .

If the voltage of the step-up power source  $V_{DD}$   
25 falls below the voltage  $V_2$  for some reason during operation (for example, the fall of battery voltage or

instantaneous termination of the battery voltage) the CPU 2 is immediately reset by the signal of the  $V_{DD}$  detecting resetter 5 so as to prevent runaway. In addition, the transistor Tr5 is turned on and the transistors Tr8, Tr9 are thus turned on, so that step-up of a strobo circuit 3 is inhibited during operation.

After the operation of the CPU 2 has been completed, the CPU 2 is reset. Therefore, if the power activation switch group 1 is turned off when the PH signal is reset, the output a of the power activation unit A goes low, so the transistor Tr5 is turned on to ensure that the step-up is stopped and the CPU is reset. The oscillation of the standby oscillator B is also stopped so that the power circuit returns to the standby state. If the operation is completed in the state wherein the power activation switch group 1 is on, the power circuit returns to the standby state when the power activation switch group 1 is turned off.

The  $V_{DD}$  detecting resetter 5 comprises a known comparator 15, a unit 14 for generating a constant current and a breeder resistor for detecting the voltage  $V_{DD}$ , as shown in Figure 4. The  $V_{DD}$  detecting regulator is constructed in the same manner as the detecting resetter 5, as shown in Figure 3, and comprises a known comparator 13, a unit 12 for generating a constant



current and a breeder resistor. In the embodiment of  
the present invention described above, each of the units  
A to E are employed independently of the CPU, but any  
5 may be formed on the same chip as the CPU.

As described above, the present invention has the  
effect that it can prevent runaway of a microcomputer,  
which is the most difficult phenomenon to prevent in an  
instrument using a microcomputer, and also brings about  
10 no undesirable malfunctioning and no increase in the  
current consumed while the device is on standby, and can  
realise control with some degree of freedom.

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**CLAIMS**

1. A power circuit for a camera comprising: a power  
5 activation means containing release switch means for  
activating said camera; a step-up means for starting to  
step up the voltage of a battery under the control of  
said power activation means; a CPU arranged to be driven  
10 by an output of said step-up means so as to control the  
operation of said camera and which has a reset terminal  
for stopping said operation; and a voltage detecting  
means for detecting the output voltage of said step-up  
means and for generating a detection signal when said  
15 output voltage is lower than a predetermined set  
voltage, said predetermined set voltage corresponding to  
a limiting operation voltage of said CPU and said  
detection signal being connected to said reset terminal  
so as to stop the operation of said CPU when the output  
of said step-up means is lower than said limiting  
20 operation voltage of said CPU.

2. A power circuit as claimed in claim 1 including  
oscillator means the output of which is provided to the  
step-up means.

3. A power circuit as claimed in claim 1 or 2 in  
25 which said voltage detecting means includes a constant  
current source and resistor means for determining said

predetermined set voltage and a comparator for  
generating said detection signal when said output  
voltage of the step-up means is lower than said  
5 predetermined set voltage.

4. A power circuit as claimed in any preceding claim  
including an inverter, which together with the voltage  
detecting means, constitutes reset means connected to  
the reset terminal of the CPU to stop operation thereof.

10 5. A power circuit as claimed in any preceding claim  
in which the step-up means includes a coil.

6. A power circuit for a camera substantially as  
herein described with reference to and as shown in  
Figures 1, 3 and 4 of the accompanying drawings.

15 7. Any novel integer or step, or combination of  
integers or steps, hereinbefore described and/or as  
shown in the accompanying drawings, irrespective of  
whether the present claim is within the scope of or  
relates to the same, or a different, invention from that  
20 of the preceding claims.

8. A power circuit for a camera comprising: a power  
activation means containing a release switch for  
activating said camera; a step-up means for starting to  
step up the voltage of a battery by said power  
25 activation means; a CPU which is driven by an output of  
said step-up means so as to control the operation of

said camera and which has a reset terminal for stopping  
said operation; and a voltage detecting means for  
detecting the output level of said step-up means and for  
5 generating a detection signal when said level is lower  
than a set value which has previously been determined;  
said set value being set to correspond to the limiting  
operation voltage of said CPU and said detection signal  
being connected to said reset terminal so as to stop the  
10 operation of said CPU when the output of said step-up  
means is lower than said limiting operation voltage of  
said CPU.

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