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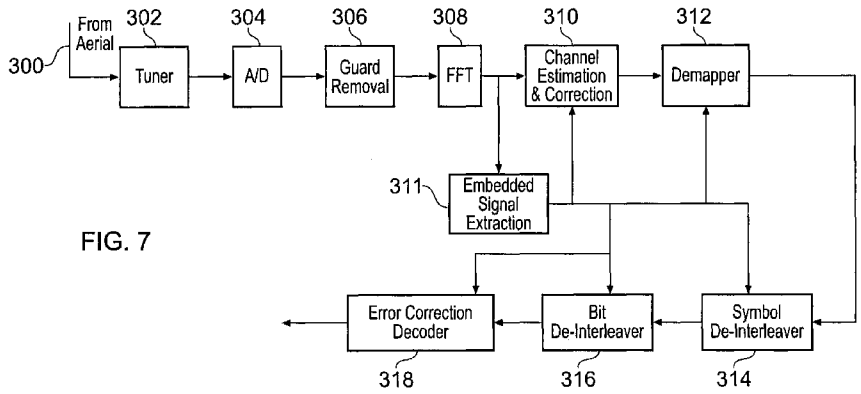

FIG. 7

(57) Abstract: A data processing apparatus maps input symbols to be communicated onto a predetermined number of sub-carrier signals of an Orthogonal Frequency Division Multiplexed (OFDM) symbol. The data processor includes an interleaver memory which reads-in the predetermined number of data symbols for mapping onto the OFDM sub-carrier signals. The interleaver memory reads-out the data symbols on to the OFDM sub-carriers to effect the mapping, the read-out being in a different order than the read-in, the order being determined from a set of addresses, with the effect that the data symbols are interleaved on to the sub-carrier signals. The set of addresses are generated from an address generator which comprises a linear feedback shift register and a permutation circuit. A generator polynomial for the linear feedback shift register of $R'_i[7] = R'_{i-1}[0] \oplus R'_{i-1}[1] \oplus R'_{i-1}[5] \oplus R'_{i-1}[6]$ is provided with a permutation order which has been established by simulation analysis to optimise communication performance via typical radio channels, of an OFDM modulated system such as a Digital Video Broadcasting (DVB) standard such as DVB- Terrestrial2 (DVB-T2).

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DATA PROCESSING APPARATUS AND METHOD

Field of Invention

The present invention relates to data processing apparatus operable to map input symbols onto sub-carrier signals of an Orthogonal Frequency Division Multiplexed (OFDM) symbol. The present invention also relates to an address generator for use in writing symbols to/reading symbols from an interleaver memory.

The present invention also relates to data processing apparatus operable to map symbols received from a predetermined number of sub-carrier signals of an OFDM symbol into an output symbol stream.

Embodiments of the present invention can provide an OFDM transmitter/receiver.

Background of the Invention

The Digital Video Broadcasting-Terrestrial standard (DVB-T) utilises Orthogonal Frequency Division Multiplexing (OFDM) to communicate data representing video images and sound to receivers via a broadcast radio communications signal. There are known to be two modes for the DVB-T standard which are known as the 2k and the 8k mode. The 2k mode provides 2048 sub-carriers whereas the 8k mode provides 8192 sub-carriers. Similarly for the Digital Video Broadcasting-Handheld standard (DVB-H) a 4k mode has been provided, in which the number of sub-carriers is 4096.

In order to improve the integrity of data communicated using DVB-T or DVB-H a symbol interleaver is provided in order to interleave input data symbols as these symbols are mapped onto the sub-carrier signals of an OFDM symbol. Such a symbol interleaver comprises an interleaver memory in combination with an address generator. The address generator generates an address for each of the input symbols, each address indicating one of the sub-carrier signals of the OFDM symbol onto which the data symbol is to be mapped. For the 2k mode and the 8k mode an arrangement has been disclosed in the DVB-T standard for generating the addresses for the mapping. Likewise for the 4k mode of the DVB-H standard, an arrangement for generating addresses for the mapping has been provided and an address generator for

implementing this mapping is disclosed in European Patent application 04251667.4. The address generator comprises a linear feed back shift register which is operable to generate a pseudo random bit sequence and a permutation circuit. The permutation circuit permutes the order of the content of the linear feed back shift register in order to generate an address. The address provides an indication of one of the OFDM sub-carriers for carrying an input data symbol stored in the interleaver memory, in order to map the input symbols onto the sub-carrier signals of the OFDM symbol.

In accordance with a further development of the Digital Video Broadcasting-Terrestrial broadcasting standard, known as DVB-T2 there has been proposed that further modes for communicating data be provided.

Summary of Invention

According to an aspect of the present invention there is provided a data processing apparatus operable to map input symbols to be communicated onto a predetermined number of sub-carrier signals of an Orthogonal Frequency Division Multiplexed (OFDM) symbol. The data processing apparatus comprises an interleaver operable to read-into a memory the predetermined number of data symbols for mapping onto the OFDM sub-carrier signals, and to read-out of the memory the data symbols for the OFDM sub-carriers to effect the mapping. The read-out is in a different order than the read-in, the order being determined from a set of addresses, with the effect that the data symbols are interleaved on the sub-carrier signals. The set of addresses is determined by an address generator, an address being generated for each of the input symbols to indicate one of the sub-carrier signals onto which the data symbol is to be mapped.

The address generator comprises a linear feedback shift register including a predetermined number of register stages and is operable to generate a pseudo-random bit sequence in accordance with a generator polynomial, and a permutation circuit and a control unit. The permutation circuit is operable to receive the content of the shift register stages and to permute the bits present in the register stages in accordance with a permutation order to form an address of one of the OFDM sub-carriers.

The control unit is operable in combination with an address check circuit to re-generate an address when a generated address exceeds a predetermined maximum valid address. The data processing apparatus is characterised in that the predetermined maximum valid address is approximately five hundred, the linear feedback shift register has eight register stages with a generator polynomial for the linear feedback shift register of $R'_i[7] = R'_{i-1}[0] \oplus R'_{i-1}[1] \oplus R'_{i-1}[5] \oplus R'_{i-1}[6]$, and the permutation order forms, with an additional bit, a nine bit address $R_i[n]$ for the i-th data symbol from the bit present in the n-th register stage $R'_i[n]$ in accordance with the table:

R'_i bit positions	7	6	5	4	3	2	1	0
R_i bit positions	3	7	4	6	1	2	0	5

Although it is known within the DVB-T standard to provide the 2k mode and the 8k mode, and the DVB-H standard provides a 4k mode, it would be beneficial to provide a 0.5k mode interleaver for DVB-T2. The lower the order of the mode, the more frequently the channel estimation can be updated allowing the receiver to track the time variation of the channel due to doppler and other effects more accurately. In some embodiments, the present invention can provide a data processing apparatus operable as a symbol interleaver for mapping data symbols to be communicated on an OFDM symbol, having substantially five hundred sub-carrier signals.

In other embodiments, the present invention can provide a data processing apparatus operable as a symbol interleaver for mapping data symbols to be communicated on an OFDM symbol having substantially one thousand sub-carrier signals wherein the data symbols are mapped as pairs onto adjacent sub carriers forming pairs of sub-carriers. This embodiment would allow the interleaving of pairs of input symbols onto pairs of sub-carriers in a 1k mode.

Furthermore, the OFDM symbol may include pilot sub-carriers, which are arranged to carry known symbols, and the predetermined maximum valid address depends on the number of the pilot sub-carrier symbols present in the OFDM symbol. In some examples the predetermined maximum valid address may vary between three hundred and substantially five hundred and twelve, for example three hundred and seventy eight. As such the 0.5k mode interleaver can be provided for example for a DVB standard, such as DVB-T2.

Mapping data symbols to be transmitted onto the sub-carrier signals of an OFDM symbol, where the number of sub-carrier signals is approximately five hundred, represents a technical problem requiring simulation analysis and testing to establish an appropriate generator polynomial for the linear feedback shift register and the permutation order. This is because the mapping requires that the symbols are interleaved onto the sub-carrier signals with the effect that successive symbols from the input data stream are separated in frequency by a greatest possible amount in order to optimise the performance of error correction coding schemes.

Error correction coding schemes such as LDPC/BCH coding, which has been proposed for DVB-T2 perform better when noise and degradation of the symbol values resulting from communication is un-correlated. Terrestrial broadcast channels may

suffer from correlated fading in both the time and the frequency domains. As such by separating encoded symbols on to different sub-carrier signals of the OFDM symbol by as much as possible, the performance of error correction coding schemes can be increased.

As will be explained, it has been discovered from simulation performance analysis that the generator polynomial for the linear feed back shift register in combination with the permutation circuit order indicated above, provides a good performance. Furthermore, by providing an arrangement which can implement address generating for each of the 1k mode, 2k mode, the 4k mode , the 8k mode, the 16k mode and the 32k mode by changing the taps of the generator polynomial for the linear feed back shift register and the permutation order, a cost effective implementation of the 0.5k mode symbol interleaver can be provided. Furthermore, a transmitter and a receiver can be changed between the 0.5k mode, 1k mode, 2k mode, 4k mode, 8k mode, 16k mode and the 32k mode by changing the generator polynomial and the permutation orders. This can be effected in software (or by the embedded signalling) whereby a flexible implementation is provided.

The additional bit, which is used to form the address from the content of the linear feedback shift register, may be produced by a toggle circuit, which changes from 1 to 0 for each address, so as to reduce a likelihood that if an address exceeds the predetermined maximum valid address, then the next address will be a valid address. In one example the additional bit is the most significant bit.

Various aspects and features of the present invention are defined in the appended claims. Further aspects of the present invention include a data processing apparatus operable to map symbols received from a predetermined number of sub-carrier signals of an Orthogonal Frequency Division Multiplexed (OFDM) symbol into an output symbol stream, as well as a transmitter and a receiver.

Brief Description of Drawings

Embodiments of the present invention will now be described by way of example only with reference to the accompanying drawings, wherein like parts are provided with corresponding reference numerals, and in which:

Figure 1 is a schematic block diagram of a Coded OFDM transmitter which may be used, for example, with the DVB-T2 standard;

Figure 2 is a schematic block diagram of parts of the transmitter shown in Figure 1 in which a symbol mapper and a frame builder illustrate the operation of an interleaver;

Figure 3 is a schematic block diagram of the symbol interleaver shown in Figure 2;

Figure 4 is a schematic block diagram of an interleaver memory shown in Figure 3 and the corresponding symbol de-interleaver in the receiver;

Figure 5 is a schematic block diagram of an address generator shown in Figure 3 for the 0.5k mode interleaver;

Figure 6(a) is diagram illustrating results for an interleaver using the address generator shown in Figure 5 for even symbols and Figure 6(b) is a diagram illustrating design simulation results for odd symbols, whereas Figure 6(c) is a diagram illustrating comparative results for an address generator using a different permutation code for even and Figure 6(d) is a corresponding diagram for odd symbols;

Figure 7 is a schematic block diagram of a Coded OFDM receiver which may be used, for example, with the DVB-T2 standard; and

Figure 8 is a schematic block diagram of a symbol de-interleaver which appears in Figure 7.

Description of Preferred Embodiments

It has been proposed that the number of modes, which are available within the DVB-T2 standard should be extended to include a 1k mode, a 16k mode and a 32k mode. It has also been proposed to provide a 0.5k mode interleaver for interleaving pairs of input data symbols onto pairs of sub-carrier signals for a 1k mode system or for providing an interleaver for a 0.5k mode system. The following description is provided to illustrate the operation of a symbol interleaver in accordance with the present technique, although it will be appreciated that the symbol interleaver can be used with other modes and other DVB standards.

Figure 1 provides an example block diagram of a Coded OFDM transmitter which may be used for example to transmit video images and audio signals in accordance with the DVB-T2 standard. In Figure 1 a program source generates data to be transmitted by the COFDM transmitter. A video coder 2, and audio coder 4 and a data coder 6 generate video, audio and other data to be transmitted which are fed to a program multiplexer 10. The output of the program multiplexer 10 forms a multiplexed stream with other information required to communicate the video, audio and other data. The multiplexer 10 provides a stream on a connecting channel 12. There may be many such multiplexed streams which are fed into different branches A, B etc. For simplicity, only branch A will be described.

As shown in Figure 1 a COFDM transmitter 20 receives the stream at a multiplexer adaptation and energy dispersal block 22. The multiplexer adaptation and energy dispersal block 22 randomises the data and feeds the appropriate data to a forward error correction encoder 24 which performs error correction encoding of the stream. A bit interleaver 26 is provided to interleave the encoded data bits which for the example of DVB-T2 is the LDCP/BCH encoder output. The output from the bit interleaver 26 is fed to a bit to constellation mapper 28, which maps groups of bits onto a constellation point, which is to be used for conveying the encoded data bits. The outputs from the bit to constellation mapper 28 are constellation point labels that represent real and imaginary components. The constellation point labels represent data symbols formed from two or more bits depending on the modulation scheme used. These will be referred to as data cells. These data cells are passed through a time-

interleaver 30 whose effect is to interleaver data cells resulting from multiple LDPC code words.

The data cells are received by a frame builder 32, with data cells produced by branch B etc in Figure 1, via other channels 31. The frame builder 32 then forms many data cells into sequences to be conveyed on COFDM symbols, where a COFDM symbol comprises a number of data cells, each data cell being mapped onto one of the sub-carriers. The number of sub-carriers will depend on the mode of operation of the system, which may include one of 0.5k 1k, 2k, 4k, 8k, 16k or 32k, each of which provides a different number of sub-carriers according, for example to the following table:

Mode	Preferred number of sub-carriers
0.5k	378
1k	756
2k	1512
4k	3024
8k	6048
16k	12096
32k	24192

Number of Sub-carriers Adapted from DVB-T/H

In some embodiments, for example those operating CODFM schemes adapted from DVB-T/H, the preferred number of carriers per mode is shown in the "Preferred number of sub carriers" column in the table above. However it will be appreciated that the number of sub-carriers for a given mode can vary depending on the requirements of the particular DVB scheme being employed. Each mode will have a maximum number of carriers which will vary for example in accordance with the number of pilot carriers.

It will be understood that in some examples substantially five hundred may refer to three hundred and seventy eight.

Each frame comprises many such COFDM symbols. The sequence of data cells to be carried in each COFDM symbol is then passed to the symbol interleaver 33. The COFDM symbol is then generated by a COFDM symbol builder block 37 which uses the constellation data labels to generate the real and imaginary parts of the constellation points and also introducing pilot and synchronising signals fed from a pilot and embedded signal former 36. An OFDM modulator 38 then forms the OFDM symbol in the time domain which is fed to a guard insertion processor 40 for generating a guard interval between symbols, and then to a digital to analogue convertor 42 and finally to an RF amplifier within an RF front 44 for eventual broadcast by the COFDM transmitter from an antenna 46.

Providing a 0.5k Mode Interleaver

As mentioned above, the 0.5k interleaver can be used to interleave input data cells onto OFDM sub-carriers of an OFDM system operating in a 0.5k mode. Additionally, the 0.5k interleaver could be used to interleave pairs of input data cells on to pairs of adjacent OFDM sub-carriers in a 1k mode system.

To create a 0.5k mode interleaver, several elements are to be defined, one of which, of course, is the 0.5K symbol interleaver 33 itself. The bit to constellation mapper 28, symbol interleaver 33 and the frame builder 32 are shown in more detail in Figure 2.

As explained above, the present invention provides a facility for providing a quasi-optimal mapping of the data symbols onto the OFDM sub-carrier signals. According to the example technique the symbol interleaver is provided to effect the optimal mapping of input data symbols onto COFDM sub-carrier signals in accordance with a permutation code and generator polynomial, which has been verified by simulation analysis.

As shown in Figure 2 a more detailed example illustration of the bit to symbol constellation mapper 28 and the frame builder 32 is provided to illustrate an example embodiment of the present technique. Data bits received from the bit interleaver 26 via a channel 62 are grouped into sets of bits to be mapped onto a data cell, in accordance with a number of bits per symbol provided by the modulation scheme. The groups of bits, which forms a data word, are fed in parallel via data channels 64 to a

mapping processor 66. The mapping processor 66 then selects one of the data symbols, in accordance with a pre-assigned mapping. The constellation point, is represented by a real and an imaginary component but only its label is provided to the output channel 29 as one of a set of inputs to the frame builder 32.

The frame builder 32 receives the data cells from the bit to constellation mapper 28 through channel 29, together with data cells from the other channels 31. After building a frame of many COFDM cell sequences, in one embodiment in order to facilitate the 0.5k mode, the cells of each COFDM symbol are then written into an interleaver memory 100 and read out of the interleaver memory 100 in accordance with write addresses and read addresses generated by an address generator 102. Alternatively in another embodiment for interleaving pairs of input data symbols on to pairs of sub-carriers in the 1k mode, pairs of cells of the COFDM symbols are written into the interleaver memory 100 and read out of the interleaver memory 100 in accordance with write addresses and read addresses generated by an address generator 102. According to the write-in and read-out order, interleaving of the data cells is achieved, by generating appropriate addresses. The operation of the address generator 102 and the interleaver memory 100 will be described in more detail shortly with reference to Figures 3, 4 and 5. The interleaved data cells are then mapped to real and imaginary components of data symbols, which are combined with pilot and synchronisation symbols received from the pilot and embedded signalling former 36 into an OFDM symbol builder 37, to form the COFDM symbol, which is fed to the OFDM modulator 38 as explained above.

Figure 3 provides an example of parts of the symbol interleaver 33, which illustrates the present technique for interleaving symbols. In Figure 3 the input data cells from the frame builder 32 are written into the interleaver memory 100. The data cells are written into the interleaver memory 100 according to a write address fed from the address generator 102 on channel 104, and read out from the interleaver memory 100 according to a read address fed from the address generator 102 on a channel 106. The address generator 102 generates the write address and the read address as explained below, depending on whether the COFDM symbol is odd or even, which is identified from a signal fed from a channel 108, and depending on a selected mode, which is identified from a signal fed from a channel 110. As explained, the mode can

be one of a 0.5k mode, 1k mode, 2k mode, 4k mode, 8k mode, 16k mode or a 32k mode. As explained below, the write address and the read address are generated differently for odd and even symbols as explained with reference to Figure 4, which provides an example implementation of the interleaver memory 100.

In the example shown in Figure 4, the interleaver memory is shown to comprise an upper part 100 illustrating the operation of the interleaver memory in the transmitter and a lower part 340, which illustrates the operation of the de-interleaver memory in the receiver. The interleaver 100 and the de-interleaver 340 are shown together in Figure 4 in order to facilitate understanding of their operation. As shown in Figure 4 a representation of the communication between the interleaver 100 and the de-interleaver 340 via other devices and via a transmission channel has been simplified and represented as a section 140 between the interleaver 100 and the de-interleaver 340. The operation of the interleaver 100 is described in the following paragraphs:

Although Figure 4 provides an illustration of only four input data cells onto an example of four sub-carrier signals of a COFDM symbol, it will be appreciated that the technique illustrated in Figure 4 can be extended to a larger number of sub-carriers such as 378 for the 0.5k mode, 756 for the 1k mode 1512 for the 2k mode, 3024 for the 4k mode and 6048 for the 8k mode, 12096 for the 16k mode and 24192 for the 32k mode, or can be adapted to interleave pairs of data cells onto pairs of sub-carriers as discussed above.

The input and output addressing of the interleaver memory 100 shown in Figure 4 is shown for odd and even symbols. For an even COFDM symbol the data cells are taken from the input channel 77 and written into the interleaver memory 124.1 in accordance with a sequence of addresses 120 generated for each COFDM symbol by the address generator 102. The write addresses are applied for the even symbol so that as illustrated interleaving is effected by the shuffling of the write-in addresses. Therefore, for each interleaved symbol $y(h(q)) = y'(q)$.

For odd symbols the same interleaver memory 124.2 is used. However, as shown in Figure 4 for the odd symbol the write-in order 132 is in the same address sequence used to read out the previous even symbol 126. This feature allows the odd and even symbol interleaver implementations to only use one interleaver memory 100 provided the read-out operation for a given address is performed before the write-in

operation. The data cells written into the interleaver memory 124 during odd symbols are then read out in a sequence 134 generated by the address generator 102 for the next even COFDM symbol and so on. Thus only one address is generated per symbol, with the read-in and write-out for the odd/even COFDM symbol being performed contemporaneously.

In summary, as represented in Figure 4, once the set of addresses H(q) has been calculated for all active sub-carriers, the input vector $Y' = (y_0', y_1', y_2', \ldots y_{Nmax-1}')$ is processed to produce the interleaved vector $Y = (y_0, y_1, y_2, \ldots y_{Nmax-1})$ defined by:

$y_{H(q)} = y'_q$ for even symbols for $q = 0,\ldots,N_{max}-1$

$y_q = y'_{H(q)}$ for odd symbols for $q = 0,\ldots,N_{max}-1$

In other words, for even OFDM symbols the input words are written in a permutated way into a memory and read back in a sequential way, whereas for odd symbols, they are written sequentially and read back permutated. In the above case, the permutation H(q) is defined by the following table:

q	0	1	2	3
H(q)	1	3	0	2

Table 1: permutation for simple case where Nmax =4

As shown in Figure 4, the de-interleaver 340 operates to reverse the interleaving applied by the interleaver 100, by applying the same set of addresses as generated by an equivalent address generator, but applying the write-in and read-out addresses in reverse. As such, for even symbols, the write-in addresses 342 are in sequential order, whereas the read out address 344 are provided by the address generator. Correspondingly, for the odd symbols, the write-in order 346 is determined from the set of addresses generated by the address generator, whereas read out 348 is in sequential order.

Address Generation for the 0.5k Mode Interleaver

A schematic block diagram of the algorithm used to generate the permutation function H(q) is represented in Figure 5 for the 0.5K mode interleaver.

An implementation of the address generator 102 for the 0.5k mode interleaver is shown in Figure 5. In Figure 5 a linear feed back shift register is formed by eight

register stages 200 and a xor-gate 202 which is connected to the stages of the shift register 200 in accordance with a generator polynomial. Therefore, in accordance with the content of the shift register 200 a next bit of the shift register is provided from the output of the xor-gate 202 by xoring the content of shift registers R[0], R[1], R[5], R[6] according to the generator polynomial:

$$R'_i[7] = R'_{i-1}[0] \oplus R'_{i-1}[1] \oplus R'_{i-1}[5] \oplus R'_{i-1}[6]$$

According to the generator polynomial a pseudo random bit sequence is generated from the content of the shift register 200. However, in order to generate an address for the 0.5k mode interleaver as illustrated, a permutation circuit 210 is provided which effectively permutes the order of the bits within the shift register 200.1 from an order $R'_i[n]$ to an order $R_i[n]$ at the output of the permutation circuit 210. Eight bits from the output of the permutation circuit 210 are then fed on a connecting channel 212 to which is added a most significant bit via a channel 214 which is provided by a toggle circuit 218. A nine bit address is therefore generated on channel 212. However, in order to ensure the authenticity of an address, an address check circuit 216 analyses the generated address to determine whether it exceeds a predetermined maximum value. The predetermined maximum value may correspond to the maximum number of sub-carrier signals or pairs of sub-carrier signals, which are available for data symbols within the COFDM symbol, available for the mode which is being used. However, the 0.5k interleaver may also be used for other modes, so that the address generator 102 may also be used for the 1k mode, 2k mode, 4k mode, 8k mode, 16k mode and the 32k mode, by adjusting accordingly the number of the maximum valid address. However it will be understood that in order to support higher modes, the number of register stages shown in Figure 5 may have to be increased.

If the generated address exceeds the predetermined maximum value then a control signal is generated by the address check unit 216 and fed via a connecting channel 220 to a control unit 224. If the generated address exceeds the predetermined maximum value then this address is rejected and a new address regenerated for the particular symbol.

For the 0.5k mode interleaver, an (N_r - 1) bit word R'_i is defined, with $N_r = \log_2 M_{max}$, where $M_{max} = 512$ using a LFSR (Linear Feedback Shift Register).

The polynomials used to generate this sequence is:

0.5k mode: $R'_i[7] = R'_{i-1}[0] \oplus R'_{i-1}[1] \oplus R'_{i-1}[5] \oplus R'_{i-1}[6]$

where i varies from 0 to $M_{max} - 1$

Once one R'_i, word has been generated, the R'_i, word goes through a permutation to produce another (N_r - 1) bit word called R_i. R_i is derived from R'_i by the bit permutations given as follows:

R'_i bit positions	7	6	5	4	3	2	1	0
R_i bit positions	3	7	4	6	1	2	0	5

Bit permutation for the 0.5K mode interleaver

As an example, this means that for the mode 0.5k, the bit number 7 of R'_i is sent in bit position number 3 of R_i.

The address H(q) is then derived from R_i through the following equation:

$$H(q) = (i \bmod 2) \cdot 2^{N_r-1} + \sum_{j=0}^{N_r-2} R_i(j) \cdot 2^j$$

The $(i \bmod 2) \cdot 2^{N_r-1}$ part of the above equation is represented in Figure 5 by the toggle block T 218.

An address check is then performed on H(q) to verify that the generated address is within the range of acceptable addresses: if ($H(q) < N_{max}$), where N_{max} = 378 for example in a preferred example of the 0.5k mode, then the address is valid. If the address is not valid, the control unit is informed and it will try to generate a new H(q) by incrementing the index i.

The role of the toggle block is to make sure that we do not generate an address exceeding N_{max} twice in a row. In effect, if an exceeding value was generated, this means that the MSB (i.e. the toggle bit) of the address H(q) was one. So the next value generated will have a MSB set to zero, insuring to produce a valid address.

The following equations sum up the overall behaviour and help to understand the loop structure of this algorithm:

q = 0;

for (i = 0; i < M_{max}; i = i + 1)

$$\{ H(q) = (i \bmod 2) \cdot 2^{N_r - 1} + \sum_{j=0}^{N_r - 2} R_i(j) \cdot 2^j ;$$

if (H(q)<N_{max}) q = q+1; }

Analysis Supporting the Address Generator for the 0.5k Mode Interleaver

The selection of the polynomial generator and the permutation code explained above for the address generator 102 for the 0.5k mode interleaver has been identified following simulation analysis of the relative performance of the interleaver. The relative performance of the interleaver has been evaluated using a relative ability of the interleaver to separate successive symbols or an "interleaving quality". As mentioned above, effectively the interleaver must perform for both odd and even symbols, in order to use a single interleaver memory. The relative measure of the interleaver quality is determined by defining a distance D (in number of sub-carriers).. A criterion C is chosen to identify a number of sub-carriers that are at distance ≤ D at the output of the interleaver that were at distance ≤ D at the input of the interleaver, the number of sub-carriers for each distance D then being weighted with respect to the relative distance. The criterion C is evaluated for both odd and even COFDM symbols. Minimising C produces a superior quality interleaver.

$$C = \sum_{1}^{d=D} N_{even}(d) / d + \sum_{1}^{d=D} N_{odd}(d) / d$$

where

Neven(d) = number of carriers from an even symbol separated by d at input and separated by less than 5 carriers at output.

Nodd(d) = number of carriers from an odd symbol separated by d at input and separated by less than 5 carriers apart at output.

Analysis of the 0.5k interleaver identified above for the 0.5k mode for a value of D = 5 is shown in Figure 6(a) for the even COFDM symbols and in Figure 6(b) for the odd COFDM symbol. According to the above analysis, the value of C for the permutation code identified above for the 0.5k mode produced a value of C = 25.6833,

that the weighted number of sub-carriers with symbols which are separated by five or less in the output according to the above equation was 25.6833.

A corresponding analysis is provided for an alternative permutation code for even COFDM symbols in Figure 6(c) for odd COFDM symbols in Figure 6(d). As can be seen in comparison to the results illustrated in Figures 6(a) and 6(b), there are more components present which represent symbols separated by small distances such as D = 1, and D = 2, when compared with the results shown in Figure 6(a) and 6(b), illustrating that the permutation code identified above for the 0.5k mode symbol interleaver produces a superior quality interleaver.

Alternative Permutation Codes

The following seven alternative possible codes ($[n]R_j$ bit positions, where n = 1 to 7) have been found to provide a symbol interleaver with a good quality as determined by the criterion C identified above.

R'_j bit positions	7	6	5	4	3	2	1	0
$[1]R_j$ bit positions	3	7	4	5	1	2	0	6
$[2]R_j$ bit positions	3	5	4	7	1	2	0	6
$[3]R_j$ bit positions	6	7	2	5	1	4	0	3
$[4]R_j$ bit positions	3	2	5	6	1	7	0	4
$[5]R_j$ bit positions	4	2	5	7	3	0	1	6
$[6]R_j$ bit positions	4	3	7	1	6	0	2	5
$[7]R_j$ bit positions	3	7	6	4	1	2	0	5

Bit permutation for the 0.5k mode interleaver

Receiver

Figure 7 provides an example illustration of a receiver which may be used with the present technique. As shown in Figure 7, a COFDM signal is received by an antenna 300 and detected by a tuner 302 and converted into a digital form by an analogue-to-digital converter 304. A guard interval removal processor 306 removes the guard interval from a received COFDM symbol, before the data is recovered from

the COFDM symbol using a Fast Fourier Transform (FFT) processor 308 in combination with a channel estimator and correction 310 in co-operation with a embedded-signalling decoding unit 311, in accordance with known techniques. The demodulated data is recovered from a mapper 312 and fed to a symbol de-interleaver 314, which operates to effect the reverse mapping of the received data symbol to re-generate an output data stream with the data de-interleaved.

The symbol de-interleaver 314 is formed from a data processing apparatus as shown in Figure 7 with an interleaver memory 340 and an address generator 342. The interleaver memory is as shown in Figure 4 and operates as already explained above to effect de-interleaving by utilising sets of addresses generated by the address generator 342. The address generator 342 is formed as shown in Figure 8 and is arranged to generate corresponding addresses to map the data symbols recovered from each COFDM sub-carrier signals into an output data stream.

The remaining parts of the COFDM receiver shown in Figure 7 are provided to effect error correction decoding 318 to correct errors and recover an estimate of the source data.

One advantage provided by the present technique for both the receiver and the transmitter is that a symbol interleaver and a symbol de-interleaver operating in the receivers and transmitters can be switched between the 0.5k, 1k, 2k, 4k, 8k, 16k and the 32k mode by changing the generator polynomials and the permutation order. Hence the address generator 342 shown in Figure 8 includes an input 344, providing an indication of the mode as well as an input 346 indicating whether there are odd/even COFDM symbols. A flexible implementation is thereby provided because a symbol interleaver and de-interleaver can be formed as shown in Figures 3 and 8, with an address generator as illustrated in Figures 5. However, it will be understood that to support an interleaver for a higher order mode, the linear feedback register 200 would require more than eight register stages. For example in order to support a 4k mode, ten register stages would be required to provide for 2048 sub-carrier addresses The address generator can be adapted to the different modes by changing to the generator polynomials and the permutation orders indicated for each of the modes. For example, this can be effected using a software change. Alternatively, in other embodiments, an embedded signal indicating the mode of the DVB-T2 transmission can be detected in

the receiver in the embedded-signalling processing unit 311 and used to configure automatically the symbol de-interleaver in accordance with the detected mode.

Various modifications may be made to the embodiments described above without departing from the scope of the present invention. In particular, the example representation of the generator polynomial and the permutation order which have been used to represent aspects of the invention are not intended to be limiting and extend to equivalent forms of the generator polynomial and the permutation order.

As will be appreciated the transmitter and receiver shown in Figures 1 and 7 respectively are provided as illustrations only and are not intended to be limiting. For example, it will be appreciated that the position of the symbol interleaver and the de-interleaver with respect, for example to the bit interleaver and the mapper can be changed. As will be appreciated the effect of the interleaver and de-interleaver is un-changed by its relative position, although the interleaver may be interleaving I/Q symbols instead of v-bit vectors. A corresponding change may be made in the receiver. Accordingly the interleaver and de-interleaver may be operating on different data types, and may be positioned differently to the position described in the example embodiments.

As explained above the permutation codes and generator polynomial of the interleaver, which has been described with reference to an implementation of a particular mode, can equally be applied to other modes, by changing the predetermined maximum allowed address in accordance with the number of sub-carriers for that mode.

As mentioned above, embodiments of the present invention find application with DVB standards such as DVB-T and DVB-H, which are incorporated herein by reference. For example embodiments of the present invention may be used in a transmitter or receiver operating in accordance with the DVB-H standard, in hand-held mobile terminals. The mobile terminals may be integrated with mobile telephones (whether second, third or higher generation) or Personal Digital Assistants or Tablet PCs for example. Such mobile terminals may be capable of receiving DVB-H or DVB-T compatible signals inside buildings or on the move in for example cars or trains, even at high speeds. The mobile terminals may be, for example, powered by batteries, mains electricity or low voltage DC supply or powered from a car battery. Services

that may be provided by DVB-H may include voice, messaging, internet browsing, radio, still and/or moving video images, television services, interactive services, video or near-video on demand and option. The services might operate in combination with one another. It will be appreciated that the present invention is not limited to application with DVB and may be extended to other standards for transmission or reception, both fixed and mobile.

CLAIMS

1. A data processing apparatus operable to map input symbols to be communicated onto a predetermined number of sub-carrier signals of an Orthogonal Frequency Division Multiplexed (OFDM) symbol, the data processing apparatus comprising

an interleaver operable to read-into a memory the predetermined number of data symbols for mapping onto the OFDM sub-carrier signals, and to read-out of the memory the data symbols for the OFDM sub-carriers to effect the mapping, the read-out being in a different order than the read-in, the order being determined from a set of addresses, with the effect that the data symbols are interleaved on the sub-carrier signals,

an address generator operable to generate the set of addresses, an address being generated for each of the input symbols to indicate one of the sub-carrier signals onto which the data symbol is to be mapped, the address generator comprising

a linear feedback shift register including a predetermined number of register stages and being operable to generate a pseudo-random bit sequence in accordance with a generator polynomial,

a permutation circuit operable to receive the content of the shift register stages and to permute the bits present in the register stages in accordance with a permutation order to form an address of one of the OFDM sub-carriers, and

a control unit operable in combination with an address check circuit to re-generate an address when a generated address exceeds a predetermined maximum valid address, characterised in that

the predetermined maximum valid address is approximately five hundred,

the linear feedback shift register has eight register stages with a generator polynomial for the linear feedback shift register of

$$R'_i[7] = R'_{i-1}[0] \oplus R'_{i-1}[1] \oplus R'_{i-1}[5] \oplus R'_{i-1}[6]$$

and the permutation order forms, with an additional bit, a nine bit address $R_i[n]$ for the i-th data symbol from the bit present in the n-th register stage $R'_i[n]$ in accordance with the table:

R'_i bit positions	7	6	5	4	3	2	1	0
R_i bit positions	3	7	4	6	1	2	0	5

2. A data processing apparatus as claimed in Claim 1, wherein the interleaver is operable to perform the mapping such that pairs of adjacent data symbols are mapped onto adjacent sub-carrier signals to the effect that data symbols are interleaved pair by pair onto the sub-carrier signals.

3. A data processing apparatus as claimed in Claim 1, wherein the predetermined maximum valid address is a value substantially between three hundred and five hundred and twelve.

4. A data processing apparatus as claimed in Claim 1, 2 or 3, wherein the OFDM symbol includes pilot sub-carriers, which are arranged to carry known symbols, and the predetermined maximum valid address depends on a number of the pilot sub-carrier symbols present in the OFDM symbol.

5. A data processing apparatus as claimed in any preceding Claim, wherein the predetermined maximum valid address is a value equal to three hundred and seventy eight.

6. A data processing apparatus as claimed in Claim 1, wherein the interleaver memory is operable to effect the mapping of the input data symbols onto the sub-carrier signals for even OFDM symbols by reading in the data symbols according to the set of addresses generated by the address generator and reading out in a sequential order, and for odd OFDM symbols by reading in the symbols into the memory in a sequential order and reading out the data symbols from the memory in accordance with the set of addresses generated by the address generator.

7. A transmitter for transmitting data using Orthogonal Frequency Division Multiplexing (OFDM), the transmitter including a data processing apparatus according to any preceding Claim.

8. A transmitter as claimed in Claim 7, wherein the transmitter is operable to transmit data in accordance with a Digital Video Broadcasting standard such as the Digital Video Broadcasting-Terrestrial, Digital Video Broadcasting-Handheld standard or the Digital Video Broadcasting-Terrestrial2 standard.

9. A data processing apparatus operable to map symbols received from a predetermined number of sub-carrier signals of an Orthogonal Frequency Division Multiplexed (OFDM) symbol into an output symbol stream, the data processing apparatus comprising

a de-interleaver operable to read-into a memory the predetermined number of data symbols from the OFDM sub-carrier signals, and to read-out of the memory the data symbols into the output symbol stream to effect the mapping, the read-out being in a different order than the read-in, the order being determined from a set of addresses, with the effect that the data symbols are de-interleaved from the OFDM sub-carrier signals,

an address generator operable to generate the set of addresses, an address being generated for each of the received data symbols to indicate the OFDM sub-carrier signal from which the received data symbol is to be mapped into the output symbol stream, the address generator comprising

a linear feedback shift register including a predetermined number of register stages and being operable to generate a pseudo-random bit sequence in accordance with a generator polynomial,

a permutation circuit operable to receive the content of the shift register stages and to permute the bits present in the register stages in accordance with a permutation order to form an address of one of the OFDM sub-carriers, and

a control unit operable in combination with an address check circuit to re-generate an address when a generated address exceeds a predetermined maximum valid address, characterised in that

the predetermined maximum valid address is approximately five hundred,

the linear feedback shift register has eight register stages with a generator polynomial for the linear feedback shift register of $R'_i[7] = R'_{i-1}[0] \oplus R'_{i-1}[1] \oplus R'_{i-1}[5] \oplus R'_{i-1}[6]$, and the permutation order forms, with an additional bit, a nine bit address $R_i[n]$ for the i-th data symbol from the bit present in the n-th register stage $R'_i[n]$ in accordance with the table:

R'_i bit positions	7	6	5	4	3	2	1	0
R_i bit positions	3	7	4	6	1	2	0	5

10. A data processing apparatus as claimed in Claim 9, wherein the de-interleaver is operable to perform the mapping such that pairs of adjacent data symbols are mapped onto adjacent sub-carrier signals to the effect that data symbols are interleaved pair by pair onto the sub-carrier signals.

11. A data processing apparatus as claimed in Claim 9 or 10, wherein the predetermined maximum valid address is a value substantially between three hundred and five hundred and twelve.

12. A data processing apparatus as claimed in Claim 9 or 10 or 11, wherein the OFDM symbol includes pilot sub-carriers, which are arranged to carry known symbols, and the predetermined maximum valid address depends on a number of the pilot sub-carrier symbols present in the OFDM symbol.

13. A data processing apparatus as claimed in any of Claims 9, 10, 11 or 12, wherein the predetermined maximum valid address is a value equal to three hundred and seventy eight.

14. A data processing apparatus as claimed in any of Claims 9 to 13, wherein the de-interleaver memory is arranged to effect the mapping of the received data symbols from the sub-carrier signals onto the output data stream for even OFDM symbols by reading in the data symbols according to a sequential order and reading out

the data symbols from memory according to the set of addresses generated by the address generator, and for odd OFDM symbols by reading in the symbols into the memory in accordance with the set of addresses generated by the address generator and reading out the data symbols from the memory in accordance with a sequential order.

15. A receiver for receiving data from Orthogonal Frequency Division Multiplexing (OFDM) modulated signal, the receiver including a data processing apparatus according to any of Claims 9 to 14.

16. A receiver as claimed in Claim 15, wherein the receiver is operable to receive data which has been modulated in accordance with a Digital Video Broadcasting standard such as the Digital Video Broadcasting-Terrestrial, Digital Video Broadcasting-Handheld or the Digital Video Broadcasting-Terrestrial2 standard.

17. A method of mapping input symbols to be communicated onto a predetermined number of sub-carrier signals of an Orthogonal Frequency Division Multiplexed (OFDM) symbol, the method comprising

reading-into a memory the predetermined number of data symbols for mapping onto the OFDM sub-carrier signals,

reading-out of the memory the data symbols for the OFDM sub-carriers to effect the mapping, the read-out being in a different order than the read-in, the order being determined from a set of addresses, with the effect that the data symbols are interleaved on the sub-carrier signals,

generating the set of addresses, an address being generated for each of the input symbols to indicate one of the sub-carrier signals onto which the data symbol is to be mapped, the generating the set of addresses comprising

using a linear feedback shift register including a predetermined number of register stages to generate a pseudo-random bit sequence in accordance with a generator polynomial,

using a permutation circuit operable to receive the content of the shift register stages to permute the bits present in the register stages in accordance with a permutation order to form an address, and

re-generating an address when a generated address exceeds a predetermined maximum valid address, characterised in that

the predetermined maximum valid address is approximately five hundred,

the linear feedback shift register has eight register stages with a generator polynomial for the linear feedback shift register of $R'_i[7] = R'_{i-1}[0] \oplus R'_{i-1}[1] \oplus R'_{i-1}[5] \oplus R'_{i-1}[6]$, and the permutation order forms, with an additional bit, a nine bit address $R_i[n]$ for the i-th data symbol from the bit present in the n-th register stage $R'_i[n]$ in accordance with the table:

R'_i bit positions	7	6	5	4	3	2	1	0
R_i bit positions	3	7	4	6	1	2	0	5

18. A method as claimed in Claim 17, wherein the mapping is such that pairs of adjacent data symbols are mapped onto adjacent sub-carrier signals to the effect that data symbols are interleaved pair by pair onto the sub-carrier signals.

19. A method as claimed in Claim 17 or 18, wherein the predetermined maximum valid address is a value substantially between three hundred and five hundred and twelve.

20. A method as claimed in Claim 17, 18 or 19 wherein the OFDM symbol includes pilot sub-carriers, which are arranged to carry known symbols, and the predetermined maximum valid address depends on a number of the pilot sub-carrier symbols present in the OFDM symbol.

21. A method as claimed in any of Claims 17, 18, 19 or 20, wherein the predetermined maximum valid address is a value equal to three hundred and seventy eight.

22. A method of mapping symbols received from a predetermined number of sub-carrier signals of an Orthogonal Frequency Division Multiplexed (OFDM) symbol into an output symbol stream, the method comprising

reading-into a memory the predetermined number of data symbols from the OFDM sub-carrier signals,

reading-out of the memory the data symbols into the output symbol stream to effect the mapping, the read-out being in a different order than the read-in, the order being determined from a set of addresses, with the effect that the data symbols are de-interleaved from the OFDM sub-carrier signals,

generating the set of addresses, an address being generated for each of the received symbols to indicate the OFDM sub-carrier signal from which the received data symbol is to be mapped into the output symbol stream, the generating the set of addresses comprising

using a linear feedback shift register including a predetermined number of register stages to generate a pseudo-random bit sequence in accordance with a generator polynomial,

using a permutation circuit to receive the content of the shift register stages and to permute the bits present in the register stages in accordance with a permutation order to form an address, and

re-generating an address when a generated address exceeds a predetermined maximum valid address, characterised in that

the predetermined maximum valid address is approximately five hundred,

the linear feedback shift register has eight register stages with a generator polynomial for the linear feedback shift register of $R'_i[7] = R'_{i-1}[0] \oplus R'_{i-1}[1] \oplus R'_{i-1}[5] \oplus R'_{i-1}[6]$, and the permutation order forms, with an additional bit, a nine bit address $R_i[n]$ for the i-th data symbol from the bit present in the n-th register stage $R'_i[n]$ in accordance with the table:

R'_i bit positions	7	6	5	4	3	2	1	0
R_i bit positions	3	7	4	6	1	2	0	5

23. A method as claimed in Claim 22, wherein the mapping is such that pairs of data input symbols are mapped onto adjacent sub-carrier signals to the effect that data symbols are interleaved pair by pair onto the sub-carrier signals.

24. A method as claimed in Claim 22 or 23, wherein the predetermined maximum valid address is a value substantially between three hundred and five hundred and twelve.

25. A method as claimed in Claim 22, 23 or 24, wherein the OFDM symbol includes pilot sub-carriers, which are arranged to carry known symbols, and the predetermined maximum valid address depends on a number of the pilot sub-carrier symbols present in the OFDM symbol.

26. A method as claimed in any of Claims 22, 23, 24 or 25, wherein the predetermined maximum valid address is a value equal to three hundred and seventy eight.

27. An address generator for use with transmission or reception of data symbols interleaved onto sub-carriers of an Orthogonal Frequency Division Multiplexed symbol, the address generator being operable to generate a set of addresses, each address being generated for each of the data symbols to indicate one of the sub-carrier signals onto which the data symbol is to be mapped, the address generator comprising

a linear feedback shift register including a predetermined number of register stages and being operable to generate a pseudo-random bit sequence in accordance with a generator polynomial,

a permutation circuit operable to receive the content of the shift register stages and to permute the bits present in the register stages in accordance with a permutation order to form an address, and

a control unit operable in combination with an address check circuit to re-generate an address when a generated address exceeds a predetermined maximum valid address, characterised in that

the predetermined maximum valid address is approximately five hundred,

the linear feedback shift register has eight register stages with a generator polynomial for the linear feedback shift register of $R'_i[7] = R'_{i-1}[0] \oplus R'_{i-1}[1] \oplus R'_{i-1}[5] \oplus R'_{i-1}[6]$, and the permutation order forms, with an additional bit, a nine bit address $R_i[n]$ for the i-th data symbol from the bit present in the n-th register stage $R'_i[n]$ in accordance with the table:

R'_i bit positions	7	6	5	4	3	2	1	0
R_i bit positions	3	7	4	6	1	2	0	5

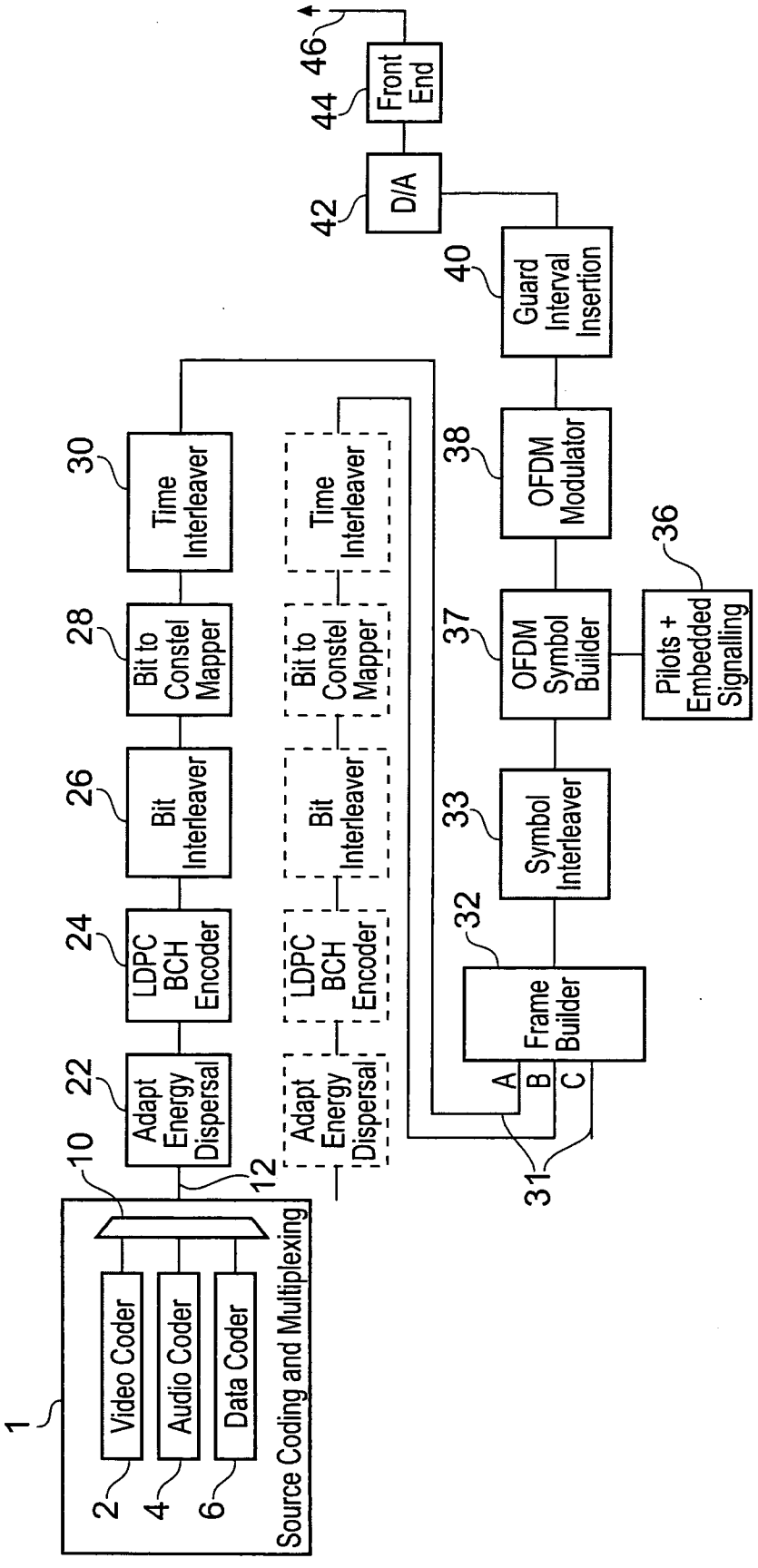
1
Source Coding and Multiplexing
Video Coder
Audio Coder
Data Coder
2
4
6
10
12
22
Adapt Energy Dispersal
24
LDPC BCH Encoder
26
Bit Interleaver
28
Bit to Constel Mapper
30
Time Interleaver
Adapt Energy Dispersal
LDPC BCH Encoder
Bit Interleaver
Bit to Constel Mapper
Time Interleaver
31
A
B
C
32
Frame Builder
33
Symbol Interleaver
37
OFDM Symbol Builder
36
Pilots + Embedded Signalling
38
OFDM Modulator
40
Guard Interval Insertion
42
D/A
44
Front End
46

FIG. 1

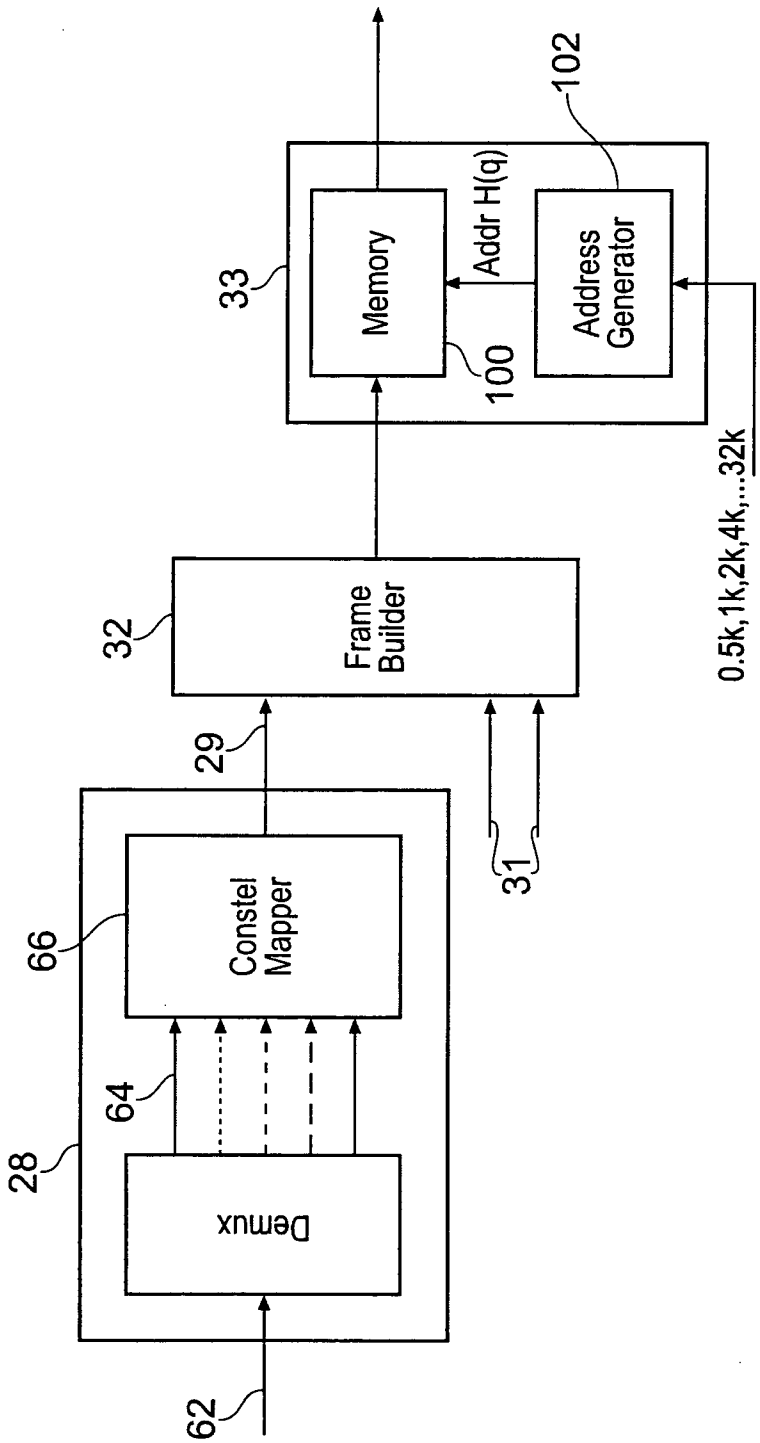
102
Addr H(q)
Memory
Address Generator
33
100
0.5k,1k,2k,4k,...32k
32
Frame Builder
29
31
66
Constel Mapper
64
28
Demux
62

FIG. 2

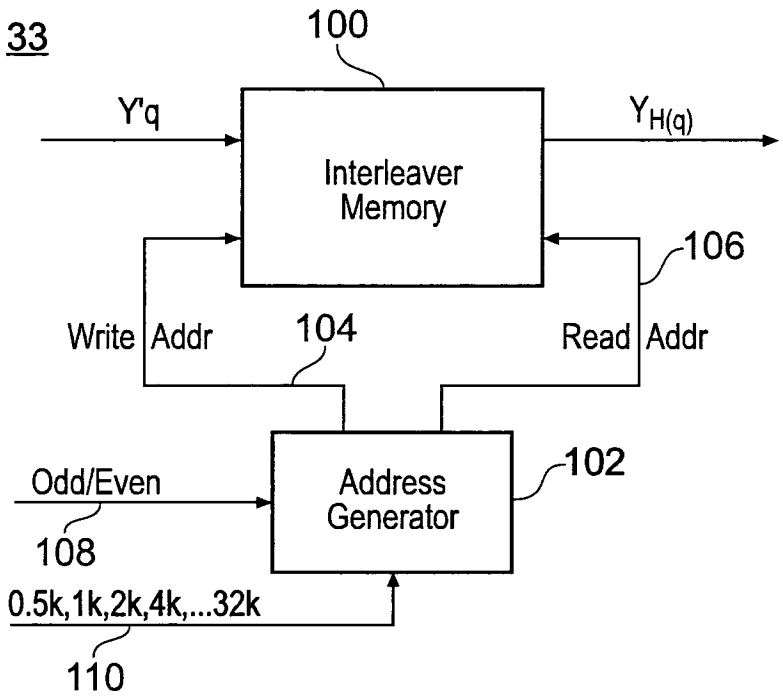
33
100
Y'q
$Y_{H(q)}$
Interleaver Memory
106
Write Addr
104
Read Addr
Odd/Even
Address Generator
102
108
0.5k,1k,2k,4k,...32k
110

FIG. 3

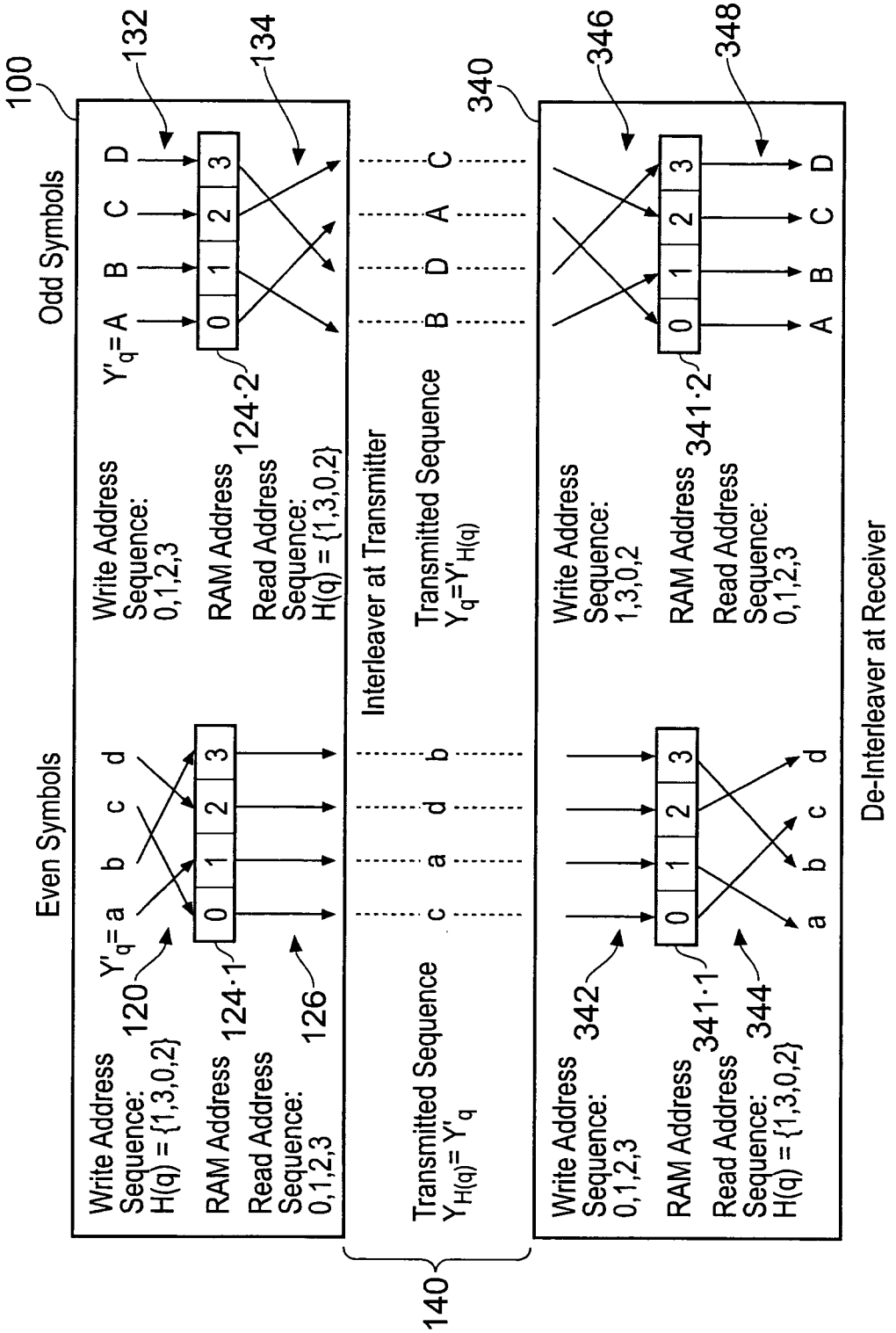
100
Odd Symbols
132
134
Write Address Sequence: 0,1,2,3
RAM Address
Read Address Sequence: H(q) = {1,3,0,2}
124·2
Y'q= A B C D
0 1 2 3
Even Symbols
Write Address Sequence: H(q) = {1,3,0,2}
120
Y'q= a b c d
RAM Address
Read Address Sequence: 0,1,2,3
124·1
126
Interleaver at Transmitter
Transmitted Sequence YH(q)= Y'q
c a d b
Transmitted Sequence Yq=Y'H(q)
B D A C
340
346
348
Write Address Sequence: 1,3,0,2
RAM Address
Read Address Sequence: 0,1,2,3
341·2
A B C D
Write Address Sequence: 0,1,2,3
342
RAM Address
Read Address Sequence: H(q) = {1,3,0,2}
341·1
344
a b c d
De-Interleaver at Receiver
140

FIG. 4

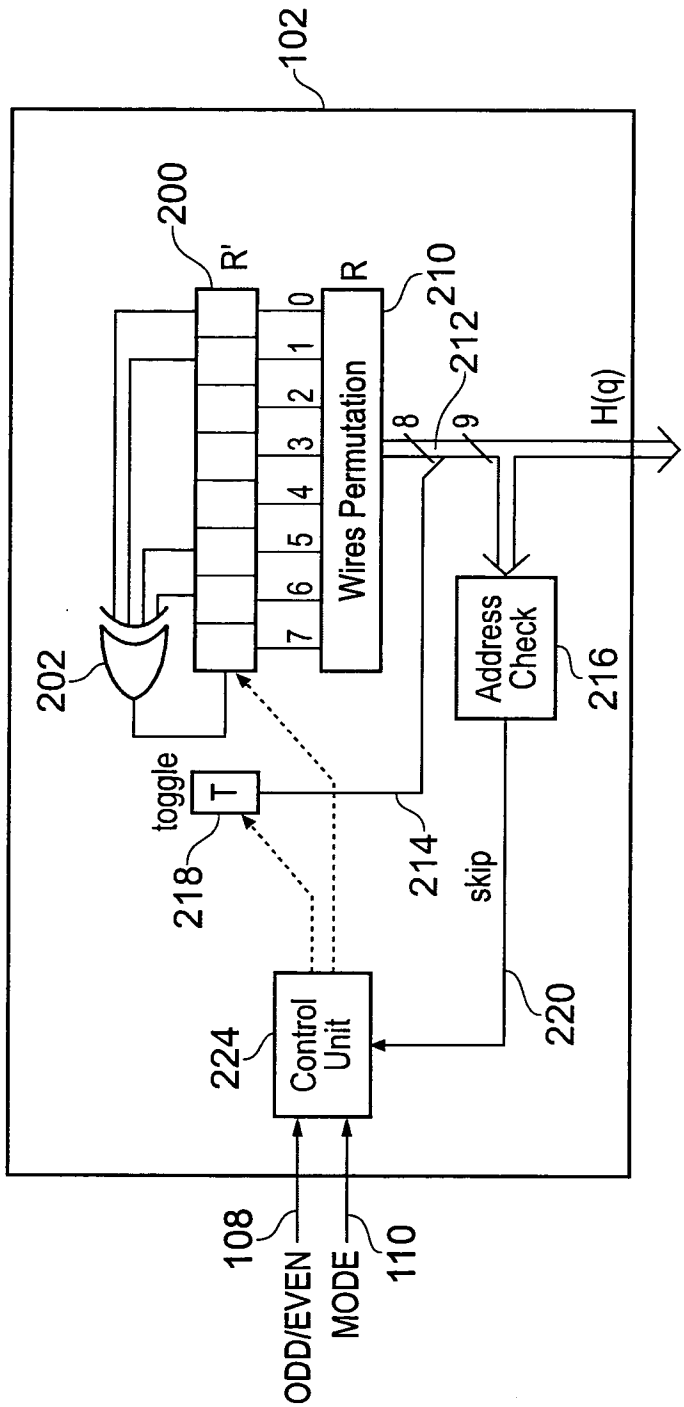
102
200
R'
R
210
212
0
1
2
3
4
5
6
7
8
9
Wires Permutation
H(q)
202
Address Check
216
toggle
T
218
214
skip
220
224
Control Unit
108
110
ODD/EVEN
MODE

FIG. 5

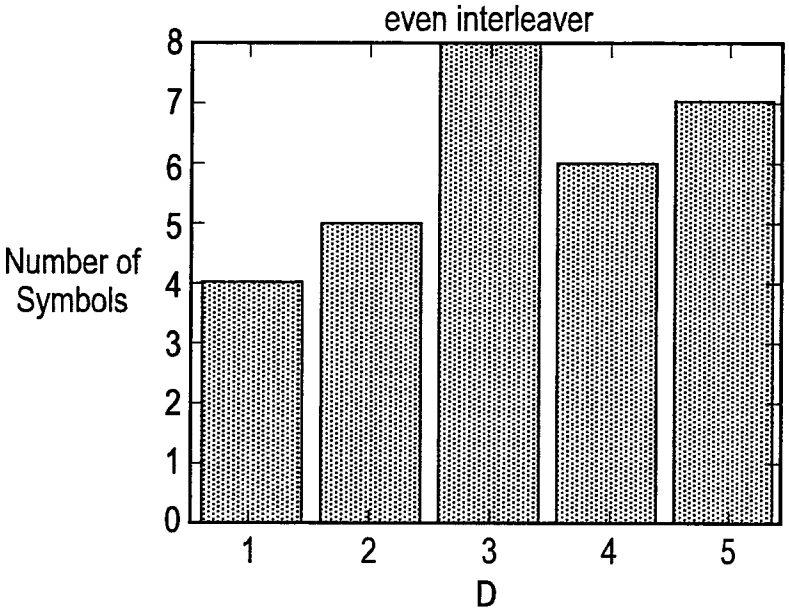
even interleaver
Number of Symbols
0
1
2
3
4
5
6
7
8
1
2
3
4
5
D

FIG. 6(a)

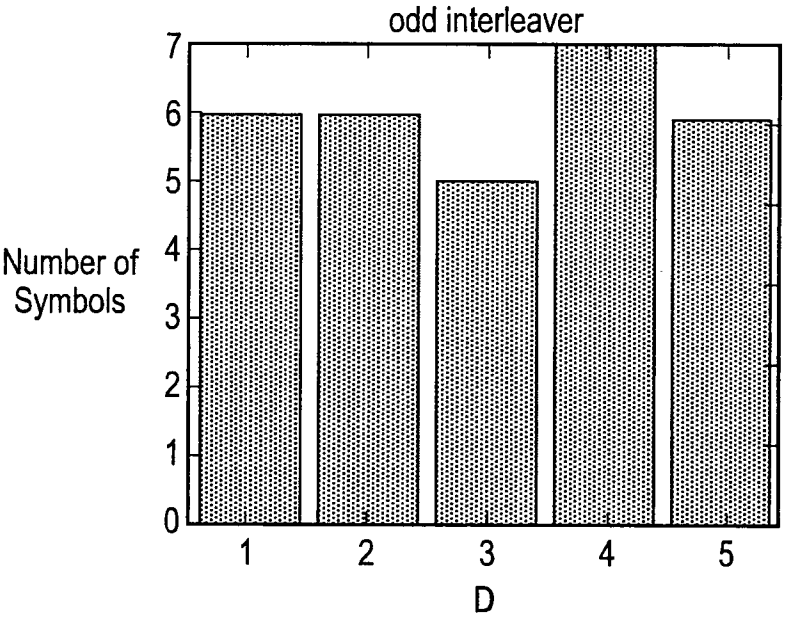
odd interleaver
Number of Symbols
0
1
2
3
4
5
6
7
1
2
3
4
5
D

FIG. 6(b)

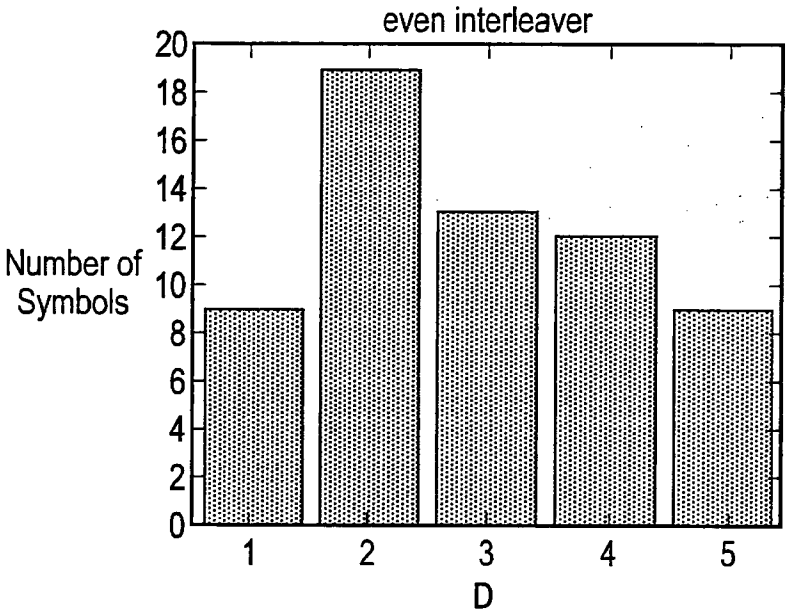
even interleaver
Number of Symbols
20
18
16
14
12
10
8
6
4
2
0
1
2
3
4
5
D

FIG. 6(c)

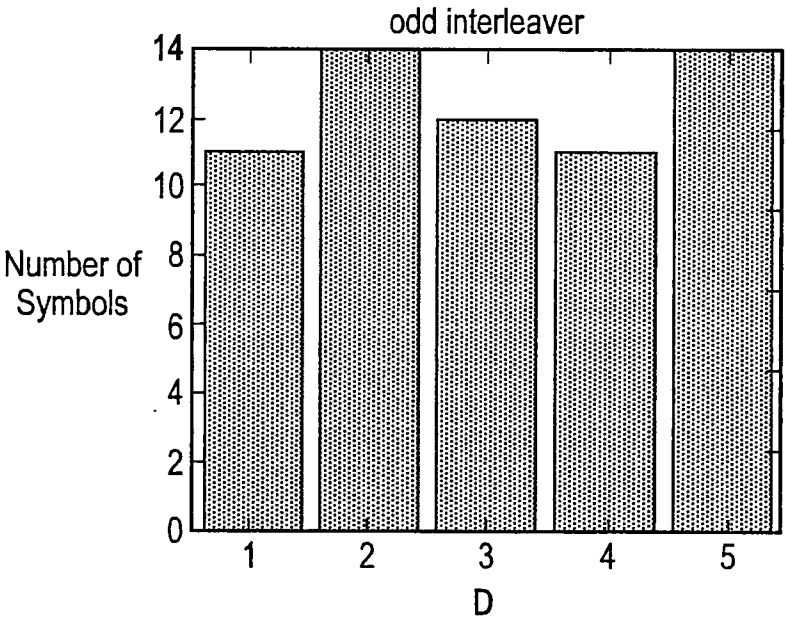
odd interleaver
Number of Symbols
14
12
10
8
6
4
2
0
1
2
3
4
5
D

FIG. 6(d)

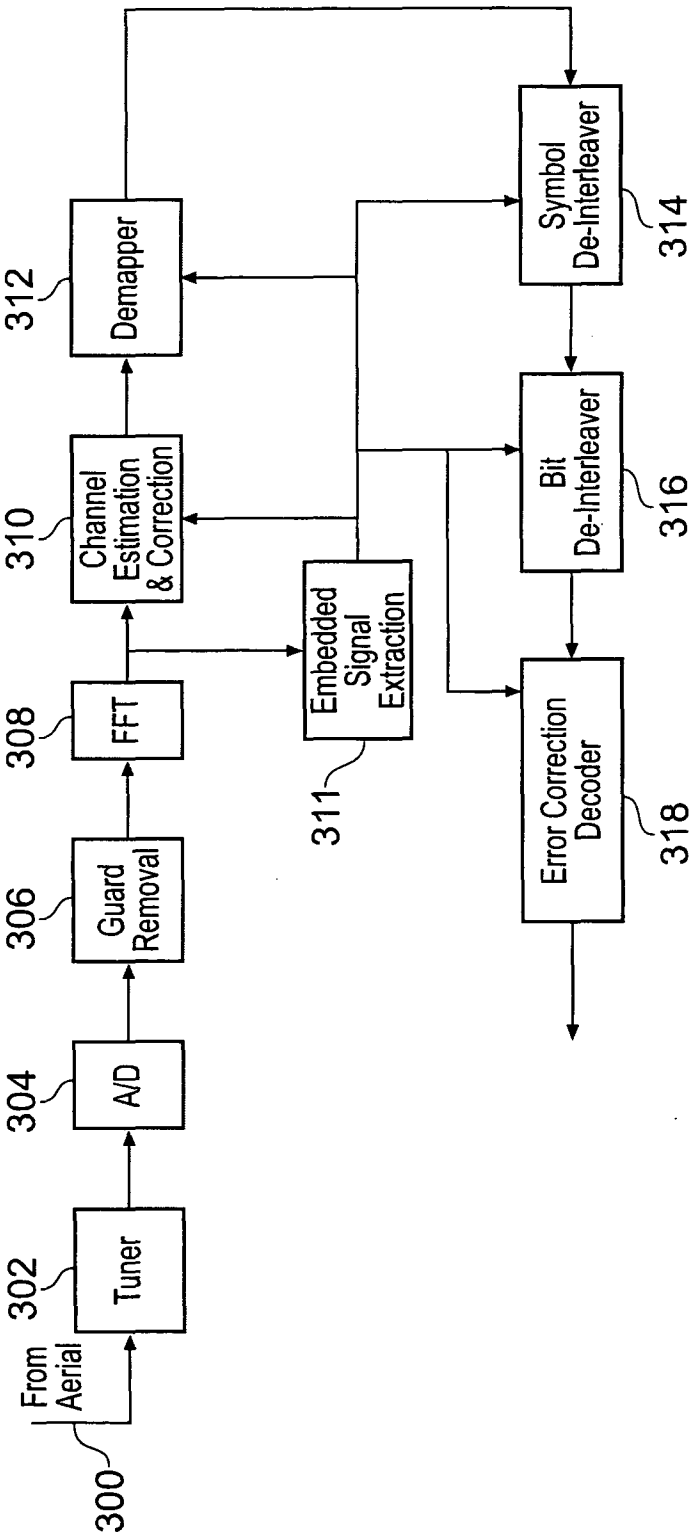
From Aerial
300
Tuner
302
A/D
304
Guard Removal
306
FFT
308
Channel Estimation & Correction
310
Demapper
312
Embedded Signal Extraction
311
Symbol De-Interleaver
314
Bit De-Interleaver
316
Error Correction Decoder
318

FIG. 7

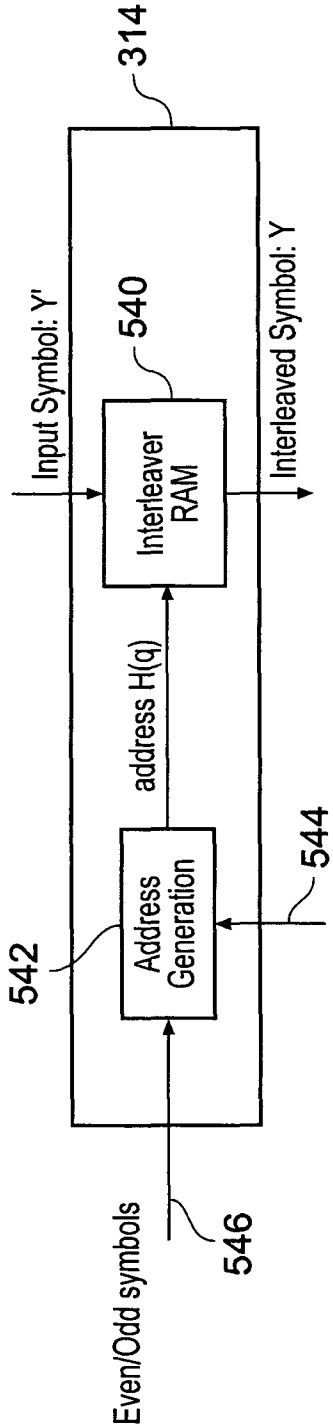
314
Input Symbol: Y'
540
Interleaver RAM
Interleaved Symbol: Y
address H(q)
542
Address Generation
544
Mode
Even/Odd symbols
546

FIG. 8

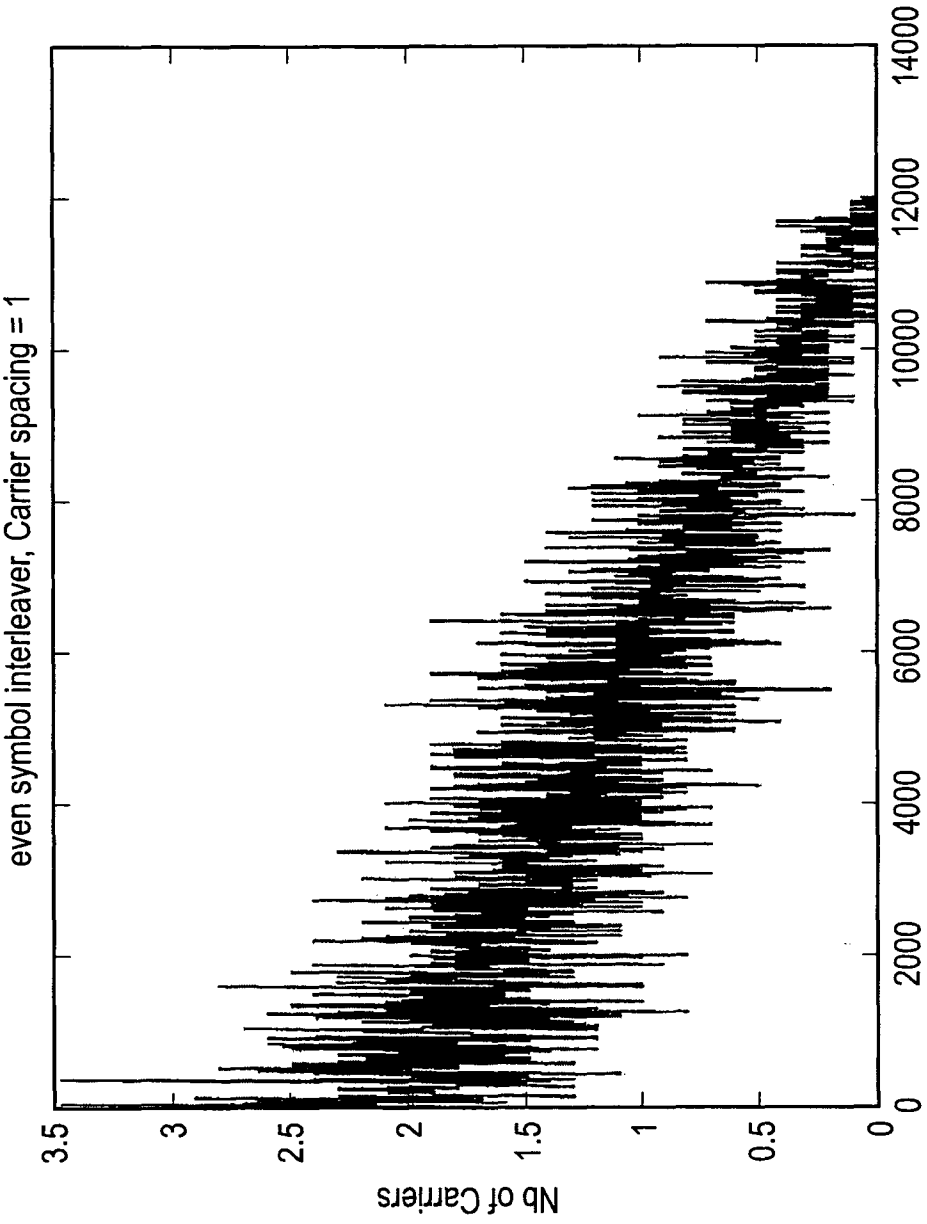
even symbol interleaver, Carrier spacing = 1
Nb of Carriers
Interleaved Carriers Distance
0
0.5
1
1.5
2
2.5
3
3.5
0
2000
4000
6000
8000
10000
12000
14000

FIG. 9(a)

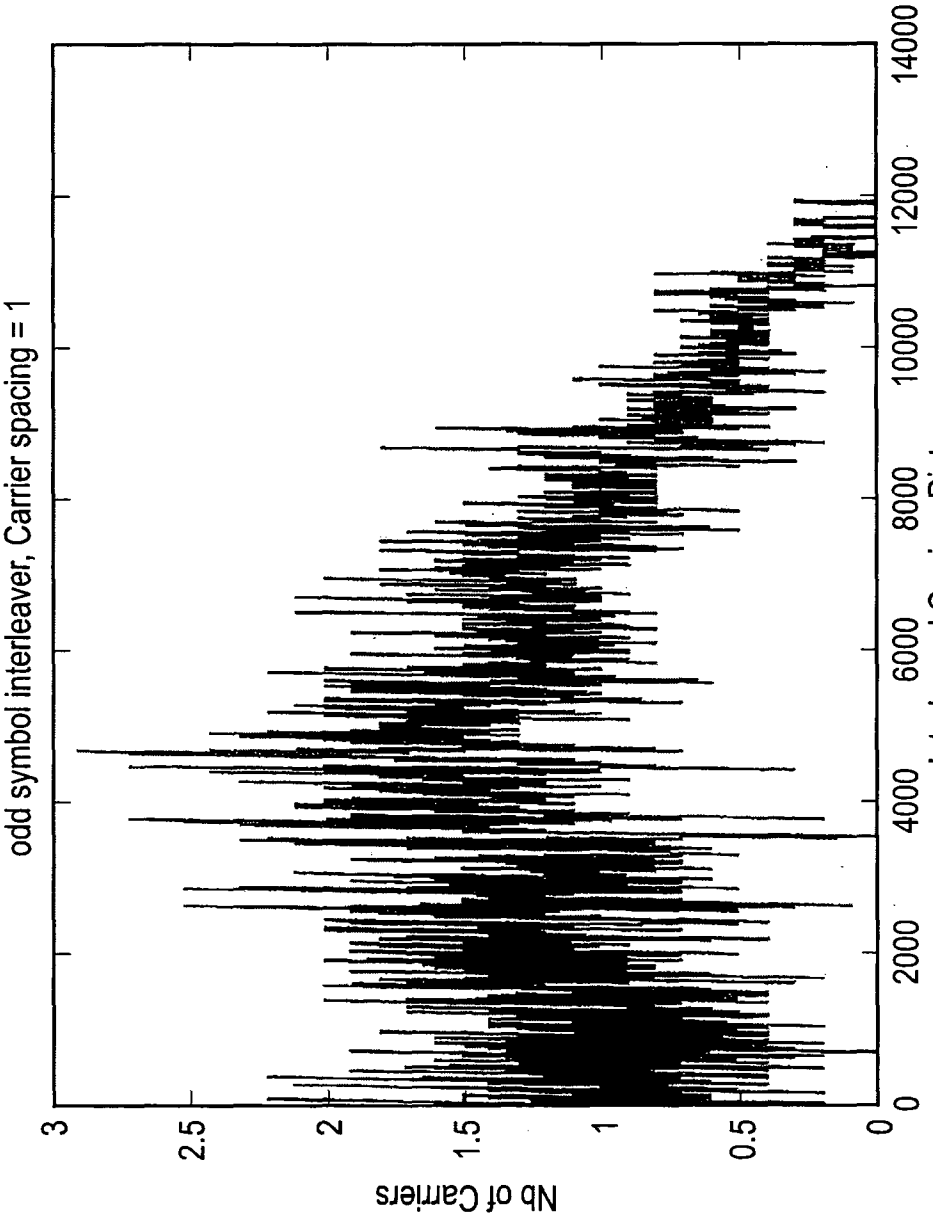
odd symbol interleaver, Carrier spacing = 1
Nb of Carriers
Interleaved Carriers Distance
0
0.5
1
1.5
2
2.5
3
0
2000
4000
6000
8000
10000
12000
14000

FIG. 9(b)

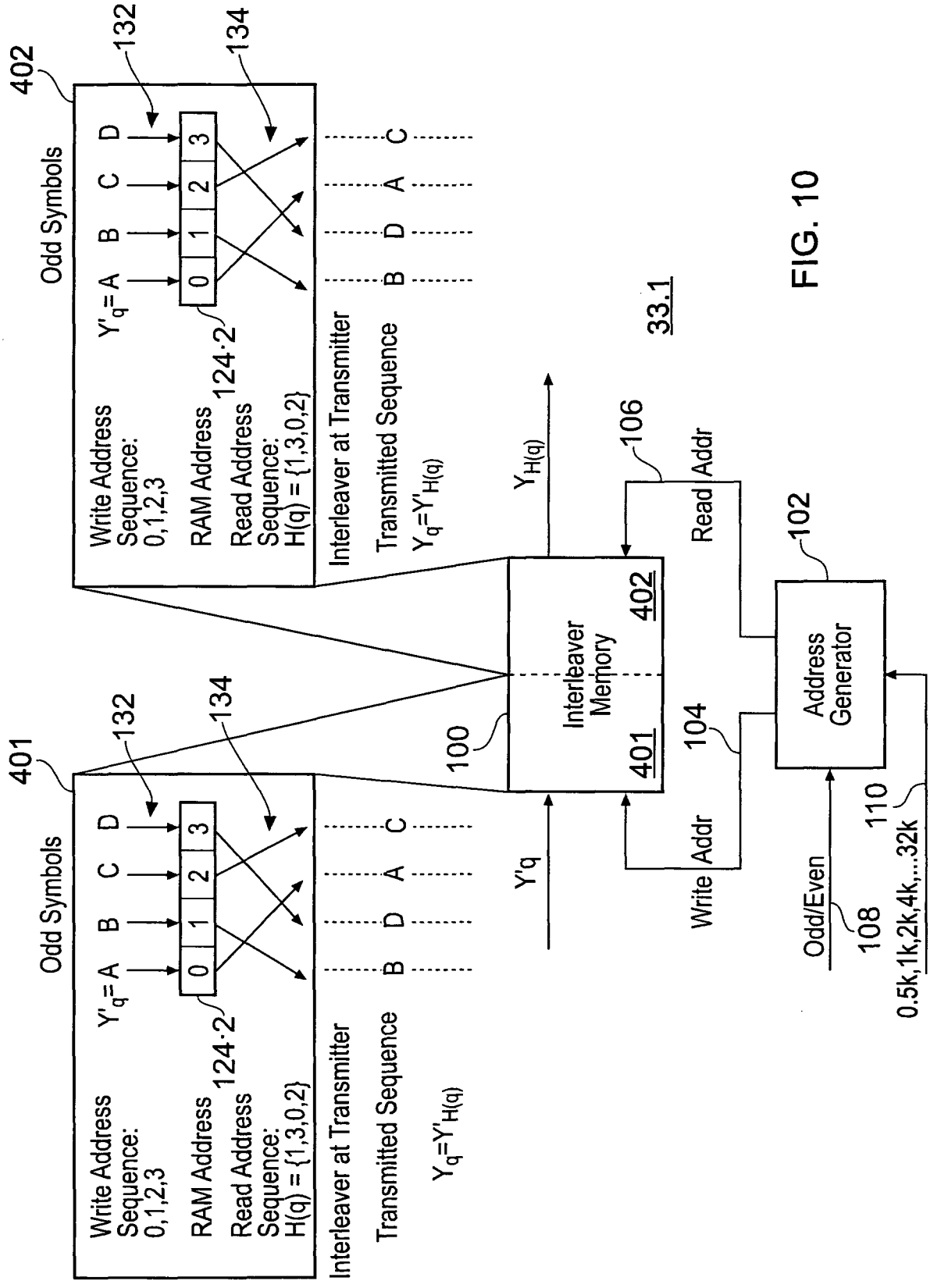
401
Odd Symbols
132
134
Write Address Sequence: 0,1,2,3
RAM Address
Read Address Sequence: H(q) = {1,3,0,2}
124·2
Interleaver at Transmitter
Transmitted Sequence
$Y_q=Y'_{H(q)}$
Y'_q=A B C D
0 1 2 3
B D A C
402
Odd Symbols
132
134
Write Address Sequence: 0,1,2,3
RAM Address
Read Address Sequence: H(q) = {1,3,0,2}
124·2
Interleaver at Transmitter
Transmitted Sequence
$Y_q=Y'_{H(q)}$
Y'_q=A B C D
0 1 2 3
B D A C
100
Interleaver Memory
401
402
33.1
Y'_q
$Y_{H(q)}$
104
Write Addr
106
Read Addr
102
Address Generator
108
Odd/Even
110
0.5k,1k,2k,4k,...32k

FIG. 10

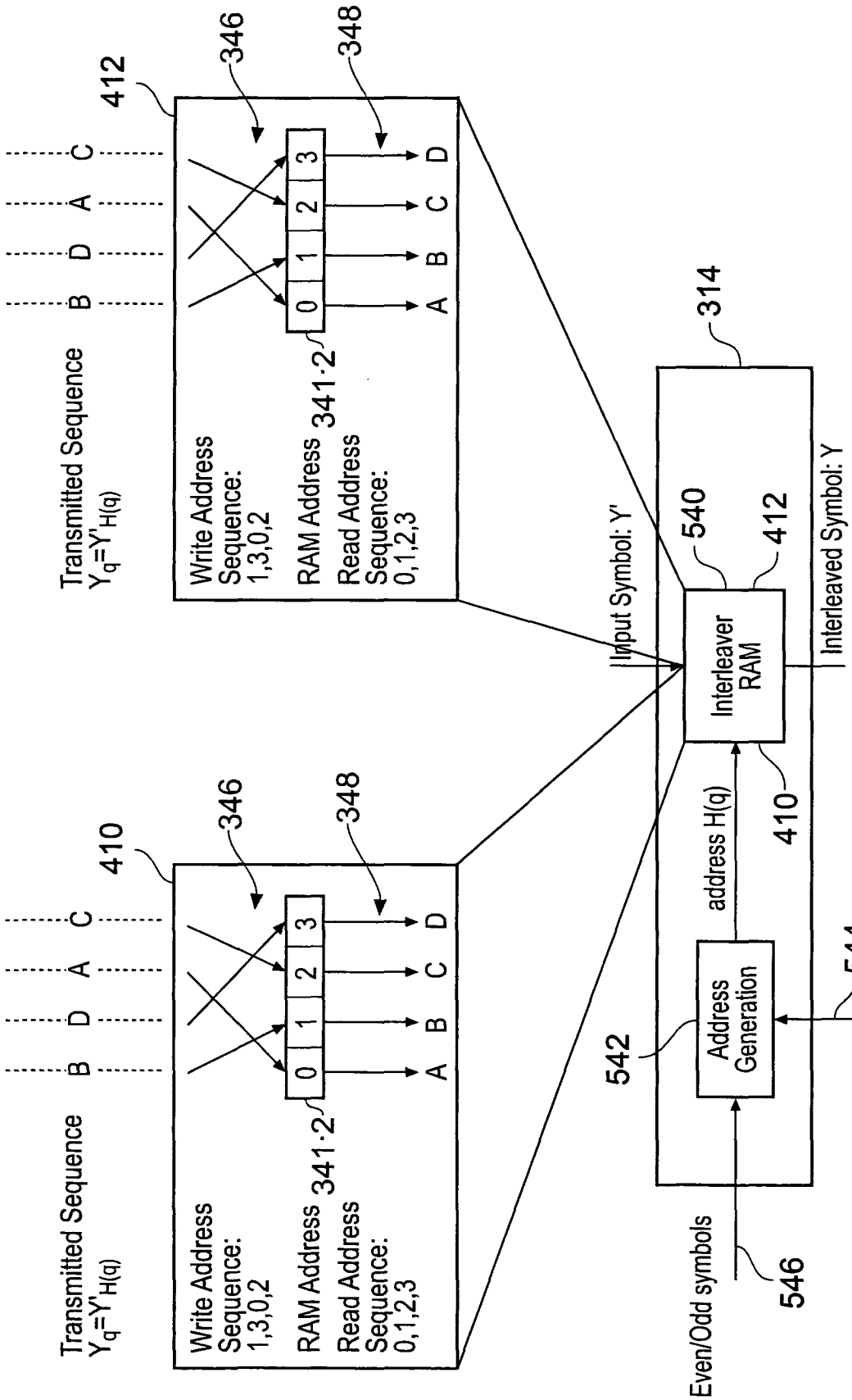
412
346
348
C
A
D
B
Transmitted Sequence
$Y_q=Y'_{H(q)}$
Write Address Sequence: 1,3,0,2
RAM Address
341-2
Read Address Sequence: 0,1,2,3
0 1 2 3
A B C D
410
346
348
C
A
D
B
Transmitted Sequence
$Y_q=Y'_{H(q)}$
Write Address Sequence: 1,3,0,2
RAM Address
341-2
Read Address Sequence: 0,1,2,3
0 1 2 3
A B C D
314
Input Symbol: Y'
540
412
Interleaver RAM
Interleaved Symbol: Y
address H(q)
410
542
Address Generation
544
Mode
Even/Odd symbols
546

FIG. 11

INTERNATIONAL SEARCH REPORT

International application No
PCT/GB2008/003606

A. CLASSIFICATION OF SUBJECT MATTER
INV. H04L1/00 H04L27/26 H03M13/27

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04L H03M H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, INSPEC, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 1 463 255 A (SONY UK LTD [GB]) 29 September 2004 (2004-09-29) claims 1,11-13 figures 1-9 paragraphs [0003] - [0012], [0015] - [0022], [0028], [0029], [0031] - [0036], [0043] - [0048]	1-27
A	EP 1 463 256 A (SONY UK LTD [GB]) 29 September 2004 (2004-09-29) claims 1,6,11-13 paragraphs [0003] - [0013], [0015] - [0022], [0029], [0031] - [0048]	1-27

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
7 January 2009	14/01/2009

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	González Gutiérrez

INTERNATIONAL SEARCH REPORT

International application No
PCT/GB2008/003606

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	"Digital Video Broadcasting (DVB)" ETS 300 744, XX, XX, 1 March 1997 (1997-03-01), pages 25-34, XP002195640 pages 26,27 pages 29,30 pages 33,34	1-27
A	US 6 353 900 B1 (SINDHUSHAYANA NAGABHUSHANA T [US] ET AL) 5 March 2002 (2002-03-05) the whole document	1-27

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/GB2008/003606

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 1463255 A	29-09-2004	AT 326105 T	15-06-2006
		AT 409383 T	15-10-2008
		AT 394003 T	15-05-2008
		DE 602004000824 T2	30-11-2006
		DK 1463256 T3	31-07-2006
		ES 2260728 T3	01-11-2006
		KR 20040084811 A	06-10-2004
		PT 1463256 T	29-09-2006
		US 2008298487 A1	04-12-2008
		US 2004246888 A1	09-12-2004
EP 1463256 A	29-09-2004	EP 1662739 A1	31-05-2006
		EP 1662740 A1	31-05-2006
		ES 2304757 T3	16-10-2008
US 6353900 B1	05-03-2002	US 6304985 B1	16-10-2001