PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 7 : H03M 1/12, H03K 3/315 — A2

(11) International Publication Number: **WO 00/41308**

(43) International Publication Date: 13 July 2000 (13.07.00)

(21) International Application Number: PCT/US00/00175

(22) International Filing Date: 5 January 2000 (05.01.00)

(30) Priority Data:
60/115,195 6 January 1999 (06.01.99) US

(71) Applicant: RAYTHEON COMPANY [US/US]; 141 Spring Street, Lexington, MA 02421 (US).

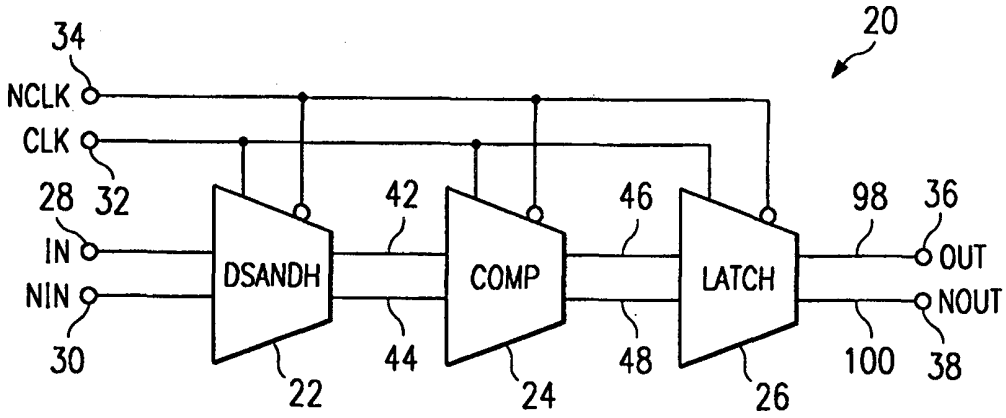
(72) Inventor: BROEKAERT, Tom, P., E.; 3925 North Ceanothus Place #F, Calabasas, CA 91302 (US).

(74) Agent: MEIER, Harold, E.; Baker Botts L.L.P., 2001 Ross Avenue, Dallas, TX 75201-2980 (US).

(81) Designated States: AE, AL, AM, AT, AT (Utility model), AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, CZ (Utility model), DE, DE (Utility model), DK, DK (Utility model), DM, EE, EE (Utility model), ES, FI, FI (Utility model), GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SK (Utility model), SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published
Without international search report and to be republished upon receipt of that report.

(54) Title: SYSTEM FOR QUANTIZING AN ANALOG SIGNAL UTILIZING A RESONANT TUNNELING DIODE DIFFERENTIAL TERNARY QUANTIZER



(57) Abstract

A system for quantizing an analog signal comprises an input terminal for receiving an analog input signal, an inverted input terminal for receiving an inverted input signal, a clock terminal for receiving a clock signal, and an inverted clock terminal for receiving an inverted clock signal. A sample-and-hold circuit is coupled to the input terminal, the inverted input terminal, the clock terminal, and the inverted clock terminal. A comparator circuit is coupled to the sample-and-hold circuit, the clock terminal, and the inverted clock terminal. A latch circuit is coupled to the comparator circuit, the clock terminal, and the inverted clock terminal. An output terminal having a quantized output signal is coupled to the latch circuit. An inverted ouput terminal having an inverted output signal is coupled to the latch circuit.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania	**ES**	Spain	**LS**	Lesotho	**SI**	Slovenia
AM	Armenia	**FI**	Finland	**LT**	Lithuania	**SK**	Slovakia
AT	Austria	**FR**	France	**LU**	Luxembourg	**SN**	Senegal
AU	Australia	**GA**	Gabon	**LV**	Latvia	**SZ**	Swaziland
AZ	Azerbaijan	**GB**	United Kingdom	**MC**	Monaco	**TD**	Chad
BA	Bosnia and Herzegovina	**GE**	Georgia	**MD**	Republic of Moldova	**TG**	Togo
BB	Barbados	**GH**	Ghana	**MG**	Madagascar	**TJ**	Tajikistan
BE	Belgium	**GN**	Guinea	**MK**	The former Yugoslav Republic of Macedonia	**TM**	Turkmenistan
BF	Burkina Faso	**GR**	Greece			**TR**	Turkey
BG	Bulgaria	**HU**	Hungary	**ML**	Mali	**TT**	Trinidad and Tobago
BJ	Benin	**IE**	Ireland	**MN**	Mongolia	**UA**	Ukraine
BR	Brazil	**IL**	Israel	**MR**	Mauritania	**UG**	Uganda
BY	Belarus	**IS**	Iceland	**MW**	Malawi	**US**	United States of America
CA	Canada	**IT**	Italy	**MX**	Mexico	**UZ**	Uzbekistan
CF	Central African Republic	**JP**	Japan	**NE**	Niger	**VN**	Viet Nam
CG	Congo	**KE**	Kenya	**NL**	Netherlands	**YU**	Yugoslavia
CH	Switzerland	**KG**	Kyrgyzstan	**NO**	Norway	**ZW**	Zimbabwe
CI	Côte d'Ivoire	**KP**	Democratic People's Republic of Korea	**NZ**	New Zealand		
CM	Cameroon			**PL**	Poland		
CN	China	**KR**	Republic of Korea	**PT**	Portugal		
CU	Cuba	**KZ**	Kazakstan	**RO**	Romania		
CZ	Czech Republic	**LC**	Saint Lucia	**RU**	Russian Federation		
DE	Germany	**LI**	Liechtenstein	**SD**	Sudan		
DK	Denmark	**LK**	Sri Lanka	**SE**	Sweden		
EE	Estonia	**LR**	Liberia	**SG**	Singapore		

SYSTEM FOR QUANTIZING AN ANALOG SIGNAL UTILIZING A RESONANT TUNNELING DIODE DIFFERENTIAL TERNARY QUANTIZER

TECHNICAL FIELD OF THE INVENTION

This invention relates generally to electronic quantizing and more particularly to a system for quantizing an analog signal utilizing a resonant tunneling diode differential ternary quantizer.

BACKGROUND OF THE INVENTION

Analog-to-digital converters have been formed in a variety of architectures. Conventionally, these architectures have been implemented with transistors. For example, one common implementation includes a cross-coupled pair of transistors. However, there are several disadvantages associated with using transistors to implement an analog-to-digital converter.

First, electronic components used in digital circuits are becoming smaller. As these devices decrease in size, quantum mechanical effects begin to appear. The electrical properties of conventional transistors may be unacceptably altered by quantum mechanical effects. Secondly, a transistor-implemented analog-to-digital converter is limited by the switching speed of the transistors, which may be too slow for some applications. Finally, conventional transistors are limited to two stable states. Thus, systems using transistors typically only convert

analog signals into binary digital signals, making the use of multi-valued logic difficult.

SUMMARY OF THE INVENTION

In accordance with the present invention, a system for quantizing an analog signal utilizing a resonant tunneling diode differential ternary quantizer is provided that substantially eliminates or reduces the disadvantages or problems associated with previously developed quantizers. In particular, the present invention provides a system for quantizing an analog signal with a resonant tunneling diode differential ternary quantizer that minimizes the limitations of transistor-only implementations.

In one embodiment of the present invention, a system for quantizing an analog signal is provided that comprises an input terminal for receiving an analog input signal, an inverted input terminal for receiving an inverted input signal, a clock terminal for receiving a clock signal, and an inverted clock terminal for receiving an inverted clock signal. A sample-and-hold circuit is coupled to the input terminal, the inverted input terminal, the clock terminal, and the inverted clock terminal. A comparator is coupled to the sample-and-hold circuit, the clock terminal, and the inverted clock terminal. A latch is coupled to the comparator, the clock terminal, and the inverted clock terminal. An output terminal for providing a quantized output signal is coupled to the latch. An inverted output terminal for providing an inverted output signal is also coupled to the latch.

Technical advantages of the present invention include providing an improved system for quantizing an analog signal. In particular, a negative-resistance device such as a resonant tunneling diode is used to implement the analog-to-digital converter. Accordingly, reliance on

transistors is avoided. As a result, quantum mechanical effects are not detrimental to system operation, switching speed is increased, and use of multi-valued logic is possible.

Other technical advantages of the present invention will be readily apparent to one skilled in the art from the following figures, descriptions, and claims.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention and its advantages, reference is now made to the following description taken in conjunction with the accompanying drawings, wherein like reference numerals represent like parts, in which:

FIGURE 1 is a schematic diagram of a resonant tunneling diode (RTD) for use as a negative-resistance element in accordance with the teachings of the present invention;

FIGURE 2 is a graph of current as a function of voltage for a negative-resistance element illustrated in FIGURE 1;

FIGURE 3 is a circuit diagram illustrating a system for quantizing an analog signal in accordance with one embodiment of the present invention;

FIGURE 4 is a circuit diagram illustrating the comparator of FIGURE 3 and

FIGURE 5 is a circuit diagram illustrating the latch of FIGURE 3.

DETAILED DESCRIPTION OF THE INVENTION

The present invention and its advantages are best understood by referring now in more detail to FIGURES 1 through 5 of the drawings.

FIGURE 1 is a schematic diagram of a resonant tunneling diode (RTD) 10 for use as a negative-resistance element in accordance with the teachings of the present invention. RTD 10 comprises an input terminal 11 for receiving an input signal, an output terminal 12 for producing an output signal, two tunnel barrier layers 13, and a quantum well layer 14.

FIGURE 2 is a graph showing current as a function of voltage for a negative-resistance element such as an RTD 10. The shape of this I-V curve is determined by the quantum effects that are a result of the extreme thinness of tunnel barrier layers 13 and quantum well layer 14. These layers 13 and 14 are approximately ten (10) to twenty (20) atoms thick.

When a voltage of low amplitude is applied to input terminal 11, almost no electrons tunnel through both tunnel barrier layers 13. This results in a negligible current and the RTD 10 is switched off. As the voltage increases, the energy of the electrons received at input terminal 11 also increases and the wavelength of these electrons decreases. When a particular voltage level is reached at input terminal 11, a specific number of electron wavelengths will fit within quantum well layer 14. At this point, resonance is established as electrons that tunnel through one tunnel barrier layer 13 remain in quantum well layer 14, giving those electrons opportunities to tunnel through the second tunnel barrier layer 13 to output terminal 12. Thus, a current flow is established from input terminal 11 to output terminal 12 and RTD 10 is switched on. However, if the voltage level continues to

rise, eventually no electrons will have the proper wavelength to tunnel through tunnel barrier layers 13 and RTD 10 is switched off. This property of negative-resistance elements such as RTDs 10 that allows switching back and forth between on and off states as the voltage increases enables biasing to operate in one of three stable states, as illustrated in FIGURE 2. These three stable states are the negative-bias valley region 16, the pre-peak region 17, and the positive-bias valley region 18.

Another property associated with the extreme thinness of tunnel barrier layers 13 and quantum well layer 14 of RTD 10 relates to switching speed. Because each of these layers 13 and 14 are only about ten (10) to twenty (20) atoms thick, an electron only travels about .01 microns from input terminal 11 to output terminal 12. Because of this short distance, RTD 10 switches on and off at a very high rate.

FIGURE 3 is a circuit diagram illustrating a system 20 for quantizing an analog signal in accordance with one embodiment of the present invention. System 20 comprises a sample-and-hold circuit 22, a comparator 24, and a latch 26. Also comprising the system 20 is an input terminal 28 for receiving an analog input signal, an inverted input terminal 30 for receiving an inverted input signal, a clock terminal 32 for receiving a clock signal, an inverted clock terminal 34 for receiving an inverted clock signal, an output terminal 36 for the quantized output signal, and an inverted output terminal 38 for an inverted output signal. The sample-and-hold circuit 22 is coupled to input terminal 28, inverted input terminal 30, clock terminal 32, and inverted clock terminal 34. The comparator 24 is connected to the sample-and-hold circuit 22 by lines 42 and 44 and is coupled to the clock terminal 32 and the inverted clock terminal 34. The latch 26 is connected to the comparator

24 by lines 46 and 48 and is coupled to clock terminal 32 and inverted clock terminal 34. The output terminal 36 and inverted output terminal 38 are coupled to the latch 26.

According to one embodiment of the present invention, the input signal received at input terminal 28 comprises a varying current, while the output signal at output terminal 36 comprises a varying voltage. In addition, the input signal may comprise a signal in the X-band range (10 or more gigahertz).

FIGURE 4 is a circuit diagram illustrating the comparator 24. Comparator 24 comprises a comparator input terminal 50 and an inverted comparator input terminal 52 for receiving the output signals from the sample-and-hold circuit 22. Also comprising the comparator 24 is a comparator output terminal 54 and an inverted comparator output terminal 56 for transmission of the output signals to the latch 26. Comparator 24 also comprises a first current source 58, a second current source 60, a third current source 62, and a fourth current source 64.

The comparator 24 further comprises a first negative-resistance device 66 and a second negative-resistance device 68. Coupled to the first negative-resistance device 66 are four switches 70, and coupled to the second negative-resistance device 68 are four switches 72. Comparator 24 also includes connecting lines 74 and 76 that transmit signals to an amplifier 78 having outputs connected to comparator output terminal 54 and inverted comparator output terminal 56.

According to the present invention, the first negative-resistance device 66 and the second negative-resistance device 68 each comprise an RTD. One method of resetting an RTD is to disconnect the diode from the circuit, allowing the RTD to discharge. In comparator 24, the first negative-resistance device 66 is disconnected

from the circuit by opening switches 70. The second negative-resistance device 68 is disconnected from the circuit by opening switches 72.

According to the present invention, switches 70 are closed during one clock cycle while switches 72 are open, allowing the second negative-resistance device 68 to discharge. During this clock cycle, the first negative-resistance device 66 is coupled to lines 74 and 76 and thereby applies a signal to amplifier 78. During the next clock cycle, the first negative-resistance device 66 is disconnected from the circuit by opening switches 70, allowing the first negative-resistance device to discharge. At the same time, the second negative-resistance device 68 is coupled to lines 74 and 76 when switches 72 are closed, allowing the second negative-resistance device to provide a signal to the amplifier 78.

In the comparator 24, the negative-resistance devices 66 and 68 operate in the pre-peak region 17 when the input voltage is zero. This produces an output signal of zero. However, when the input voltage reaches a specified value, the negative-resistance devices 66 and 68 are forced during alternating clock cycles into either the negative-bias valley region 16, thereby producing an output signal of -1, or the positive-bias valley region 18, to produce an output signal of +1.

FIGURE 5 is a circuit diagram illustrating the latch 26. The latch 26 comprises a two-to-one multiplexer 90, a latch amplifier 92, a negative-resistance device 94, and a feedback amplifier 96. According to one embodiment, the negative-resistance device 94 comprises an RTD. Latch 26 further comprises a latch input terminal connected to line 46, an inverted latch input terminal connected to line 48, latch output terminal connected to line 98, and inverted latch output terminal connected to line 100. Latch

amplifier 92 is connected to the two-to-one multiplexer 90 by connecting lines 102 and 104. Negative-resistance device 94 is connected to the output of the latch amplifier 92 at terminals 106 and 108. Also coupled to the negative-resistance device 94 at the terminals 106 and 108 is the feedback amplifier 96. The two-to-one multiplexer 90 is coupled to the input terminal by connecting line 46 and the inverted input terminal by connecting line 48. The two-to-one multiplexer 90 is also coupled to the feedback amplifier 96 by connecting lines 110 and 112. The latch output terminal 36 is coupled to negative-resistance device 94 at the terminal 106, and inverted latch output terminal 38 is coupled to negative-resistance device 94 at terminal 108. The latch output terminal 36 is the output terminal 34 of system 20 shown in FIGURE 3, and the inverted latch output terminal 38 is the inverted output terminal of system 20.

The latch 26 receives a comparator output signal and an inverted comparator output signal from the comparator 24 transmitted on connecting lines 46 and 48. During one clock cycle, the signals received over connecting lines 46 and 48 are applied to the two-to-one multiplexer 90 and will be the outputs on connecting lines 102 and 104. During the next clock cycle, the signals received by the two-to-one multiplexer 90 from the feedback amplifier 96 on lines 110 and 112 will be outputs on lines 102 and 104.

In the latch 26, the negative-resistance device 94 operates in the pre-peak region 17 when the current through the device received over connecting lines 106 and 108 is zero. This produces an output signal of zero. However, when the current on the connecting lines 106 and 108 reaches a specified value, the negative-resistance device 94 is forced into either the negative-bias valley region 16, which produces an output signal of -1, or the positive-

bias valley region 18, which produces an output signal of +1.

According to the present invention, the latch amplifier 92 amplifies the signals received on lines 102 and 104 and the feedback amplifier 96 amplifies the signals received over lines 106 and 108. In one embodiment, latch output terminal 36 produces a +1 for the output signal when the input signal is greater than a first threshold, a -1 for the output signal when the input signal is less than a second threshold, and a zero for the output signal when the input signal is between the first threshold and the second threshold.

Although the present invention has been described, various changes and modifications may be suggested in the art. It is intended that the present invention encompass such changes and modifications as fall within the scope of the appended claims.

WHAT IS CLAIMED IS:

1. A system for quantizing an analog signal comprising:

a sample-and-hold circuit coupled to receive an input signal, the input signal inverted, a clock signal, and the clock signal inverted;

a comparator connected to the sample-and-hold circuit, and coupled to receive the clock signal and the inverted clock signal;

a latch circuit connected to the comparator, and coupled to receive the clock signal and the inverted clock signal;

an output terminal coupled to an output of the latch circuit to provide a quantized output signal; and

an inverted output terminal also coupled to an output of the latch circuit to provide an inverted output signal.

2. The system of Claim 1 wherein the input signal comprises a varying current.

3. The system of Claim 1 wherein the output signal comprises a varying voltage.

4. The system of Claim 1 wherein the output signal comprises one of three levels represented by -1, 0, and +1.

5. The system of Claim 1 wherein the input signal comprises a signal in the X-band range.

6. The system of Claim 1 wherein the comparator comprises:

a plurality of eight switches;

a first negative-resistance device having a first terminal coupled to a first switch and a second switch of the plurality of eight switches and having a second terminal coupled to a third switch and a fourth switch of the plurality of eight switches;

a second negative-resistance device having a first terminal coupled to a fifth switch and a sixth switch of the plurality of eight switches and having a second terminal coupled to a seventh switch and an eighth switch of the plurality of eight switches;

a comparator input terminal coupled to the first switch and the fifth switch;

an inverted comparator input terminal coupled to the third switch and the seventh switch;

an output amplifier coupled to the second switch, the fourth switch, the sixth switch and the eighth switch;

a comparator output terminal coupled to the output amplifier to provide a comparator output signal; and

an inverted comparator output terminal also coupled to the output amplifier to provide an inverted comparator output signal.

7. The system of Claim 6, the comparator circuit further comprising:

a first current source coupled to the first switch and the fifth switch;

a second current source coupled to the third switch and the seventh switch;

a third current source coupled to the comparator input terminal and the inverted comparator input terminal; and

a fourth current source coupled to the inverted comparator input terminal and the comparator input terminal.

8. The system of Claim 7 wherein the comparator input terminal couples to the first switch, the fifth switch, the first current source, the third current source, and the fourth current source, and wherein the inverted comparator input terminal couples to the third switch, the seventh switch, the second current source, the third current source, and the fourth current source.

9. The system of Claim 6 wherein the first negative-resistance device and the second negative-resistance device comprise a resonant tunneling diode.

10. The system of Claim 1 wherein the latch circuit comprises:

a latch amplifier;

a negative-resistance device having a first terminal coupled to the latch amplifier and a second terminal coupled to the latch amplifier;

a feedback amplifier coupled to the first terminal and the second terminal of the negative-resistance device, the feedback amplifier producing a first feedback output and a second feedback output;

a two-to-one multiplexer coupled to the latch input terminal, the inverted latch input terminal, the first feedback output and the second feedback output;

wherein the multiplexer operates to pass the signals associated with the latch input terminal and the inverted latch input terminal during one clock cycle and the signals associated with the first feedback output and the second feedback output during the next clock cycle and wherein the latch amplifier couples to the multiplexer;

a latch output terminal coupled to the first terminal of the negative-resistance device to provide a latch output signal; and

an inverted latch output terminal coupled to the second terminal of the negative-resistance device to provide an inverted latch output signal.

11. The system of Claim 10 wherein the negative-resistance device comprises a resonant tunneling diode.

12. A comparator for quantizing an analog signal comprising:

a plurality of eight switches;

a first negative-resistance device having a first terminal coupled to a first switch and a second switch of the plurality of eight switches and having a second terminal coupled to a third switch and a fourth switch of the plurality of eight switches;

a second negative-resistance device having a first terminal coupled to a fifth switch and a sixth switch of the plurality of eight switches and having a second terminal coupled to a seventh switch and an eighth switch of the plurality of eight switches;

an output amplifier coupled to the second switch, the fourth switch, the sixth switch and the eighth switch;

a comparator output terminal coupled to the output amplifier to provide a comparator output signal; and

an inverted comparator output terminal coupled to the output amplifier to provide an inverted comparator output signal.

13. The comparator of Claim 12, further comprising:

a comparator input terminal for receiving an input signal;

an inverted comparator input terminal for receiving an inverted input signal;

a first current source coupled to the first switch and the fifth switch of the plurality of eight switches;

a second current source coupled to the third switch and the seventh switch of the plurality of eight switches;

a third current source coupled to the comparator input terminal and the inverted comparator input terminal; and

a fourth current source coupled to the inverted comparator input terminal and the comparator input terminal.

14. The comparator of Claim 13 wherein the comparator input terminal couples to the first switch, the fifth switch, the first current source, the third current source, and the fourth current source, and wherein the inverted comparator input terminal couples to the third switch, the seventh switch, the second current source, the third current source, and the fourth current source.

15. The comparator circuit of Claim 12 wherein the first negative-resistance device and the second negative-resistance device comprise a resonant tunneling diode.

16. A latch circuit comprising:

a latch input terminal for receiving an input signal;

an inverted latch input terminal for receiving an inverted input signal;

a latch amplifier;

a negative-resistance device having a first terminal coupled to the latch amplifier and a second terminal coupled to the latch amplifier;

a feedback amplifier coupled to the first terminal and the second terminal of the negative-resistance device, the feedback amplifier generating a first feedback output and a second feedback output;

a multiplexer coupled to the latch input terminal, the inverted latch input terminal, the first feedback output and the second feedback output;

wherein the multiplexer passes the signals received at the latch input terminal and the inverted latch input terminal during one clock cycle and passes the first feedback output and the second feedback output during the next clock cycle and wherein the latch amplifier couples to the multiplexer;

a latch output terminal having a latch output signal, the latch output terminal coupled to the first terminal of the negative-resistance device; and

an inverted latch output terminal having an inverted latch output signal, the inverted latch output terminal coupled to the second terminal of the negative-resistance device.

17. The system of Claim 16 wherein the negative-resistance device comprises a resonant tunneling diode.

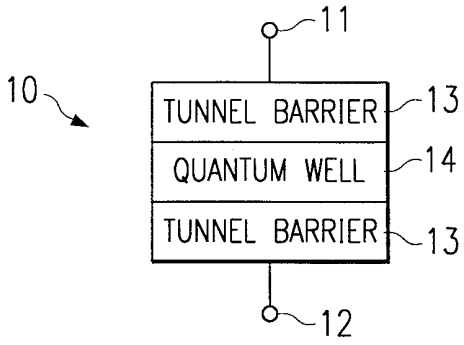


FIG. 1

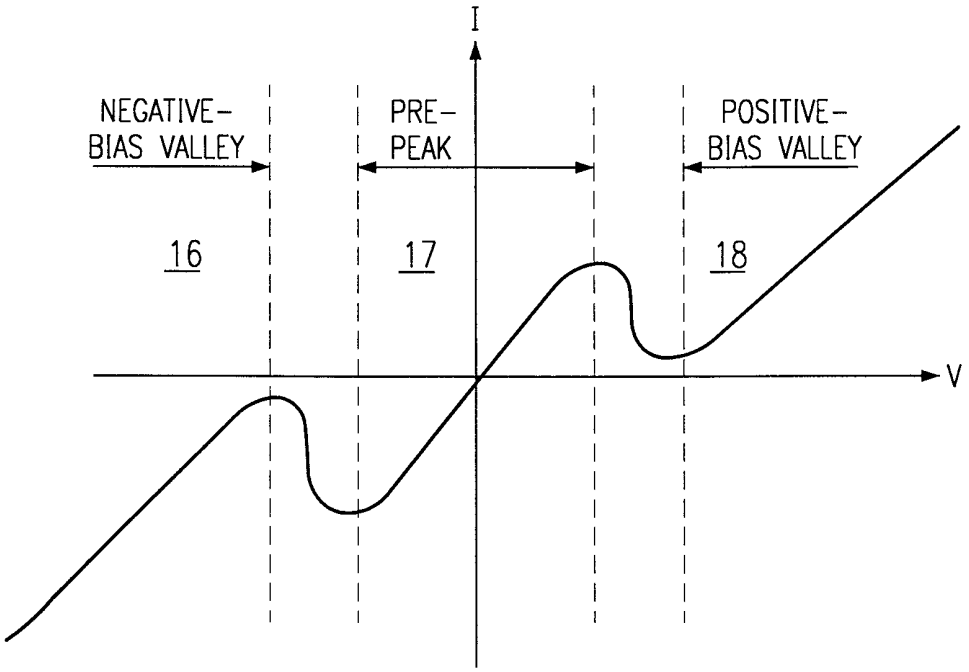


FIG. 2

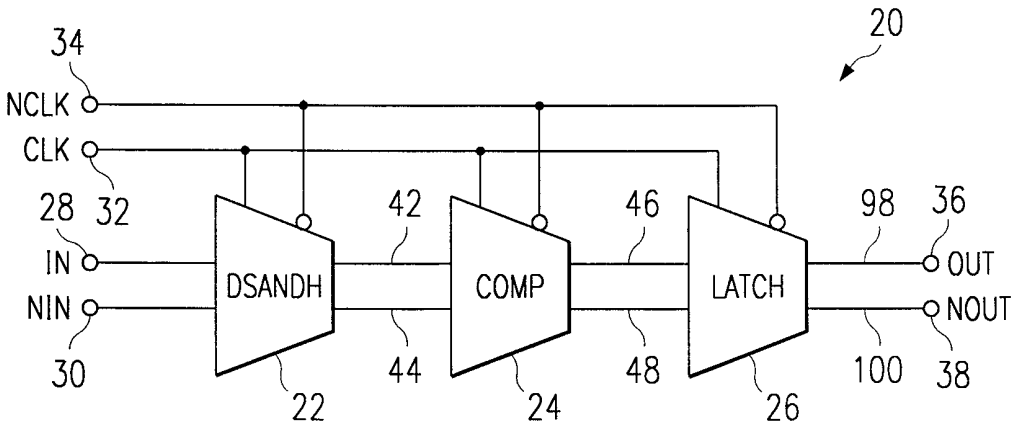


FIG. 3

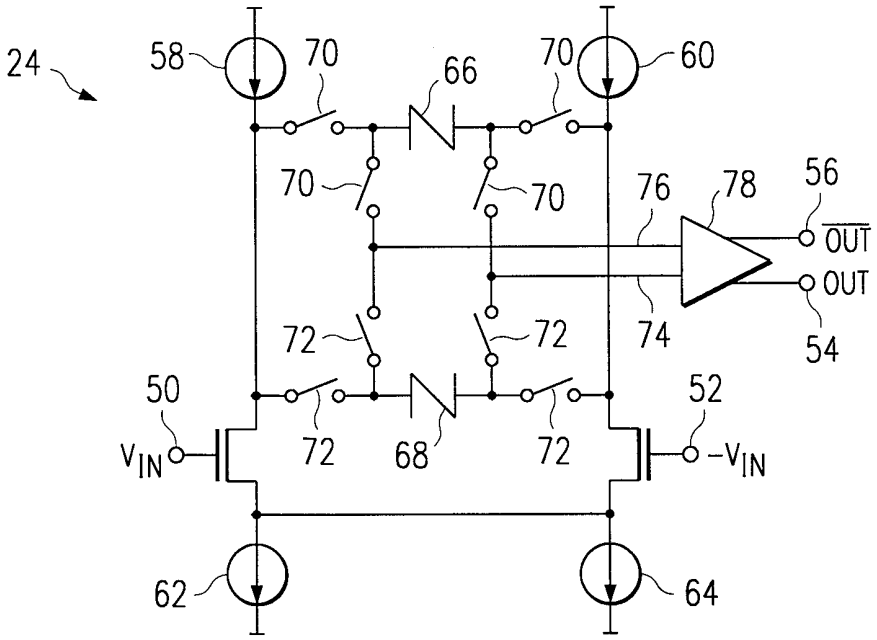

24
58
70
66
70
60
70
70
76
78
56
OUT
OUT
54
72
72
74
50
52
V_{IN}
72
68
72
$-V_{IN}$
62
64

FIG. 4

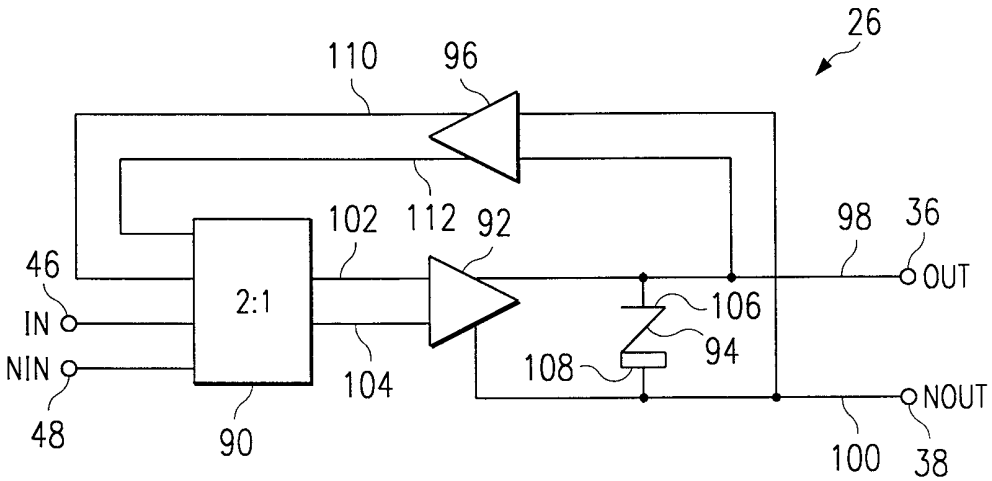

26
110
96
102
112
92
98
36
46
2:1
OUT
IN
106
94
NIN
108
104
NOUT
48
90
100
38

FIG. 5