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(54) Class AB amplifying circuit

(57) A class AB amplifying circuit includes a circuit arrangement for controlling the quiescent current through amplifier transistors (T1, T2) incorporated therein so the load current (I_L) is zero when the input voltage (U_{IN}) to the circuit is zero. The arrangement comprises two feedback loops, connected respectively to the bases of the transistors. One feedback loop comprises a sensing resistor (R1) connected to a load (Z) such as deflection coils, an adder (S1) and an amplifier (A1) with high gain and input impedance. The second feedback loop comprises a sensing resistor (R2) in the main current flow of the second transistor (T2), an adder (S2) and an amplifier (A2) of the same kind as the first one (A1). The degree of feedback in the second loop is suitably selected greater than that of the first loop to achieve a greater control range for the amplifying circuit. Transistors (T1, T2) may be of complementary types, and VMOS types may be used.

Fig. 1

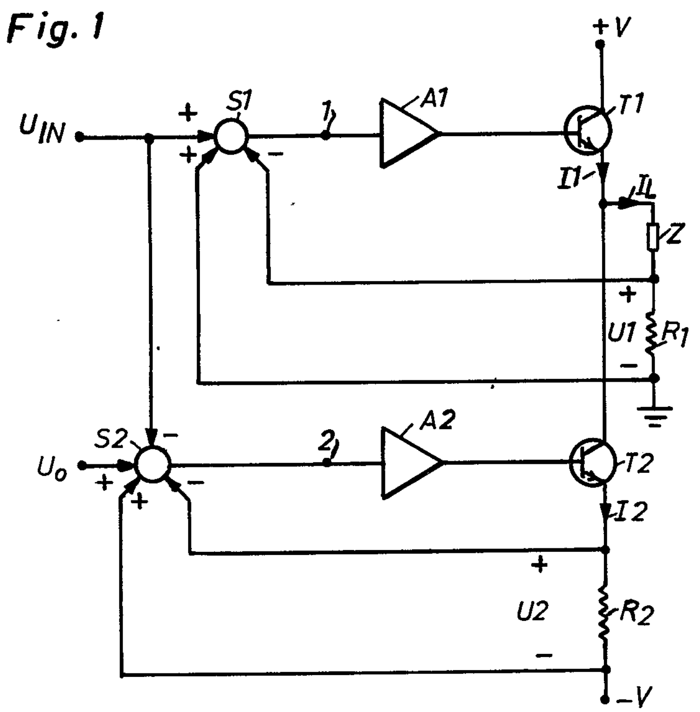

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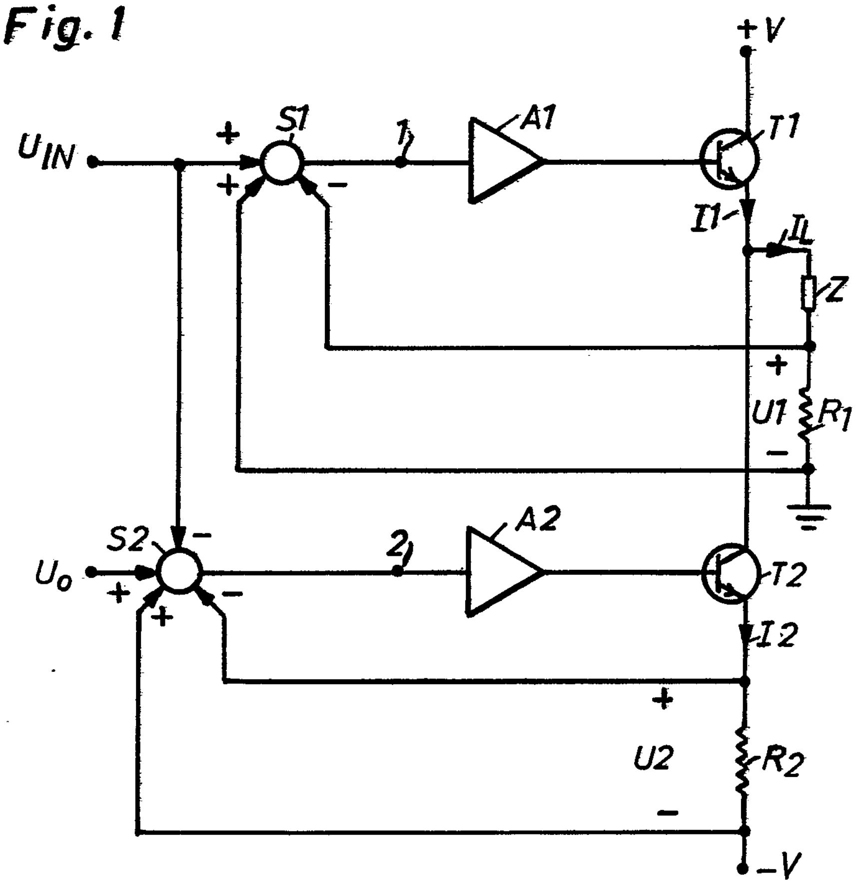
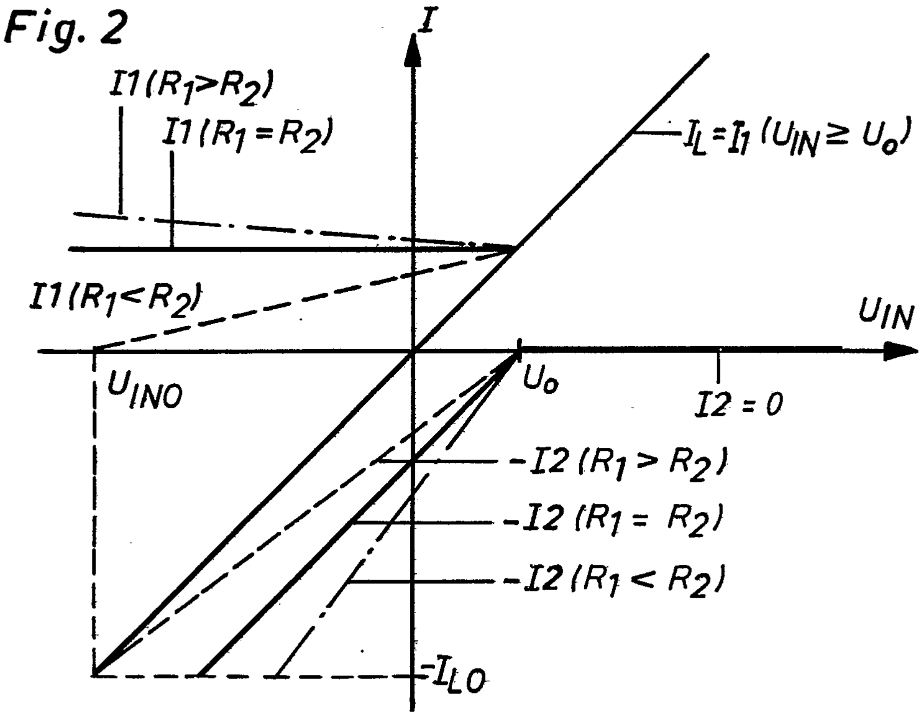
Fig. 1



+V
UIN
S1
A1
T1
I1
IL
Z
U1
R1
S2
A2
Uo
T2
I2
U2
R2
-V

Fig. 2



I
I1 (R1>R2)
I1 (R1=R2)
I1 (R1<R2)
IL=I1 (UIN ≥ Uo)
UIN
UIN0
Uo
I2 = 0
-I2 (R1 > R2)
-I2 (R1 = R2)
-I2 (R1 < R2)
-IL0

SPECIFICATION

A class AB amplifying circuit

The present invention relates to a class AB amplifying circuit, including a circuit arrangement for controlling the quiescent current (zero current) in the amplifying circuit. An area of application for such circuits is the control of current to the deflection coils in graphic image screens.

An amplifier stage operates in class A if the included amplifying elements, usually transistors, are biassed so that they operate within their linear (active) range for all the input signals to the amplifier stage. In a class B amplifier stage, the included transistors are biassed so that they are controlled to full conductive or non-conductive states for input signals of given polarity. In such amplifier stages where the input signal is sinusoidal, for example, a transistor is controlled to a conductive state during one half-period of the input signal, while the transistor is blocked during the other half-period. A second transistor is therefore provided in the amplifier, which is controlled to a conductive state during the second half-period, so that an amplified output signal is obtained during both half-periods of the input signal.

A class AB amplifier stage operates substantially as a class B amplifier stage. In a range around zero where the load current reverses, however, both amplifying elements are conductive in class AB. The current flowing through both amplifying elements when the load current is zero is designated the zero current, or quiescent current. Previously known amplifier circuits for controlling the quiescent current are described in, for example, German Offenlegungsschrifts 22 52 666 and 26 14 399.

According to the present invention, there is provided a class AB amplifying circuit including a circuit arrangement for controlling the quiescent current in the circuit, comprising a first amplifier element for conducting a first main current in response to an input signal voltage to the circuit, and a second amplifier element for conducting a second main current in response to the input signal and a constant quiescent voltage to the circuit, there being a load connected to a connection point between the first and second amplifier elements, and to a terminal for connection to first reference potential in use of the circuit, the circuit arrangement comprising a first negative feedback loop to the first amplifier element, this loop comprising 1) a first sensing element connected in the load path for sensing the load current and for forming a quantity, the value of which is dependent on the load current, and an adder connected via a first amplifier to a control electrode of the first amplifier element, for adding the input signal and the said value dependent on the load current, and 2) a second negative feedback loop to the second amplifier element, this loop comprising a second sensing element connected in a main current path for sensing the second main current and for forming a quantity, whose value depends on the second main current, and a second adder connected via a further amplifier to a control electrode of the second amplifier element for adding the said quiescent voltage and the value dependent on the second main current.

The present invention will now be described by way of example with reference to the accompanying drawing, in which Figure 1 illustrates a circuit of a class AB amplifier stage and Figure 2 is a diagram of the relationships between certain quantities occurring in the circuit of Figure 1.

A class AB amplifier stage divided into two separate negative feedback loops is illustrated in Figure 1. The first negative feedback loop includes an adder S1, which receives an incoming signal voltage U_{IN} on a non-inverting (plus) input. The output of the adder S1 is connected to the input of an amplifier A1 with very high open loop gain and input impedance (A, $Z_{in} \approx \infty$). The output of the amplifier A1 is connected to the base of a transistor T1, illustrated in Figure 1 as a bipolar n-p-n transistor, which is connected in the main current path of the amplifier stage between both terminals +V, −V of a supply voltage source. A load Z, e.g. the inductance of a deflecting coil, is in series with a sensing resistor R1 connected to a reference potential (earth or ground). The voltage drop U1 across the sensing resistor R1 is connected across a non-inverting (plus) input and an inverting (minus) input of the adder S1 so that the negative feedback loop is obtained. The current I_L through the load is thus sensed by the resistor R1 and is fed back via the adder to the input side of the amplifier stage.

The second negative feedback loop comprises a second adder S2, an amplifier A2 with high open loop gain and input impedance, an n-p-n transistor T2 and a sensing resistor R2 connected to the second terminal −V of the supply voltage source. The current I2 through the transistor T2, i.e. in the amplifier stage main current path, is sensed by the resistor R2, and a voltage U2 proportional to this current is connected to the adder S2 in the same way as in the first negative feedback loop.

The amplifier stage operates such that when a certain quiescent voltage U_o is connected and the input voltage $U_{IN} = 0$, both the transistors are controlled such that they operate within their linear ranges and a given quiescent current I_o flows into the main current path of the amplifier stage between the two terminals +V, −V of the source. The demand on the amplifier stage is thus that the current I_L through the load Z shall be zero, since $U_{IN} = O$. If it is assumed that the quiescent voltage U_o is positive relative to the reference, ground, then the voltage drop across the resistor R2 is equal to $R2.I2 = U_o$, since $U_o > O$ and the point 2 is at a potential close to O (virtual ground) due to the high gain in the amplifier A2, i.e.

$I1 = U_o/R2$

The voltage drop across the resistor R1 is simultaneously equal to $R1.I_L = O$, since $U_{IN} = O$, i.e.

$I_L = O$.

The current through the load is thus equal to zero when the input signal is equal to zero, and the quiescent current $I_o = I1 = I2 = U_o/R2$ is determined solely by the quiescent voltage U_o and the resistor R2.

For $U_{IN} \leqslant U_o$, the load current I_L flows through the transistor T1. In addition, the quiescent current I_o flows through the transistors T1 and T2 as well as possibly and excess current, if $R2 < R1$.

For $U_{IN} = O$, the quiescent current *Io* flows through both transistors T1 and T2. The load current I_L is then = 0. For $U_{IN} > Uo$, the load current I_L is conducted through the transistor T1. The current I2 is then = O. The following relationships are valid:

$I_L = U_{IN}/R1$

$I2 = (Uo - U_{IN})/R2 = Io - U_{IN}/R2$ for $I2 > O$

$I1 = I_L + I2$ for $I1 > O$

The load current I_L is thus determined solely by the first negative feedback loop containing the resistor R1 and the input voltage U_{IN}.

The diagram according to Figure 2 illustrates the variation of the transistor currents I1 and I2 and the load current I_L (for $I1 > O$) as a function of the input voltage U_{IN}. For $U_{IN} \leq Uo$, $I2 = O$ in accordance with the above, and the load current solely consists of the current I1 through the transistor T1. For $U_{IN} \leq Uo$, the current I_L is composed of both currents I1 and I2, but the load current value is equal to $U_{IN}/R1$, i.e. solely dependent on the first negative feedback loop and the input voltage U_{IN}. The diagram according to Figure 2 shows, however, that the transistor currents I1 and I2 have different courses depending on the degree of negative feedback in both loops. This is determined by the value of the sensing resistors R1 and R2, respectively.

For $R1 > R2$, the transistor current I1 increases *pro rata* with increasing negative value of the input voltage U_{IN}, the transistor current $-I2$ decreasing to a corresponding degree, so that the load current continuously decreases in proportion to $-U_{IN}$, of the dash-dotted lines in Figure 2.

For $R1 < R2$ instead, the current I1 diminishes towards zero when U_{IN} increases towards a higher negative value, and the current I2 diminishes less than in the previous case, of the dashed lines in Figure 2. Since the current I1 must be greater than zero, there is obtained in this case a limitation of the control range of the amplifier for the input value U_{INo} and the load current value I_{Lo}. In the boundary case (full lines in Figure 2) when $R1 = R2$ there is obtained that $I1 = Io$ and I2 will be equal to the load current minus the constant quiescent current *Io*.

It is obvious that such a negative feedback degree of the amplifier stage determined by the condition $R1 > R2$ according to the above is to be preferred, since this gives a large control range for the input voltage U_{IN}. In the case where $R1 < R2$, there is obtained, according to Figure 2, a limitation of the input voltage U_{IN} and the load voltage Ii.

The circuit arrangement can also be applied in such amplifiers which, instead of bipolar transistors according to Figure 1, contain MOS transistors, e.g. of the VMOS type. Simiarlly, the arrangement can be applied when the transistors T1 and T2 are arranged complementary, whether they are bipolar or of the MOS type.

CLAIMS

1. A class AB amplifying circuit, including a circuit arrangement for controlling the quiescent current in the circuit, comprising a first amplifier element for conducting a first main current in response to an input signal voltage to the circuit, and a second amplifier element for conducting a second main current in response to the input signal and a constant quiescent voltage to the circuit, there being a load connected to a connection point between the first and second amplifier elements, and to a terminal for connection to first reference potential in use of the circuit, the circuit arrangement comprising a first negative feedback loop to the first amplifier element, this loop comprising 1) a first sensing element connected in the load path for sensing the load current and for forming a quantity, the value of which is dependent on the load current, and an adder connected via a first amplifier to a control electrode of the first amplifier element, for adding the input signal and the said value dependent on the load current, and 2) a second negative feedback loop to the second amplifier element, this loop comprising a second sensing element connected in a main current path for sensing the second main current and for forming a quantity, whose value depends on the second main current, and a second adder connected via a further amplifier to a control electrode of the second amplifier element for adding the said quiescent voltage and the value depending on the second main current.

2. A circuit as claimed in claim 1, wherein the first sensing element comprises a resistor connected in series with an impedance, which forms the said load, and the second sensing element comprises a resistor connected to an output electrode of the second amplifier element and to a terminal for connection to a second reference potential.

3. A circuit as claimed in claim 2, wherein the resistance of the first resistor is greater than the resistance of the second resistor to achieve a higher degree of negative feedback in the second loop as compared with that of the first loop.

4. A class AB amplifying circuit, substantially as herein described with reference to the accompanying drawing.

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