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(71) Applicant: **HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P.** [US/US]; 11445 Compaq Center Drive W., Houston, Texas 77070 (US).

(72) Inventors: **GE, Ning**; 1501 Page Mill Road, Palo Alto, California 94304 (US). **SIMSKE, Steven J.**; 3390 E Harmony Road, Ft. Collins, Colorado 80528 (US). **GEORGE, David**; 1501 Page Mill Road, Palo Alto, California 94304-1100 (US).

(74) Agent: **MAISAMI, Ceyda Azakli** et al.; HP Inc., Mail Stop 35 3390 E. Harmony Road, Fort Collins, Colorado 80528 (US).

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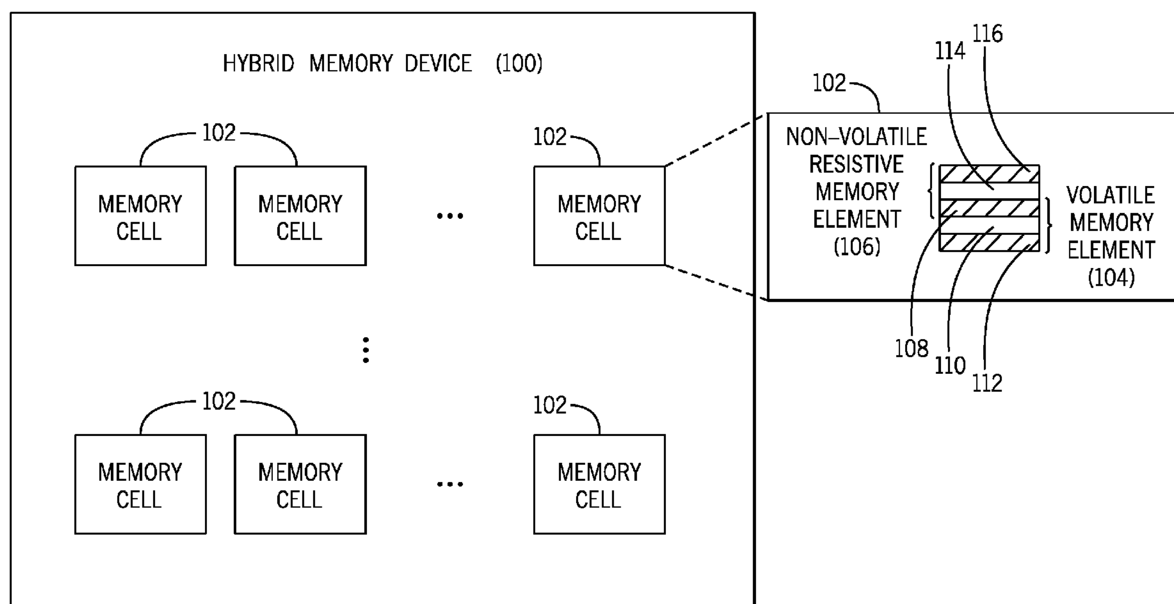

FIG. 1

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(57) Abstract: In some examples, a hybrid memory device includes multiple memory cells, where a given memory cell of the multiple memory cells includes a volatile memory element having a plurality of layers including electrically conductive layers and a dielectric layer between the electrically conductive layers, and a non-volatile resistive memory element to store different data states represented by respective different resistances of the non-volatile resistive memory element, the non-volatile resistive memory element having a plurality of layers including electrically conductive layers and a resistive switching layer between the electrically conductive layers of the non-volatile resistive memory element.

[Continued on next page]

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HYBRID MEMORY DEVICES

Background

[0001] Electronic devices include memory devices to store data. In some examples, memory devices include dynamic random access memory (DRAM) memory devices. A DRAM device can be used as the main memory of an electronic device, where the DRAM device has a higher access speed than persistent storage such as a hard disk drive or a solid state drive.

Brief Description Of The Drawings

[0002] Some implementations of the present disclosure are described with respect to the following figures.

[0003] Fig. 1 is a block diagram of a hybrid memory device according to some examples.

[0004] Fig. 2A is a schematic diagram of memory cells of a hybrid memory device according to some examples.

[0005] Fig. 2B is a schematic diagram of a memory cell according to alternative examples.

[0006] Fig. 3 is a block diagram of various components of a hybrid memory device according to further examples.

[0007] Fig. 4 is a block diagram of an electronic device that includes a hybrid memory device according to some examples.

[0008] Fig. 5 is a flow diagram of a process of forming a hybrid memory device according to some examples.

[0009] Fig. 6 is a flow diagram of a process of operating a hybrid memory device according to further examples.

Detailed Description

[0010] In the present disclosure, the article “a,” “an”, or “the” can be used to refer to a singular element, or alternatively to multiple elements unless the context clearly indicates otherwise. Also, the term “includes,” “including,” “comprises,” “comprising,” “have,” or “having” is open ended and specifies the presence of the stated element(s), but does not preclude the presence or addition of other elements.

[0011] A dynamic random access memory (DRAM) device has several desirable characteristics as compared to other types of memory or storage devices, where such characteristics can include any or some combination of the following: higher access speed, lower power consumption, higher endurance, and lower cost per bit. An issue with DRAM devices is that they have to be refreshed on a continual basis, and moreover, DRAM devices are volatile or non-persistent; if electrical power is removed from a DRAM device, then data stored by the DRAM device is lost.

[0012] A DRAM device includes an array of memory cells each including a storage capacitor. The storage capacitor can be written with a ‘0’ or a ‘1’ data state, where a ‘0’ data state corresponds to a low voltage level written to the storage capacitor, and a ‘1’ data state corresponds to a high voltage level written to the storage capacitor. A low voltage level is a voltage level that is less than a specified threshold, while a high voltage level is a voltage level that is greater than the specified threshold.

[0013] After a high voltage level (for a ‘1’ data state) is written to the storage capacitor of a DRAM memory cell, the charge in the storage capacitor begins to leak away. Over time, the voltage level of the storage capacitor can drop below the specified threshold such that the storage capacitor no longer stores a ‘1’ data state. To address this issue, a refresh of the DRAM memory cells can be performed. In a refresh operation, data states of the DRAM memory cells can be read by circuitry of the DRAM device, and such data states are written back to the DRAM memory cells to refresh the charge of the DRAM memory cells.

[0014] When power is removed from a DRAM device, such as when an electronic device in which the DRAM device is included is powered off or placed into a sleep state, the data stored in the memory cells of the DRAM device is lost due to leakage of charge away from storage capacitors of the DRAM device. When the electronic device later transitions back to an operational state (a higher power state where power is restored to electronic components of the electronic device) from a power off state, the data that was previously stored in the DRAM device is no longer available. As a result, the electronic device would have to retrieve data from a slower persistent storage, such as a hard disk drive implemented with a magnetic rotational storage medium or a solid state drive implemented with a flash memory device or other non-volatile memory device, in order to populate the data in the DRAM device. Populating data in the DRAM device with data from persistent storage takes time and can slow down the operation of the electronic device when transitioning back to an operational state from a power off state. A power off state is a state where power is removed from various electronic components, including a memory device, of an electronic device.

[0015] In accordance with some implementations of the present disclosure, a hybrid memory device includes memory cells where each of at least some of the memory cells includes both a volatile memory element (e.g., a DRAM memory element) and a non-volatile resistive memory element (which is also referred to as a memristor element). The memristor element is able to store different data states that are represented by respective different resistances of the memristor element. During a write of the memristor element, the memristor element can be programmed to a first resistance to represent a first data state, or a second, different resistance to represent a second, different data state. During a read of the memristor element, the resistance of the memristor element can be sensed to determine the data state stored by the memristor element. In further examples, a memristor element can store more than two data states using more than two resistances.

[0016] Fig. 1 is a block diagram of an example hybrid memory device 100 according to some implementations of the present disclosure. The hybrid memory

device 100 includes multiple memory cells 102, which can be arranged as an array of memory cells, where the array includes rows of memory cells and columns of memory cells.

[0017] Each of at least some of the memory cells includes both a volatile memory element 104 and a non-volatile resistive memory element 106. The non-volatile resistive memory element 106 is also referred to as a memristor element 106. The volatile memory element 104 is formed using multiple layers, including a first electrically conductive layer 108, a first dielectric layer 110, and a second electrically conductive layer 112. The memristor element 106 is formed using multiple layers including the first electrically conductive layer 108, a resistive switching layer 114, and a third electrically conductive layer 116. The resistive switching layer 114 is a layer whose resistance can be changed by input energy, such as by a bias voltage.

[0018] In Fig. 1, the layers 108, 110, 112, 114, and 116 are shown as being arranged in a vertical stack. In other examples, the layers 108, 110, 112, 114, and 116 can be formed in a horizontal stack, or a stack of a different orientation. In yet further examples, the layers 108, 110, 112, 114, and 116 do not have to be arranged in a stack, but rather can be arranged in different stacks, where a portion of the layer 108 and the layers 110 and 112 are arranged in a first stack, and another portion of the layer 108 and the layers 114 and 116 are arranged in a second stack.

[0019] Additionally, although Fig. 1 shows each of the layers 108, 110, 112, 114, and 116 as being a generally planar layer, in other examples, a layer of the volatile memory element 104 and/or memristor element 106 can have a non-planar shape, such as a serpentine shape, a general U shape, a vertical arrangement, a three-dimensional arrangement, and so forth.

[0020] In arrangements according to Fig. 1, the volatile memory element 104 and the memristor element 106 share a common electrically conductive layer (i.e., the electrically conductive layer 108). However, at least one electrically conductive layer (e.g., 112) of the volatile memory element 104 is separate and distinct from at least one electrically conductive layer (e.g., 116) of the memristor element 106 (in other

words, the electrically conductive layer 112 of the volatile memory element 104 is not part of the memristor element 106, and the electrically conductive layer 116 of the memristor element 106 is not part of the volatile memory element 104). In other examples, the stack of layers of the volatile memory element 104 and the stack of layers of memristor element 106 do not share layers. In the latter examples, an electrically conductive layer of the volatile memory element 104 is electrically connected to an electrically conductive layer of the memristor element 106.

[0021] In some examples, the electrically conductive layers 108, 112, and 116 can be formed of a metal, such as tantalum, platinum, titanium, aluminum, copper, and so forth. In other examples, the electrically conductive layers 108, 112, and 116 can be formed of a metal allow (e.g., an aluminum-copper alloy, a tantalum-aluminum alloy, etc.), a metal compound (e.g., titanium nitride, etc.), a conductive oxide (e.g., titanium oxide, indium tin oxide (ITO), etc.), transition metal dichalcogenides, and a conductive polymer (e.g., poly(3,4-ethylenedioxythiophene) polystyrene sulfonate, etc.). In further examples, the electrically conductive layers 108, 112, and 116 can be formed of a non-metallic electrically conductive material, such as graphene (MoS_2), graphite, iodine doped poly-acethylene, and so forth.

[0022] In some examples, the resistive switching layer 114 of the memristor element 106 can include an oxide-containing material, where the oxide-containing material includes a non-stoichiometric oxide, such as hafnium oxide (HfO_x), tantalum oxide (TaO_x), titanium oxide (TiO_x), yttrium oxide (YO_x), niobium oxide (NbO_x), zirconium oxide (ZrO_x), aluminum oxide (AlO_x), magnesium oxide (MgO_x), dysprosium oxide (DyO_x), lanthanum oxide (LaO_x), and so forth. In additional examples, the resistive switching layer 114 can include transition metal oxides (TMO) (oxide compounds composed of oxygen atoms bound to transition metals), complex oxides (a chemical oxide compound that contains oxygen and at least two other elements (or oxygen and just one other element that is in at least two oxidation states), perovskite oxides (a class of oxide compounds with general perovskite formula ABO_3 or A_2BO_4), and some non-oxide insulators, such as chalcogenides (a chemical compound made up of at least one chalcogen anion and at least one more

electropositive element) including transition metal dichalcogenide (TMD), flexible and organic materials, and even carbon nanotube and graphene-based structures. In other examples, the resistive switching layer 114 of the memristor element 106 can include another type of material, such as a nitride-containing material, for example, aluminum nitride, gallium nitride, tantalum nitride, silicon nitride, and so forth.

[0023] In some examples, the dielectric layer 110 of the volatile memory element 104 includes an insulating material, such as an oxide-containing material, where the oxide-containing material includes a full oxide or a stoichiometric oxide. Examples of such oxide-containing materials include hafnium oxide (Hf_2O_5), tantalum oxide (Ta_2O_5), titanium oxide (Ti_2O_5), hafnium oxide (Hf_2O_5), tantalum oxide (Ta_2O_5), titanium oxide (Ti_2O_5), yttrium oxide (Y_2O_5), niobium oxide (Nb_2O_5), zirconium oxide (Zr_2O_5), aluminum oxide (Al_2O_5), magnesium oxide (Mg_2O_5), dysprosium oxide (Dy_2O_5), lanthanum oxide (La_2O_5), and so forth. In other examples, the dielectric layer 110 can include another type of material, such as a nitride-containing material, including those listed above.

[0024] In further examples, other materials can be used to form the dielectric layer 110 or the resistive switching layer 114.

[0025] Fig. 2A is a schematic diagram that illustrates some memory cells 102 of an array of memory cells. Each memory cell 102 has a volatile memory element 104 that includes a storage capacitor, and a memristor element 106. In examples according to Fig. 2A, in each memory cell 102, the volatile memory element 104 is arranged in series with the memristor element 106. In addition, each memory cell 102 includes an access transistor 202 that controls access of the memory cell 102. In some examples, the access transistor 202 can be implemented as a metal-oxide-silicon (MOS) field effect transistor (MOSFET). When the access transistor 202 of a given memory cell 102 is turned on in response to assertion of a respective word line (word line i and word line i+1 are shown in Fig. 2A) to a high voltage, the volatile memory element 104 or memristor element 106 of the given memory cell 102 can be accessed through the activated access transistor 202. The volatile memory element 104 or memristor element 106 of the given memory cell 102 is coupled through the

activated access transistor 202 to a respective bit line (bit line j and bit line j+1 are shown in Fig. 2A). An electrical voltage or electrical current of the respective bit line is affected by the data state stored by the volatile memory element 104 or memristor element 106 of the given memory cell 102. A reading circuit (not shown in Fig. 2A) can sense the voltage or current of the respective bit line to determine the data state that is stored in the volatile memory element 104 or memristor element 106 of the given memory cell 102.

[0026] On the other hand, when the respective word line of the given memory cell 102 is de-asserted to a low voltage, the access transistor 202 is turned off, which isolates the given memory cell 102 from the respective bit line.

[0027] In some examples, each word line corresponds to a row of memory cells and each bit line corresponds to a column of memory cells. The combination of a word line and a bit line corresponds to a respective memory cell 102.

[0028] Fig. 2B shows a memory cell 102A according to alternative examples, which includes a volatile memory element 106 arranged in parallel with the memristor element 106. The volatile memory element 106 and the memristor element 106 are accessed through an access transistor 202 of the memory cell 102A.

[0029] Fig. 3 is a block diagram that shows circuitry to perform a read and write of a memory cell 102. The hybrid memory device 100 includes a row decoder 302 and a column decoder 304. Each of the row decoder 302 and the column decoder 304 receives an input address 306. A first portion of the input address 306 is used by the row decoder 302 to assert a word line 301 (from among multiple word lines output by the row decoder 302). In other words, in response to the input address 306, the row decoder 302 asserts a selected word line to an active state, and maintains the remaining word lines in an inactive state.

[0030] The column decoder 304 is responsive to a second portion of the input address 306 to select a column, and more specifically, a bit line 300 of multiple bit

lines. Outputs from the column decoder 304 are used to select from among multiple circuits to read from the selected bit line 300.

[0031] The hybrid memory device 100 further includes a volatile memory access controller 308 that is to perform read and write of volatile memory elements 104 in the memory cells 102, and a non-volatile memory access controller 310 to perform reads and writes of memristor elements 106 in the memory cells 102. A “controller” can refer to a hardware processing circuit implemented with transistors and associated circuitry.

[0032] In the example of Fig. 3, the volatile memory access controller 308 and non-volatile memory access controller 310 are depicted as performing reads and writes with respect to a memory cell 102 connected to a specific bit line 300. Note that more generally, each of the volatile memory access controller 308 and non-volatile memory access controller 310 can be used to selectively perform reads and writes from respective bit lines, in response to outputs of the column decoder 304.

[0033] Although the example of Fig. 3 depicts performing reads and writes of just one memory cell 102, it is noted that reads and writes of multiple memory cells can be performed concurrently by the volatile memory access controller 308 or the non-volatile memory access controller 310.

[0034] The volatile memory access controller 308 is connected to the bit line 300 by a first switch implemented as a first transistor 312, while the non-volatile memory access controller 310 is connected to the bit line 300 through a second switch implemented as a second transistor 314. The transistor 312 is controlled by a volatile memory select signal VSEL, which is asserted to an active state when performing reads and writes of the volatile memory elements 104 of the memory cells 102. On the other hand, the transistor 314 is controlled by a non-volatile memory select signal NVSEL, which is asserted to an active state to perform reads and writes of memristor elements 106 of the memory cells 102. Although not shown, the signals VSEL and NVSEL are generated by a controller that is able to receive an instruction regarding whether to perform an access of volatile memory elements or

memristor elements. Note that just one of the transistors 312 and 314 would be activated at any given time.

[0035] The volatile memory access controller 308 includes a read circuit 316 and a write circuit 318. The read circuit 316 includes a sense amplifier 320. Assuming that a read operation of volatile memory elements 104 is being performed, the VSEL signal is asserted to an active state, while the NVSEL signal is de-asserted to an inactive state. Also, it is assumed that the word line 301 has been asserted to an active state, which turns on the access transistor 202 of the memory cell 102. The voltage of the storage capacitor of the volatile memory element 104 is transferred to the bit line 300, and passed through the transistor 312 to the sense amplifier 320. The sense amplifier 320 detects the voltage level of the bit line 300 and outputs either a high voltage level (corresponding to a ‘1’ data state) or a low voltage level (corresponding to a ‘0’ data state), where the output voltage from the sense amplifier 320 is stored in a read buffer 322. The data stored in the buffer 322 can be retrieved for output from the hybrid memory device 100.

[0036] The write circuit 318 of the volatile memory access controller 308 includes a write driver 324. During a write operation, depending on the data value that is to be written to the volatile memory element 104 of the memory cell 102, the write driver 324 can either drive the bit line 300 to a high voltage level or a low voltage level through the transistor 312. The voltage is passed through the access transistor 202 for storage in the storage capacitor of the volatile memory element 104.

[0037] The non-volatile memory access controller 310 includes a read circuit 330 and a write circuit 335. In accordance with some implementations of the present disclosure, the read circuit 330 can use an alternating current (AC) sense technique that provides an AC measurement indicative of the impedance of the memory cell 102. Since the impedance of the storage capacitor of the volatile memory element 104 in the memory cell 102 is known, the impedance or resistance of the memristor element 106 in the memory cell 102 can be derived based on the overall impedance of the memory cell 102.

[0038] An AC sense technique involves using an AC signal, which can be in the form of a sine way having a voltage amplitude. In some examples, the voltage amplitude of the oscillating signal is relatively low, such as on the order of less than or equal to 0.5 volts, or in other examples, less than or equal to 0.3 volts, or in further examples, less than or equal to 0.2 volts. By using an AC signal having a low voltage amplitude to sense the resistance of the memristor element 106 in the memory cell 102, the resistance of the memristor element 106 would not be disturbed by the read operation. In this way, the data state stored by the memristor element 106 is not destroyed by a read operation.

[0039] Assuming that a read operation is in progress of the non-volatile memory portion of the hybrid memory device 100, the NVSEL signal is asserted to an active state, while the VSEL signal is de-asserted to an inactive state. Also, it is assumed that the memory cell 102 in Fig. 3 is selected by asserting the word line 301 to an active state. In examples where the volatile memory element 104 and the memristor element 106 are arranged in series, as shown in Fig. 3, an AC signal generated by the read circuit 330 propagates through the transistors 314 and 202 and through the storage capacitor of the volatile memory element 104 to the memristor element 106. Note that if the oscillating signal has a sufficiently high frequency, the storage capacitor of the volatile memory element 104 appears as a short circuit to the oscillating signal. Generally, the impedance of the capacitor is inversely proportional to the frequency of a signal. The higher the frequency, the lower the impedance of the capacitor. In examples where the volatile memory element 104 and the memristor element 106 are arranged in parallel, as shown in Fig. 2B, the AC signal generated by the read circuit propagates through the transistors 314 and 202 to the memristor element 106.

[0040] In response to the AC signal, the AC current through the memristor element 106 can be measured by the AC sensor 332, to derive the resistance of the memristor element 106. The AC sensor 332 outputs a data value that corresponds to the sensed resistance, and this data value is stored in a data buffer 334 that can be retrieved for output by the hybrid memory device 100. A first resistance

corresponds to a first data state, while a second resistance corresponds to a second, different data state.

[0041] The write circuit 335 of the non-volatile memory access controller 310 includes a write driver 336, which can perform a write of the memristor element 106 through the transistors 314, 202 and through the storage capacitor of the volatile memory element 104. The write circuit 336 uses a direct current (DC) write of the memristor element 106. The write driver 336 can apply either a positive bias voltage across the memristor element 106, or a negative bias voltage across the memristor element 106. The positive or negative bias voltage has an amplitude that is much greater than the amplitude of the AC signal used to read the memristor element 106. For example, the positive or negative bias voltage for programming a resistance of the memristor element 106 can have an amplitude of about 5 volts, or some other voltage level. In such examples, the positive bias voltage applied to the memristor element 106 is +5 volts, and the negative bias voltage applied to the memristor element 106 is -5 volts. Memristors are two-terminal passive devices that can be electrically switched between two states including a high-resistance state (HRS) and a low-resistance state (LRS). The switching event from a HRS to a LRS is called a “Set” or “On” switching process, which occurs if the amplitude of the applied positive bias voltage is greater than a Set threshold voltage. Conversely, the switching from a LRS to a HRS is called a “Reset” or “Off” switching process, which occurs if the amplitude of the applied negative bias voltage is less than a Reset threshold voltage.

[0042] Under a positive bias voltage, the resistance of the memristor element 106 can be reduced. Under a negative bias voltage, the resistance of the memristor element 106 can be increased. Once the resistance of the memristor element 106 is modified by the application of the respective bias voltage by the write driver 336, the resistance of the memristor element 106 is maintained persistently, such that the memristor element 106 can “remember” the data state to which the memristor element 106 is programmed.

[0043] Fig. 4 is a block diagram of an example electronic device 400, which can be a computer (e.g., a notebook computer, a desktop computer, a tablet computer, a

server computer, etc.), a handheld device (e.g., a smartphone, a personal digital assistant, etc.), a wearable device (e.g., a smart watch, smart eyeglasses, a head-mounted device, etc.), a game appliance, a household appliance, a vehicle, a sensor device, a printing system, a communications node, and so forth. The electronic device 400 includes a processor 402, which can include any or some combination of the following: a microprocessor, a core of a multi-core microprocessor, a microcontroller, a programmable gate array, a programmable integrated circuit device, or other hardware processing circuit.

[0044] The processor 402 is able to access the hybrid memory device 100 to perform reads and writes of the hybrid memory device 100. The hybrid memory device 100 includes memory cells, where each of at least some of the memory cells 102 includes both a volatile memory element 104 and a memristor element 106 as discussed above.

[0045] Fig. 5 is a flow diagram of a process of forming a hybrid memory device according to some examples. The process of Fig. 5 includes forming (at 502) first multiple layers on a substrate to form a dynamic random access memory storage capacitor of a memory cell of the hybrid memory device, the first multiple layers including electrically conductive layers and a dielectric layer between the electrically conductive layers.

[0046] The process further includes forming (at 504) second multiple layers on the substrate to form a non-volatile resistive memory element of the memory cell, the second multiple layers including electrically conductive layers and a resistive switching layer between the electrically conductive layers of the non-volatile resistive memory element, and where an electrically conductive layer of the non-volatile resistive memory element is electrically connected to an electrically conductive layer of the dynamic random access memory storage capacitor. The first multiple layers and the second multiple layers are formed on a region of the substrate that corresponds to the memory cell.

[0047] Fig. 6 is a flow diagram of example operations that can be performed by the hybrid memory device 100 according to some implementations. The hybrid memory device 100 powers on (at 602). It is assumed that at the time of powering on (at 602), the non-resistive memory elements of the hybrid memory device 100 do not store any data, and that it is desired to use the volatile memory elements of the hybrid memory device 100, in other words, the DRAM portion of the hybrid memory device 100. The hybrid memory device 100, after powering on, programs (at 604) the memristor memory elements 106 of the memory cells 102 of the hybrid memory device 100 to a specified resistance state. In examples where the memristor element of each memory cell is connected in series to the storage capacitor of the volatile memory element of the memory cell (as shown in Fig. 2A), the memristor element can increase the overall capacitance and/or resistance of the memory cell. To reduce the amount of additional capacitance and/or resistance added by the memristor element, the memristor element is programmed to its low resistance state. Note that, in such examples, a high resistance state of the memristor element would add a greater amount of capacitance and/or resistance to the memory cell. By setting the memristor elements of the memory cells to the low resistance state, impact to performance of the DRAM portion of the hybrid memory cell 100 is reduced as compared to the impact of memristor elements set to a high resistance state.

[0048] On the other hand, in examples where the memristor element of each memory cell is connected in parallel to the storage capacitor of the volatile memory element of the memory cell (as shown in Fig. 2B), the memristor element can reduce the overall capacitance and/or resistance of the memory cell. In such latter examples, the memristor elements of the memory cells are programmed to the high resistance state to reduce the impact to performance of the DRAM portion.

[0049] After the memristor elements have been programmed to a specified resistance state, the hybrid memory device 100 is operated (at 606) in DRAM mode, i.e., read and write operations are performed with respect to the volatile memory elements of the memory cells 102.

[0050] At a later time, an electronic device in which the hybrid memory device 100 is included can receive an indication to power off. For example, a user may have activated a control element to power off the electronic device, or alternatively, the electronic device has determined that it should power off in response to determining that the electronic device has been idle for greater than a specified time duration, or that the electronic device has a low battery condition.

[0051] The electronic device can send an instruction to the hybrid memory device 100 to program (at 608) the memristor elements of a hybrid memory device 100 to target data values. For example, the instruction can specify that the memristor elements of the hybrid memory device 100 are to be programmed with the data states stored in the volatile memory elements of the hybrid memory device 100. To do so, the data states of the volatile memory elements are first read, and then written back to the memristor elements. In this way, prior to powering off the hybrid memory device 100, the data values stored in the DRAM portion of the hybrid memory device 100 can be made persistent in the memristor elements. In other examples, the memristor elements can be programmed to other data values.

[0052] The hybrid memory device 100 is power cycled (at 610), in which the hybrid memory device 100 is powered off, followed at a later time by powering on of the hybrid memory device 100. After the hybrid memory device 100 is powered on again, the hybrid memory device 100 reads (at 612) the memristor elements and stores the read data values in the volatile memory elements. In this way, data values stored in the DRAM portion of the hybrid memory device 100 are made available again after the power cycle 610.

[0053] By using the hybrid memory device 100 according to some implementations of the present disclosure, various features may be available, including higher speed, enhanced durability, and greater memory density. Additionally, data persistence is available due to the presence of the memristor elements. Further, since the memristor elements of the memory cells of the hybrid memory device 100 can be formed by adding a few more layers, the overall

manufacturing cost of the hybrid memory device 100 would not be greatly increased as compared to the cost of manufacturing a DRAM-only device.

[0054] In the foregoing description, numerous details are set forth to provide an understanding of the subject disclosed herein. However, implementations may be practiced without some of these details. Other implementations may include modifications and variations from the details discussed above. It is intended that the appended claims cover such modifications and variations.

What is claimed is:

1 1. A hybrid memory device comprising:
2 a plurality of memory cells, wherein a given memory cell of the plurality of
3 memory cells comprises:
4 a volatile memory element comprising a plurality of layers including
5 electrically conductive layers and a dielectric layer between the electrically
6 conductive layers; and
7 a non-volatile resistive memory element to store different data states
8 represented by respective different resistances of the non-volatile resistive memory
9 element, the non-volatile resistive memory element comprising a plurality of layers
10 including electrically conductive layers and a resistive switching layer between the
11 electrically conductive layers of the non-volatile resistive memory element.

1 2. The memory device of claim 1, wherein the volatile memory element and the
2 non-volatile resistive memory element of the given memory cell share a common
3 electrically conductive layer.

1 3. The memory device of claim 1, wherein the plurality of layers of the volatile
2 memory element form a dynamic random access memory (DRAM) storage
3 capacitor, the plurality of layers of the volatile memory element comprising a first
4 electrically conductive layer, the dielectric layer, and a second electrically conductive
5 layer.

1 4. The memory device of claim 3, wherein the plurality of layers of the non-
2 volatile resistive memory element comprise the first electrically conductive layer, the
3 resistive switching layer, and a third electrically conductive layer.

1 5. The memory device of claim 4, wherein the first electrically conductive layer,
2 the dielectric layer, the second electrically conductive layer, the resistive switching
3 layer, and the third electrically conductive layer are arranged in a stack of layers.

1 6. The memory device of claim 1, wherein the given memory cell further
2 comprises:
3 a transistor activatable to access the given memory cell.

1 7. The memory device of claim 1, further comprising:
2 a volatile memory access controller to access volatile memory elements of the
3 plurality of memory cells; and
4 a non-volatile memory access controller to access non-volatile resistive
5 memory elements of the plurality of memory cells.

1 8. The memory device of claim 7, wherein the non-volatile memory access
2 controller is to read the non-volatile resistive memory element of the given memory
3 cell by using an alternating current (AC) read signal to sense a resistance of the non-
4 volatile resistive memory element of the given memory cell.

1 9. The memory device of claim 8, herein the non-volatile memory access
2 controller is to write the non-volatile resistive memory element of the given memory
3 cell by using a direct current bias voltage to program a resistance of the non-volatile
4 resistive memory element of the given memory cell.

1 10. The memory device of claim 1, wherein the non-volatile resistive memory
2 element and the volatile memory element of the given memory cell are arranged in
3 series.

1 11. The memory device of claim 1, wherein the non-volatile resistive memory
2 element and the volatile memory element of the given memory cell are arranged in
3 parallel.

12. An electronic device comprising:

a processor; and

a hybrid memory device accessible by the processor, the hybrid memory device comprising:

a plurality of memory cells, wherein a given memory cell of the plurality of memory cells comprises:

a storage capacitor formed with a first electrically conductive layer, a dielectric layer, and a second electrically conductive layer; and

a memristor element formed with the first electrically conductive layer, a resistive switching layer, and a third electrically conductive layer.

13. The electronic device of claim 12, wherein the given memory cell further comprises a transistor activatable to access the given memory cell, the hybrid memory device further comprising:

a first access controller to access the storage capacitor of the given memory cell through the transistor; and

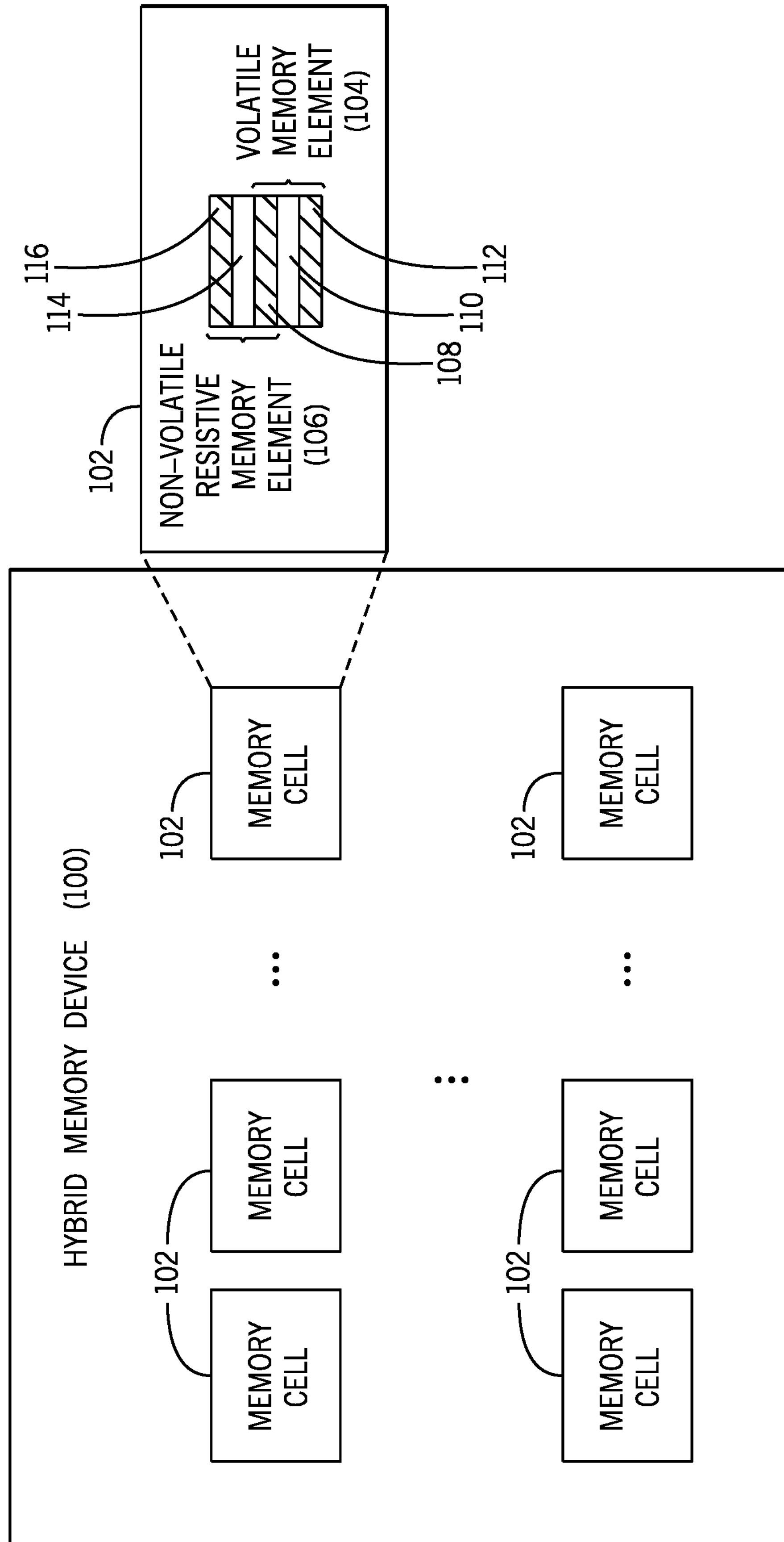
a second access controller to access the memristor element of the given memory cell through the transistor.

14. A method of forming a hybrid memory device, comprising:

forming a first plurality of layers on a substrate to form a dynamic random access memory storage capacitor of a memory cell of the hybrid memory device, the first plurality of layers comprising electrically conductive layers and a dielectric conductive layer between the electrically conductive layers; and

forming a second plurality of layers on the substrate to form a non-volatile resistive memory element of the memory cell, the second plurality of layers comprising electrically conductive layers and a resistive switching layer between the electrically conductive layers of the non-volatile resistive memory element, wherein an electrically conductive layer of the non-volatile resistive memory element is electrically connected to an electrically conductive layer of the dynamic random access memory storage capacitor.

1 15. The method of claim 14, wherein the first plurality of layers and the second
2 plurality of layers are formed on a region of the substrate that corresponds to the
3 memory cell.


HYBRID MEMORY DEVICE (100)
MEMORY CELL
102
NON-VOLATILE RESISTIVE MEMORY ELEMENT (106)
VOLATILE MEMORY ELEMENT (104)
108
110
112
114
116
FIG. 1

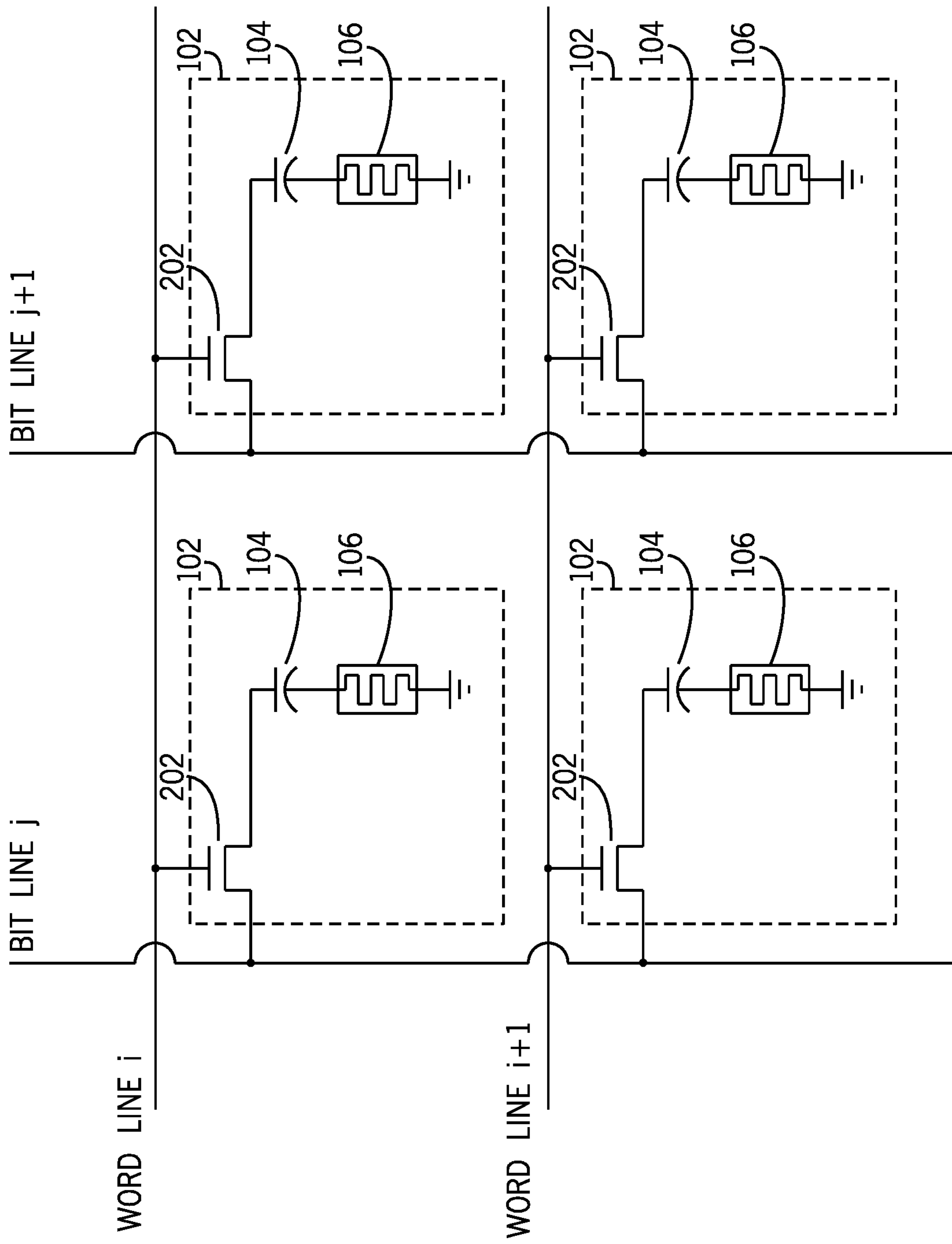


FIG. 2A

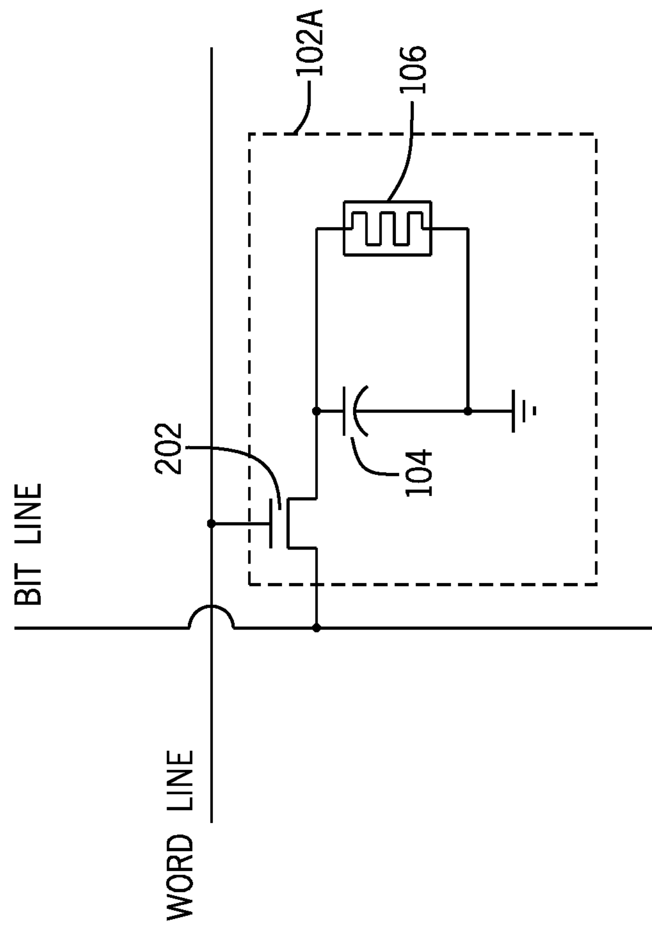


FIG. 2B

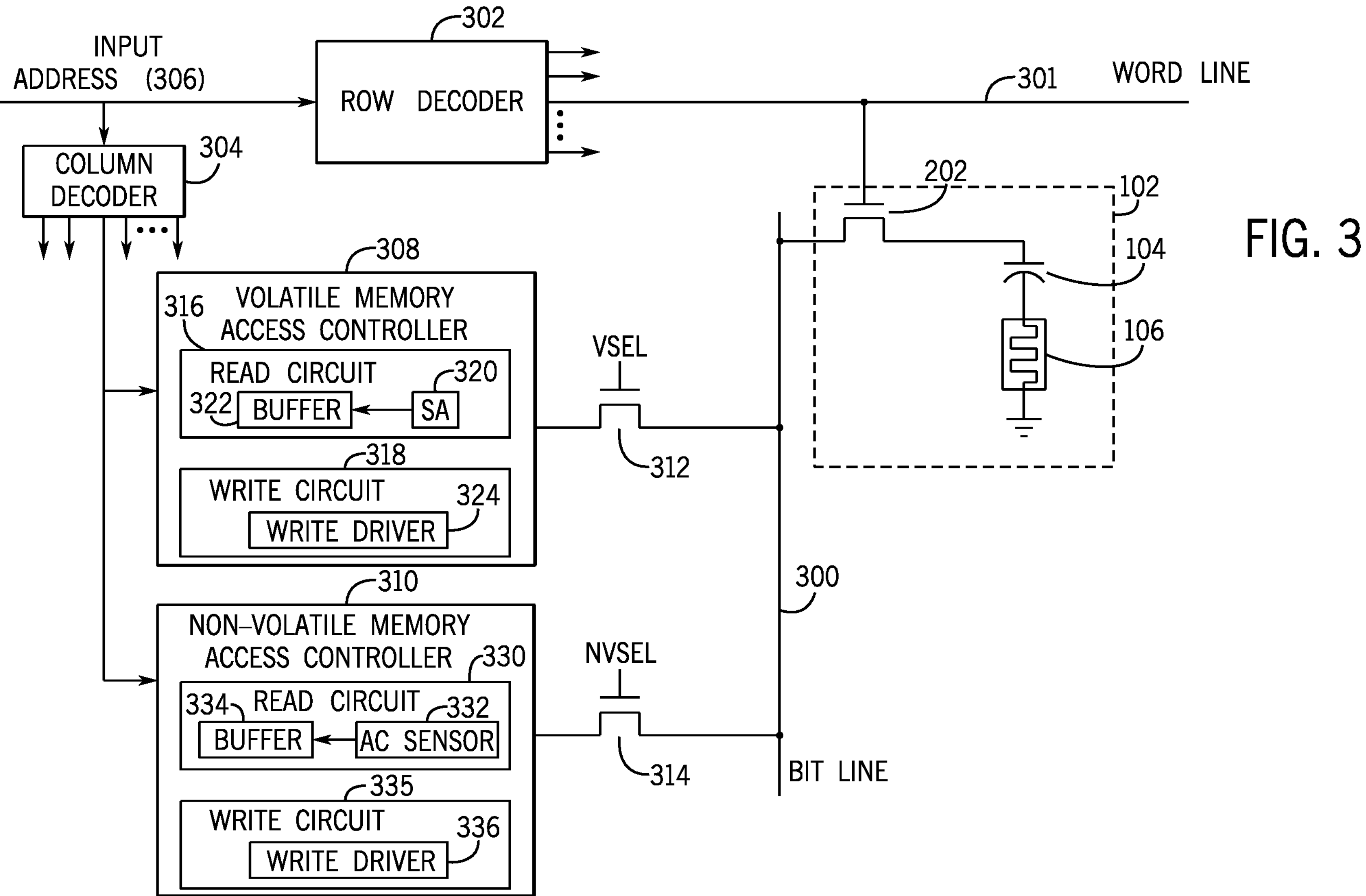
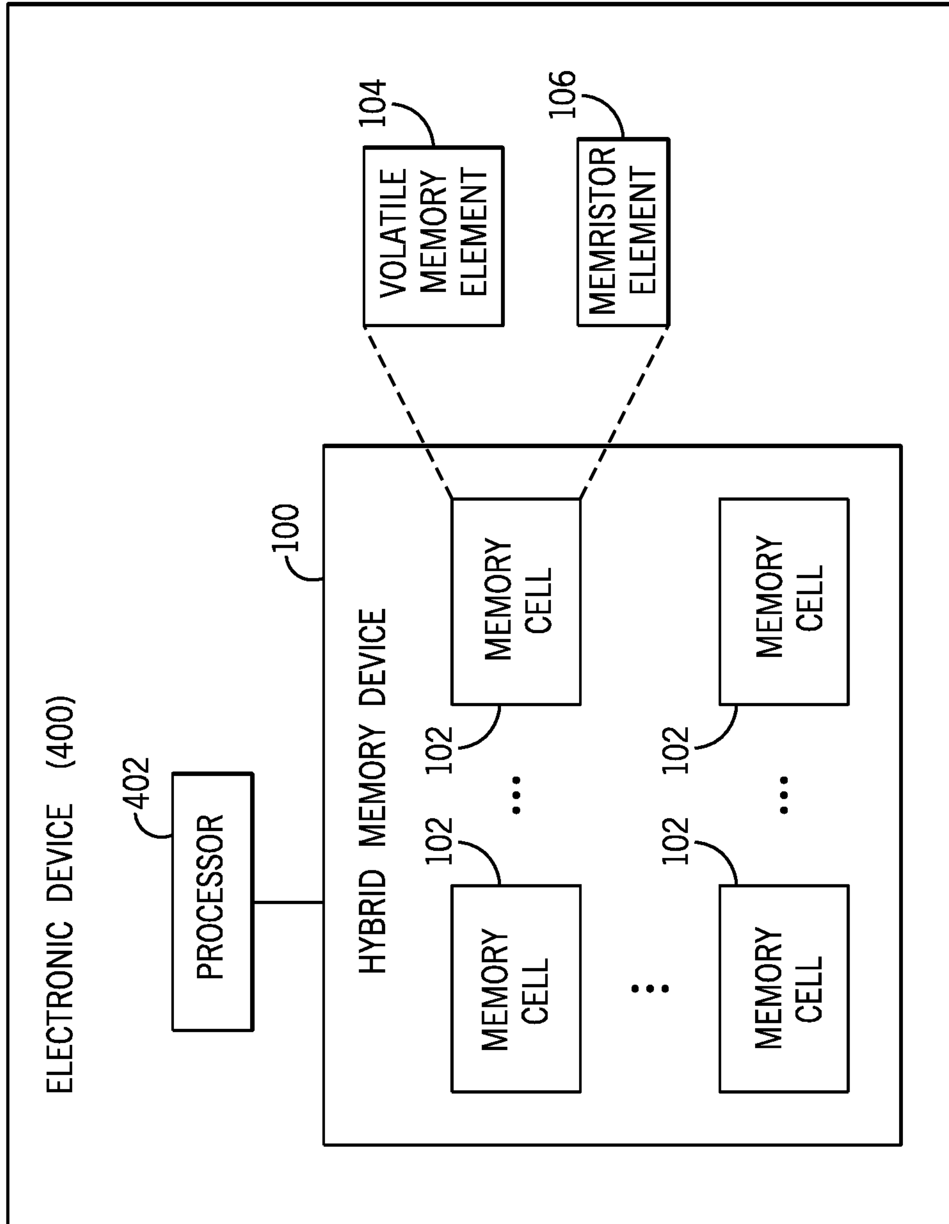

INPUT
ADDRESS (306)
302
ROW DECODER
301
WORD LINE
304
COLUMN
DECODER
202
102
104
106
FIG. 3
308
316
VOLATILE MEMORY
ACCESS CONTROLLER
READ CIRCUIT
320
322
BUFFER
SA
318
WRITE CIRCUIT
324
WRITE DRIVER
VSEL
312
300
310
NON-VOLATILE MEMORY
ACCESS CONTROLLER
330
334
READ CIRCUIT
332
BUFFER
AC SENSOR
335
WRITE CIRCUIT
336
WRITE DRIVER
NVSEL
314
BIT LINE

FIG. 4



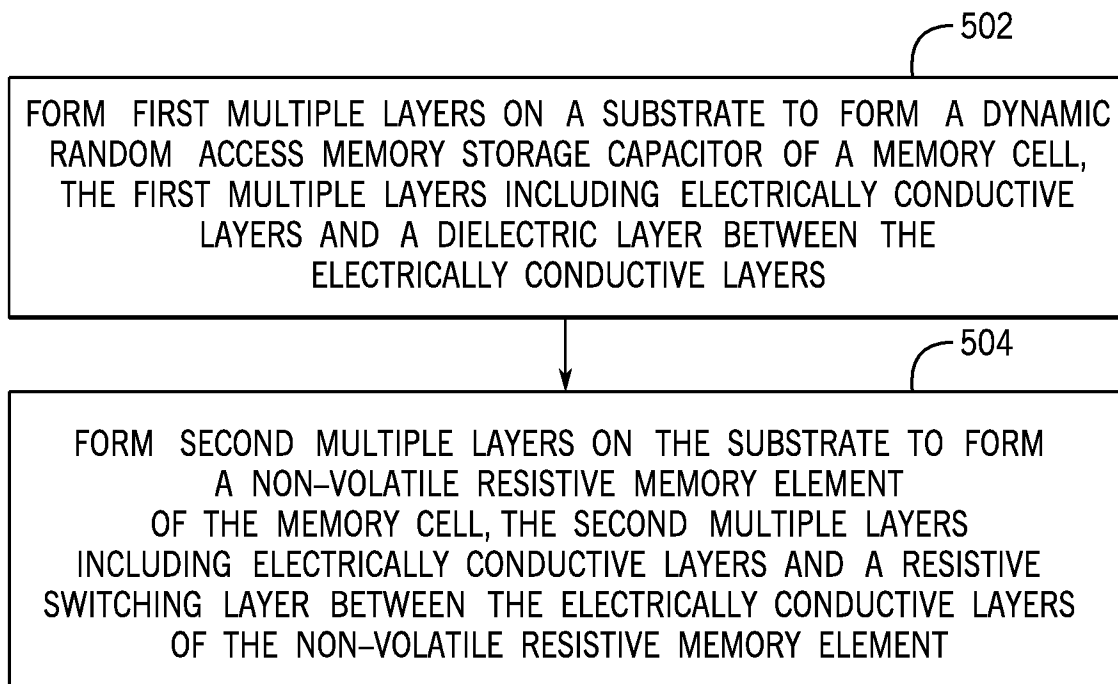


FIG. 5

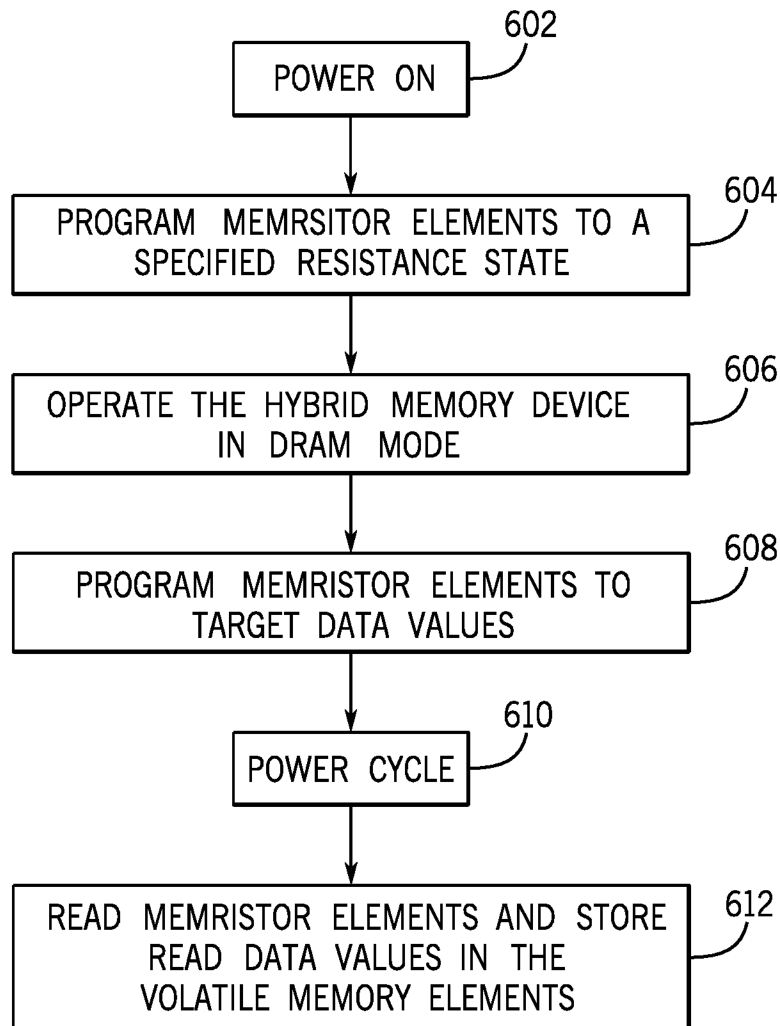


FIG. 6

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2016/055911

A. CLASSIFICATION OF SUBJECT MATTER

G11C 14/00 *(2006.01)*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G11C 14/00, 11/02, 11/14, 11/15, G06F 12/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

DWPI, ESP@CENET, K-PION, PAJ, SIPO, PatSearch, RUPTO, USPTO, WIPO

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 8576607 B1 (FARID NEMATI) 05.11.2013, col.1, lines 6-8, col.3, lines 32-37, col. 5, lines 48-50, 64-67, col. 6, lines 1-8, 22, 23, 50-59, col. 7, lines 7-24, 37-51, 57-59, col. 8, lines 40-42,col. 12, lines 5-42	1-15
Y	US 2015/0243886 A1 (CROSSBAR, INC.) 27.08.2015, paragraphs [0002], [0029], [0034], claim 16	1-15
Y	US 2015/0003175 A1 (RAJ K. RAMANUJAN) 01.01.2015, paragraphs [0013], [0016], [0030], [0076]	12, 13
Y	US 2009/0152608 A1 (SEMICONDUCTOR MANUFACTURING INTERNATIONAL (SHANGHAI) CORPORATION) 18.06.2009, paragraph [0007], claim 16	3-5, 12-15
Y	US 2012/0127779 A1 (ROY E. SCHEUERLEIN et al.) 24.05.2012, paragraphs [0098], [0244], [0280], [0298]	2, 11, 14, 15

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
06 June 2017 (06.06.2017)	13 July 2017 (13.07.2017)

Name and mailing address of the ISA/RU:
Federal Institute of Industrial Property,
Berezhkovskaya nab., 30-1, Moscow, G-59,
GSP-3, Russia, 125993
Facsimile No: (8-495) 531-63-18, (8-499) 243-33-37

Authorized officer

I. Kryazhev

Telephone No. 495 531 65 15