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(56) Documents cited
GB 2144606 A **GB 1374228 A** **EP 0013103 A1**

(58) Field of search
UK CL (Edition J) **G4H HNK HRD HV, H4P PEE**
INT CL⁴ **H03M, H04L**

(54) Data communication system

(57) A train of signals is generated by clocking an 8 bit word from an 8 bit shift register 10 which has been loaded with the initial data word. The register 8 is provided with feed-back loop 11 as shown. The serial data is supplied along a communication link 12 to a similar or identical 8 bit shift register 13 at the receiving end of the link 12. A comparator 14 is arranged to compare the output data of the register 13 with the first stage of the register 13 and to provide an accept signal provided such comparison indicates inversions at the receipt of each bit for 9 bits onwards. After transmission of 24 bits, the shift register 13 contains the 8 bit data word, which has been checked twice for any inaccuracy generally resulting from the transmission problems.

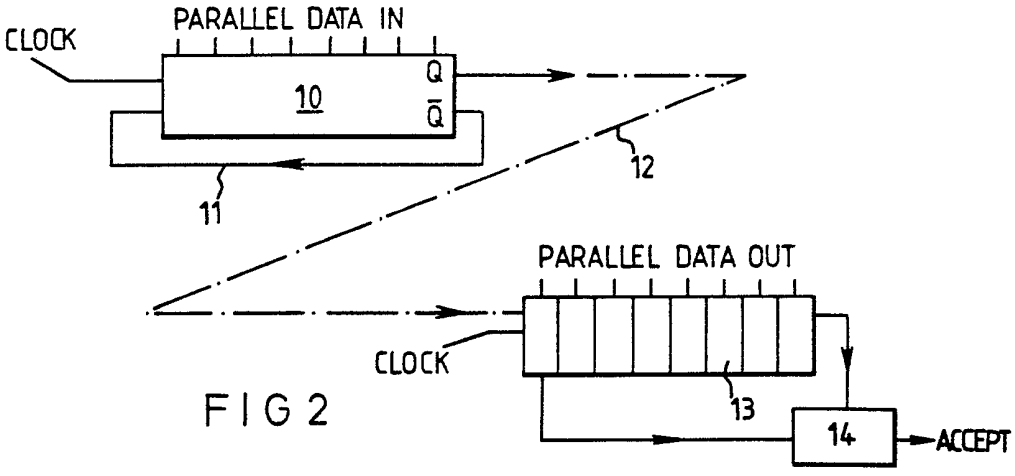

FIG 2

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At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

The claims were filed later than the filing date within the period prescribed by Rule 25(1) of the Patents Rules 1982.

D7 D6 D5 D4 D3 D2 D1 D0 $\overline{D7}$ $\overline{D6}$ $\overline{D5}$ $\overline{D4}$ $\overline{D3}$ $\overline{D2}$ $\overline{D1}$ $\overline{D0}$ D7 D6 D5 D4 D3 D2 D1 D0

FIG.1.

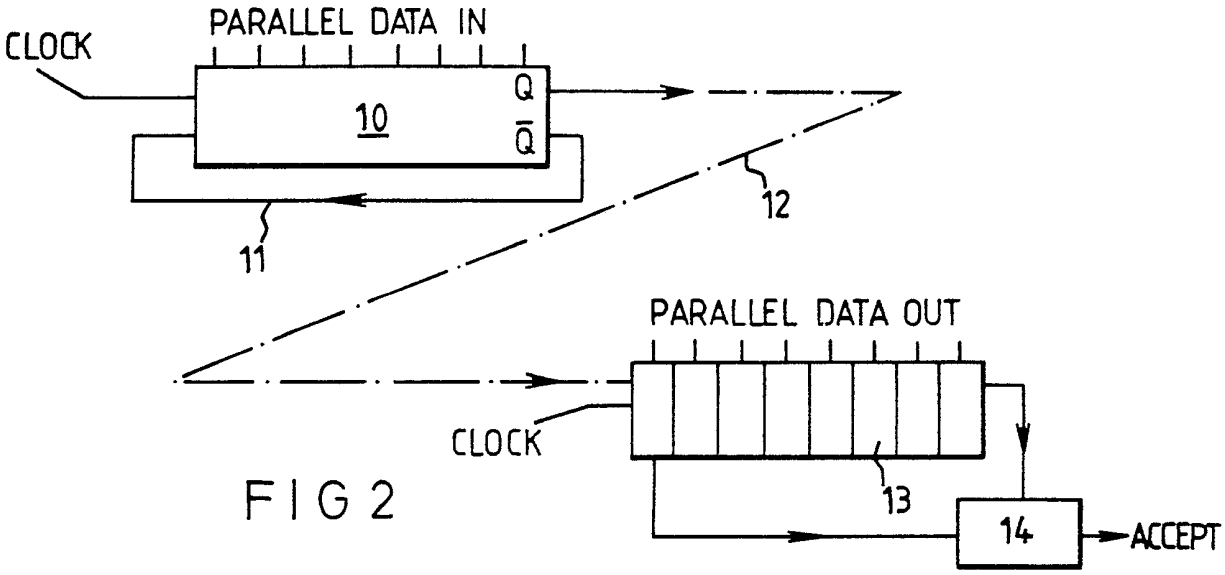

FIG 2

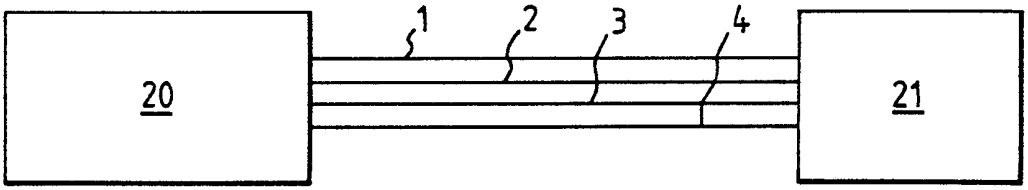

FIG.3.

H L (8-bit data) (8-bit data inverse) (8-bit data) L H H H H H

start bits — end bits

FIG 4

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"Data Communication System"

The invention relates to data communication systems.

More paricularly the invention relates to systems for the communication of serial data. As the application of electronic control systems becomes more wide spread and complex, the need for data to be sent about such systems with high reliability has become an important factor. To minimise the complexity and cost of communication links multiplexed or serial communication systems are used. However, it is necessary that the circuitry communicating upon a serial link be as simple and hence as cost effective as possible whilst being very reliable. Coding systems currently used are generally either not reliable enough or too complicated and would take up a lot of space within a device. An example of the latter case is that of cyclic redundancy coding (CRC) where large check words are generated and sent along with the data word. The generation of such a coding sequence requires extensive shift register networks to implement coding polynomials and with increasing use of ASIC technology such large coding systems are expensive.

An object of the invention is to provide a system for serial data transmission which is reliable and uncomplicated.

According to one aspect of the invention there is provided a method of verifying the accurate transmission of an n-bit word comprising transmitting the n-bit word followed by transmitting an inversion of the n-bit word, receiving the words in an n-bit shift register and checking for inversion of the n + 1 bit and all subsequent bits up to n + n bits by synchronised comparison with the corresponding output of the shift register, and providing an accept signal only if all the compared bits are inversions of one another, the word then stored in the shift register being the accurate inversion of the n-bit word.

The method may comprise sending the n-bit word again after transmitting the inverted n-bit word in which case the checking for inversion is carried out for n + 1 to n + 2n bits, in which case the word then stored in the shift register is the n-bit word and not its inversion, the checking having being carried out twice.

In a similar manner the transmitting method may include transmitting the n-bit word several times and alternatively sending the inversion of the word so that the checking is carried out three or more times respectively.

According to another aspect of the invention there is provided an apparatus for checking the accuracy of serially transmitted data, the apparatus including a transmitter for sending the n-bit words of data and an inversion of the n-bit words alternatively, an n-bit shift register for receiving the data, means for comparing the first stage of the register with its output arranged to provide an accept signal if that stage and the output are inversions of one another for all the data received after the first nth bit.

A data transmission system according to the invention will now be described by way of example with reference to the accompanying schematic drawings in which:-

Fig 1 is a code sequence;
Fig 2 shows a part of the transmission and receiving end of the system;
Fig 3 shows the layout of the system; and
Fig 4 shows a code sequence used in practice.

Referring to the drawings, the data to be communicated along a communication link each comprise data words of 8 bits. For each transmission, a train of signal comprises in sequence the required 8 bit data word, its inversion and the word again, see

Figure 1.

A train of signals is generated by clocking an 8 bit word from an 8-bit shift register 10 which has been loaded with the initial data word. The register 8 is provided with feed-back loop 11 as shown in Fig 2. The serial data is supplied along a communication link 12 to a similar or identical 8-bit shift register 13 at the receiving end of the link 12. A comparator 14 is arranged to compare the output data of the register 13 with the first stage of the register 13 and to provide an accept signal provided such comparison indicates inversions at the receipt of each bit for 9 bits onwards. After transmission of 24 bits, the shift register 13 contains the 8-bit data word, which has been checked twice for any inaccuracy generally resulting from the transmission problems.

In a practical situation as shown in Figure 3, a micro-controller 20 is used in a vehicle for use in controlling a number of remote systems 21, only one of which is shown. the microcontroller 20 is used to communicate with remote systems located within seats and doors for example of the vehicle and each remote controller is connected to the microcontroller by four wire links.

Link 1 is a bi-directional data link along which the 8-bit words are transmitted. Link 2 carries clocking signals generated at the microcontroller for the remote systems to maintain synchronised operation. link 3 is used for directional instructions to control which of the circuits transmit the data and which receive the data at any time. Link 4 is a logical zero or earth link to provide a controlled reference for the system.

A typical signal is shown in Figure 4. The data is 8-bits long and is framed in a high-low start and a low-high end sequence. This contitutes a 28 bit stream and the direction is changed

every 32 clock pulses. Thus, after each low-high stop bit, high states are sent until the next direction change. The start and stop sequences are monitorted as well as the nature of the received "tricyclic" data bits and any errors detected by the comparator 14. When the direction signal changes state, the received data them in the shift register 13 is accepted only if no errors have been detected by the comparator 14.

The described arrangement carries out transmission error checking with minimum of components. It will be further noted that the shift registers 10 and 13 can be and are both used for in transmitting and receiving signals. Each data bit is checked as it is received (in the described system this is carried out twice for each bit of the data) using relatively simple and otherwise well-tried and reliable shift-register components.

As described above, the data can be sent repeatedly and there is no facility provided or required for implementing data correction, again keeping the system extremely simple. Any temporary interference or fault in the transmission link can be ignored, because the data is repeatedly sent as described until a complete sequence without an error is satisfactorily received.

CLAIMS:

1. A method of verifying the accurate transmission of an n-bit word comprising transmitting the n-bit word followed by transmitting an inversion of the n-bit word, receiving the words in an n-bit shift register and checking for inversion of the n + 1 bit and all subsequent bits up to n + n bits by synchronised comparison with the corresponding output of the shift register, and providing an accept signal only if all the compared bits are inversions of one another, the word then stored in the shift register being the accurate inversion of the n-bit word.

2. A method according to Claim 1 comprising sending the n-bit word again after transmitting the inverted n-bit in which case the checking for inversion is carried out for n + 1 to n + 2n bits, in which case the word then stored in the shift register is the n-bit word and not its inversion, the checking having been carried out twice.

3. A method according to Claim 1 or 2, including transmitting the n-bit word several times and alternatively sending the inversion of the word so that the checking is carried out three or more times respectively.

4. An apparatus for checking the accuracy of serially transmitted data, the apparatus including a transmitter for sending the n-bit words of data and an inversion of the n-bit words alternatively, an n-bit shift register for receiving the date, means for comparing the first stage of the register with its output arranged to provide an accept signal if that stage and the output are inversions of one another for all the data received after the first n-bit.

5. A data transmission system substantially as described with reference to the accompanying drawings.

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