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(71) Applicant *(for all designated States except US)*: **MIMOS BERHAD** [MY/MY]; Technology Park Malaysia, 57000 Kuala Lumpur (MY).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: **TAN, Kong Yew** [MY/MY]; c/o MIMOS BERHAD, Technology Park Malaysia, 57000 Kuala Lumpur (MY).

(74) Agent: **YAP, Kah Hong**; PYPRUS SDN BHD, Suite 8.02, 8th Floor, Plaza First Nationwide 161, Jalan Tun H.S. Lee, 50000 Kuala Lumpur (MY).

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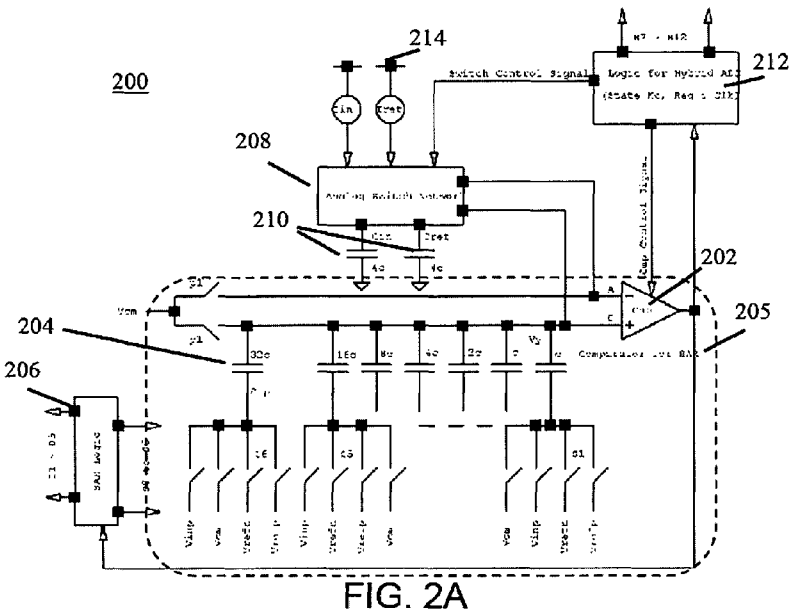

FIG. 2A

(57) Abstract: The present invention provides a hybrid analogue-to-digital converter (ADC) that comprises a successive approximation analogue-to-digital converter (SAR-ADC); and a time based integrating and cyclic analogue-to-digital converter (CYC-ADC) integrated with the SAR-ADC. An input analogue signal is processed through the SAR-ADC to output a first output constituting most significant bits (MSBs) of an digital output signal and a residue signal, the residue signal is further processed through the CYC-ADC to output a second output constituting the least significant bits (LSBs). A method of carrying out the analogue to digital conversion is also provided.

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Low Power High Resolution Analogue to Digital Converter and Method Thereof

Field of the Invention

[0001] The present invention relates to analogue to digital conversion (ADC). In particular, the present invention relates to a low power hybrid ADC for high-resolution analogue to digital signal conversion.

Background

[0002] In CMOS technology, power consumption of analog to digital converter does not scale linearly with resolution, $P_{ADC} \propto FS \times 2^N$, where FS is sampling frequency and N is resolution of the analog to digital converter. This is due to larger capacitors and transistors that are needed to prevent the process and circuit errors limiting the precision under a required design specification. In the case of high-resolution binary weighted charge redistribution successive approximation analog to digital converter (CR SA-ADC), the precision is limited by matching of integrated capacitors. The bigger the ratio of largest capacitor to smallest capacitor, more challenges to achieve a required accuracy. For example, in a 12-bit binary weighted CR SA-ADC, the largest capacitor is $2^{11} \times$ Cunit, where Cunit is the capacitance of the smallest capacitor, and accordingly, the total capacitance in the binary array is $2^{12} \times$ Cunit. This results in large power consumption in order to charge and discharge these capacitors during data conversion and also the accuracy is severely affected due to poor matching.

[0003] FIG. 1A illustrates a block diagram of a typical successive approximation analogue-digital converter (SA-ADC) well known in the art. The SA-ADC typically includes a sample and hold (S/H) circuit **102** for acquiring input voltage, V_{in}, a successive approximation register (SAR) for supplying an approximate digitalized V_{in} to an internal digital-to-analogue converter (DAC) **106**, an analogue voltage comparator **108** for comparing the V_{in} to the output of the internal DAC **106**, and an internal reference DAC that supplies the comparator **108** with an analogue voltage equivalent of the digitized output of the SAR **104** for comparison with V_{in}.

[0004] Operationally, the SAR **104** is initialized to set the most significant bit (MSB) to 1. The MSB is fed into the DAC **106**, which then supplies the analog equivalent of the digital code (i.e. $V_{ref}/2$) into the comparator **108** for comparison with the sampled input voltage. If this analog voltage exceeds V_{in}, the comparator **108** causes the SAR to reset this bit; otherwise, the bit is left as 1. Then the next bit is set to 1 and the same test is done, continuing this binary search until every bit in the SAR has been tested. The resulting output is the digital approximation of the sampled input voltage and is ultimately output by the DAC at the end of the conversion (EOC).

[0005] SAR ADC is designed with low power consumption, high resolution and accuracy, and a small form factor. The main limitations of the SAR architecture are the lower sampling rates and the requirements that the building blocks, the DAC and the comparator, be as accurate as the overall system.

[0006] FIG. 1B illustrates a block diagram of a known time based cyclic/algorithmic ADC (CYC-ADC). The CYC-ADC has a sample and hold stage implemented by a capacitor array and an amplifier. Residue voltage is generated in the

CYC-ADC. Such CYC-ADC is relatively slower than a SAR ADC because it cycles through or generates one bit of conversion for many clock cycles as compared to one bit of resolution per cycle for the SA ADC.

Summary

[0007] In one aspect of the present invention provides a hybrid analogue-to-digital converter (ADC) comprise a successive approximation analogue-to-digital converter (SAR-ADC); and a time based integrating and cyclic analogue-to-digital converter (CYC-ADC) integrated with the SAR-ADC. An input analogue signal is processed through the SAR-ADC to output a first output constituting most significant bits (MSBs) of an digital output signal and a residue signal, the residue signal is further processed through the CYC-ADC to output a second output constituting the least significant bits (LSBs).

[0008] In one embodiment, the SAR-ADC further comprises a comparator, a capacitor array, a successive approximation register (SAR) and a digital to analog converter (DAC), and the CYC-ADC further comprises an analogue switch network, a pair of capacitor, a state-machine, a reference current generator, wherein the CYC-ADC is coupled to share the comparator with the SAR-ADC. The DAC of the SAR-ADC is coupled with the SAR and output analogue signal to the comparator. The pair of capacitors may also be adapted for performing signal integrating over time; the network of switches for directing different charging currents to different capacitors; the state-machine to generate control signals for the analogue switch network and the comparator; an output register to store converted bits.

[0009] In another embodiment, the SAR-ADC is adapted to process the analogue input signal to acquire first M-bit MSBs of the output digital signal and the residue signal is processed through the CYC-ADC to acquire the remaining LSBs.

[0010] In another aspect of the present invention, there is provided a method of converting an analogue input signal to a digital output signal. The method comprises converting the analogue input signal through a successive approximation to output a first output constituting part of the total bits of the digital output signal and a residue signal; processing the residue signal through a time-based integrating cyclic analog to digital conversion to output a second output constituting the remaining bits of the digital output signal; and combining the first output and the second output to output the digital output signal.

[0011] In one embodiment, the method further comprises identifying the first output as the most significant bits of the digital output signal; identifying the second output as the least significant bits of the digital output signal; and adding the first output to the second output to output the digital output signal.

[0012] In another embodiment, adding the first output and the second output further comprises shifting bits of the first output such the first output constitute the most significant bits of the second portion of the conversion result are added to one or more least significant bits of the digital output signal.

[0013] In a further embodiment, converting the analogue input signal through the successive approximation further include performing a number of analog to digital conversion iterations, the number of analog to digital conversion iterations is less than

the number of bits in the digital output signal. Yet, processing the residue signal through the time- based integrating cyclic conversion includes performing a number of analog to digital conversion iterations, wherein the number of analog to digital conversion iterations is less than the number of bits in the digital output signal.

[0014] The successive approximation may produce a single bit of resolution for each iteration and the time based integrating cyclic based analog to digital conversion produces two bits of resolution during the first iteration and a single bit of resolution for subsequent iterations.

Brief Description of the Drawings

[0015] This invention will be described by way of non-limiting embodiments of the present invention, with reference to the accompanying drawings, in which:

[0016] **FIG. 1A** shows a typical successive approximation analogue to digital converter;

[0017] **FIG. 1B** shows a typical time based cyclic/algorithmic ADC;

[0018] **FIG. 2A** illustrates a schematic diagram of an ULPH-ADC **200** in accordance with one embodiment of the present invention;

[0019] **FIG. 2B** illustrates a general flow process of the ADC conversion in accordance with an embodiment of the present invention;

[0020] **FIGs. 3A** to **3D** illustrate a first step of the ULPH-ADC of the present invention; and

[0021] FIGs. 4A and 4B illustrate a second step of the ULPII-ADC of the present invention.

Detailed Description

[0022] In line with the above summary, the following description of a number of specific and alternative embodiments is provided to understand the inventive features of the present invention. It shall be apparent to one skilled in the art, however that this invention may be practiced without such specific details. Some of the details may not be described at length so as not to obscure the invention. For ease of reference, common reference numerals will be used throughout the figures when referring to the same or similar features common to the figures.

[0023] In ultra-low power operation applications, the most optimal resolution in terms of power consumption for different analogue-to-digital conversion (ADC) topologies can be combined to yield a very power efficient architecture especially for high-resolution Nyquist rate ADC. Such combination must however be synergistic in terms of low power circuit blocks (i.e. without op-amps) and method of conversion (i.e. power should scale linearly with resolution and speed).

[0024] The present invention provides an Ultra Low Power Hybrid Analog Digital Converter (ULPII-ADC) adapted for converting an analogue input signal to a digital output signal using a two-step approach: resolving the analogue input signal through a successive approximation algorithm; and resolving analogue residue voltage, $V_{RES\,SAR}$ through time based integrating cyclic ADC.

[0025] **FIG. 2A** illustrates a schematic diagram of an ULPH-ADC **200** in accordance with one embodiment of the present invention. The ULPH-ADC **200** is a hybrid of a successive approximation ADC (SAR-ADC) and a time based integrating and cyclic ADC (CYC-ADC) adapted for converting an analogue input signal into a digital signal at a desire bit. The ULPH-ADC comprises a comparator **202**, a capacitor array **204**, a digital-to-analogue converter (DAC) **205** and a successive approximation register **206** coupled to form a SAR-ADC, and an analogue switch network **208**, a pair of capacitors **210**, a logic circuit **212** and a reference current generator **214** coupled with the same comparator **202** to form the CYC-ADC. The logic circuit **212** further comprises a state-machine to generate control signals for the analogue switch network and an output register to store converted bits. The output of the capacitor array **204** is electrically coupled to comparator **202**. The pair of capacitors **210** are provided for performing signal integrating over time, the analogue switch network **208** is used for directing different charging currents to different capacitors **210** for performing signal integration over time.

[0026] **FIG. 2B** illustrates a general flow process of the ADC conversion in accordance with an embodiment of the present invention. The ADC conversion encompasses two different known methods for converting analogue signals to digital signals. The two known method are carrying out in two main steps. In the first step **250**, first half most significant bits (MSBs) are processed through a successive approximation. A residue voltage is generated at the end of the successive approximation A/D conversion **250**.

[0027] In a second stage **260**, the next half least significant bits (LSBs) are resolved from the residue voltage output with an integrated cyclic/algorithmic conversion.

[0028] Through the above method, as only part of the bits are converted through the successive approximation method, it requires a smaller capacitance for the largest binary weighted capacitor when compared with one that process all the bits through the successive approximation method. Accordingly, the ratio of the largest to smallest capacitor is reduced resulting in improved capacitor matching and accuracy. For example, when a 12-bits digital output is desired from an analogue input, 6 out of 12 bits output is processed using successive approximation method, the largest binary weighted capacitor size for MSB bit is $2^5 \times$ Cunit instead of $2^{11} \times$ Cunit. Accordingly, the total capacitance that the reference voltage needs to be driven is also much smaller, i.e $2^6 \times$ Cunit instead of $2^{12} \times$ Cunit, which reduces overall power consumption.

[0029] The use of a time based integrating cyclic analogue-to-digital converter to resolve the next 6 (i.e. the remaining) LSBs does not increase power consumption the converter is designed for 6 bit accuracy instead of 12 bit accuracy. Further, as the hybrid ADC **200** is implemented with a single comparator shared by the SA-ADC and a reference current to keep the power consumption low. Further, the gain and subtraction routines are performed by using time as an intermediate variable instead of voltage or current so substantial energy is saved.

[0030] Thus both types of converters benefit from reduced power consumption due to the fact that the circuit blocks of which are designed for half the resolution and

accuracy of the final ADC. Further, as some of the components are shared by the two converters, it reduces the overall size.

[0031] **FIGs. 3A to 3D** illustrate the first step of the ULPII-ADC in accordance with one embodiment of the present invention. The successive approximation algorithm is further carried in two phases: a sampling phase and a bit cycling phase.

[0032] As shown in **FIG. 3A**, the sampling phase is carried out by having an analogue input V_{IN} sampled through the bottom plates of the capacitor array, when the top plate nodes are switched to $V_{REF} = V_{dd}$. As shown in **FIG. 3B**, the bottom plates of the capacitor array are then switched to V_{GND}, with the top plates disconnected, i.e. V_{DAC} is a floating node. Through charge conservation, top plate node voltage VDAC becomes $V_{REF} - V_{IN}$.

[0033] The successive approximation goes on to the bit cycling phase, where the register in SAR Logic block is first set to midscale, setting the MSB to '1' and all other bits to '0'. The bottom plate of the largest capacitor is switched to V_{REF}, redistributing the charge on the top plates of the capacitors driving V_{DAC} to $-V_{IN} + V_{REF}/2$ as shown in **FIG. 3C**. V_{IN} is then compared to V_{DAC}, if V_{IN} is greater than V_{DAC} or $V_{DAC} < 0$, comparator output is logic '1' and the MSB of the M-bit register remains at 1. Conversely, if V_{IN} is less than V_{DAC} or $V_{DAC} > 0$, the comparator output is logic '0' and the MSB of the register is cleared to 0. The SAR control logic then moves to the next bit down, forces that bit high, and does another comparison as above. The sequence continues all the way down to the least significant bit (LSB). Once this is done, the conversion is completed, and the M-bit digital word is available in the register. **FIG. 3D** exemplifies a switch arrangement when the SA-ADC is completed.

[0034] Through the SA-DAC illustrates above, the top plate of the capacitor array would have residue voltage V_{RES_SAR}. The V_{RES_SAR} can be derived by the following:

[0035] $V_{RES\_SAR} = -V_{IN} + V_{REF} (B_1/2 + B_2/4 + ... + B_M/2M)$

[0036] wherein $B_1, B_2, \ldots B_N$ has value +/- 1, M is the resolution.

[0037] Subsequently, the analog residue voltage, V_{RES_SAR} is resolved in the second-step by using the time based integrating cyclic ADC, which will also be carrying out in two-phases, a MSB phase and a residue quantization phase. During the MSB phase as shown in FIG. 4A, the residue voltage is initially transferred (i.e. sampled and held) onto capacitor C_{IN} by charging the capacitor C_{IN} with an input current I_{IN} until the voltage equals to V_{RES_SAR} ($V_{RES\_SAR} = V_{DAC}$). Once the capacitor C_{IN} is charged up, C_{REF} is charged with I_{REF} until its voltage is also equals to V_{RES_SAR} ($V_{RES\_SAR} = V_{DAC}$) as shown in FIG. 4A. The operation can be done by the comparator **202**. In this charging operation, the ratio $I_{IN}/I_{REF} = T_{REF}/T_{CLK}$ is to be obtained, wherein the T_{REF} is the time required to charge C_{REF} up to the voltage V_{RES_SAR} and I_{IN} is the current required for charging capacitor C_{IN}. Further, the I_{IN} must be less than $4I_{REF}$ for conversion efficiency. A 2-bit counter can be used for counting the number of clock edges during T_{REF}, so that the input current I_{REF} can be quantized to within two bits of the reference current I_{IN}. A residual time, T_{RES}, defined as time remaining beyond the last clock edge as shown in FIG. 4B is formed at the end of the T_{REF}. At the end of the MSB phase, the comparator's output goes high. The MSB phase signals as a state-machine to reset both capacitors C_{IN} and C_{REF} to zero and to rearrange the analog circuitry such that I_{REF} is now redirected to charge C_{IN}.

[0038] During the residue quantization phase, T_{RES} is obtained by subtracting the quantized signal from T_{REF}. Subtraction of intermediate quantization results is automatic in the algorithm if integer number of quantization clock cycles that have already passed (or not) are ignored and the residual time signal is always referenced to the next neighboring clock edge.

[0039] If T_{RESB} is defined as the time from end of T_{REF} up to the next clock edge, then $T_{RESB} = T_{CLK} - T_{RES}$

[0040] Quantizing T_{RESB} is then equivalent to quantizing T_{RES}: quantizing x and (1 – x) are equivalent as long as we can digitally compensate for referencing with respect to 1 rather than with respect to 0.

[0041] The time T_{RESB} can be converted into a voltage by integrating C_{IN} with I_{REF} from the end of T_{REF} up to the next clock edge. Then, the voltage on C_{IN} is

[0042] $$V_{C1} = (I_{REF} \times T_{RESB}) / C_{IN} \quad (2)$$

[0043] I_{REF}/C_{IN} is time-to-voltage conversion gain, and accordingly the conversion of T_{RESB} to V_{C1} as time-to-voltage conversion. At this time, I_{REF} is switched over to charge C_{REF} until the voltage on C_{REF} is equal to V_{C1}. The latter comparison can be achieved by using the same comparator used during the MSB phase. As soon as the two voltages are equal, the voltage on capacitor C_{IN} is reset to zero, and the same charge integration on C_{IN} is repeated. At the end of this comparison, the T_{RESB} may be amplified by two. By counting the number of clock edges seen within $2T_{RESB}$, the number of clock edges seen within one bit of T_{CLK} can be quantized accordingly.

[0044] After $2T_{RESB}$ is quantized, it is subtracted from the un-quantized value to produce a new residue for successive conversions. To do so, the "subtraction" routine is repeated by encoding the time from the end of $2T_{RESB}$ to the next clock edge as a new residue. At the end of the amplification stage, both capacitors C_{IN} and C_{REF} are reset to zero, and the state-machine reconfigures the analog circuitry such that I_{REF} is now set to charge C_{REF}. The elements are now in place to repeat the previous subtraction and amplification processes except that the time-to-voltage conversions are carrying out on C_{REF} and voltage-to-time conversions are carrying out using C_{IN}. Each successive subtraction-and-amplification process recursively yields one more bit through the hybrid ADC according to the present invention.

[0045] While specific embodiments have been described and illustrated, it is understood that many changes, modifications, variations and combinations thereof could be made to the present invention without departing from the scope of the invention.

Claims

1. A hybrid analogue-to-digital converter (ADC) for converting comprising:

a successive approximation analogue-to-digital converter (SAR-ADC); and

a time based integrating and cyclic analogue-to-digital converter (CYC-ADC) integrated with the SAR-ADC, wherein

an input analogue signal is processed through the SAR-ADC to output a first output constituting most significant bits (MSBs) of an digital output signal and a residue signal, the residue signal is further processed through the CYC-ADC to output a second output constituting the least significant bits (LSBs).

2. The hybrid ADC according to claim 1, wherein the SAR-ADC further comprises a comparator, a capacitor array, a successive approximation register (SAR) and a digital to analog converter (DAC), and the CYC-ADC further comprises an analogue switch network, a pair of capacitor, a state-machine, a reference current generator, wherein the CYC-ADC is coupled to share the comparator with the SAR-ADC.

3. The hybrid ADC according to claim 2, wherein the DAC of the SAR-ADC is coupled with the SAR and output analogue signal to the comparator.

4. The hybrid ADC according to claim 2, wherein the pair of capacitors is adapted for performing signal integrating over time; the network of switches for directing different charging currents to different capacitors; the state-machine to generate control signals for the analogue switch network and the comparator; an output register to store converted bits.

5. The hybrid ADC according to claim 1, wherein the SAR-ADC is adapted to process the analogue input signal to acquire first M-bit MSBs of the output digital signal and the residue signal is processed through the CYC-ADC to acquire the remaining LSBs.

6. The hybrid ADC according to claim 1, wherein the hybrid ADC is adapted for ultra-low power high resolution analogue-to-digital conversion.

7. A method of converting an analogue input signal to a digital output signal, the method comprising:

converting the analogue input signal through a successive approximation to output a first output constituting part of the total bits of the digital output signal and a residue signal;

processing the residue signal through a time-based integrating cyclic analog to digital conversion to output a second output constituting the remaining bits of the digital output signal; and

combining the first output and the second output to output the digital output signal.

8. The method according to claim 7, further comprising

identifying the first output as the most significant bits of the digital output signal and

identifying the second output as the least significant bits of the digital output signal; and

adding the first output to the second output to output the digital output signal.

9. The method according to claim 8, wherein adding the first output and the second output further comprises shifting bits of the first output such the first output constitute the most significant bits of the second portion of the conversion result are added to one or more least significant bits of the digital output signal.

10. The method of claim 7, wherein converting the analogue input signal through the successive approximation further include performing a number of analog to digital conversion iterations, the number of analog to digital conversion iterations is less than the number of bits in the digital output signal.

11. The method of claim 7, wherein processing the residue signal through the time-based integrating cyclic conversion includes performing a number of analog to digital conversion iterations, wherein the number of analog to digital conversion iterations is less than the number of bits in the digital output signal.

12. The method of claim 7, wherein the successive approximation produces a single bit of resolution for each iteration.

13. The method of claim 7, wherein the time based integrating cyclic based analog to digital conversion produces two bits of resolution during the first iteration and a single bit of resolution for subsequent iterations.

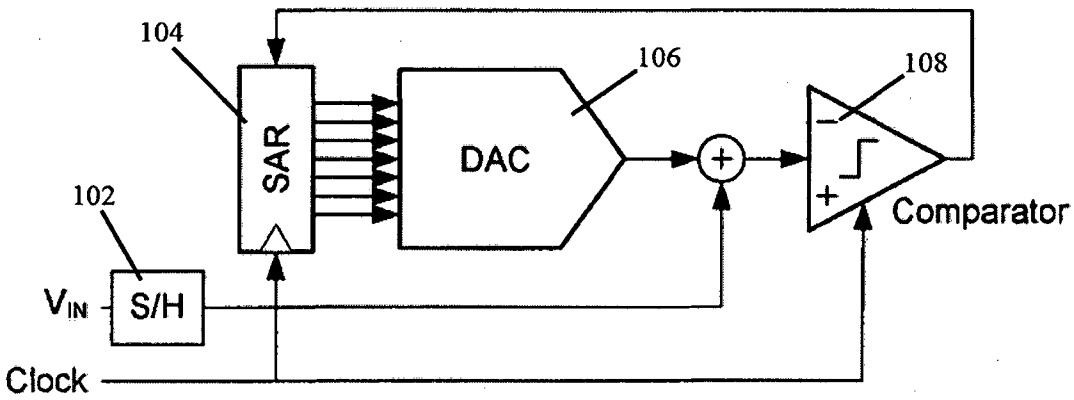


FIG. 1 (Prior Art)

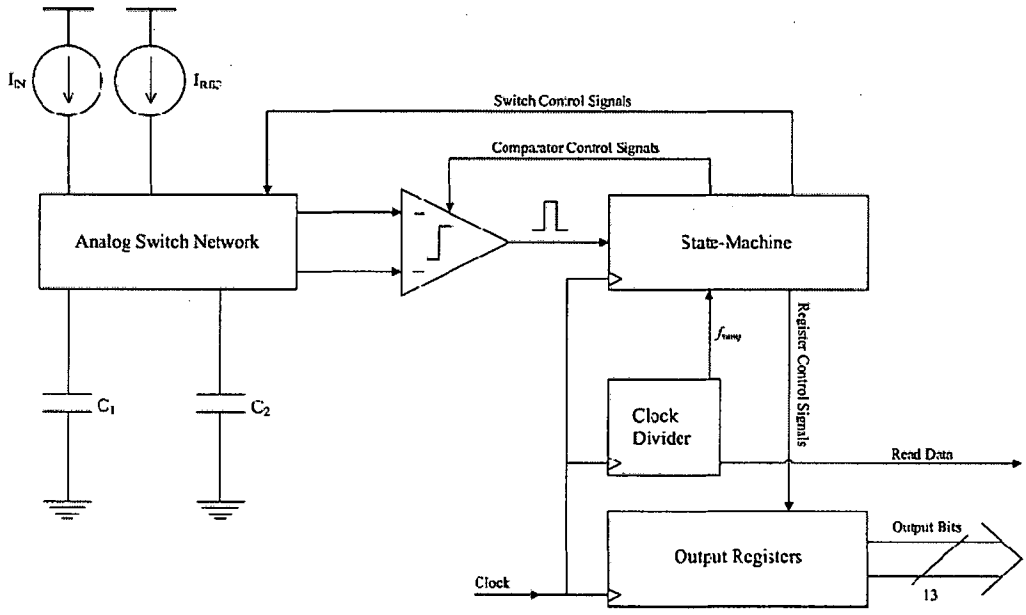


FIG. 1B (Prior Art)

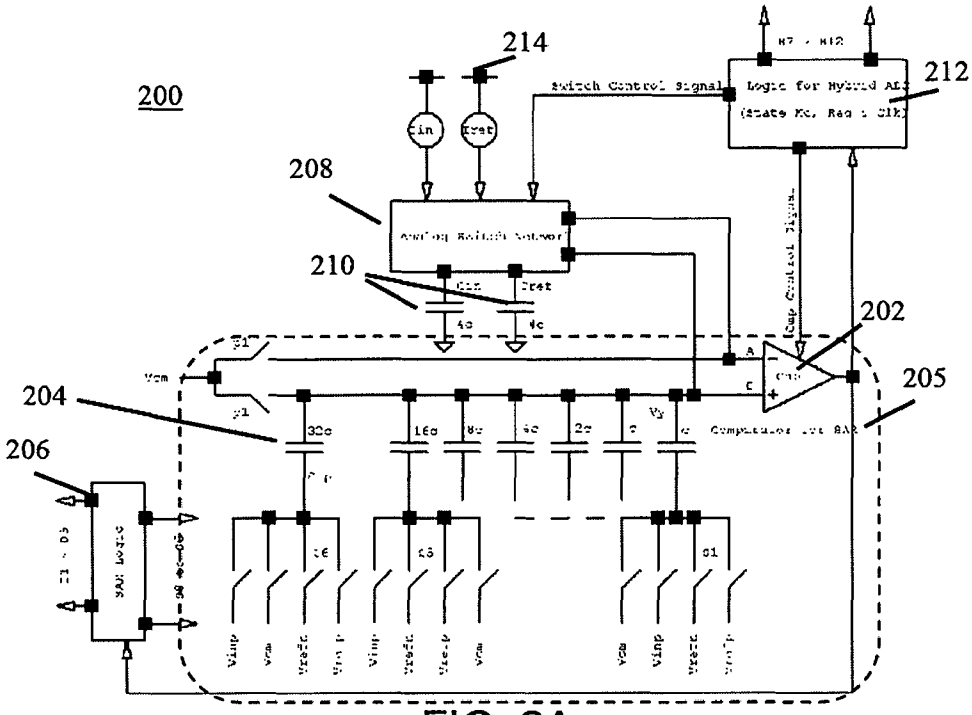

200
214
212
208
210
202
205
204
206

FIG. 2A

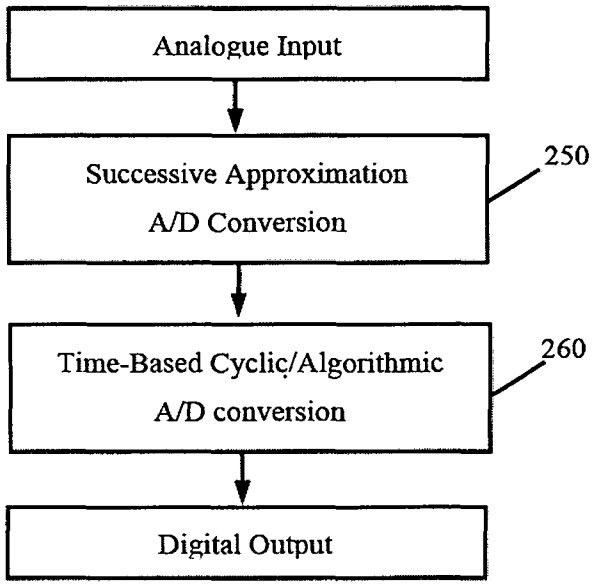

Analogue Input
Successive Approximation
A/D Conversion
250
Time-Based Cyclic/Algorithmic
A/D conversion
260
Digital Output

FIG. 2B

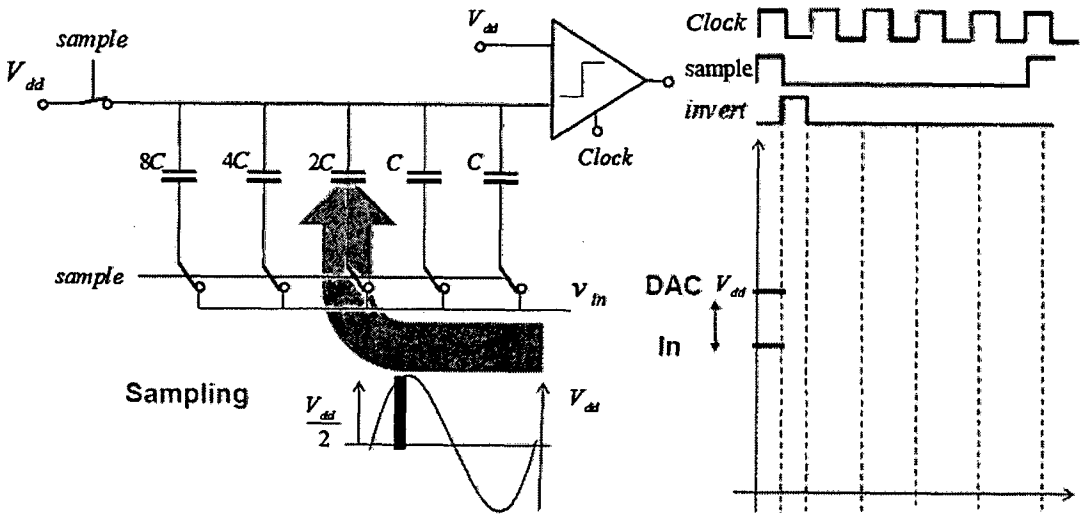

sample
V_{dd}
8C
4C
2C
C
C
Clock
sample
v_{in}
Sampling
$\frac{V_{dd}}{2}$
V_{dd}
Clock
sample
invert
DAC V_{dd}
In

FIG. 3A

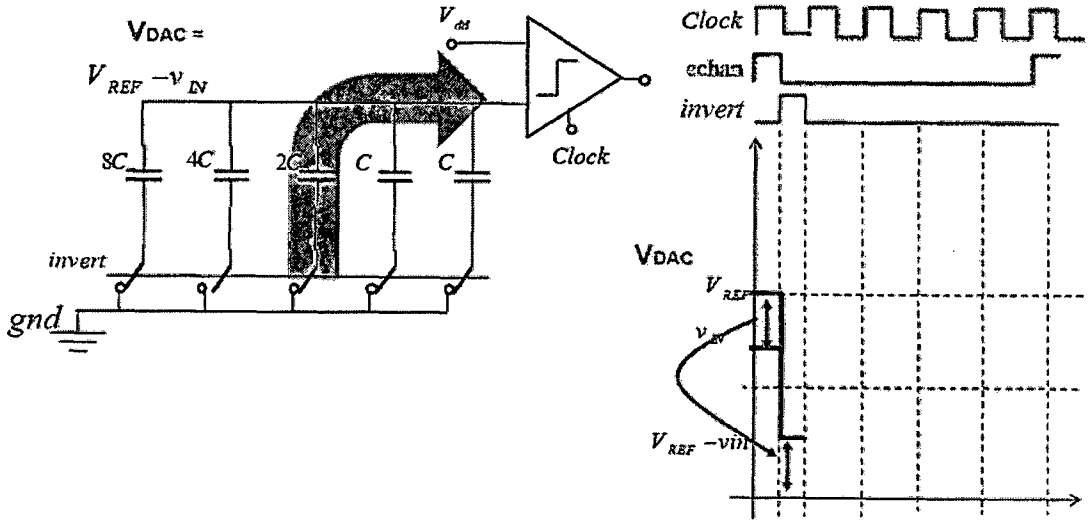

VDAC =
$V_{REF} - v_{IN}$
V_{dd}
8C
4C
2C
C
C
Clock
invert
gnd
Clock
echan
invert
VDAC
V_{REF}
v_{IN}
$V_{REF} - vin$

FIG. 3B

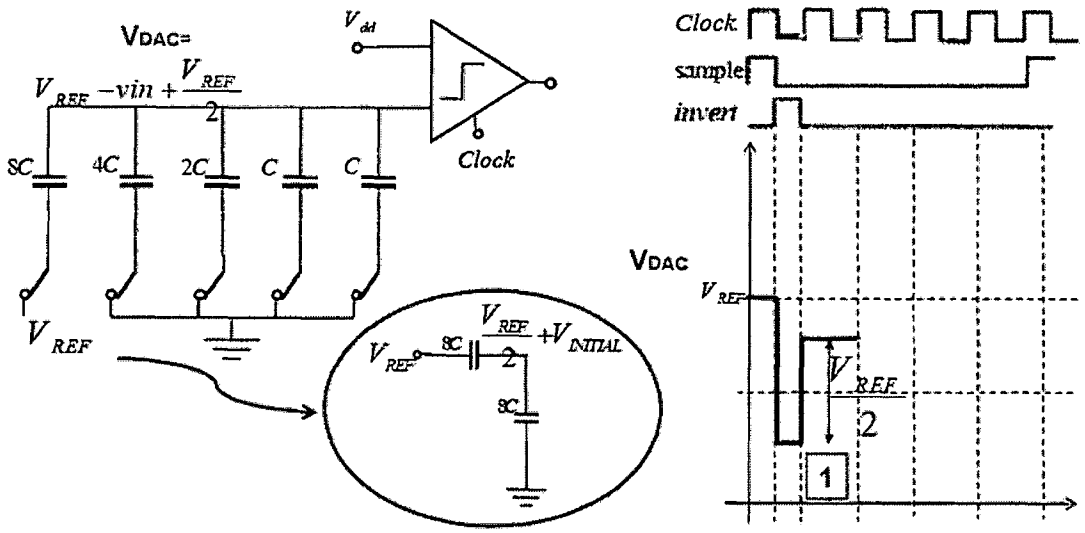
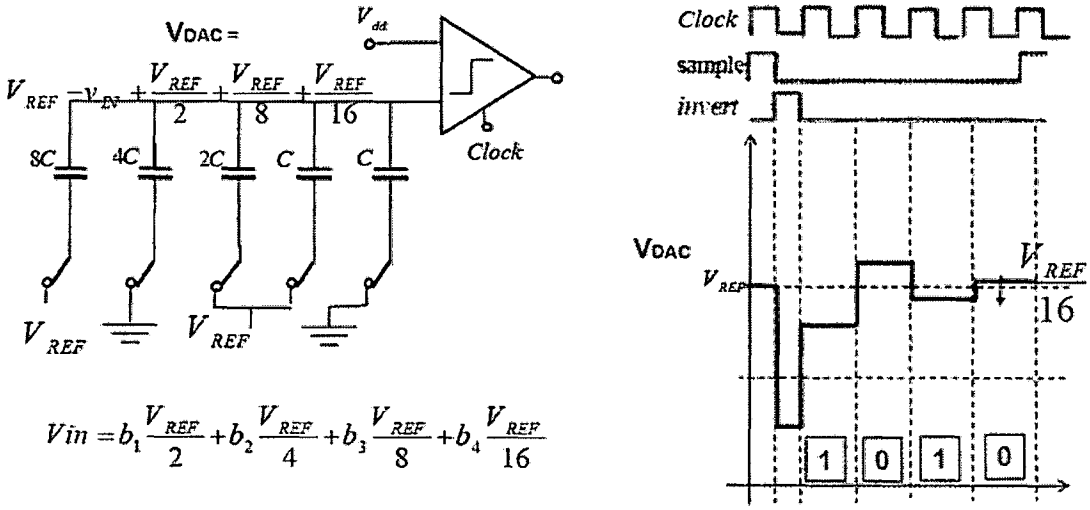


FIG. 3C



$$Vin = b_1 \frac{V_{REF}}{2} + b_2 \frac{V_{REF}}{4} + b_3 \frac{V_{REF}}{8} + b_4 \frac{V_{REF}}{16}$$

FIG. 3D

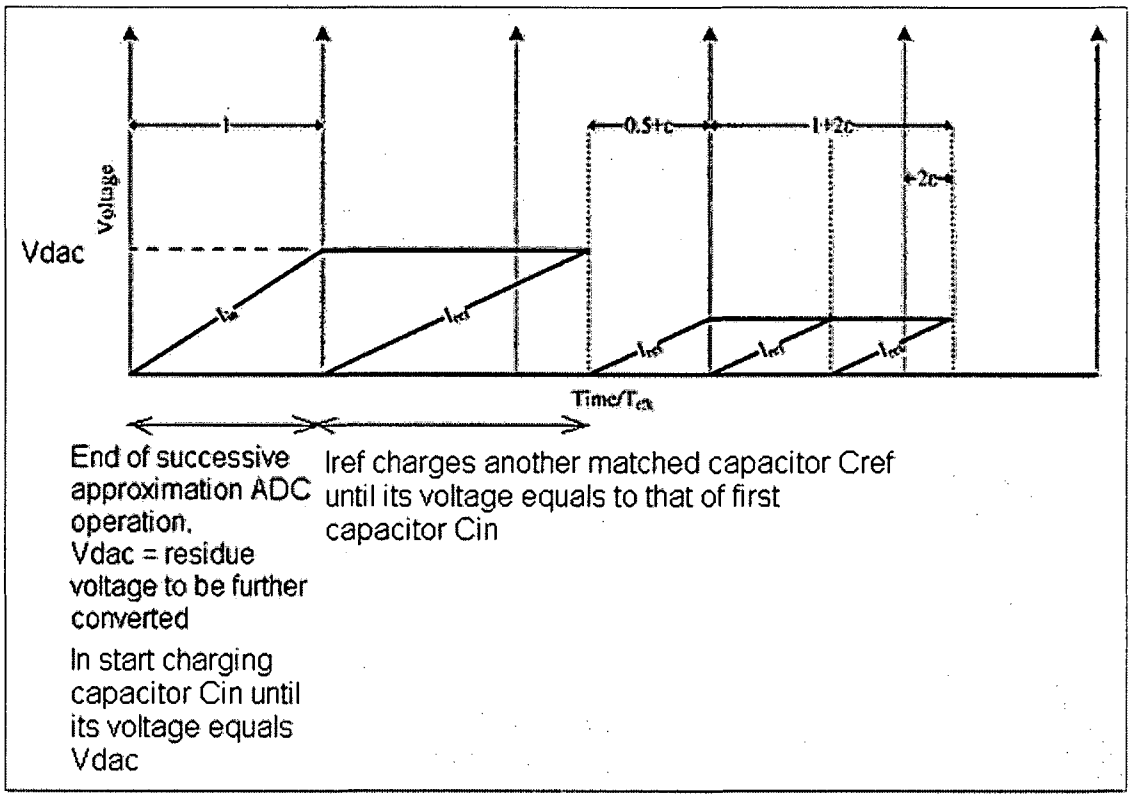

Voltage
Vdac
1
0.5+c
1+2c
2c
Time/Tclk
End of successive approximation ADC operation. Vdac = residue voltage to be further converted
In start charging capacitor Cin until its voltage equals Vdac
Iref charges another matched capacitor Cref until its voltage equals to that of first capacitor Cin

FIG. 4A

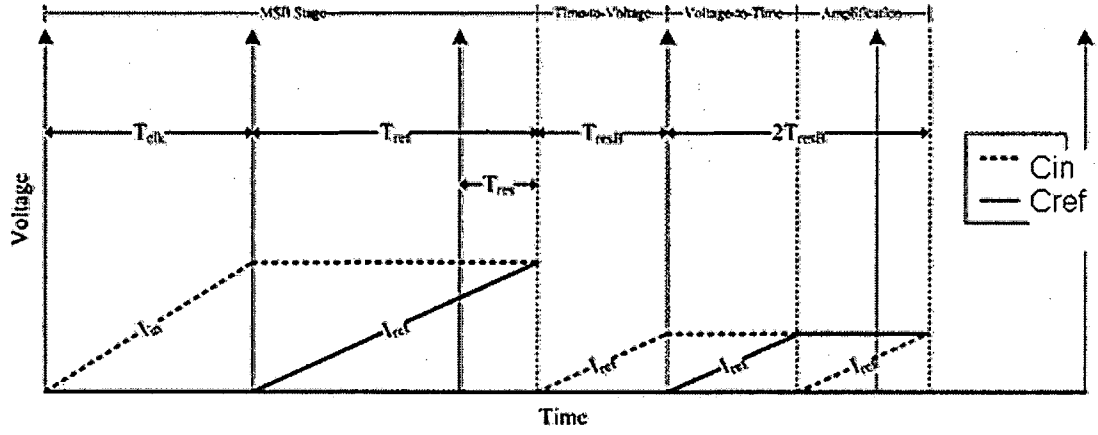

MSB Stage
Time-to-Voltage
Voltage-to-Time
Amplification
Tclk
Tref
Tres
Tres/8
2Tres/8
Voltage
Time
Cin
Cref

FIG. 4B

INTERNATIONAL SEARCH REPORT

International application No
PCT/MY2012/000143

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03M1/14
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data, COMPENDEX, INSPEC, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2008/291072 A1 (SANO TAKAFUMI [JP]) 27 November 2008 (2008-11-27) figures 2,3,7 paragraph [0048] - paragraph [0070] -----	1-13
X	XIANG FANG ET AL: "CMOS 12 bits 50kS/s micropower SAR and dual-slope hybrid ADC", CIRCUITS AND SYSTEMS, 2009. MWSCAS '09. 52ND IEEE INTERNATIONAL MIDWEST SYMPOSIUM ON, IEEE, PISCATAWAY, NJ, USA, 2 August 2009 (2009-08-02), pages 180-183, XP031528186, ISBN: 978-1-4244-4479-3 abstract; figure 1 Section II, last 7 lines Section III.A, III.B, III.D -----	1-13

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

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"O" document referring to an oral disclosure, use, exhibition or other means

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
27 November 2012	06/12/2012

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Galardi, Leonardo

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/MY2012/000143

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2008291072 A1	27-11-2008	NONE	