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GB 1531528 EP A 0066084
GB 1528100 EP A 0032957
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G4A

(54) Method and System of Ensuring Integrity of Data in an Electronic Memory

(57) Upon recognition that some memory cells in a memory may become defective, the initial data together with the initial address (N_i) are stored at a replacement address (N_i'). A register, further, stores those addresses (N_i) which relate to memory cells or locations which have become defective. When a computer (1) addresses data, a comparator (9) compares the called-for address with the address stored in the defective cell register (10) and, upon equality, routes the data request to the replacement address (N_i') which may be a complete address or a specific location related to a reference address, such as a terminal portion of an auxiliary memory, the main memory, or the like. A warning signal can be given when most, but not yet all, auxiliary memory locations are occupied.

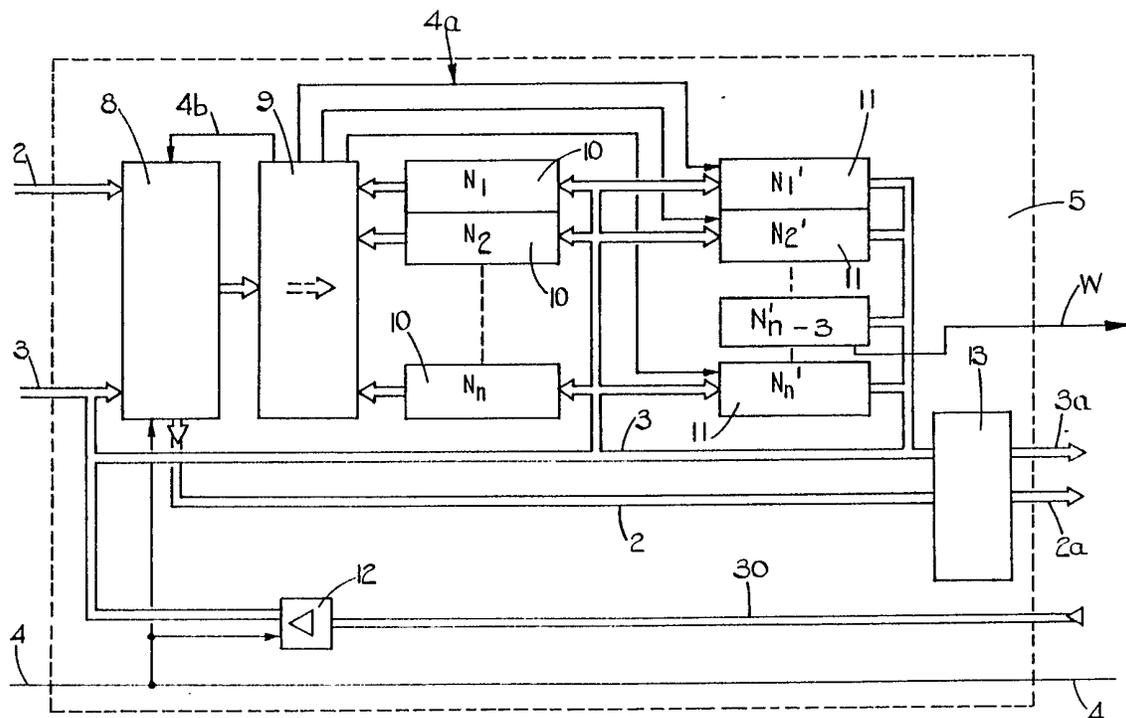


FIG.3.

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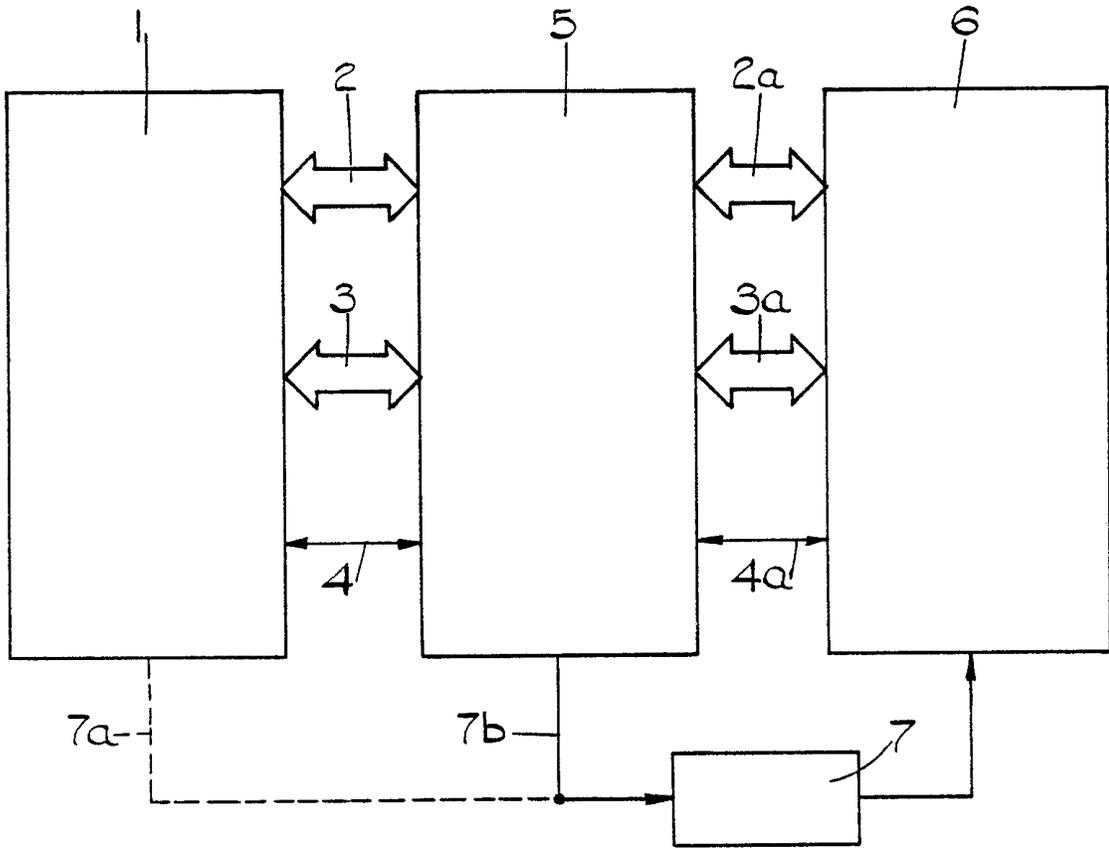
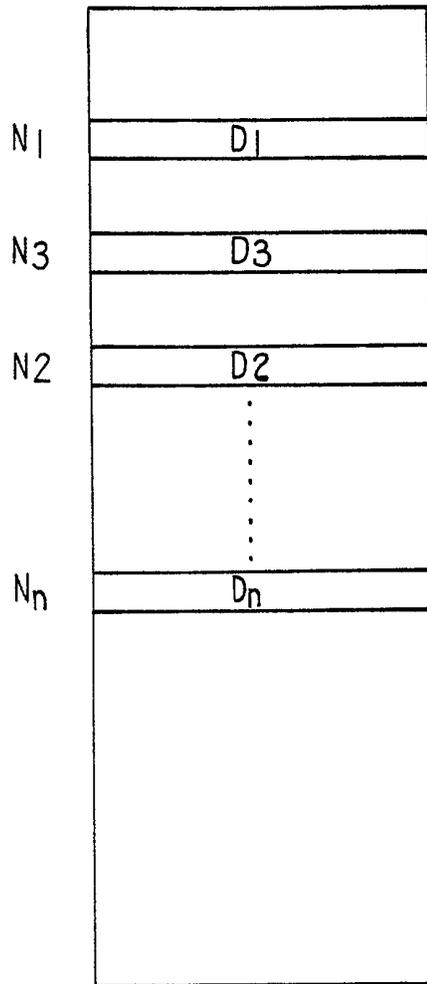
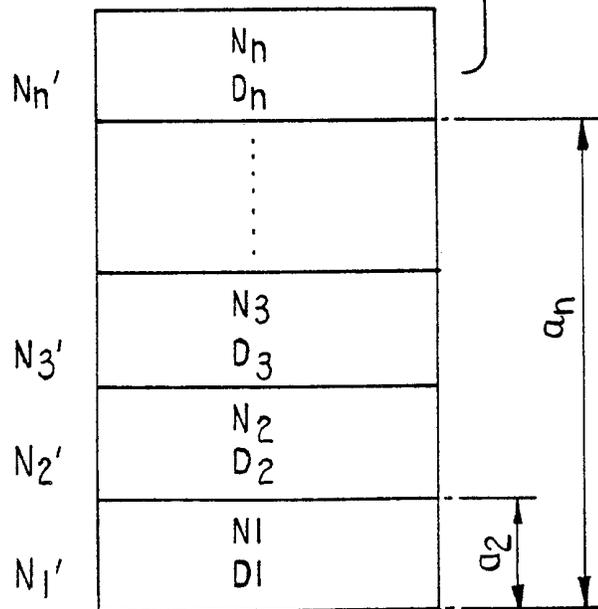


FIG. 1.

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} FIG.2.



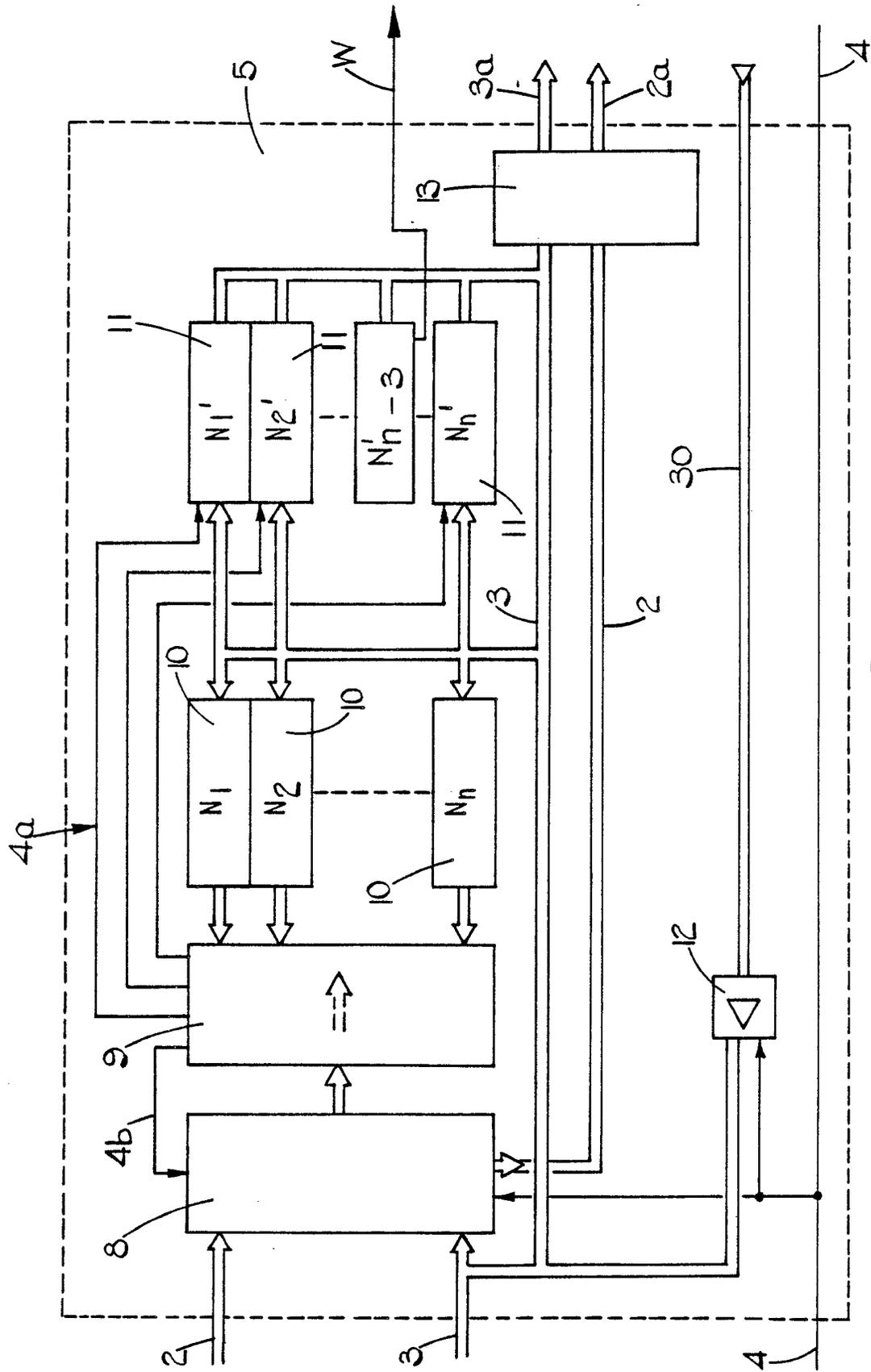


FIG.3.

SPECIFICATION

Method and System of Ensuring Integrity of Data in an Electronic Memory

The present invention relates to a method and
 5 system of ensuring integrity of data in an
 electronic memory and more particularly to
 electronic memory elements or units which are
 installed on-board an automotive vehicle to store
 information and data relating to the operating
 10 characteristics of the vehicle engine for example
 data relating to ignition timing and the like.

Various types of memory units which include
 memory elements or cells use erasable
 programmable read-only memories (EPROMs).
 15 Such memory elements or cells may be formed by
 two serially connected field effect transistors
 (FETs), in which one FET acts as a constant
 current source, and the other changes its
 resistance under control of pulses applied to the
 20 gate thereof. Read-out of the stored data, which
 are represented by either high or low resistance
 values of the controlled FET, and hence the
 voltage thereacross, is obtained by determining
 the voltage level at the junction between the main
 25 current carrying paths of the two serially
 connected FETs.

It is known that memory cells of this type can
 change their data storage characteristics due to
 various external influences which particularly
 30 include temperature, incidence of light,
 penetration of moisture or humidity, and the like.
 German Offenlegungsschrift DE—OS 28 53 925
 described such changes. Change in the
 characteristics of operation of the EPROM may
 35 be caused by external effects which detract from
 the insulating capability of the gate of the FET, so
 that charge carriers may leak off from the gate.
 The opposite effect may, however, occur, namely
 that charge carriers can be applied to the gate of a
 40 storage cell, for example because insulation to the
 surrounding area is defective, or energy is being
 applied thereto, for example by leakage of light.
 The change in charge state of the gate electrode
 usually is not abrupt, but rather is a gradual, slow
 45 change; yet after some time, the charge will be
 lost.

It has previously been proposed to avoid loss of
 charge on an EPROM by refreshing the data
 stored therein. The on-board control computer for
 50 a motor vehicle, for example, can be so arranged
 that a refreshing circuit reprograms the EPROMs
 of the memory at uniform intervals. This method
 can be used, however, only if the memory
 cells are still at least of such integrity that their
 55 original data can be read out, for reprogramming
 or refreshing the data therein. Refreshing the data
 in a memory cell of course will not lead to the
 desired result if the cell itself is defective, and the
 loss of the data is not caused by external
 60 influences.

Loss of data in a memory can be avoided by
 providing redundant storage. It is, for example,
 possible to store all data twice in a memory of
 sufficiently large storage capacity and then

65 provide comparisons or subtractions or summing
 of the data stored in the respective memories, and
 then, with a test program, determining which set
 of data in the two memories is in order, and which
 may have been stored in a defective manner.

70 The requirement of memory capacity in such
 units is, however, high, which substantially
 increases the price of the electronic equipment,
 contributes to complexity, which is another cause
 of possible malfunction, and requires additional
 75 space and auxiliary equipment.

It is an object to provide a method and system
 in which the integrity of data stored in electronic
 memories, particularly in EPROMs of
 the multiple field effect transistor (FET) type, can
 80 be ensured, so that the data will always be
 available, correctly, for processing in a
 computer, and especially in an on-board
 computer of an automotive vehicle.

Briefly, it is suspected that a specific data cell
 85 has a tendency to become defective, the original
 data, together with the original address, are
 stored in an auxiliary memory cell, or a
 replacement memory which may have only a
 substantially smaller number of memory
 90 addresses and locations than the overall memory
 itself, together with a replacement address.

In accordance with a feature of the invention,
 the original address is addressed by the computer,
 and a determination is made if the original
 95 address stores data subject to malfunction of the
 memory; if so, the data are then addressed with
 reference to the original address in an auxiliary
 memory location.

In accordance with a feature of the invention, a
 100 memory correction unit is provided, located
 between the computer and a memory unit, the
 memory correction unit including a comparator in
 which addresses which are supplied by the
 computer are compared with the addresses
 105 stored therein, the addresses stored in the
 memory correction unit, of course, being those
 which relate to defective memory cells. If
 the comparator indicates equality—in other
 words, that an addressed memory location is in a
 110 defective storage cell—a replacement or auxiliary
 address then will be addressed.

The method and system has the advantage
 that only the data on those addresses which
 characterize data cells which are or may become
 115 defective need be stored in a replacement or
 auxiliary address, together with the original
 address. Usually, only a few memory cells of a
 memory unit will be defective; thus, it is only
 necessary to provide only so many replacement or
 120 auxiliary cells at respective replacement or
 auxiliary addresses which, reasonably, may be
 required to replace possibly defective cells or cells
 which become defective in course of time.
 Consequently, only a comparatively small number
 125 of additional memory cells are required in order to
 ensure operating reliability and storage of the
 required data and programs for a computer, and
 especially for an on-board vehicular type
 computer.

In accordance with a preferred feature of the invention, it is desirable to so arrange the auxiliary or replacement cells that, if a predetermined number thereof, which should be somewhat less than the overall number available, is utilized to store data from defective cells, a warning signal or indicating signal is supplied so that the operator or user is warned that the replacement capability of memory cells is about to become exhausted, so that replacement of the entire memory can be considered. Some arrangements thus are available which permit recognition that the original memory contains a larger number of defective cells, or cells which tend to become defective.

In accordance with a further and preferred feature of the invention, the replacement addresses can be stored in a correction memory which forms a part of the program and/or data memory of the computer system. This arrangement avoids the requirement of adding additional memory units or structures. The correction memory may be part of an existing memory module or the like, that is, an existing memory in which a portion of the available memory addresses is reserved for correction or replacement. The system is highly versatile and, in dependence on the system conception, the correction memory can be combined with the memory correction unit, or can be constructed as a separate memory element. The replacement address, preferably, is correlated in the correction memory with the original address. This permits immediate addressing of the data if the program of the original data calls for an address of the memory. Upon addressing of the original address, the replacement address will then be automatically and immediately addressed.

For fast and easy addressing of the replacement memory, the replacement addresses preferably are given with respect to their distance from the beginning or terminal or final address of the correction memory. Thus, and by correlating the replacement cells with the initial and final addresses, memory locations in the replacement memory register unit can be saved, since it is then only necessary to provide an indication of the difference of the address from a fixed end point. This decreases the number of the addressing bits for each address, since it is not necessary to provide a full second replacement address. In accordance with another and desirable feature, the data in the memory correction unit can be so placed that they can be addressed immediately adjacent the original address.

The system preferably includes a memory correction unit which has a comparator in which the called-for address is compared with those addresses which have been recognized to relate to defective cells or cells which tend to become defective. Upon equality, a signal is generated which can be termed a "defect" or "check replacement address" signal. This is an easily constructed circuit from which it can be recognized if, when data from a particular address

are wanted, the data are stored in a properly operating cell or if a replacement or auxiliary address is to be addressed in order to obtain the correct data.

The memory correction unit, preferably, includes a register in which the addresses and data can be stored, and, in accordance with a feature of the invention, so arranged that the memory locations can be related to the initial or final addresses of the memory. The register is preferably so controllable that addresses can be retained and/or exchanged, which arrangement permits easy addressing of the memory arrangement by a microprocessor over the memory correction unit.

Recognition of whether a memory cell is defective or tends to become defective, so that the data thereof can be stored in a properly operating cell before the first cell has become totally inoperative, can be done in accordance with the disclosure of German Offenlegungsschrift DE—OS 28 53 925, the disclosure of which is hereby incorporated by reference. Briefly, as disclosed in this referenced application, a trend of the particular cell to become defective can be determined by reading-out the data from the cell, and storing the data; and then changing the read-out or recall voltage being applied to the respective memory cell, either in an increasing or decreasing direction, or sequentially increasing and decreasing, and comparing the data retrieved therefrom when the read-out voltage was at design level, or varied. If the data do not match, a trend of the cell to become defective is thereby recognised before the data from the particular cell actually have been altered over those that the cell should have contained. Thus, that particular cell should then be labelled as one from which data are to be stored at an auxiliary address, and the particular cell considered "defective". Thus, the integrity of the original data within the overall memory unit is retained, unless the number of cells which have a tendency to become defective, by leakage of charge carriers or accumulation of undesired charge carriers, approaches the capacity limit of the replacement cells.

The invention will now be described further by way of example with reference to the accompanying drawings in which:—

Fig. 1 is a schematic representation of the system;

Fig. 2 is a diagram illustrating the organization of data in a memory; and

Fig. 3 is a detailed diagram of the memory correction unit forming part of the system.

A computer 1 (Fig. 1) is connected over a data bus 2 and an address bus 3 and over a control bus 4 with a memory correction unit 5. The memory correction unit 5 is connected over further data, address, and control busses 2a, 3a, 4a with the main memory 6 of the overall computer system. Solid-state memory elements in which the memory content can be programmed are particularly suitable for the memory unit 6. Such

memory units are, for example, programmable read-only memories (PROMs), erasable programmable read-only memories (EPROMs), and electrically erasable programmable read-only memories (EEPROMs) or E²PROMs) made, for example, by the company INTEL (RTM) under Nos. 2316, 2716, 3636. A programming unit 7 is connected to the memory 6 and to the memory correction unit 5. The programming unit 7 can be controlled from the computer, either directly as shown by broken-line connection *a*, or through the control bus 4 and the memory correction unit 5, as shown by solid line *7b*. The programming unit 7 enters the respective data at the replacement or auxiliary addresses. The memory correction unit 5 is an element between the address counter, normally contained in the computer 1 and the memory 6 which stores both the program as well as the data. The memory correction unit 5 can, physically, form part of the computer unit 1, or part of the memory unit 6, or may be a separate element. The drawing of Fig. 1 shows the memory correction unit as a separate element for convenience and for ease of explanation of the operation. Of course, the computer 1, which may be a microprocessor, memory correction unit 5, as well as the solid-state memory, may be retained on one semiconductor chip.

A circuit arrangement, which is described in detail in German Offenlegungsschrift No. DE—OS 28 53 925, can be used to recognize a trend towards defects in the memory cells of memory 6, that is, to predict that data may be lost in the future, before such loss has actually occurred. Other systems to recognize errors or a trend towards errors, and to localize the errors, can be used.

Referring to Fig. 2, the correct information $D_1, D_2, D_3, \dots, D_n$, which may be termed, collectively, information D_i , is stored at original addresses $N_1, N_2, N_3, \dots, N_n$, collectively referred to as initial or correct address N_i . Upon recognition of an error, a replacement initial address N_i' which, specifically, is formed by the addresses N_1', N_2', \dots, N_n' , together with the original or initial address N_i . To load the initial data, together with the initial address, for example data D_1 and initial address N_1 at an auxiliary memory location N_1' , the additional programming unit 7 is used. Such additional programming units 7 are known, and may be constructed, for example, as described in DE—OS 28 53 925; other arrangements also may be used, as described, for example, in the relevant technical literature.

The correction memory locations may be placed in a separate correction memory, or can be placed as part of the program memory, the data memory, or any other suitable and convenient physical unit. The correction memory, thus can be a portion of the memory unit, with memory cells which do not exhibit a defect or a trend towards defective operation.

Fig. 2 illustrates a suitable form of organization of the memory 6. The control program with data

is stored in the upper portion of the memory 6. In a further portion of the memory 6, addresses N_1' to N_n' are located; the replacement addresses N_i' will contain not only the data D_1 to D_n , but also the original or initial addresses N_1 to N_n . As far as address locations are concerned, the correction memory will have fewer storage addresses and storage places than the program and data memory; the difference in storage locations may be substantial. In accordance with a feature of the invention, a method and system is provided to prevent overflow of data in the correction memory upon introduction of new information thereto. The processor or computer 1 is arranged to determine as the correction memory or correction memory addresses are being occupied since, when they are all occupied, replacement of the memory unit 6 will be required.

Computer systems in which repetitively recurring events arise, for example reset, start of a rerun of a program and the like, the initial addresses N_i transferred to the correction memory when a particular address is found to have a trend towards becoming defective are stored in special register provided for the initial addresses, and compared by the address which is generated by the computer 1. Upon coincidence between the addresses supplied by the computer 1 and the addresses stored in the correction register, the data are retrieved not from the original or initial address N_i , but rather from the auxiliary or replacement address N_i' . The address N_i' can be so addressed that, rather than transferring the initial address N_i , the address N_i' is transferred to the memory 6. In another alternative, the relative distance of the correction address N_i' from a reference may be given, for example from either one of the end or terminal addresses available in the memory 6. Providing a difference address, that is, the distance from a reference point, has the advantage that storage capacity is saved since a distance can be defined by a lesser number of bits than the complete address. Fig. 2 shows two examples in which the distance a_2 and the distance a_n , respectively, are shown. Addressing the replacement address thus is possible in various modes:

For one, the replacement address N_i' can be given completely; for another, the distance to a reference, and especially to the beginning or end of the memory locations of the correction memory are given. This, however, requires that the base or reference address additionally is stored, if the program memory and the data memory as well as the correction formed one structural unit.

Memory correction, with reference to Fig. 3: The data bus 2, address bus 3, and control bus 4 are shown schematically. These buses are connected to the memory correction unit 5, both at its input as well as from its output. The control for the programming unit 7 has been omitted for clarity; its arrangement is well known in the art. The address bus 3 which comes from the computer 2 provides addresses to an input register 8. The addresses in the input register 8

are compared in a comparator 9 with the initial addresses N_i which are stored in the initial address register 10. The address register 10, forming the original address memory, stores only those addresses which relate to defective memory cells, or to cells which tend to become defective, as determined for example in accordance with the disclosure of the German Offenlegungsschrift DE—OS 28 53 925. If no comparison is indicated by comparator 9, that is, if the address supplied by address bus 3 does not have an equal address of a defective cell, the address line 3 is directly connected from the input register to the output register 13 for subsequent connection to the commanded address in the memory 6 on the output address line 3a. If, however, a correlation is established between an address in the register 10 and the address on bus 3 derived from processor 1, the address in the input 8 is blocked and, rather, a corresponding replacement address N_i' , stored in a register forming the replacement address memory 11, is connected to the output register 13. Control of the respective comparison, and either through switching of the address from bus 3, or switching of the replacement address from memory 11 is effected by control connecting lines 4a, 4b, which interconnect the register positions of the replacement address memory 11, the address comparator 9, and the input register 8. The data which are stored either in good cells forming the original address or in cells at the replacement address are read-out over a return data bus 30 through a buffer 12 and the data bus 3. Other read-out arrangements, for example connecting of the buffer 12 to the data bus 2, of course, can be used, in dependence on the system's concept. Control and timing are effected by suitable signals on the control bus 4.

The replacement address memory 11 may store either a complete address or an address with respect to a reference address. Storing data with respect to a reference requires, usually, a lesser number of addressing bits than storing a complete address. It requires, however, a computation section which reconstitutes a complete replacement address which includes the reference address as well as the particular location from the reference address.

A further possibility is this: The address register 11 may receive the data D_i directly, and in such arrangement, storing and providing a replacement address N_i' in the memory correction unit can be entirely eliminated. Upon placing the initial address N_i in the memory correction unit, then, the additional information D_i must also be placed therein. This provides for a very compact storage of replacement addresses, provided, however, the bits required for the data, that is, the set of data bits, is no longer than the address itself.

The system and method permits correction of data, as well as prevents loss of data. There is no overprogramming. It avoids the necessity of continuously and prophelactically refreshing memories which, as known, degrade upon

continuous re-programming. Thus, inherently perfectly operating memory structures may be abused by continuous re-programming. Such abuse is avoided by only selecting for exchange of addresses those cells in which a trend towards defective operation has been discovered. The requirement for redundancy in storage of memory locations is substantially reduced since, from experience, only a small portion of memory cells in an overall memory may become defective.

A warning signal can be generated, for example, by a replacement address memory 11 when all but three of the replacement addresses are occupied, as schematically shown by the fragmentary address memory N_{n-3}' , providing a warning signal over line W that only two more replacement memory locations are available.

CLAIMS

1. Method of ensuring the integrity of data in an electronic memory particularly including erasable programmable read-only memory elements (EPROMs) forming said memory unit, in case of incipient or actual malfunction of one or more data storage cells in the memory unit, in which the data are stored at auxiliary memory locations, comprising storing the original data together with the original address in the auxiliary memory cell or replacement memory location at a replacement address.

2. Method as claimed in claim 1, including the step of storing replacement addresses in a correction or replacement address memory.

3. Method as claimed in claim 2, including the step of storing the replacement addresses in a correction or replacement address memory section forming a portion of said memory unit.

4. Method as claimed in claim 1, including the step of generating a replacement address inherently characterising the replacement address of the auxiliary memory cell.

5. Method as claimed in claim 1, including the step of generating a replacement address with respect to a reference address or reference location of a replacement address memory unit.

6. Method as claimed in claim 5, in which said reference address is a terminal address of said correction memory unit.

7. Method of ensuring the integrity of data in an electronic memory particularly including erasable programmable read-only memory elements forming said memory unit, in case of incipient or actual malfunction of one or more data storage cells in the memory unit, in which the data are stored at auxiliary memory locations comprising the steps of re-storing the original data stored at an original address in an auxiliary memory at a replacement address together with the original address, addressing the original address, and determining if the original address contained data subject to malfunction of the memory and, if so, retrieving said data with reference to the original address in the auxiliary memory location.

8. Method as claimed in claim 1 or 7, including

the step of providing a warning signal if a predetermined number of replacement addresses have been occupied by data.

5 9. System to ensure the integrity of data in an electronic memory unit particularly including erasable programmable read-only memory elements (EPROMs) in case of incipient or actual malfunction of a data storage cell in the memory and having a computer connected to the electronic memory unit, and comprising a memory correction unit connected between the computer and the memory unit and including a comparator means for storing addresses of memory cells or memory locations which are subject to possible malfunction connected to the comparator; and a replacement address memory storing replacement addresses, said comparator comparing an address supplied thereto from the computer with the address in the possible malfunction address storage means, the comparator providing an output signal upon equality to supply data to the computer from a replacement address as determined by the replacement address memory.

25 10. System as claimed in claim 9, in which said memory correction unit comprises an input register and an output register for temporary storage of addresses or data.

30 11. System as claimed in claim 9, in which the means for storing addresses of possible malfunctioning memory cells or locations comprises a first register and in which the replacement address memory comprises a second register in the form of a complete address.

35 12. System as claimed in claim 9, in which the means for storing addresses of possible

malfunctioning memory cells or locations comprises a first register and the replacement address memory comprises a second register storing the distance of replacement addresses from a reference position or reference address.

40 13. System as claimed in claim 9, in which the means for storing addresses of possible malfunctioning memory cells or locations comprises a first register and the replacement address memory has sufficient memory locations for storing the original address and the data at a replacement address location.

45 14. System as claimed in claim 9, in which the means for storing addresses of possible malfunctioning memory cells or locations comprises a first register and the replacement address memory has sufficient memory locations for storing the original address and the data at adjacent replacement address locations.

50 15. System as claimed in claim 9, in which said comparator is connected to an input register and said replacement address memory is connected to an output register to respectively control one of said registers to change the address data as received to modified output address data in the output register for addressing of data in replacement addresses.

55 16. Method of ensuring the integrity of data in an electronic memory substantially as herein described with reference to and as illustrated in the accompanying drawings.

60 17. System to ensure the integrity of data in an electronic memory unit substantially as herein described with reference to and as illustrated in the accompanying drawings.