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(73) 가 가

1 1 1

(72) 가 가 가 1가 가

가 가 가 1가 가

(74)

:

(54)

( , , )

( )

가

" "

" "

가  
NCS

NRS + NCS C<sub>NRS</sub> 가

, NRS

1  
2  
3 ( )  
4 3 가 " "  
5 1 " " ( )  
6 1 " " ( )  
7 1 " " ( )  
8 1 " " ( )  
9 1 " " ( )  
10 2 " " ( )  
11 2 " " ( )  
12 2 " " ( )  
13 2 " " ( )  
14 2 " " ( )  
15 2 " " ( )  
16 " "  
17 " "  
18 M  
19 SR  
20 M  
21 SR  
22 20 21 " "  
23 " "  
24

25 ( )  
 26 25 RDTEST  
 27 25 FT  
 28 25 SRT  
 29 25 RESET  
 30 25  
 31 25  
 32 25  
 33 25 가 (NR=NC=2 )  
 34 33 BLOCK<sub>i</sub> (NR=NC=2 )  
 35 34 (SRAM ) M<sub>ij</sub>  
 36 35 (SRAM) M<sub>ijl</sub>  
 37 34 ( ) SR<sub>ik</sub>  
 38 33 ( ) TSR BLOCK  
 39 38 TCLK  
 40 38 TSR<sub>1</sub> TSR<sub>4</sub>  
 41 38 TSR<sub>5</sub>  
 42 25 ( )  
 43 42 ( ) BSR BLOCK  
 44 43 BCLK  
 45 43 BSR<sub>2</sub> BSR<sub>6</sub>  
 46 43 BSR<sub>1</sub>  
 47 42 ( ) DSR BLOCK  
 48 47 DCLK  
 49 47 DSR<sub>1</sub>

50 33 BLOCK1 .

51 33 BLOCK2 .

52 33 BLOCK3 .

53 33 BLOCK4 .

54 33 BLOCK5 .

55 33 BLOCK6 .

56 ( ) .

57 .

58 가 .

59 가 .

60 59 .

< >

11 :

12 :

13 :

14 :

15 : 가

16 :

17 :

,

,

(particle: , )가

가

,

,

.











(E)

NRS , 1 , NCS , , NRS+NCS  $C_{NRS}$  (NRS+NCS NRS ) ( , ) .

(F)

가 NRS , NRS  
 , 가 ,  
 , 가 NCS , NCS  
 , 가 ,

, NRS 가, NRS , NCS , ,

(G) , 가 , ,

1 , , ,

1 , , .

1 , , .

NRS , 1 가, , NRS+NCS  $C_{NRS}$  (NRS+NCS NRS ) ( , , NCS , )

1 , , .

1 , , .

1 가 1 , ,

1 , , .

, , 가, , , 가, ,

가 , , ,

가, , 가

가 NRS , NRS , 가

가 NCS , NCS , 가

가, NRS , NCS , , , , NRS ,

가

A.

가 ( ) 가

CPU 가 가 ( )

가 가 가

가

( ) 가

가 가

가<sup>1</sup> ( ) ( ) 가 ( )  
 가 ( ) 가<sup>2</sup> 가 ( )

( ) 가

( ) 가 가

( ) 가

가

가

B.

a.

( ) 가

(1 ( , ) ) ,

가

가

( )

( )

( , ) , ( ) 가가

3 , 4 3 4가

, 2 가 (R0, C0), (R1, C1) 가 , Rx , Cy , x, y

2

. 2

, R0, R1

. 2

C0, C1

, C1 R0 , .

, R1 C0 , .

b.

1 : , ( ) .

2 : 가 , 가 가

, 가 가 가

c.

3 : , 2 가 .

, 가 . ,

4 : ) , ( 가 ) , (

(가 ) ( 2 가 , 가 (

, 가 , 가 , (가 )

가 가 (가 ) 가 , ( 6).

가 ( 7). , 가 , (가 )

4 , ( ) ,

5 : ) , ( 가 ) , (

가 (가 ) ( , )

6 : NRS, NCS, NCS, 가 NRS, 가 NCS, (가 ) 가

7 : 가

d. 1 가 2 (NRS=2), 가 2 (NCS=2) R0, C0 Rn, Cn Rk (k=0 n) C0 Cn

1 5a 4 5b R0, C0 (1) 5b ( ) 가 가 R0 C0 R0, C0 ( ) (1) , R0 가 R0, C0 ( ) (1) , R0, C0 (1) , 2가

2 3, 「root ( ) 가 가 가 6a 4 6b R1, C1 (2) 가

, ( ) (2) R1, C1 , 5b R0, C0  
 가 가 , C0 가 가 , 가 가 , R1 C1 가 가 C1  
 , R1, C1 (2) (2)  
 가

, (1) 가 , (2) 2가  
 , 6b , 4가 ( a d)가 .

. 3

, 7a 4 6 7b R2, C2 가 (3)  
 ,

, ( ) (3) R2, C2 6b b, c  
 R0, R1, C0, C1 가 가 , 가 R2 C2 가 가 . b, c

, 6b a 가 R0, R1 , (2 )  
 6 , a 가 가 , 가 C2 . 가

가 , 6b d 가 C0, C1 , (2 )  
 , 6 , d 가 가 , 가 R2  
 가 .

, 6b b, c 가 7b  
 , 6가 ( a f)가 .

. 4

, 8a 6 8b R3, C3 (4)  
 ,

, 7b a, b, d R0, R1, R2 , (2 )  
 C3 , 6 , a, b, d 가 가 , 가

가 , 7b c, e, f C0, C1, C2 (2 )  
 R3 , 6 , c, e, f 가 가 , 가

, 8b , 6가 ( a f)가 .

. 5

, 9a 6 R4, C4 (5)  
 , 9b 7 a f

가

8b a e , R0 R3 C0 C3  
 (2 ) (2 ) .

6, 7 a f 가  
 (5) 가 .

e. 2  
 가 2 (NRS=2), 가 2 (NCS=2)

(k=0 n) , C0 Cn R0, C0 Rn, Cn Rk

1  
 10a 4 10b R0, C0 (1)  
 가 가 가 가 R0 C0

R0 , R0, C0 ( ) (1) ,  
 , 2 가 R0 가 .

가 , C0 R0, C0 ( ) (1) ,  
 , 2 가 C0 가 .

R0, C0 (1) (1) ,  
 가

3, 「root ( )」 2 가 가 .

2  
 11a 4 5 11b R0, C2 (2)  
 가 가 가

( ) (2) R0, C2 10b b C0 R0 C  
 4 가 가 10b b C0 가 가 , 가 R0 C  
 2 가 가 .

10b a R0 (2) R0 , 5가 ,  
 a R0 가 가 .



11b , 3가 ( a c)가 .

3

12a R0, C3 (3)  
5 6 12b 가 .

( ) (3) R0, C3 11b c C0, C2  
c 가 C0, C2 , .

6 11b c C2 가 , 가  
R0 가 가 .

11b a, b R0 R0 (3) R0  
5가 , a, b R0 가 가 .

12b , 3가 ( a c)가 .

4

13a R1, C0 (4)  
4 5 13b 가 .

( ) (4) R1, C0 12b a R0 R1  
4 가 가 12b a 가 가 , 가 R1  
C0 가 가 .

12b b C0 (4) C0  
5가 , 12b b R0 가 가 C0

가 , 12b c , C0 (4) C0  
5가 , 12b c R0 가 가 C0 .

13b , 4가 ( a d) 가 .

5

14a R1, C1 (5)  
4 6 14b 가 .

( ) (5) R1, C1 , 13b b, c R0, C0  
4 , 13b b, c C0, R0 가 가  
가 R1 C1 가 가 .

13b a R1 (5) R1  
5가 , 13b a R1 가 가 R1 .

( ) (5) R1, C1 , 13b d R0, C0, C2  
d C0, C2 , .

R1, 6가 (13b d R0 가 , 가  
 , 14b , 6가 ( a f) 가 .  
 . 6  
 , 15a 4 6 15b R2, C1 (6)  
 , 14b c, e C1 , 14b c, e C1 (6) C1  
 . (5) , 14b c, e C1 가 가 .  
 , ( ) (6) R2, C1 14b a, b, d R0, R1, C0  
 . a, b, d R0, R1 ,  
 , 6 14b a, b, d R1 가 , 가  
 C1 가 가 .  
 , 14b f R0, R1, C0, C1 , 14b f R1 가 , f  
 (6) .  
 , 15b , 5가 ( a e) 가 .  
 , 가 15b 5가 가 ,  
 ,  
 3 a, c, e 가 (3 ) 가 ,  
 ( a, c, e) .  
 f.  
 , 1 7 ,  
 1 7 , NRS, NCS , NRS+NCS C  
 NRS (NRS+NCS NRS ) .  
 , NRS=2, NCS=2 ,  ${}^4C_2 = (4 \times 3) / (2 \times 1) = 6$  .  
 , 3, 6 , ( , ) ,  
 , NRS=2, NCS=2 , ( ) , 16 17 ,  
 6 가 . , 16 17 R ,  
 , C .

17 가 가 , 가 , 16  
 , 1 가 가 , NRS+N  
 CS , NRS+NCS , NRS+NCS C<sub>NRS</sub> 가 , 가  
 , 가 NRS+NCS  
 , 가  
 . 4, 5 가 , 가  
 (가 , 가)  
 . ( , ) 가 , ( ) ,  
 NRS+NCS N<sub>NRS</sub>

g.  
 ,  
 .  
 , 18 NRS+NCS C<sub>NRS</sub> × (NRS+NCS) ( )  
 M

, 18 M NRS가 2, NCS가 2 , 16  
 17

18 M<sub>i1</sub>, M<sub>i2</sub>, M<sub>i3</sub>, M<sub>i4</sub> (i, 1 6 ) , ( ) ,  
 M<sub>11</sub>, M<sub>i2</sub>, M<sub>i3</sub>, M<sub>i4</sub>  
 , i=1 ( 18 1 ) , 가 , M<sub>11</sub>, M  
 12 , 가 , 가  
 M<sub>13</sub>, M<sub>14</sub>

, 17 1 가 R, R, C, C . , 18 ( ) i=2 6  
 17 18 1 1

, 19 18 M M<sub>ij</sub> ( )가 , 1  
 6 17 가  
 NRS+NCS C<sub>NRS</sub> × (NRS+NCS+1) ( ) SR

, 19 SR 18 M(NRS=2, NCS=2 )

19 SR<sub>ij</sub>, SR<sub>i2</sub>, SR<sub>i3</sub>, SR<sub>i4</sub> (i, 1 6 ) ( ) 가  
 SR<sub>i1</sub>, SR<sub>i2</sub>, SR<sub>i3</sub>, SR<sub>i4</sub>  
 , SR<sub>ij</sub> 가 1 , M M<sub>ij</sub> , SR<sub>ij</sub> 가 0  
 M M<sub>ij</sub> ( , j 1 4 )

SR<sub>i5</sub> i , SR<sub>ij</sub> (j=1 4) , 1 i , 0  
 , SR<sub>ij</sub> (j=1 4) 1 , 0  
 SR<sub>i1</sub> , SR<sub>i2</sub> , SR<sub>i3</sub> , SR<sub>i4</sub> , SR<sub>i5</sub> 0 , 가 SR<sub>i1</sub> , SR<sub>i2</sub> , SR<sub>i3</sub> , SR<sub>i4</sub> , SR<sub>i5</sub> 1 .  
 , SR<sub>ij</sub> , SR<sub>i2</sub> , SR<sub>i3</sub> , SR<sub>i4</sub> , SR<sub>i5</sub> 가 1 , SR<sub>i5</sub> 가 1 , i

20 , 22 ( )가 M M<sub>ij</sub> ( )  
 22 SR SR<sub>ij</sub> , 21

23 NRS=4, NCS=4 ,  
 70(=8 C<sub>4</sub>) , M 70×8 ,  
 M 가 , SR 70×9 .  
 , NRS, NCS , Nconb(= N  
 RS+NCS C<sub>NRS</sub> ) , 가

24 Nconb .  
 , i(i=1, 2, ...Nconb) , 가 ,

SR SR<sub>ij</sub> 0 , SR<sub>ij</sub> = 0 M  
 M<sub>ij</sub> 가 .  
 [ ]

A. 25 1 (DRAM) . 2  
 6 29 25 DRAM

, /RAS, /CAS, /WE, /OE ,  
 , DRAM 가 (11)  
 가 , (12)가 (11)  
 가 , (13) .  
 , (12) (13) .

DRAM LSI  
 , 가

가 DRAM (15), (16)  
 DRAM , 26 28 RDTEST, FT, SRT, RESET  
 /RAS, /CAS

1: ( 30)

2: 가 ( 33)

NR=2, NC=2, Nconb=6

2.1 : ( ) BLOCK<sub>i</sub>

i=1 Nconb, Nconb= ( 34)

2.2 : TSR BLOCK( 38 41)

2.1 BLOCK<sub>i</sub>

2.1.1 : (SRAM) ( 35, 36)

2.1.2 : ( 37)

3 : ( ) ( 42)

( 43 49)가

4 : ( ) FOUT, (17)

5 : (RDTEST) (18), (19)

6 : (SRT) (20), (21)

7 : (FT) (22), (23)

8 : (RESET) (24), (25)

B. , 25 DRAM

30 , 25

가 ,

31 , . 32

/OE가 ( H L ), /WE가 H

, /WE가 , /OE가 H

RWD, /RWD

, OEINT가 L H 30 , /OE가 H L  
COMPON H ( )

, 가 . RWD, /RWD 가  
/OE가 H L

OR EX - OR ) , COMPON Fail , AND AND ( (exclusive) Fa  
il 가

, Fail L 가 , Fail 가  
H 가

COMPON Fail 가 , L 가 PRCH  
H , OEINT가 H 가 , COMPON H 가 , L PRCH  
PRCH (MATCH<sub>ij</sub>) H PRCH Fail  
가

33 , 가 . 34 39 33

34 , 33 BLOCK<sub>i</sub>(i=1 6) . 35 , 34 Mij(j=1 4)  
. 36 , 35 Mij1(l=1 10)

37 , 34 SRik(k=1 5) . 38 , 33 TSRBLOCK  
. 39 , 38 TCLK

DRAM 4 가 ( ) 4 가×n(n , 가 )  
A0R, A0C 2 , A0R A10R, A0C A10C

33 ( ) , 가 33  
가 .

NCS 가 2 ( ) , ( ) 가 NRS 가 2 ,  
 ( 16, 17 ) . Nconb =  ${}_4C_2 = 6$  ,

$i, j$   $i=1 \dots Nconb, j=1 \dots NRS+NCS$  .  
 BLOCK<sub>i</sub> (i=1 ~ 6) ( ) (SRAM)  
 M<sub>ij</sub>(1=1 ~ 10) 가 .

a. ( 36)

24 가  
 , 10 1 , M<sub>ijl</sub> ( , )  
 36 )  
 T1 T6 SRAM , T7 T10  
 WL<sub>ij</sub>가 L , COMP<sub>ij</sub>가 H , SRAM , SRAM  
 WL<sub>ij</sub>가 L , COMP<sub>ij</sub>가 H , SRAM BL<sub>ijl</sub> , /BL<sub>ijl</sub>

SRAM BL<sub>ijl</sub> , /BL<sub>ijl</sub> MATCH<sub>ij</sub> H ( )  
 ) MATCH<sub>ij</sub> H ( )  
 BL<sub>ijl</sub> , /BL<sub>ijl</sub> 가 MATCH<sub>ij</sub> , T7, T8, T9, 10  
 MATCH<sub>ij</sub> L 가 .

b. ( 35)

M<sub>ijl</sub> [ , (i, j) = (1, 1), (1, 2), (2, 1), (2, 3), (3, 1), (3, 4), (4, 2), (4, 3), (5, 2), (5, 4), (6, 3), (6, 4), 1 = 1 ~ 10] BL<sub>ijl</sub> , /BL<sub>ijl</sub> AR1, /AR1 AR10, /AR10

M<sub>ijl</sub> [ , (i, j) = (1, 3), (1, 4), (2, 2), (2, 4), (3, 2), (3, 3), (4, 1), (4, 4), (5, 1), (5, 3), (6, 1), (6, 2), 1=1 ~ 10] BL<sub>ijl</sub> , /BL<sub>ijl</sub> AC1, /AC1 AC10, /AC1  
 0

10 SRAM M<sub>ij</sub> ( 18 M )가 . 10 ( )  
 M<sub>ijl</sub> WL<sub>ij</sub> COMP<sub>ij</sub>가 .

WL<sub>ij</sub> COMP<sub>ij</sub> ( ) , WL<sub>ij</sub>가 " H" , COMP<sub>ij</sub> " L"  
 WL<sub>ij</sub>가 " L" COMP<sub>ij</sub> " H" .

MATCH<sub>ij</sub> (10 ) M<sub>ijl</sub> (AND) , A1R A10R 1  
 0 가 SRAM (10 ) , MATCH<sub>ij</sub> " H" 가  
 1 가 MATCH<sub>ij</sub>) " L" .

MATCH<sub>ij</sub> COMP<sub>ij</sub> (AND) AMATCH<sub>ij</sub> SRA  
 M<sub>ij</sub> COMP<sub>ij</sub>가 " H" 가 , MATCH<sub>ij</sub> , SRAM  
 M<sub>ij</sub> COMP<sub>ij</sub>가 " L" , AMATCH<sub>ij</sub> " L" .





가 ( )

, 4 가 NRS 가 2, 4 가 × n(n ) DRAM( NCS 가 2 )

1

[ 1 ]

	10	NRA
	10	NCA
	2	NRS
	2	NCS
	4	NRS + NCS
Nconb	6	$NRS + NCS \cdot C_{NRS}$
TSR	5	$NRS + NCS + 1$
SR	30	$Nconb \times (NRS + NCS + 1)$
SRAM	240	$Nconb \times (NRS \times NRA + NCS \times NCA)$

42 ( ) . 43 49 42

BSR BLOCK( 43 46) BLOCK<sub>i</sub> BLOCK<sub>i</sub>  
BLOCK<sub>i</sub> 10 ( )  
DSR BLOCK

( ) DSR BLOCK 10 , 1 FOUT  
LSI ( )

4 가 NRS 가 2, NCS 가 2 4 가 × n(n ) DRAM ( )

2

[ 2 ]

BSR	6	Nconb
DSR	10	NRA NCA

RDTEST , SRT  
FT , RESET

가 ( N MOS " L" )

" H"

C. LSI

A, B DRAM LSI ( ) LSI( ) LSI( )  
 가 LSI  
 LSI  
 ( )  
 ( ) FOUT  
 ( LSI  
 ).

D.

3

(1)

25 41

RDTEST " H" 가 가

(2)

25 가  
 ( ) 가

가 ( )

40 41 SRT FT " L"  
 RESET " H"

OTSR<sub>1</sub> OTSR<sub>5</sub> " L"

OSR<sub>i1</sub> OSR<sub>i5</sub> " L"

, SRAM 가 WL<sub>ij</sub> " H" 가 , SRAM ( )

, SRAM 가 WL<sub>ij</sub> 가 가 가 .

, 가 WL<sub>ij</sub>가 " L" 가 SRAM ( 24 ).

34). SR<sub>i1</sub> SR<sub>i5</sub> OSR<sub>i1</sub> OSR<sub>i5</sub> IN<sub>i1</sub> " 1" " 0" (" 0" " L" ) ( SR<sub>i1</sub> SR<sub>i5</sub> " 1" Fail TMATCH<sub>i</sub> ) ( AND) 가 ] SCLK<sub>i</sub>[ 34

" 1" SRAM M<sub>ij</sub> WL<sub>ij</sub> " L" . , WL<sub>ij</sub>가 " L" SRAM M<sub>ij</sub> SRAM M<sub>ij</sub> SR<sub>i1</sub> SR<sub>i4</sub> " 1" SRAM M<sub>ij</sub> 가 ( 19, 21 ).

LOCK<sub>i</sub> ( SR<sub>i1</sub> SR<sub>i5</sub> , SR<sub>i5</sub> OSR<sub>i5</sub>가 " 1" , B BLOCK<sub>i</sub> ( ) 가 .

, OSR<sub>i5</sub>가 " 0" SR<sub>i5</sub> OSR<sub>i5</sub> BLOCK<sub>i</sub> ( )가 OSR<sub>i5</sub>가 " 1" 가 .

50 55 BLOCK<sub>i</sub> (i=1 6)

, (R0, C0), (R0, C1), (R0, C2), (R0, C3), (R1, C0), (R1, C1), (R1, C2), (R1, C3), (R2, C0), (R2, C1), (R2, C2), (R2, C3), (R3, C0), (R3, C1), (R3, C2), (R3, C3) , (R0, C0), (R0, C2), (R0, C3), (R1, C0), (R1, C1), (R2, C1) , N R = 2, NC = 2 가 ( ) .

(3)

, 가 ( 가 )

가 ( )

SR<sub>i1</sub> SR<sub>i5</sub> , SRT " H" FT " H" FOUT

56 ( ) 57 .  
 , ( ) .  
 a. ( 56)  
 , SRT " H" , ,  
 OSTR<sub>1</sub> OSTR<sub>4</sub> " L" " H" " H" , ,  
 WL<sub>ij</sub> " L" .  
 , SR<sub>i1</sub> SR<sub>i5</sub> SRAM ( ) ( )  
 , )  
 , 44 /CAS CINT가 SCLK<sub>i</sub>가 . RINT가 BCLK가  
 BCLK BSR BLOCK , /RAS ("  
 H" " L" ) BSR BLOCK .  
 , 43 44 BSR BLOCK OBSR<sub>i1</sub> OBSR<sub>i6</sub> OBSR<sub>i1</sub> "  
 H" , OBSR<sub>i2</sub> OBSR<sub>1</sub> " L" BCLK " H" "  
 가 . " H" OBSR<sub>ij</sub> 42 ,  
 , SCLK<sub>i</sub> Fail TMATCH<sub>i</sub> (AND)  
 , /CAS가 /CAS CINT가 .  
 /CAS (" H" " L" ) , 가 .  
 , /RAS " H" /CAS " H" , " L"  
 가 5 BLOCK<sub>i</sub>  
 가 .  
 가 가  
 /CAS가 SCLK<sub>i</sub>가 ,  
 /CAS " H"  
 , /RAS " H" " L" BCLK  
 ) , 42 FOUT OSR<sub>i5</sub> ( )  
 가 ,  
 가 SCLK<sub>i</sub> ( ) FOUT SR<sub>i1</sub> SR<sub>i5</sub>  
 가 가 SRAM  
 (" 1" )

$SR_{i5}, SR_{i1}$  ( 1 )가 0, 0, 1, 1, 1, 1 ( 1  
 $SR_{i5}, SR_{i4}, SR_{i3}, SR_{i2}, SR_{i1}$   
 0, 0, 1, 1, 1  
 $SR_{i5}$  1  
 ( )가 ( " 0", " 1" ). 1  
 1 가 4 (0, 1, 1, 1) SRAM  $M_{ij} (j = 1 \dots 4)$   
 ,  $SR_{ij}$   $SR_{i5}$   $SR_{i1}, SR_{i5}$  ( 34). ,  
 가  
 56 ,  
 , 가 1, 3, 5  
 3  
 b. ( 57)  
 T " H" SRT " H" F  
 , SRAM  $M_{i1}, M_{i2}, M_{i3}, M_{i4}$  (10 )  
 FOUT  
 $TSR_1, TSR_5$   
 /CAS BSR BLOCK /RAS BSR BLOCK BCLK가  
 CLK가 , /WE가 - 1  $SR_{ij}, TSR_k$  SCLK<sub>i</sub>, T  
 DCLK가 DSR BLOCK  
 ,  $OBSR_1$  " 1", 가  $OBSR_2, OBSR_6$  " 0"  $BSR_1, BSR_6$   $OBSR_1, OBSR_6$  " 1"  
 BCLK 가  
 ,  $TRS_1$  TCLK (" L" " H" ) " 0" 가  
 가  $TSR_4$  " 0" SRAM  $M_{ij}$   
 " 0" 4  
 SRAM 가 , ( )RWD, /RWD  
 FOUT , 1 10 TCLK  
 FOUT DSR 10 - 1  
 FOUT  
 /WE DCLK  
 , 2  $SR_{ij}$   
 " L"

57 1 5 FOUT

RESET " H"

BSR TSR

( BLOCK<sub>i</sub> TSR<sub>1</sub> TSR<sub>5</sub> BLOCK<sub>i</sub>  
SR<sub>i1</sub> SR<sub>i5</sub>

TSR<sub>1</sub> TSR<sub>5</sub> SRAM  
SR<sub>i1</sub> SR<sub>i5</sub> SRAM

가

(1) (2) ( BLOCK<sub>i</sub> OTSR<sub>1</sub> OTSR<sub>4</sub> " L" )  
SR<sub>5</sub> " L" SR<sub>i1</sub> SR<sub>i5</sub> (SRAM SR<sub>i1</sub> SR<sub>i5</sub>)

BLOCK<sub>i</sub> WL<sub>ij</sub> OTSR<sub>1</sub> OTSR<sub>4</sub> " L" " H" 가 , " H"  
" L" 가

TSR<sub>1</sub> TSR<sub>5</sub> 가 BLOCK<sub>i</sub> SR<sub>i1</sub> SR<sub>i5</sub> SRAM ( ) SCLK  
BLOCK<sub>i</sub> SR<sub>i1</sub> SR<sub>i5</sub>

BLOCK<sub>i</sub> SR<sub>i1</sub> SR<sub>i5</sub> TSR BLOCK OTSR  
1 OTSR<sub>4</sub> TSR BLOCK OTSR<sub>1</sub> OTSR<sub>4</sub> OTSR  
0"

SR<sub>i1</sub> , SR<sub>i5</sub> OTSR<sub>1</sub> OTSR<sub>4</sub> (NOR) SRAM  
TSR BLOCK OTSR<sub>1</sub> OTSR<sub>4</sub> 가 " 0" SRAM  
SRAM M<sub>ij</sub> ( , 가 )

TSR<sub>1</sub> TSR<sub>5</sub> 가 SRAM BLOCK<sub>i</sub>  
SR<sub>i1</sub> , SR<sub>i5</sub> " 1" (5)

C.

SSET " H"  
가

가 가 .

/RAS, SSET " H" /CAS .

58 59 ( )  
FOUT .

가 FOUT

59 (1) A1R = " 1" (1)  
SA1R " L" SA1R " L" A1R=" 1"

60  
60

가 2 , 가 2 SSR<sub>j</sub>  
SA1R<sub>j</sub> / SA1R<sub>j</sub> SA10R<sub>j</sub> /SA10R<sub>j</sub> .

( )

가 .

가

( )

가

가

LSI .

LSI

가

가

가

가

LSI

(57)

1.

1

2.

1

1

3.

1

4.

2

5.

1

1

6.

2

1

7.

1

1

( , NRS , , NCS , )

, NRS+NCS C<sub>NRS</sub> (NRS+NCS NRS )



8.

2 ,  
 1 , , NRS+NCS  $C_{NRS}$  (NRS+NCS NRS )  
 ( , NRS , , NCS , )

9.

7 ,  
 1 , NRS+NCS  $C_{NRS}$  , , , 1  
 가 .

10.

8 ,  
 1 , NRS+NCS  $C_{NRS}$  , , , 1  
 가 .

11.

9 ,  
 1 , , , ,  
 , .

12.

10 ,  
 1 , , , ,  
 , .

13.

11 ,  
 1 , .

14.

12 ,

1 ,

15.

1 ,

1 , , 가

16.

2 ,

가 , 1 , ,

17.

15 ,

, , , 1

18.

16 ,

, , , 1

19.

15 ,

1 , , , ,

20.

16 ,

1 , , , ,

21.

1 ,

, 1  
.

22.

21 ,

1 , , 가

23.

2 ,

, 1  
.

24.

23 ,

가 , 1 , ,

25.

22 ,

, , , 1  
.

26.

24 ,

, , , 1  
.

27.

22 ,

1 , , , ,

28.

24 ,

1 , , , ,

29.

1 , , 1 ,

30.

2 , , 1 ,

31.

1 , , 1 , ,

32.

2 , , 1 , ,

33.

29 , , 1 가 1

34.

30 , , 1 가 1

35.

31 , , 1 가 1

36.

32 ,

, 1 가 1

37.

,

,

,  
1

1

38.

1

,  
1

39.

,  
1

40.

39 ,

1

41.

40 ,

42.

40 ,

43.

39 ,

1 ,

44.

39 , 1 , , NRS+NCS  $C_{NRS}$  (NRS+NCS NRS )

( , NRS , , NCS , )

45.

39 ,

1 ,

46.

45 ,

1 ,

47.

39 ,

1 1 가 1 ,

48.

,  
가

가

49.

48 ,

가

가

50.

48 ,

가 NRS

,  
가  
가

NRS

51.

48 ,

가 NCS

,  
가  
가

NCS

52.

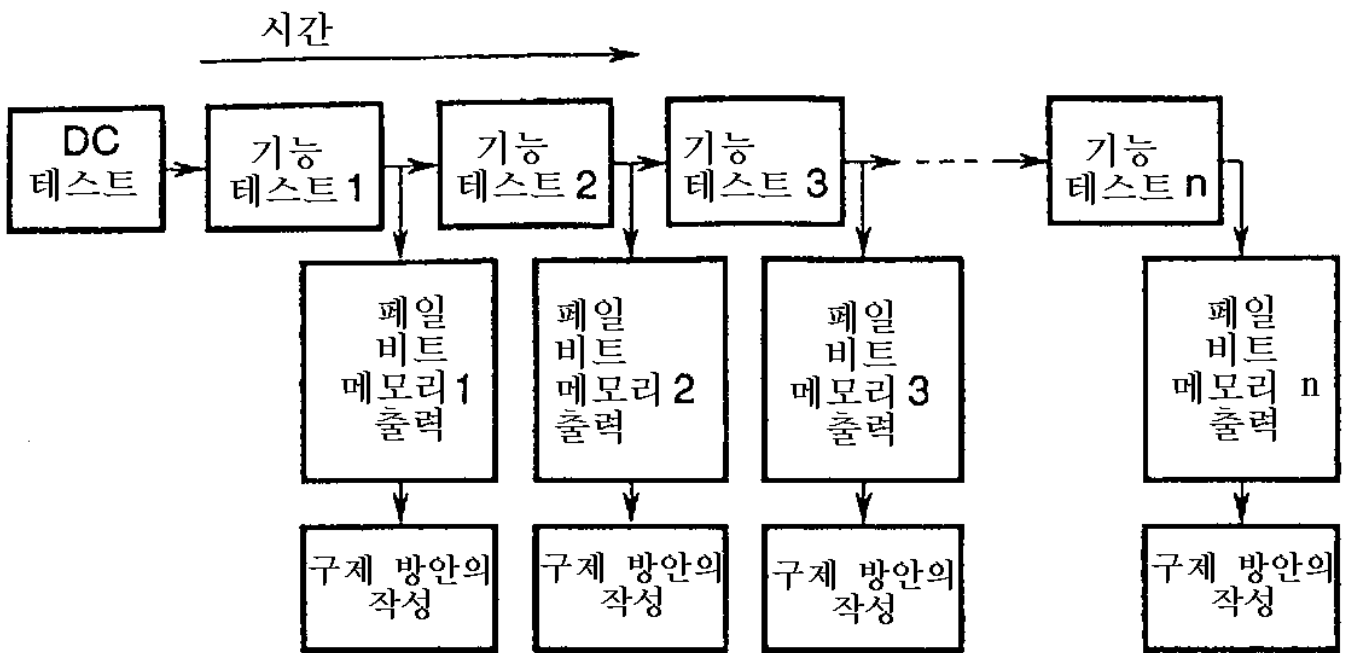
48 ,

가, NRS  
NCS

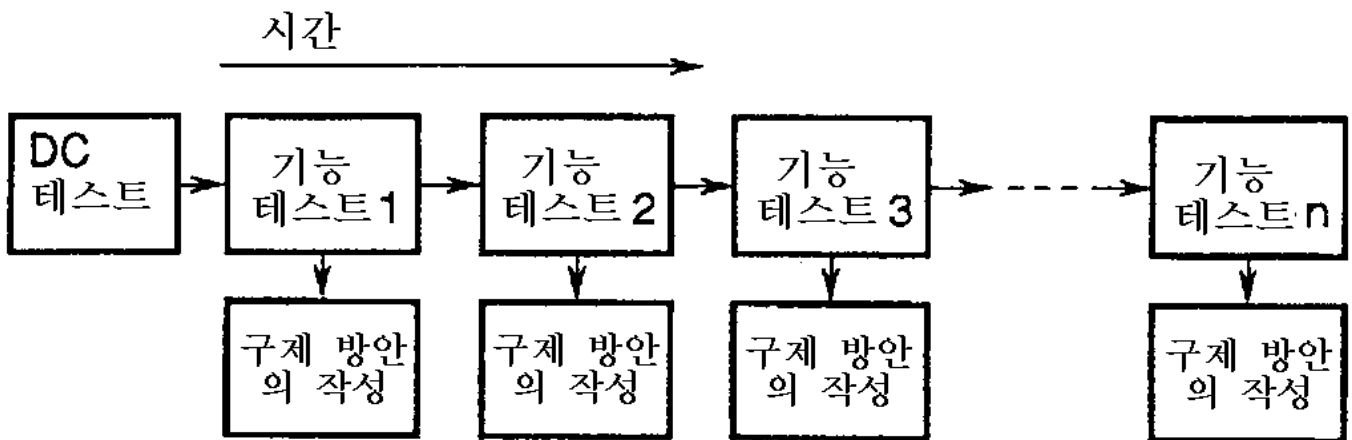
, NCS

가

1

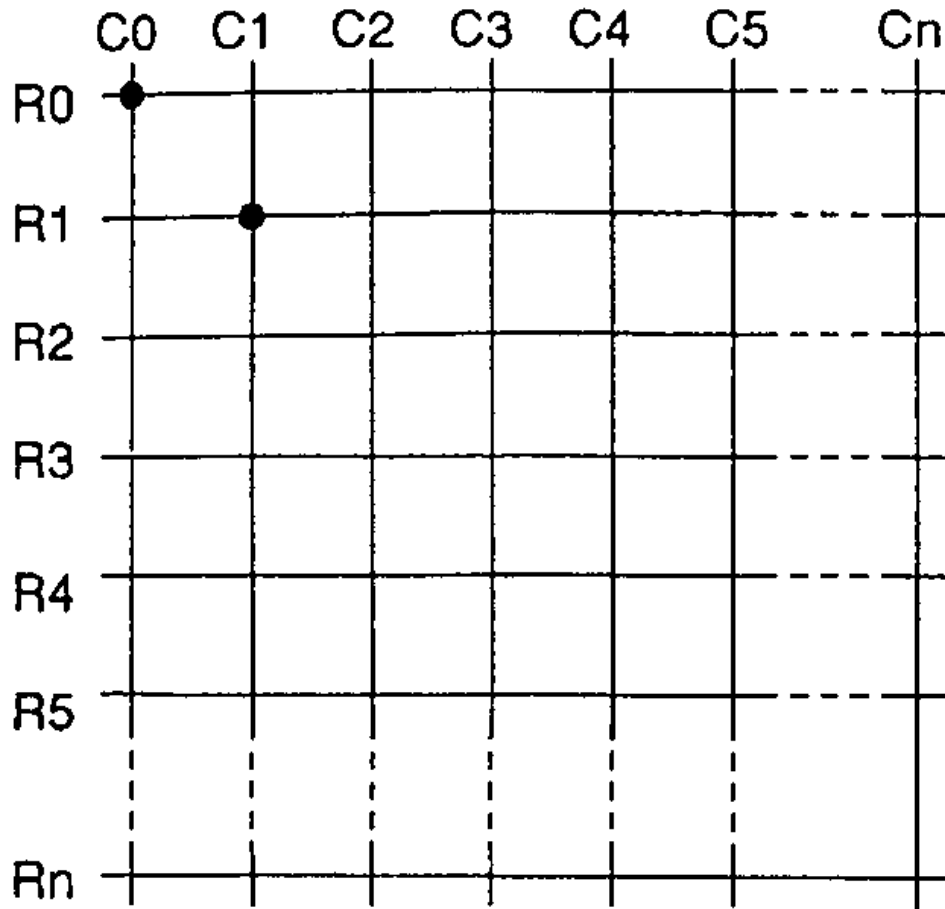


2



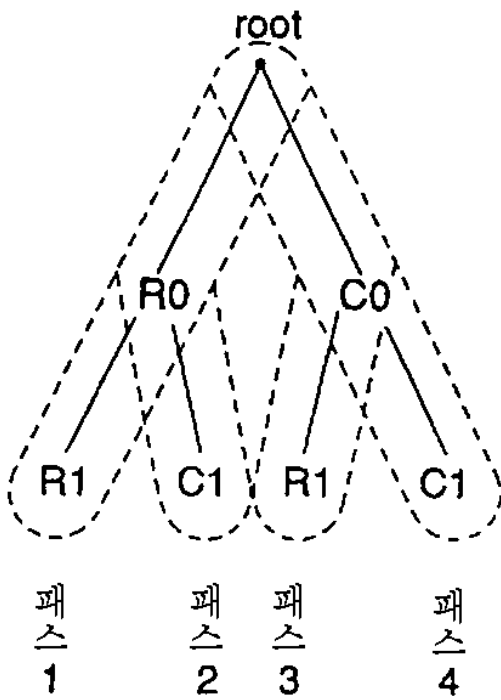


3



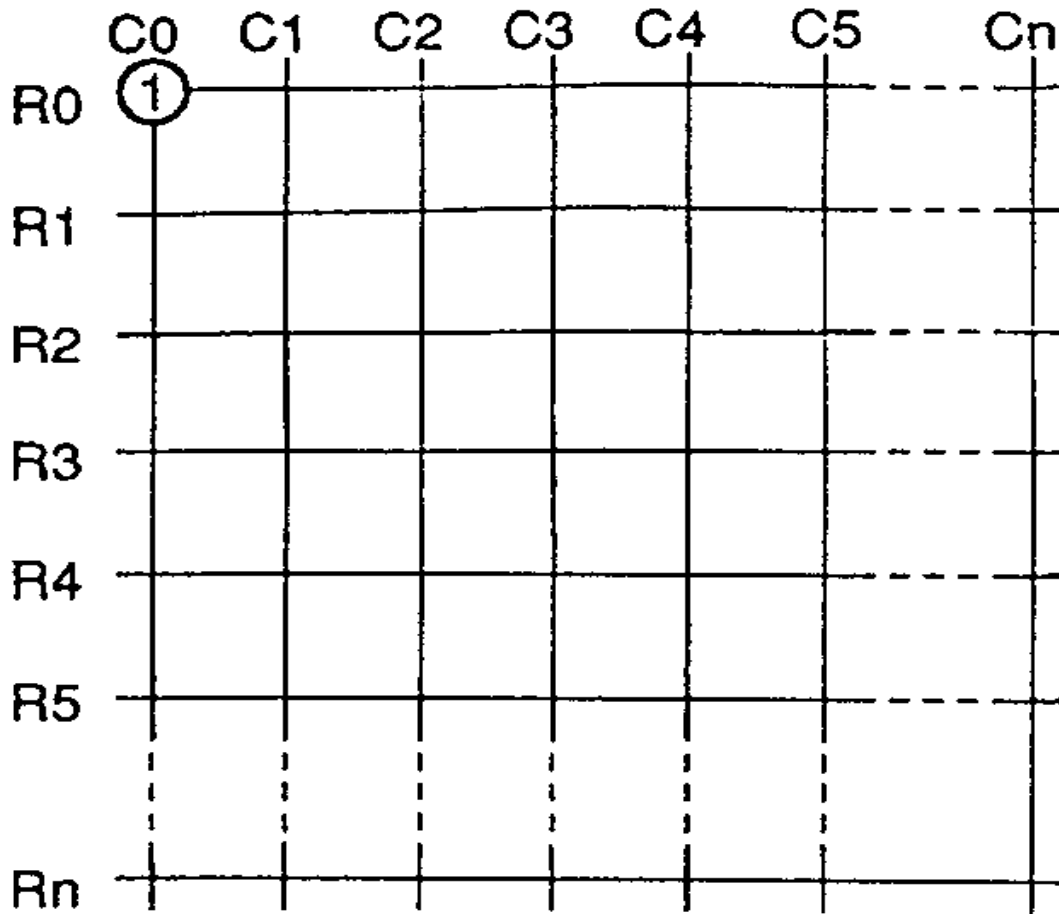
불량 비트의 분포 ( ● ; 불량 비트 )

4

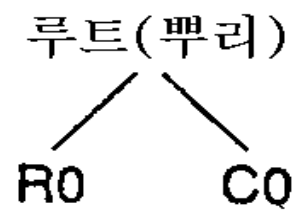


- 패스 1(구제 방안 1) : R0, R1  
스페어 라인으로 치환
- 패스 2(구제 방안 2) : R0, C1  
스페어 라인으로 치환
- 패스 3(구제 방안 3) : C0, R1  
스페어 라인으로 치환
- 패스 4(구제 방안 4) : C0, C1  
스페어 라인으로 치환

5



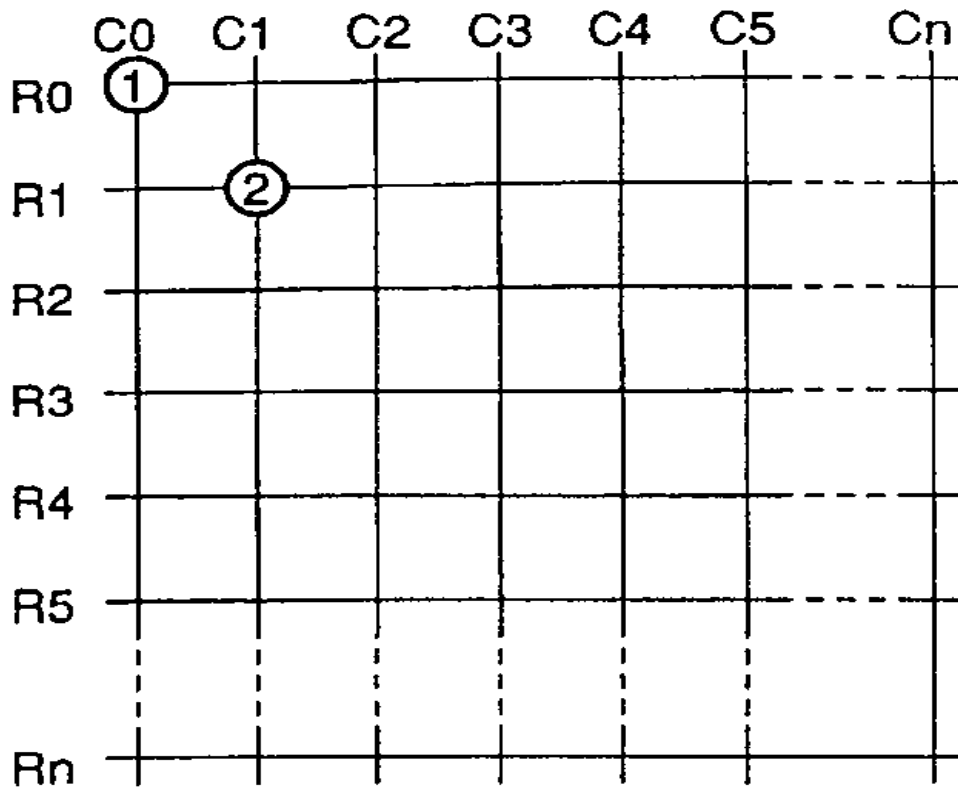
(a)



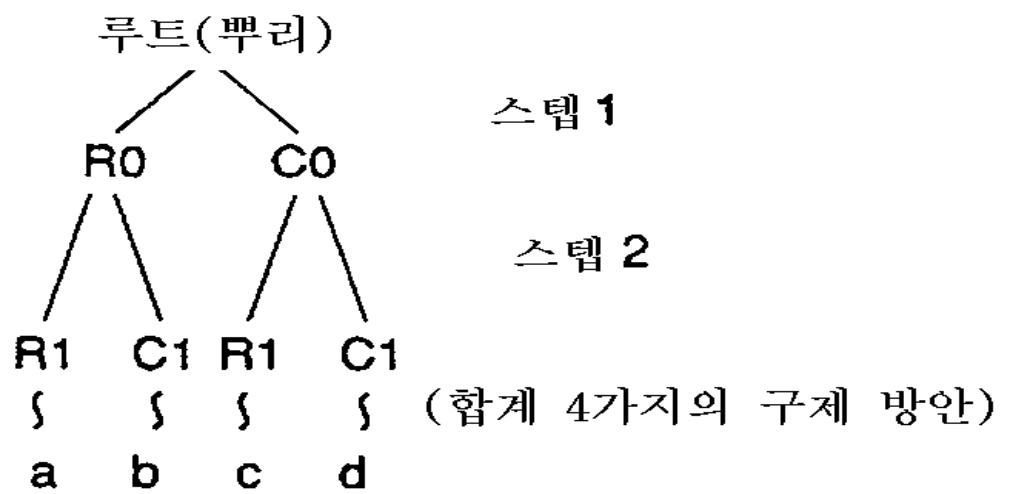
스텝 1

(합계 2가지의 구체 방안)

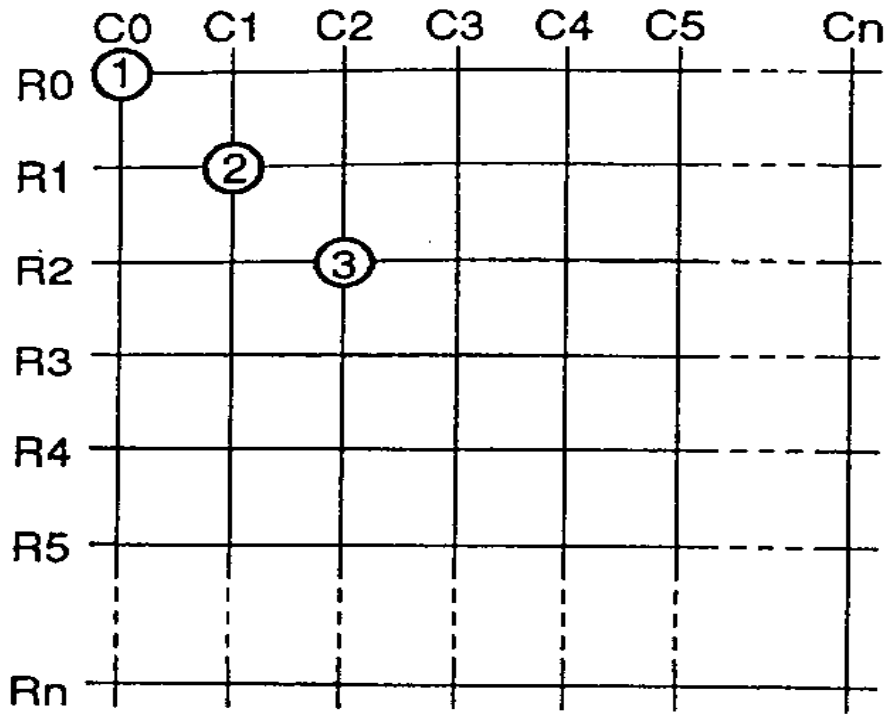
(b)



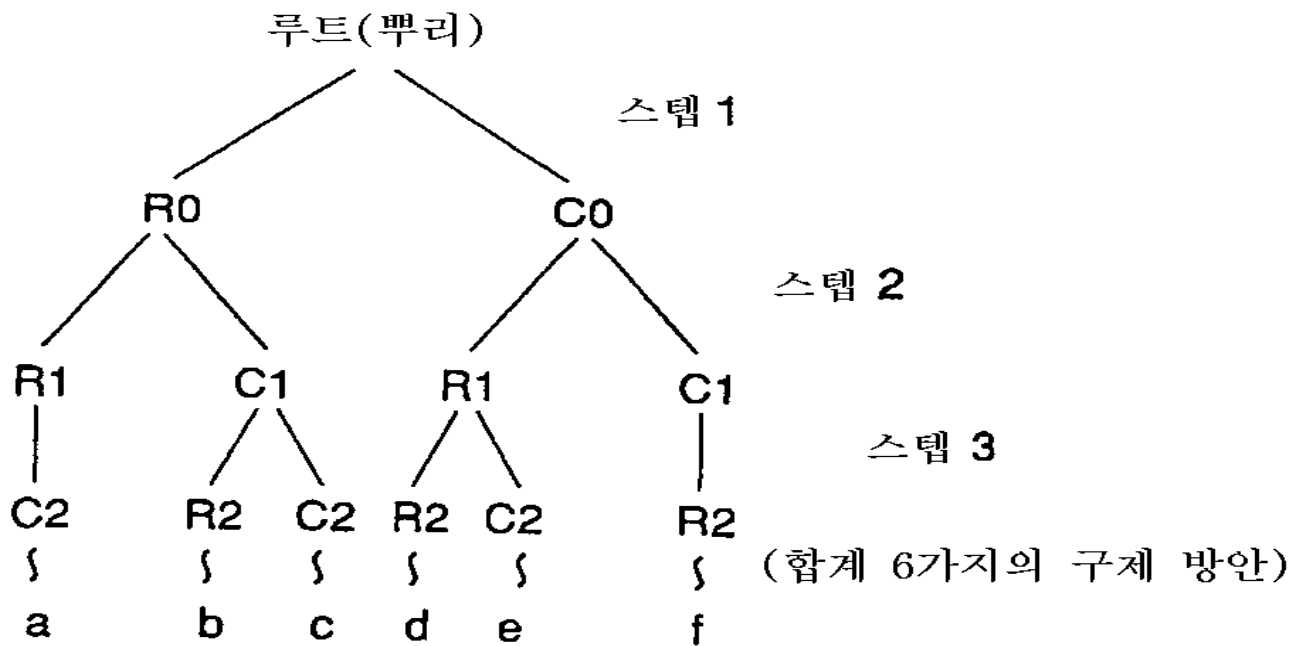
(a)



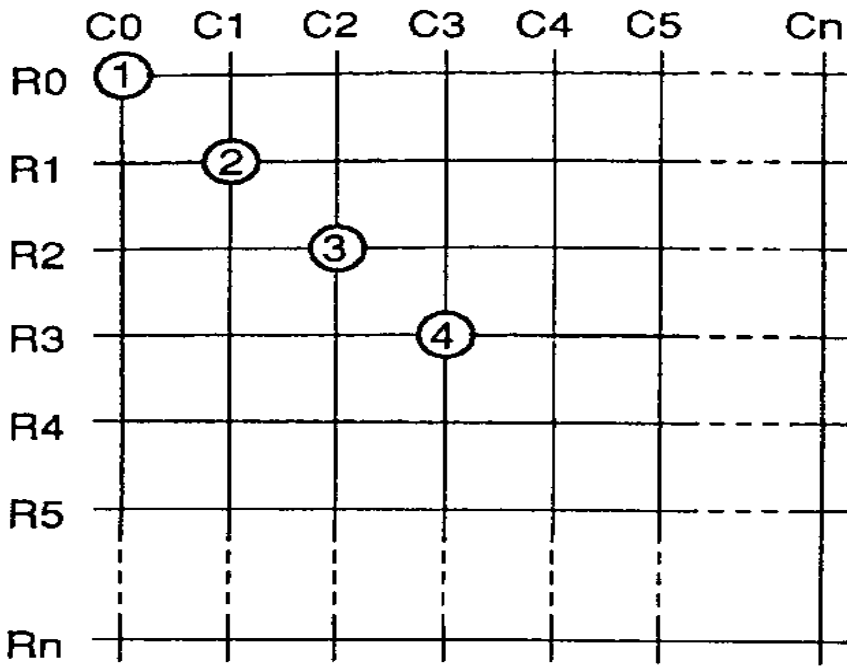
(b)



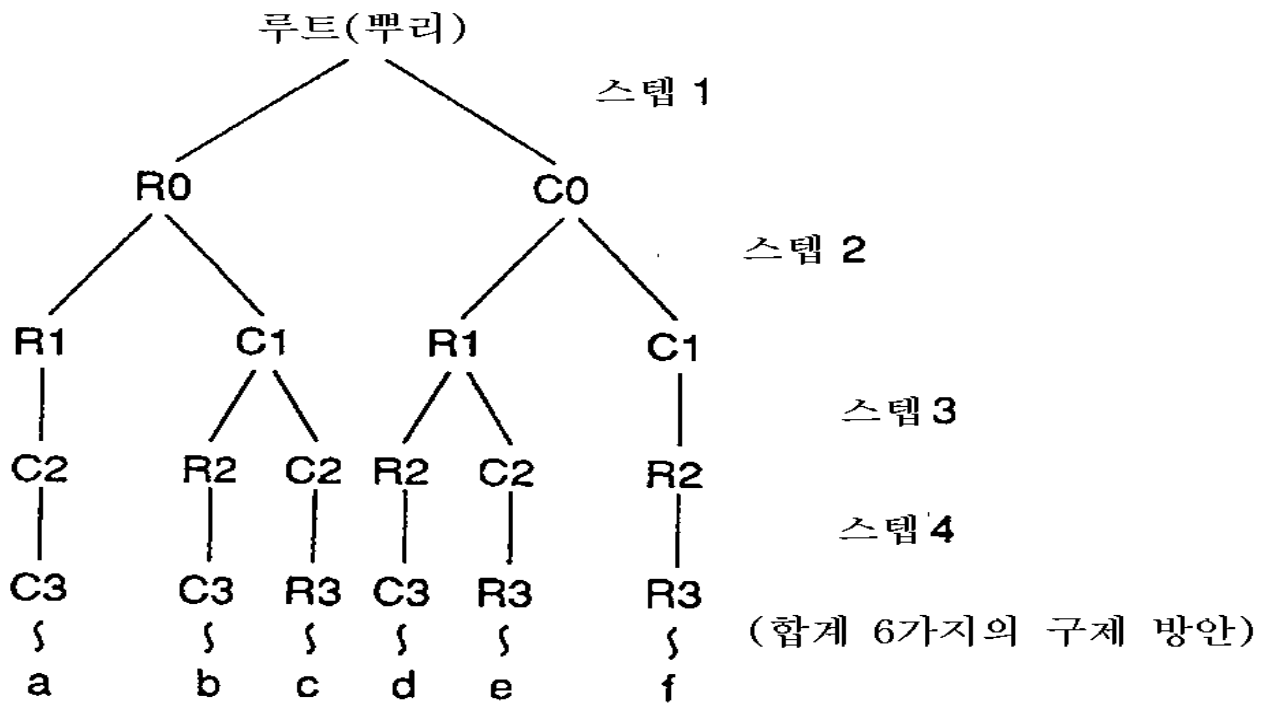
(a)



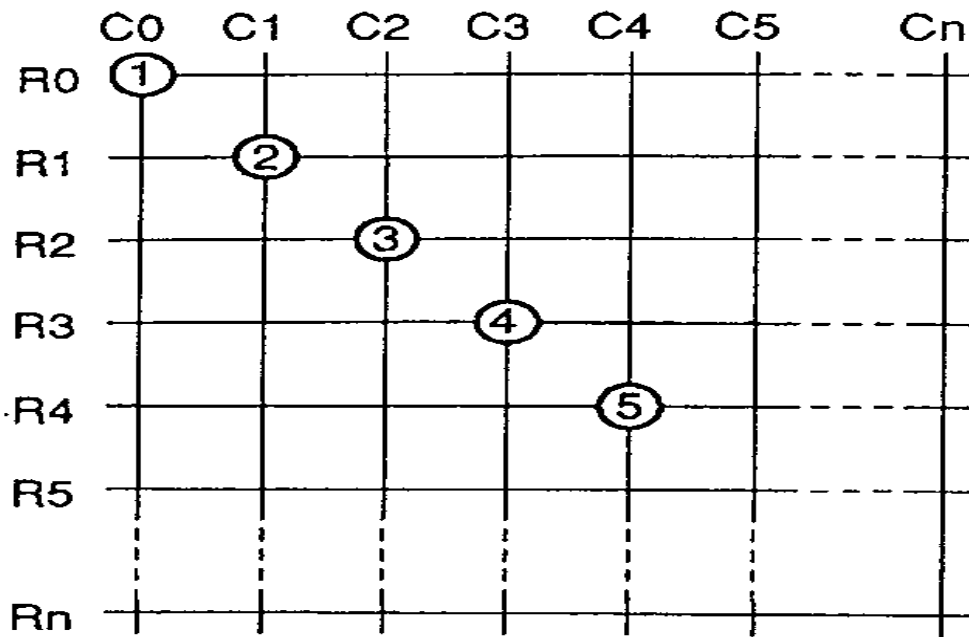
(b)



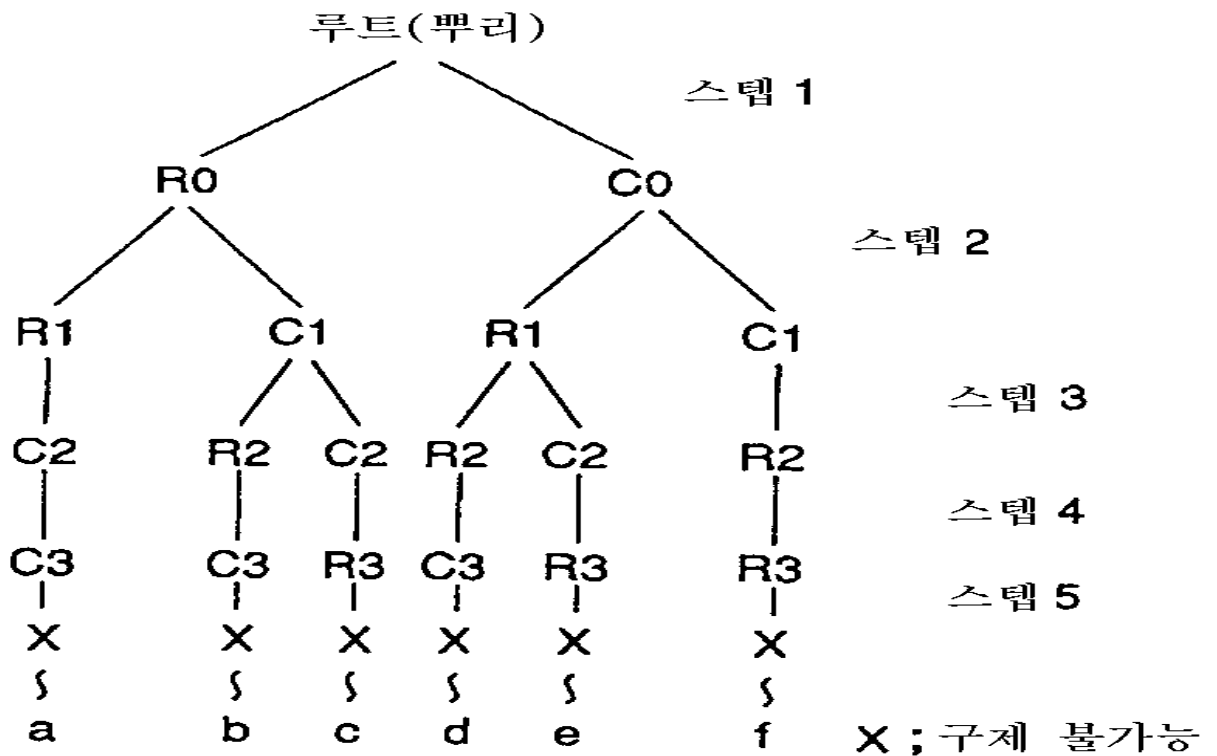
(a)



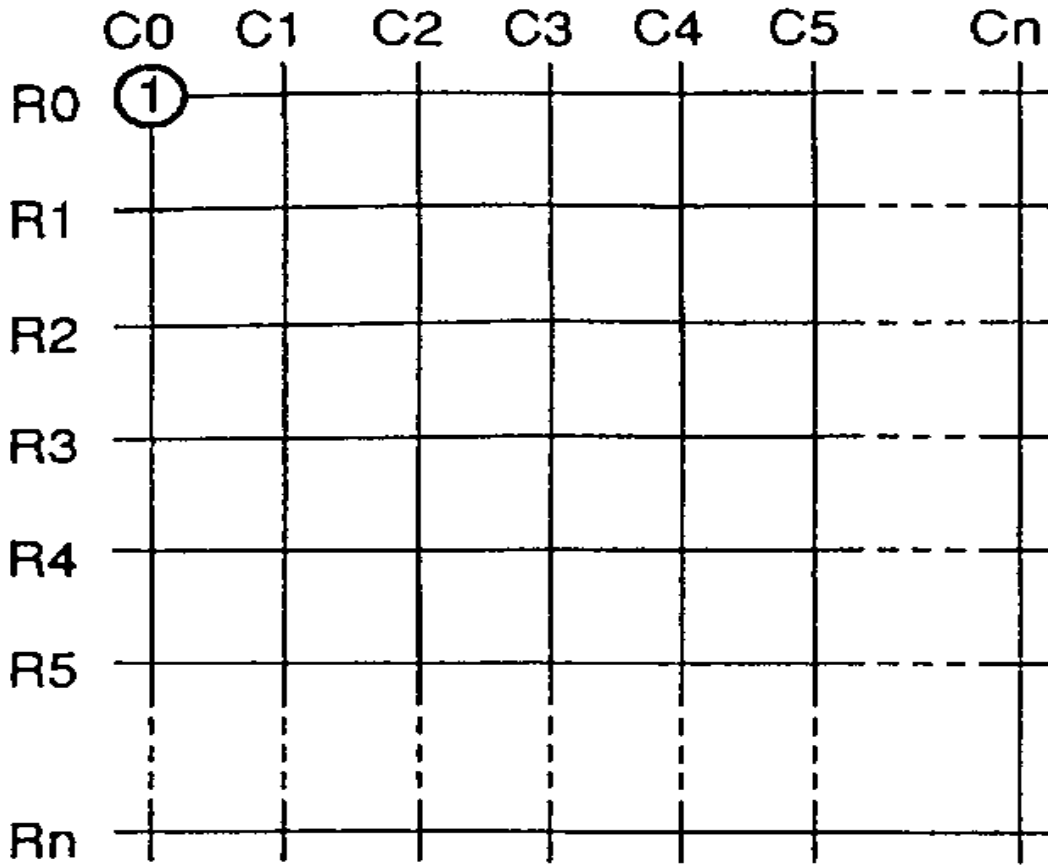
(b)



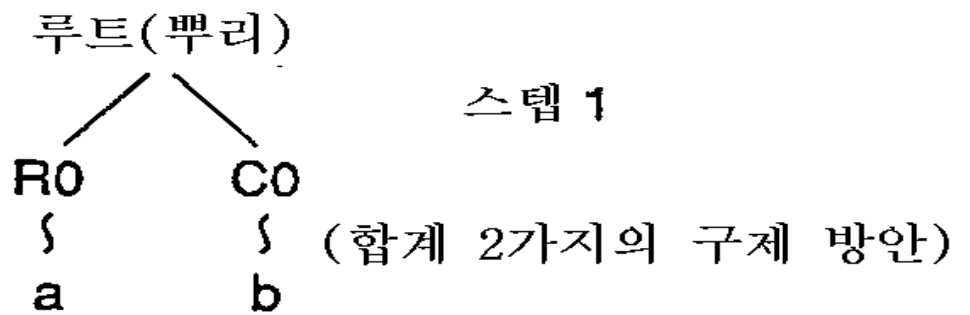
(a)



(b)

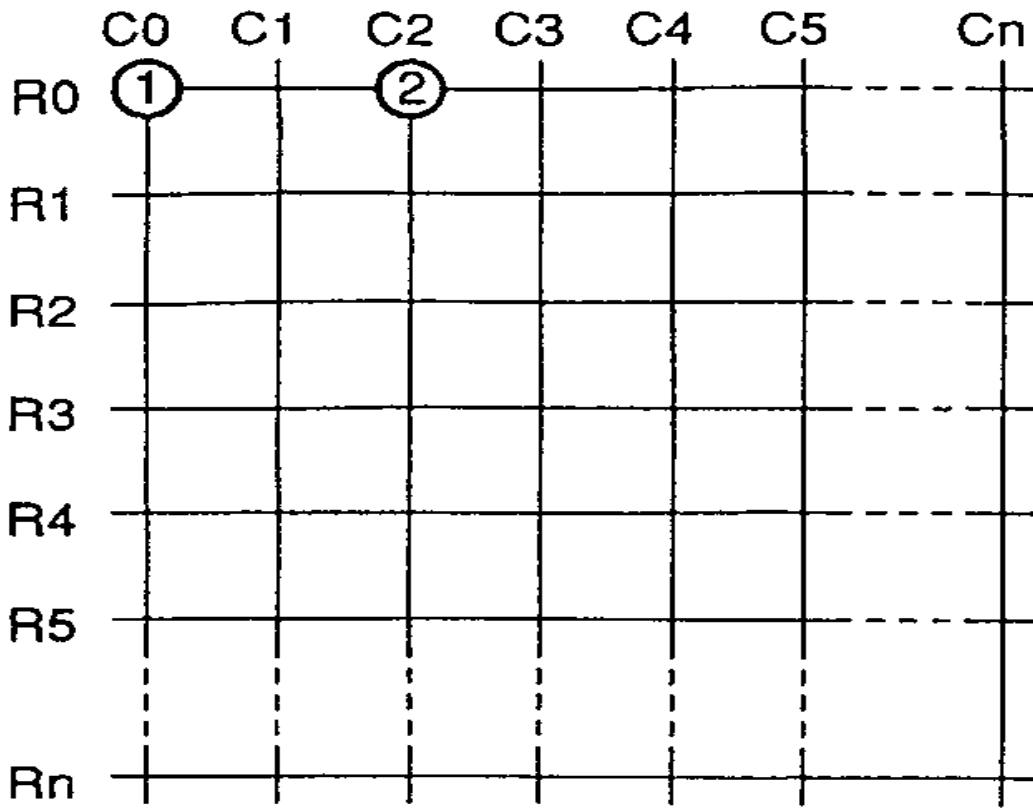


(a)

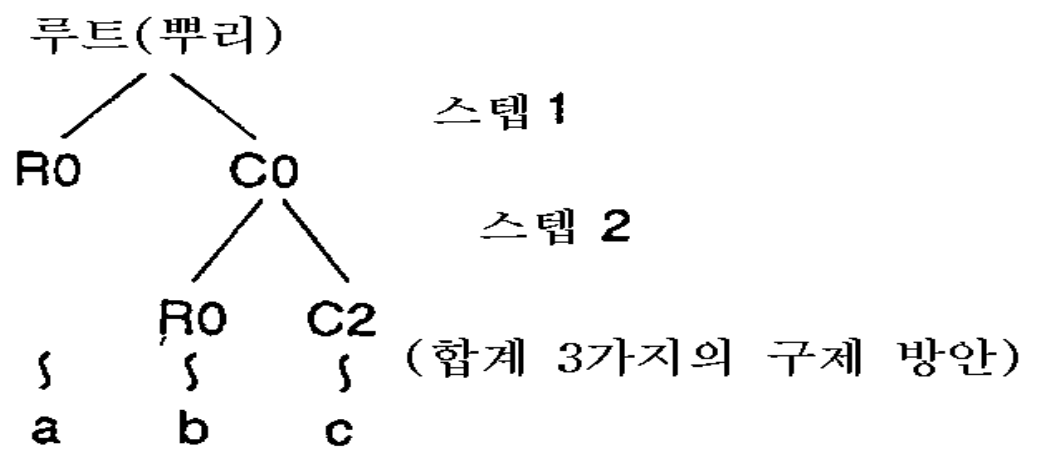


(b)

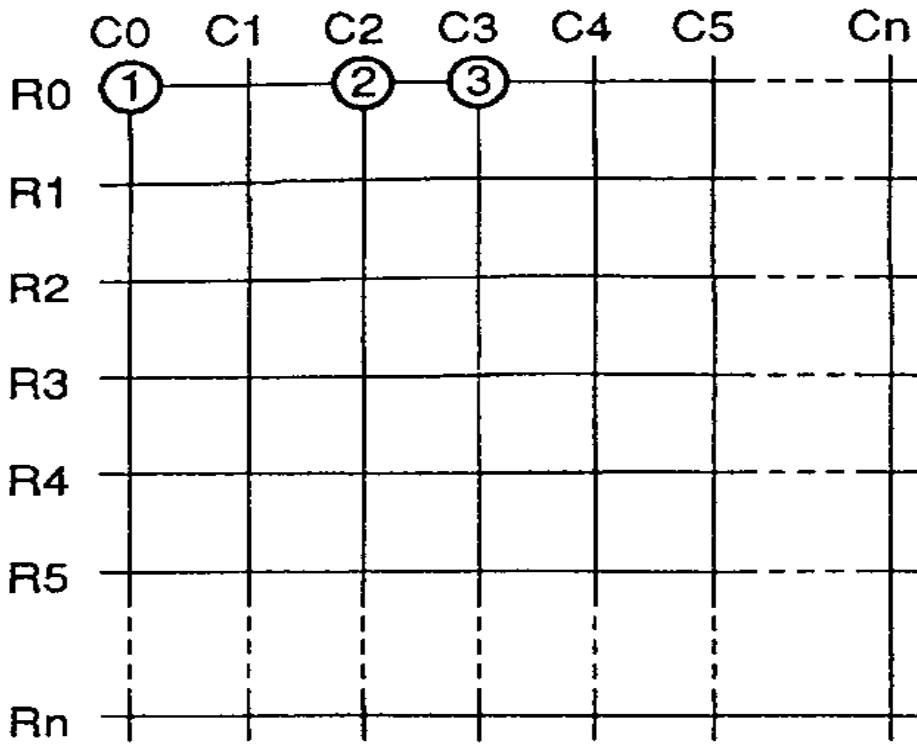




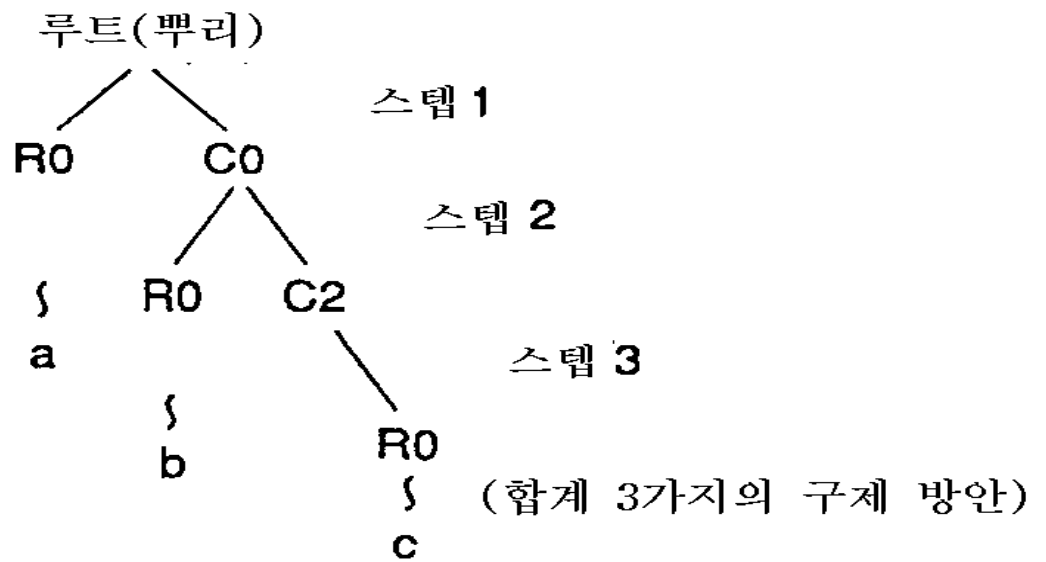
(a)



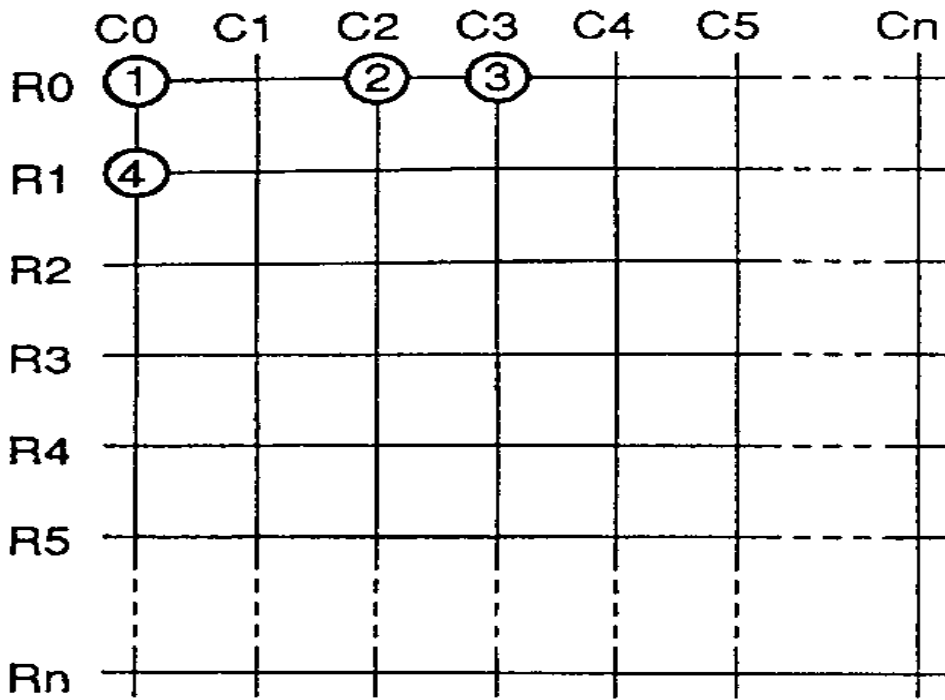
(b)



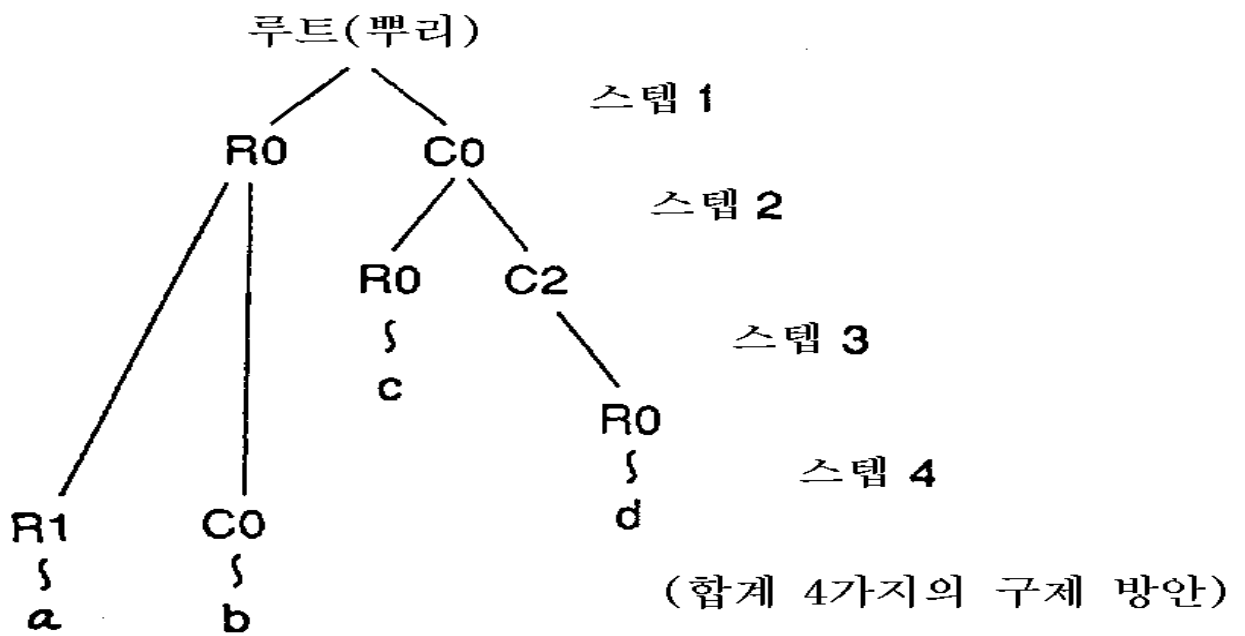
(a)



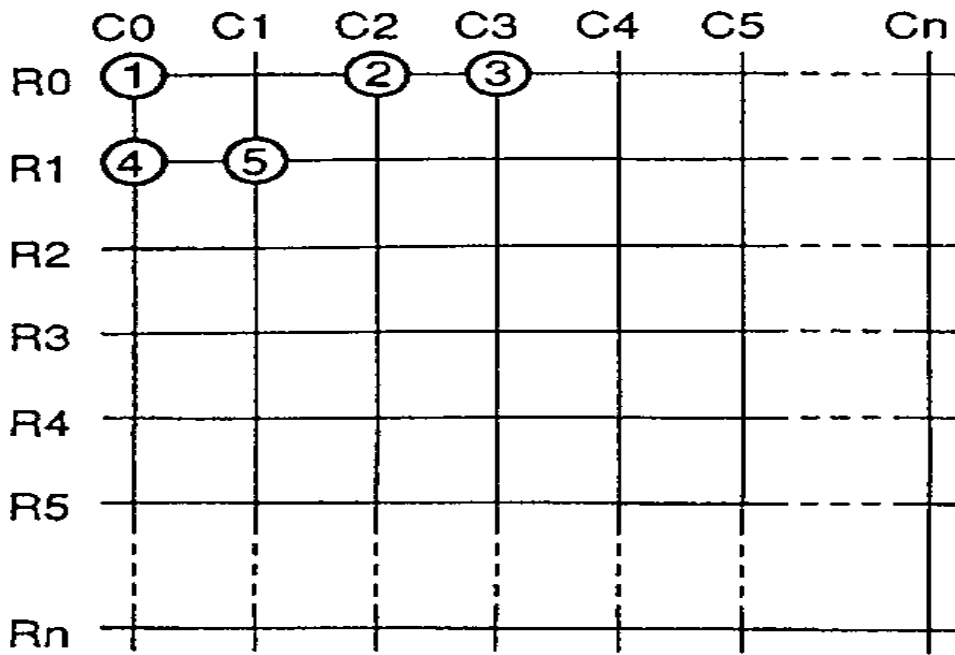
(b)



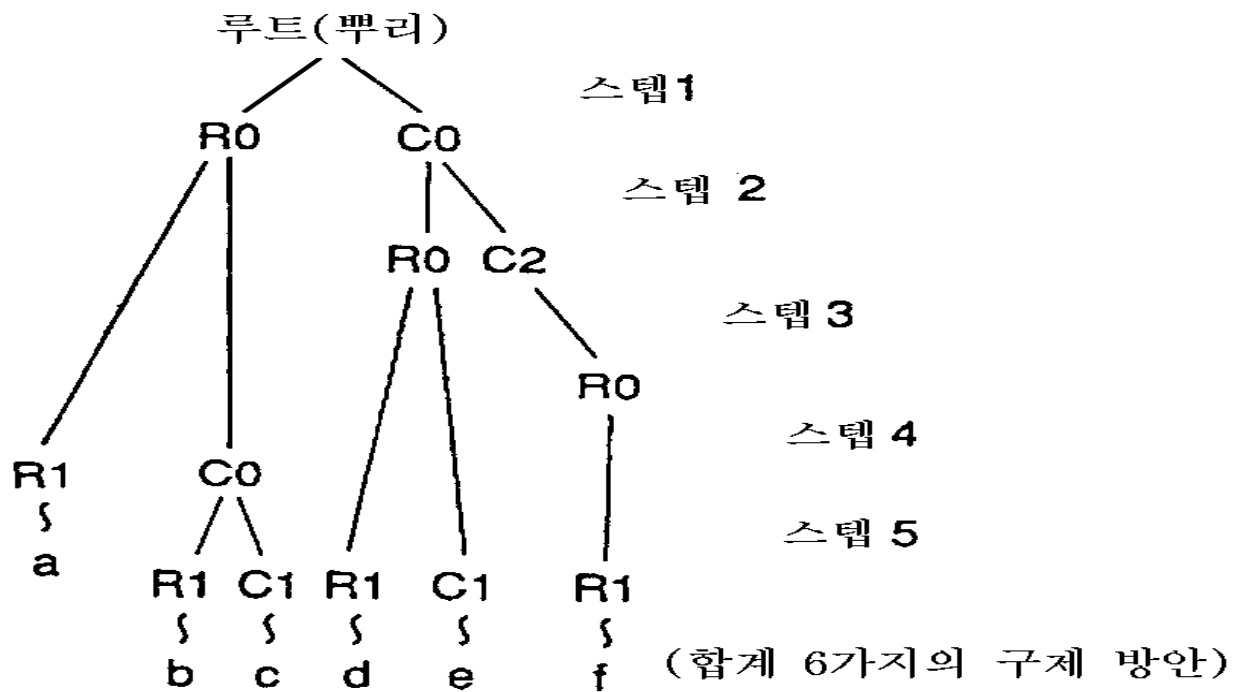
(a)



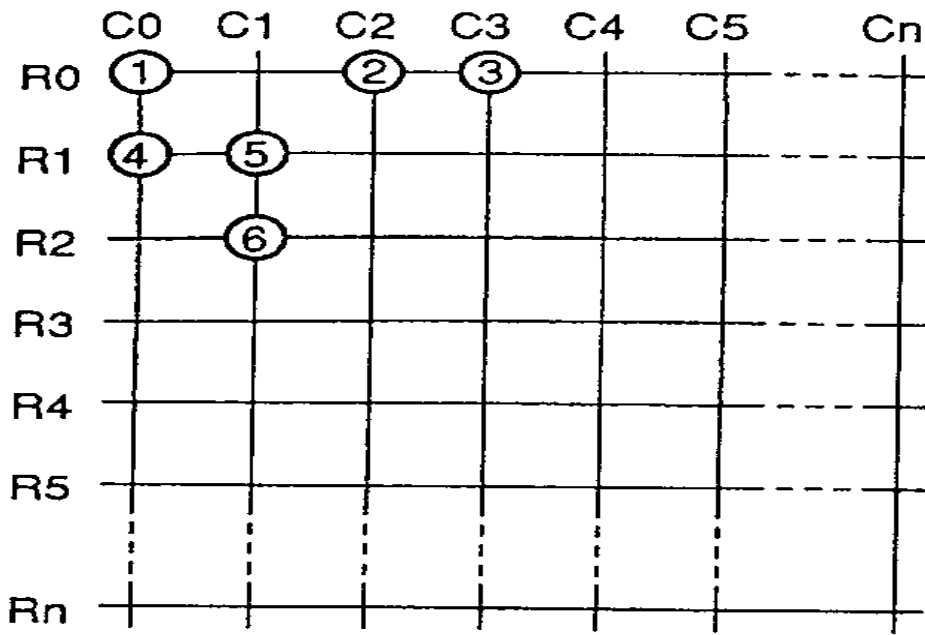
(b)



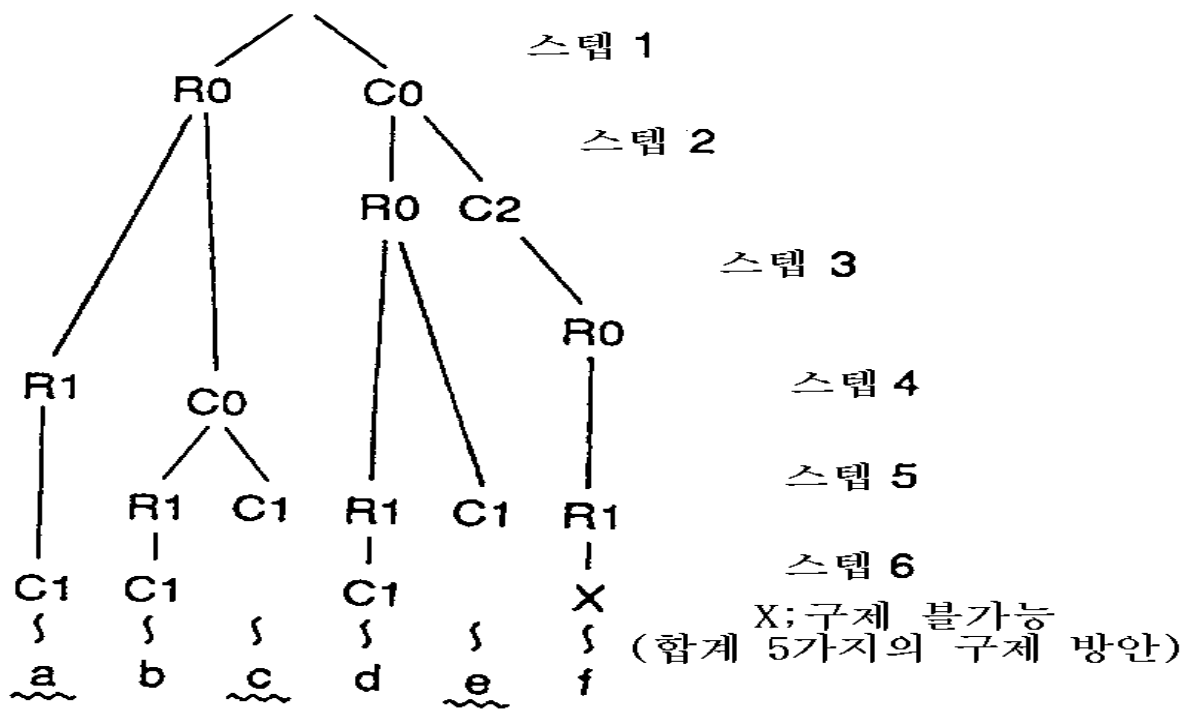
(a)



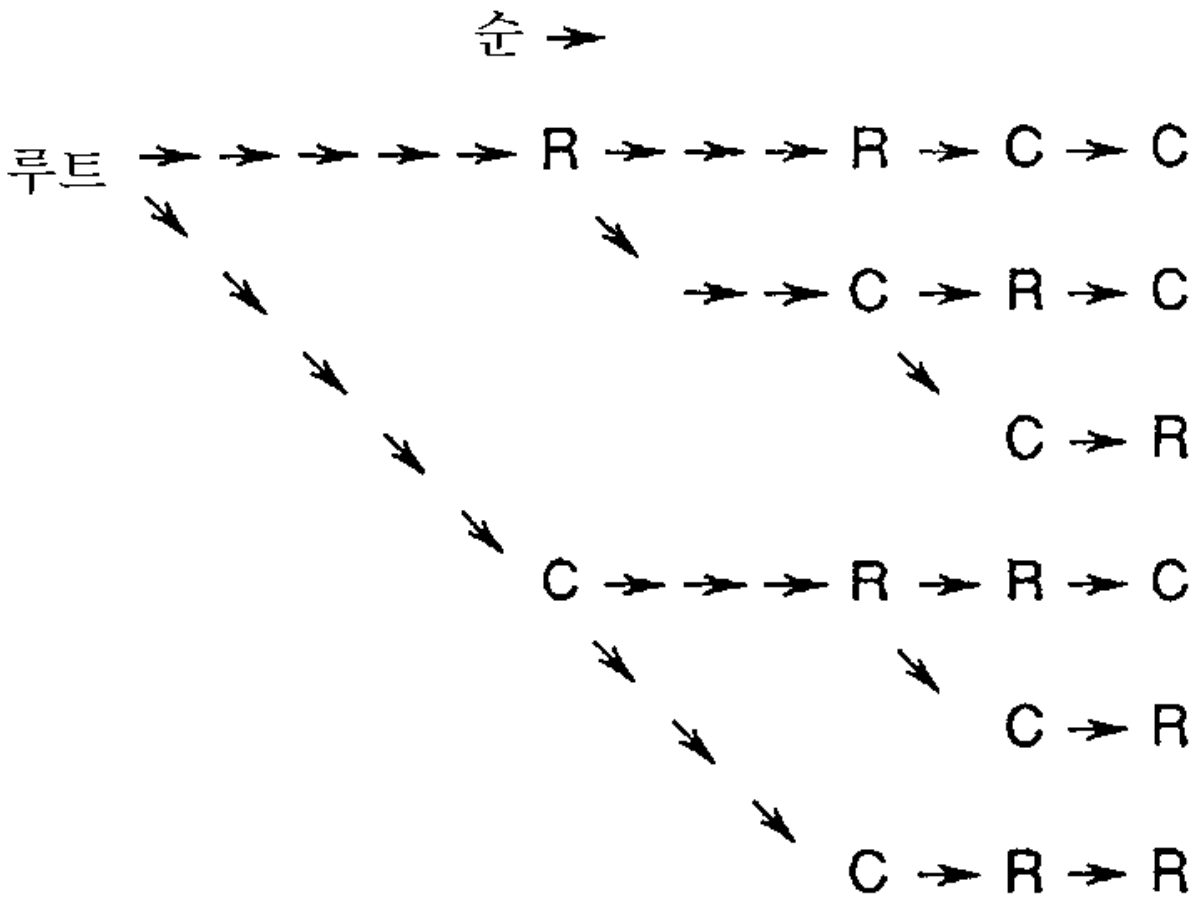
(b)



(a)



(b)



"나무" 구조의 템플레이트  
 {NRS(스페이스 로우수)=2, NCS(스페이스 컬럼수)=2의 경우}

17



R	R	C	C
R	C	R	C
R	C	C	R
C	R	R	C
C	R	C	R
C	C	R	R

"나무" 구조의 템플레이트의 배열  
 {NRS(스페이스 로우수)=2, NCS(스페이스 컬럼수)=2의 경우}

18

순 →

M <sub>11</sub>	M <sub>12</sub>	M <sub>13</sub>	M <sub>14</sub>
M <sub>21</sub>	M <sub>22</sub>	M <sub>23</sub>	M <sub>24</sub>
M <sub>31</sub>	M <sub>32</sub>	M <sub>33</sub>	M <sub>34</sub>
M <sub>41</sub>	M <sub>42</sub>	M <sub>43</sub>	M <sub>44</sub>
M <sub>51</sub>	M <sub>52</sub>	M <sub>53</sub>	M <sub>54</sub>
M <sub>61</sub>	M <sub>62</sub>	M <sub>63</sub>	M <sub>64</sub>

배열 M(블랑 비트 어드레스 유지)  
 {NRS(스페어 로우수)=2, NCS(스페어 컬럼수)=2의 경우}



19

순 →

SR <sub>11</sub>	SR <sub>12</sub>	SR <sub>13</sub>	SR <sub>14</sub>	SR <sub>15</sub>
SR <sub>21</sub>	SR <sub>22</sub>	SR <sub>23</sub>	SR <sub>24</sub>	SR <sub>25</sub>
SR <sub>31</sub>	SR <sub>32</sub>	SR <sub>33</sub>	SR <sub>34</sub>	SR <sub>35</sub>
SR <sub>41</sub>	SR <sub>42</sub>	SR <sub>43</sub>	SR <sub>44</sub>	SR <sub>45</sub>
SR <sub>51</sub>	SR <sub>52</sub>	SR <sub>53</sub>	SR <sub>54</sub>	SR <sub>55</sub>
SR <sub>61</sub>	SR <sub>62</sub>	SR <sub>63</sub>	SR <sub>64</sub>	SR <sub>65</sub>

배열 SR(유효 비트 유지)  
 {NRS(스페어 로우수)=2, NCS(스페어 컬럼수)=2의 경우}

20

순 →

R0	R1	C1	
R0	C0	R1	C1
R0	C0	C1	
C0	R0	R1	C1
C0	R0	C1	
C0	C2	R0	R1

배열 M  
 {NRS(스페어 로우수)=2, NCS(스페어 컬럼수)=2의 경우}

21

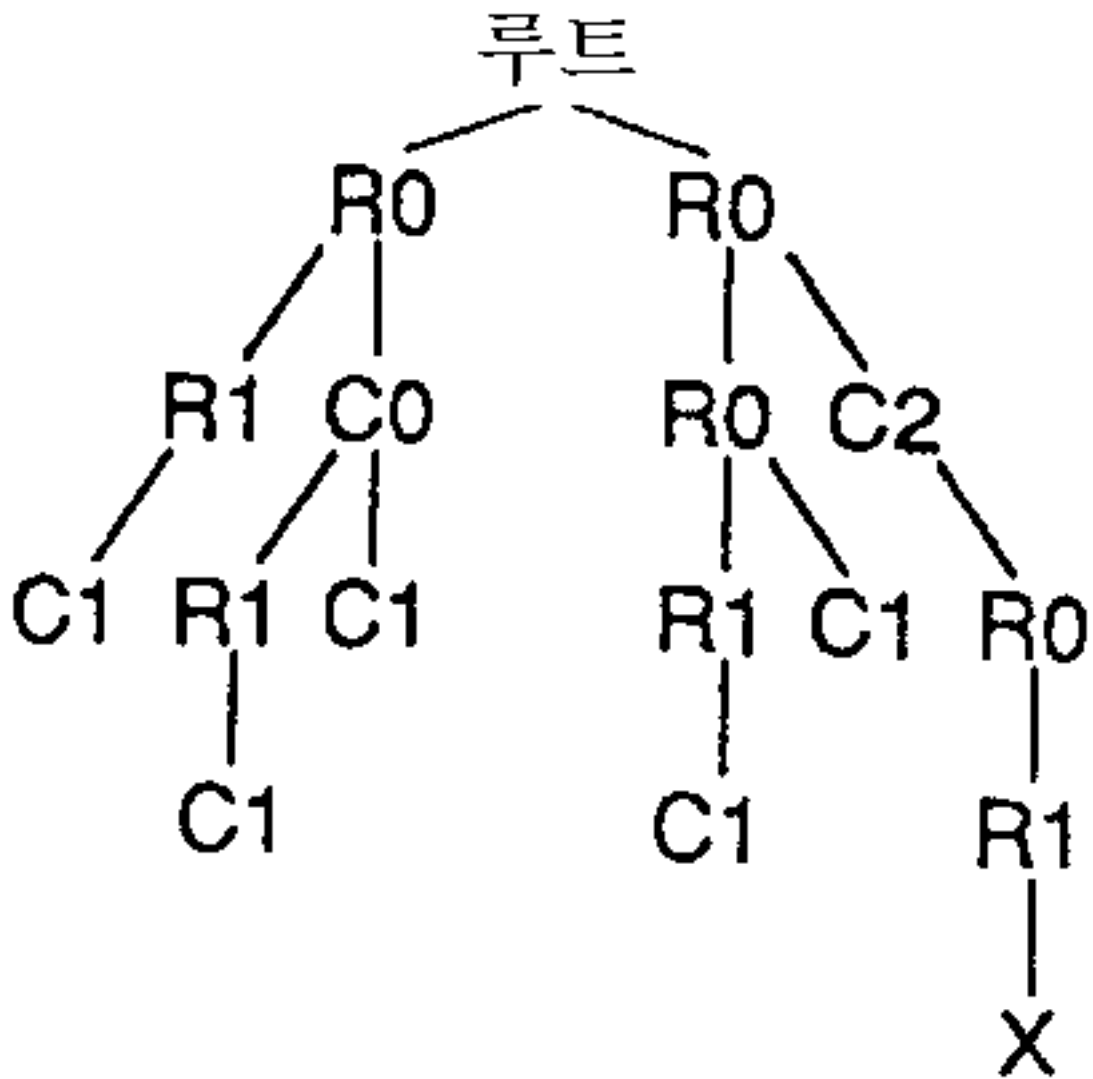
순 →

1	1	1	0	0
1	1	1	1	0
1	1	1	0	0
1	1	1	1	0
1	1	1	0	0
1	1	1	1	1

배열 SR

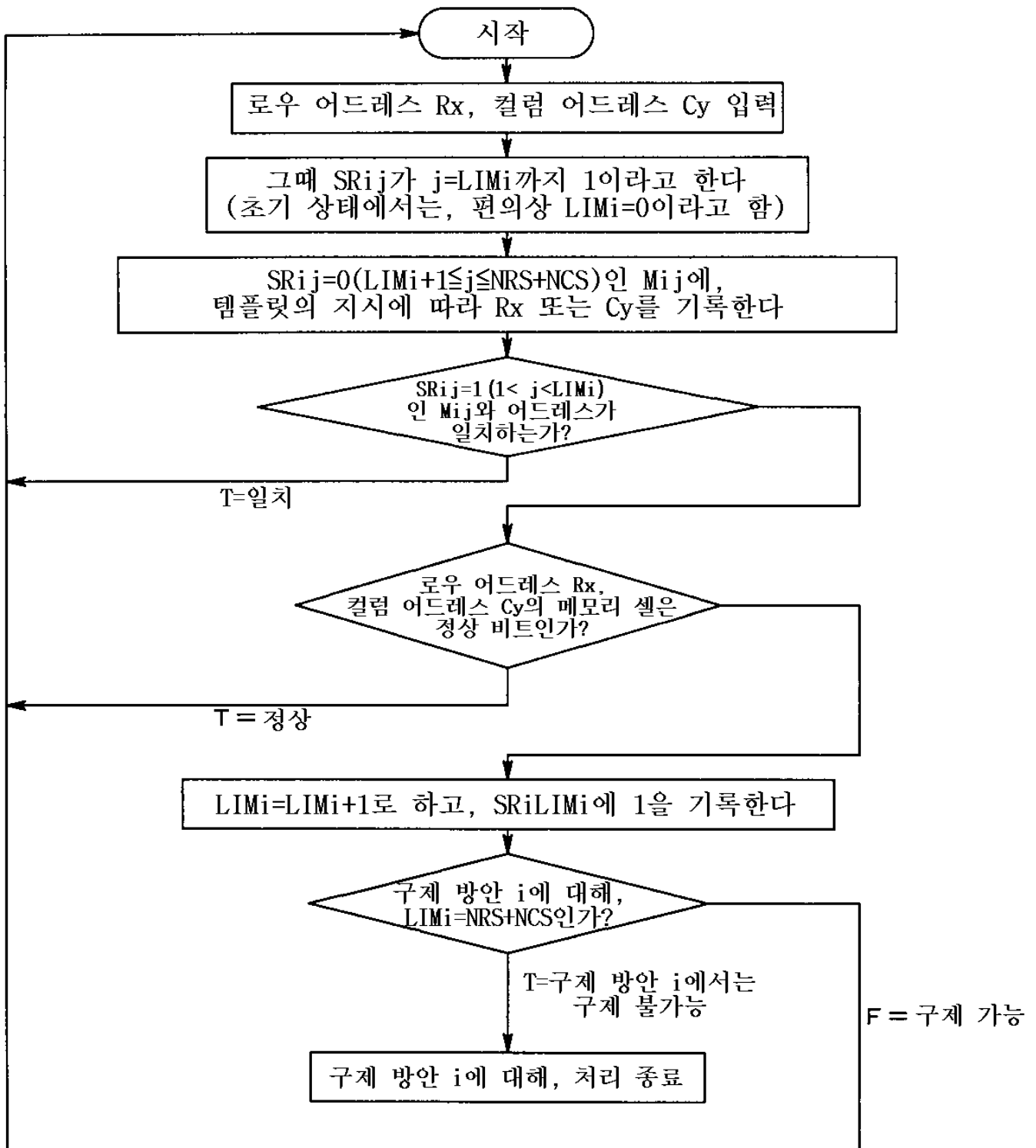
{NRS(스페어 로우수)=2, NCS(스페어 컬럼수)=2의 경우}

22



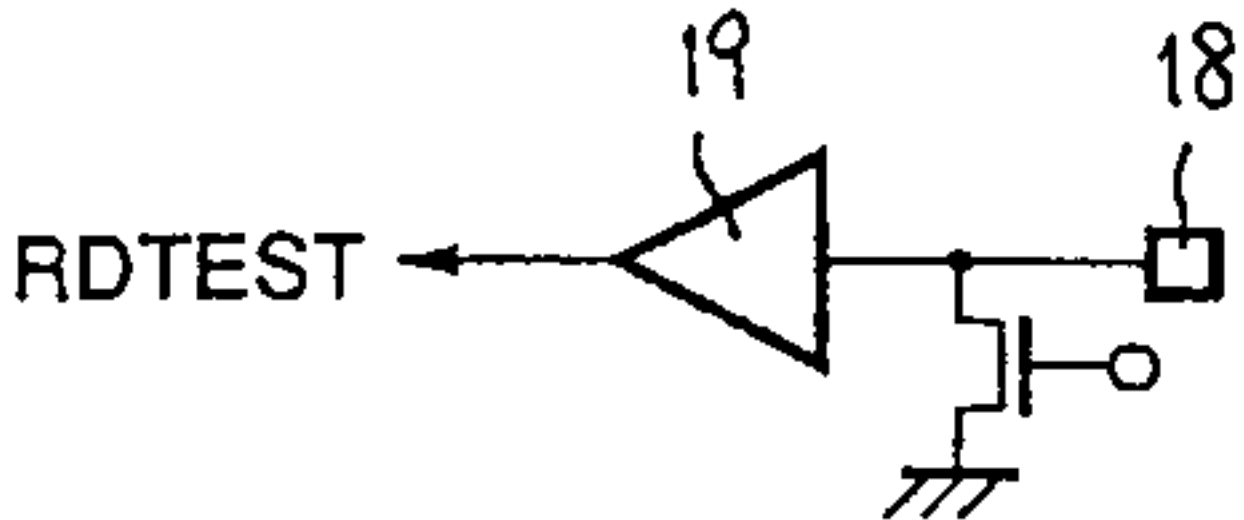
1	R	R	R	R	C	C	C	C	36	C	R	R	R	R	C	C	C
2	R	R	R	C	R	C	C	C	37	C	R	R	R	C	R	C	C
3	R	R	R	C	C	R	C	C	38	C	R	R	R	C	C	R	C
4	R	R	R	C	C	C	R	C	39	C	R	R	R	C	C	C	R
5	R	R	R	C	C	C	C	R	40	C	R	R	C	R	R	C	C
6	R	R	C	R	R	C	C	C	41	C	R	R	C	R	C	R	C
7	R	R	C	R	C	R	C	C	42	C	R	R	C	R	C	C	R
8	R	R	C	R	C	C	R	C	43	C	R	R	C	C	R	R	C
9	R	R	C	R	C	C	C	R	44	C	R	R	C	C	R	C	R
10	R	R	C	C	R	R	C	C	45	C	R	R	C	C	C	R	R
11	R	R	C	C	R	C	R	C	46	C	R	C	R	R	R	C	C
12	R	R	C	C	R	C	C	R	47	C	R	C	R	R	C	R	C
13	R	R	C	C	C	R	R	C	48	C	R	C	R	R	C	C	R
14	R	R	C	C	C	R	C	R	49	C	R	C	R	C	R	R	C
15	R	R	C	C	C	C	R	R	50	C	R	C	R	C	R	C	R
16	R	C	R	R	R	C	C	C	51	C	R	C	R	C	C	R	R
17	R	C	R	R	C	R	C	C	52	C	R	C	C	R	R	R	C
18	R	C	R	R	C	C	R	C	53	C	R	C	C	R	R	C	R
19	R	C	R	R	C	C	C	R	54	C	R	C	C	R	C	R	R
20	R	C	R	C	R	R	C	C	55	C	R	C	C	C	R	R	R
21	R	C	R	C	R	C	R	C	56	C	C	R	R	R	R	C	C
22	R	C	R	C	R	C	C	R	57	C	C	R	R	R	C	R	C
23	R	C	R	C	C	R	R	C	58	C	C	R	R	R	C	C	R
24	R	C	R	C	C	R	C	R	59	C	C	R	R	C	R	R	C
25	R	C	R	C	C	C	R	C	60	C	C	R	R	C	R	C	R
26	R	C	C	R	R	R	C	C	61	C	C	R	R	C	C	R	R
27	R	C	C	R	R	C	R	C	62	C	C	R	C	R	R	R	R
28	R	C	C	R	R	C	C	R	63	C	C	R	C	R	R	C	R
29	R	C	C	R	C	R	R	C	64	C	C	R	C	R	C	R	R
30	R	C	C	R	C	R	C	R	65	C	C	R	C	C	R	R	R
31	R	C	C	R	C	C	R	R	66	C	C	C	R	R	R	R	C
32	R	C	C	C	R	R	R	C	67	C	C	C	R	R	R	C	R
33	R	C	C	C	R	R	C	R	68	C	C	C	R	R	C	R	R
34	R	C	C	C	R	C	R	R	69	C	C	C	R	C	R	R	R
35	R	C	C	C	C	R	R	R	70	C	C	C	C	R	R	R	R

"나무" 구조의 템플릿의 배열  
 {NRS(스페이스 로우수)=4, NCS(스페이스 컬럼수)=4의 경우}

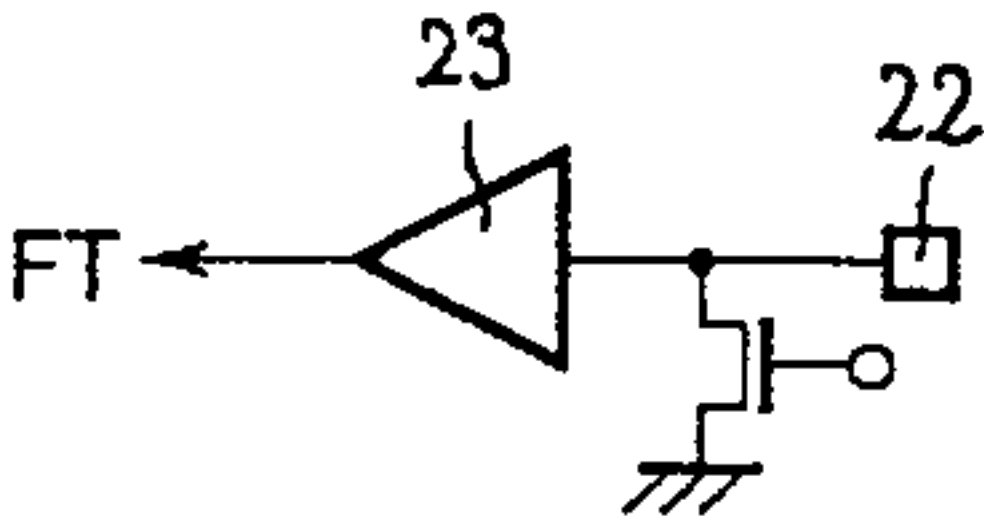




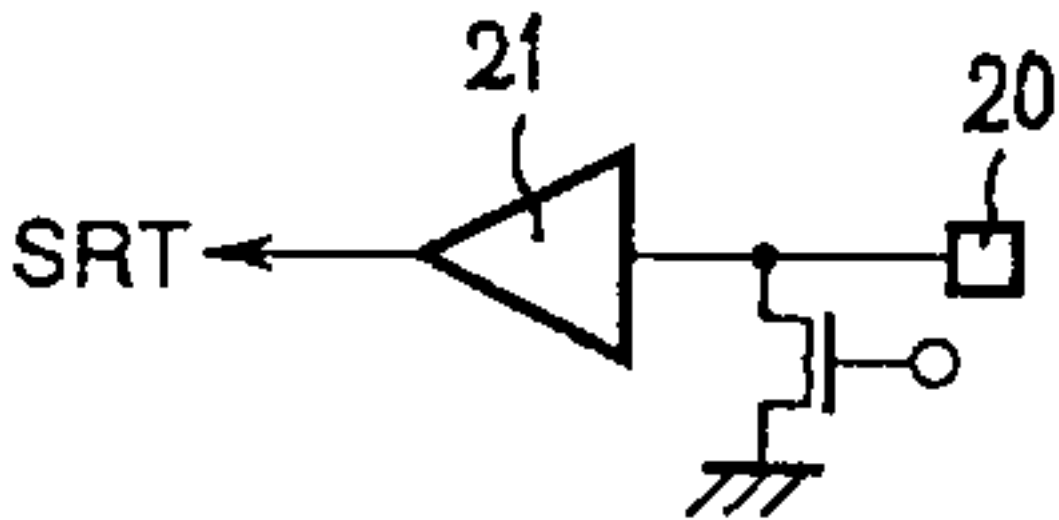
26



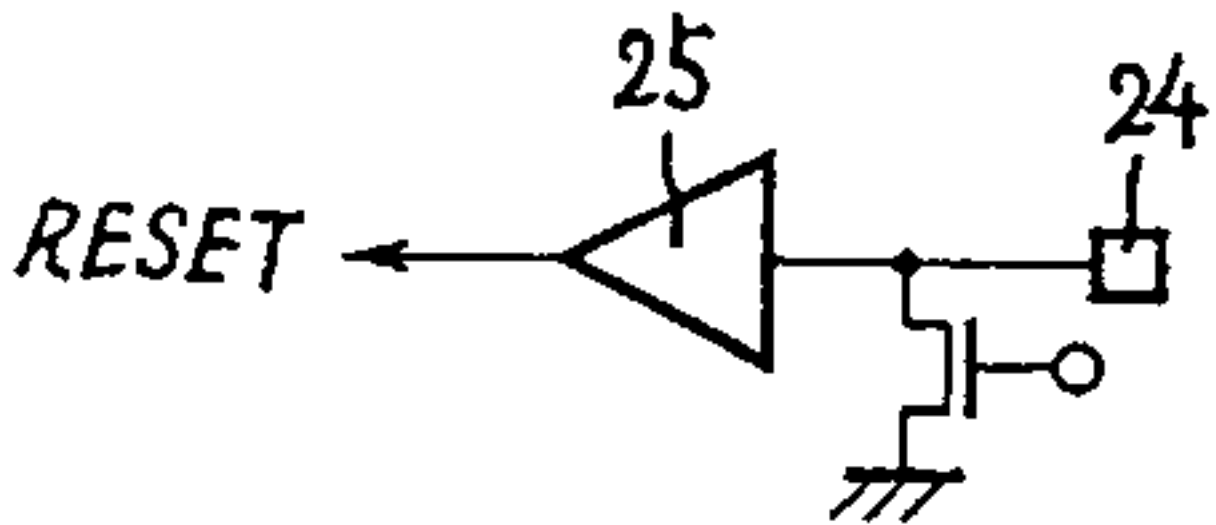
27



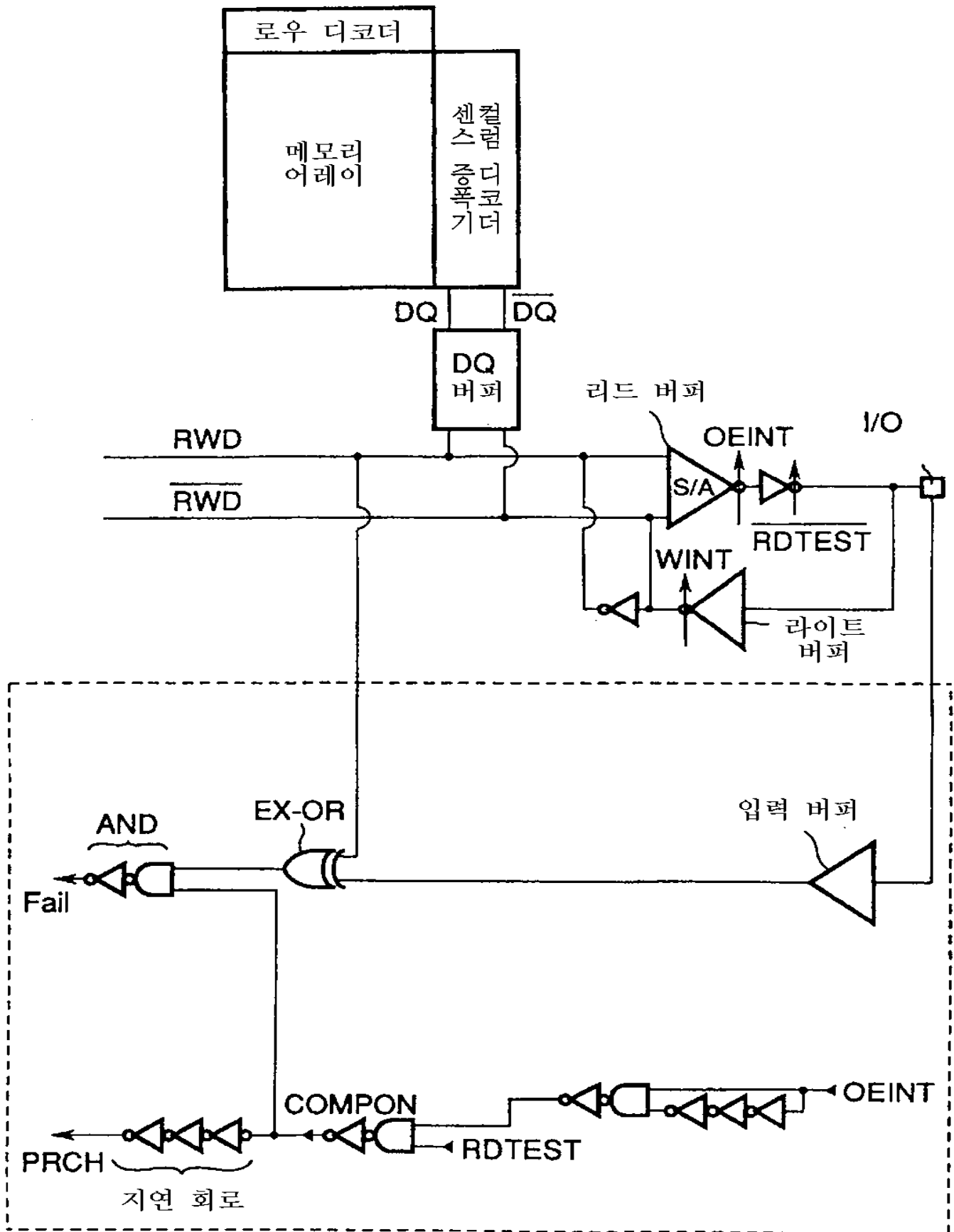
28



29

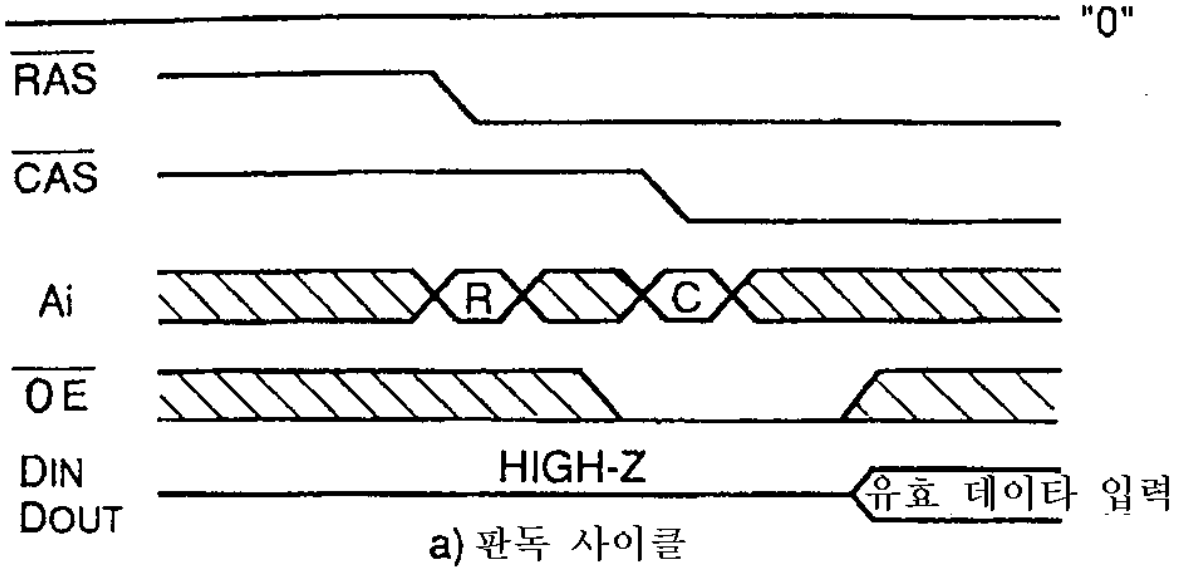




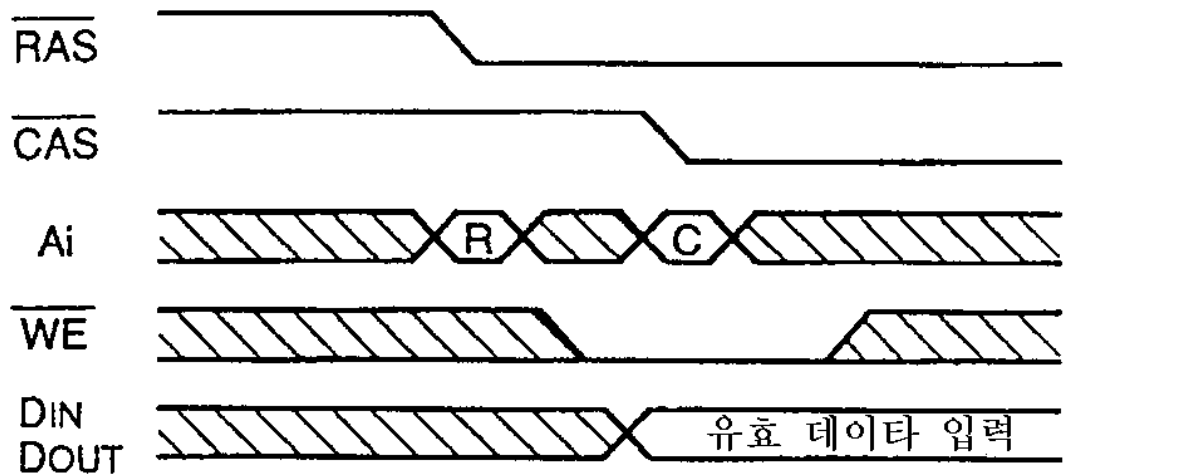


RDTEST

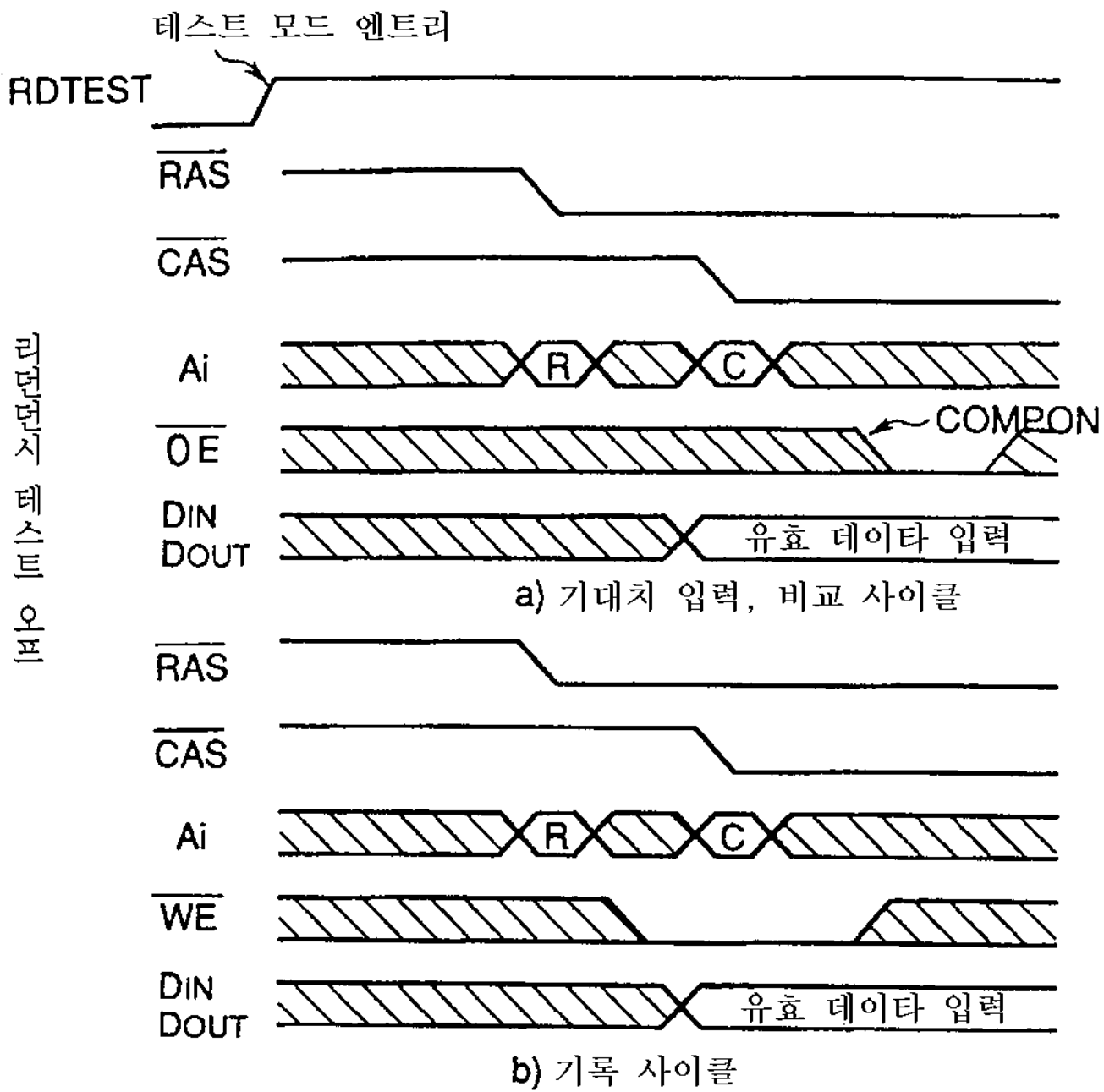
통상 모드

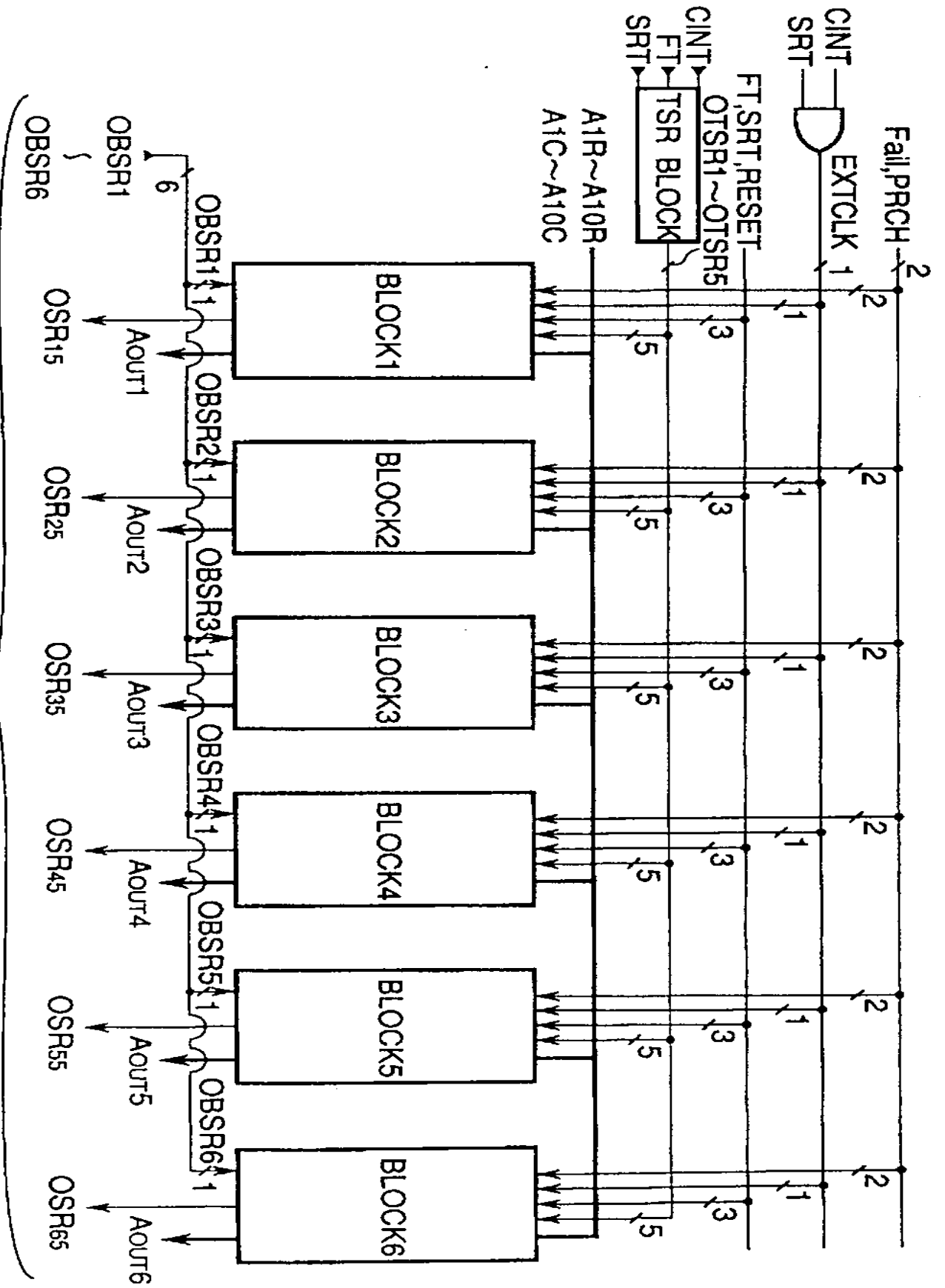


a) 판독 사이클

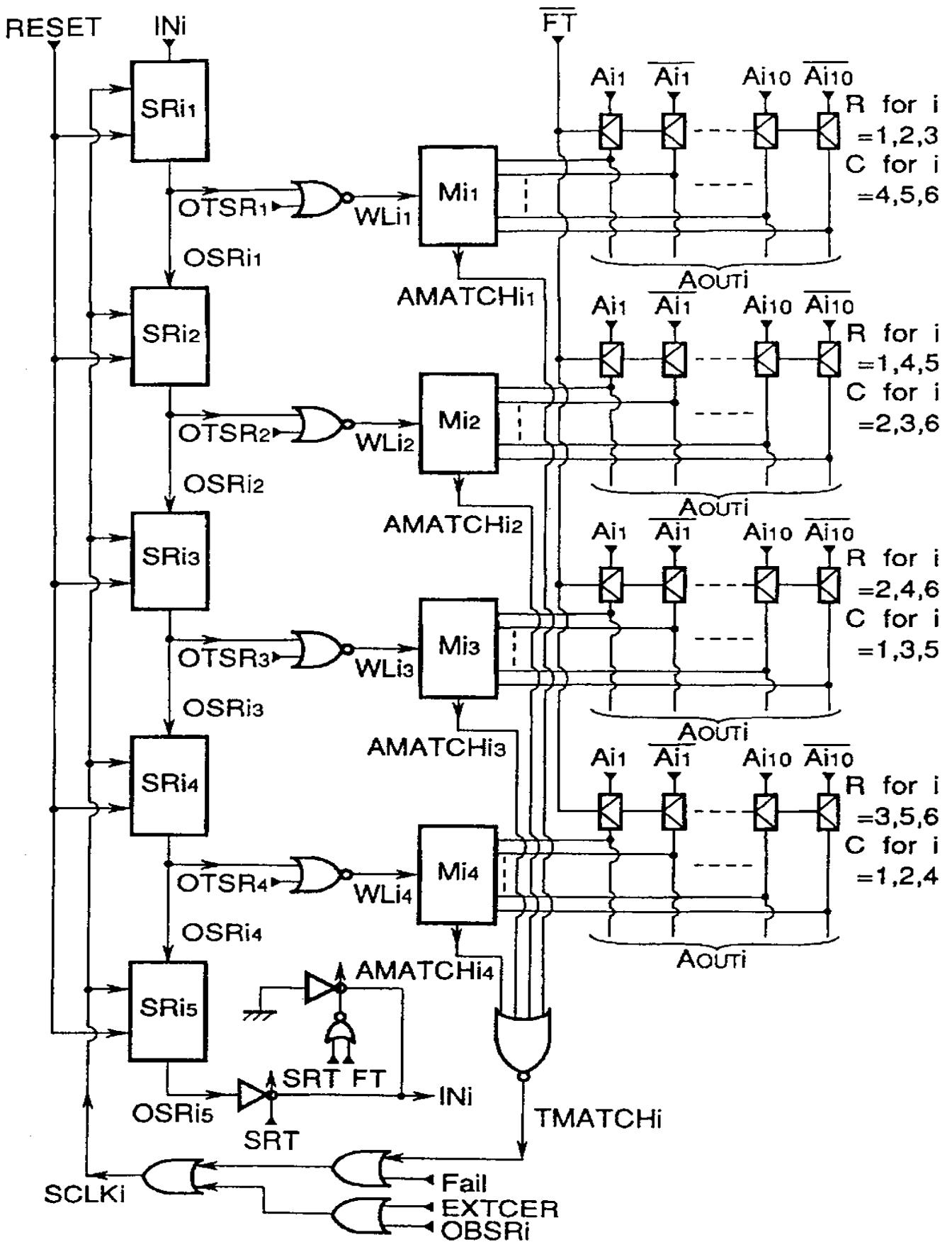


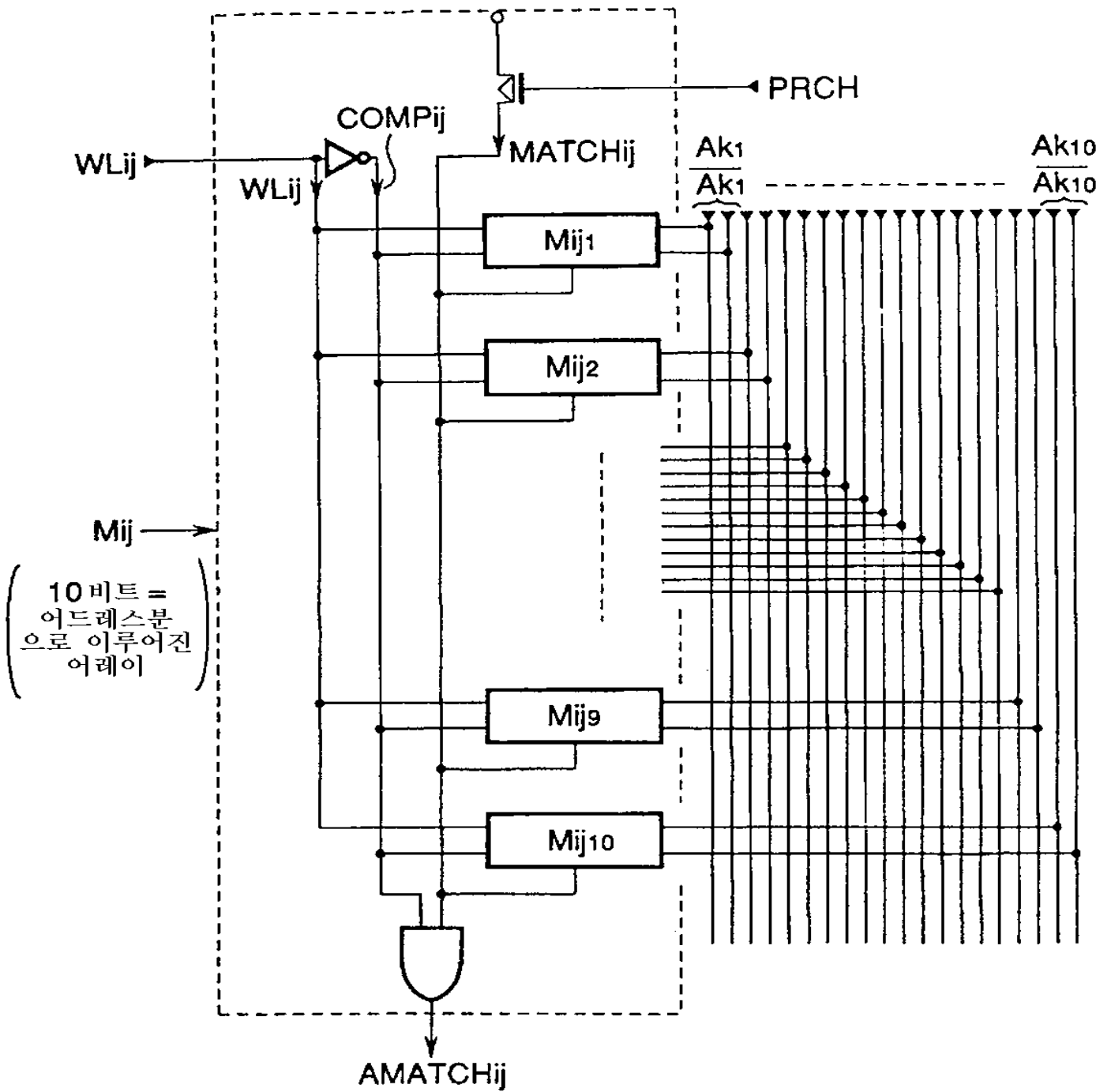
b) 기록 사이클





페이지 데이터 출력 제어 회로

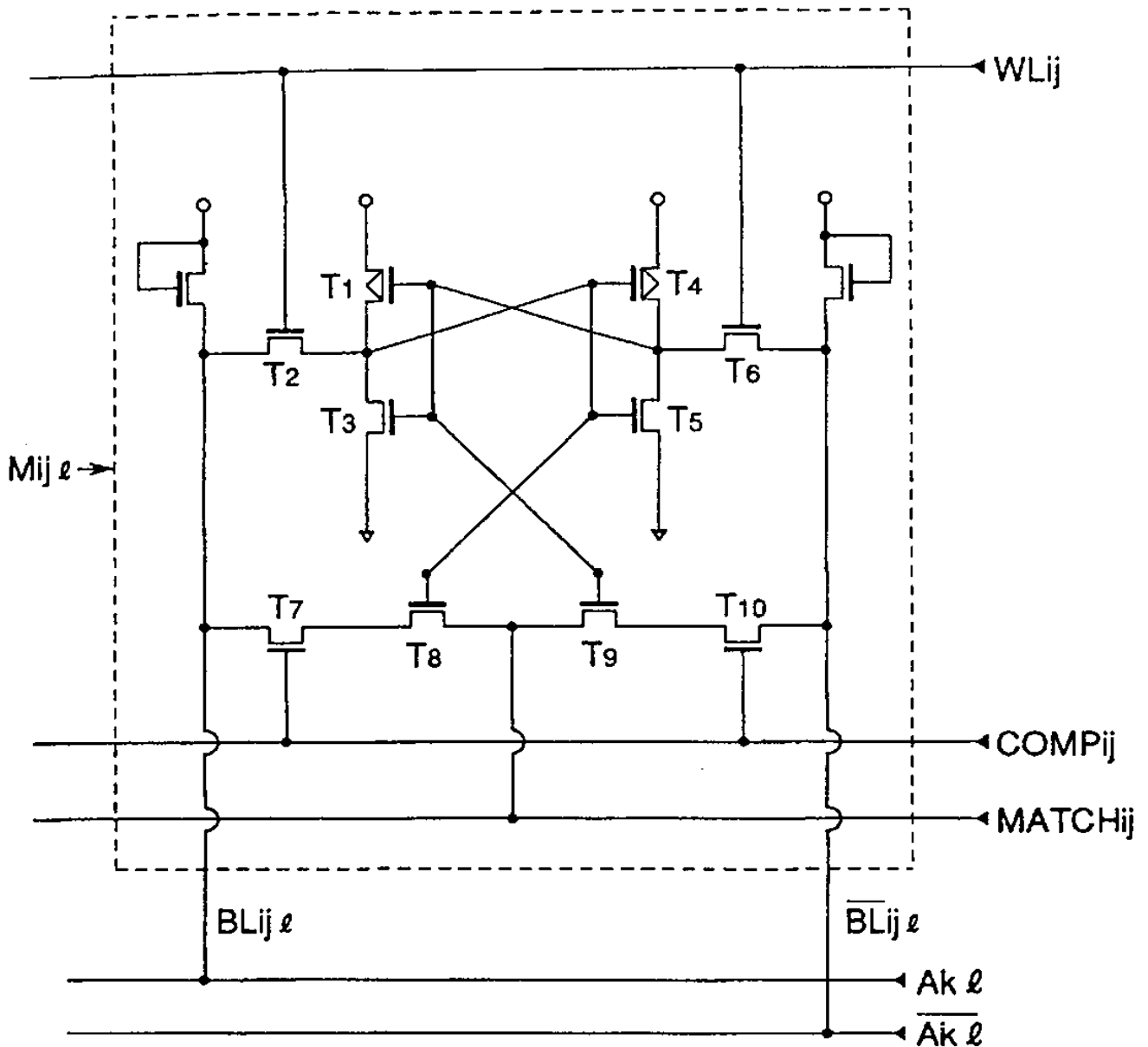




$$i=1 \sim 6, j=1 \sim 4$$

$$k=R(\text{로우}) \text{ for}(i,j) = (1,1)(1,2)(2,1)(2,3) \\ (3,1)(3,4)(4,2)(4,3) \\ (5,2)(5,4)(6,3)(6,4)$$

$$=C(\text{컬럼}) \text{ for}(i,j) = (1,3)(1,4)(2,2)(2,4) \\ (3,2)(3,3)(4,1)(4,4) \\ (5,1)(5,3)(6,1)(6,2)$$



$i=1\sim 6, j=1\sim 4$

$k=R(\text{로우}) \text{ for}(i,j) = (1,1)(1,2)(2,1)(2,3)$   
 $(3,1)(3,4)(4,2)(4,3)$   
 $(5,2)(5,4)(6,3)(6,4)$

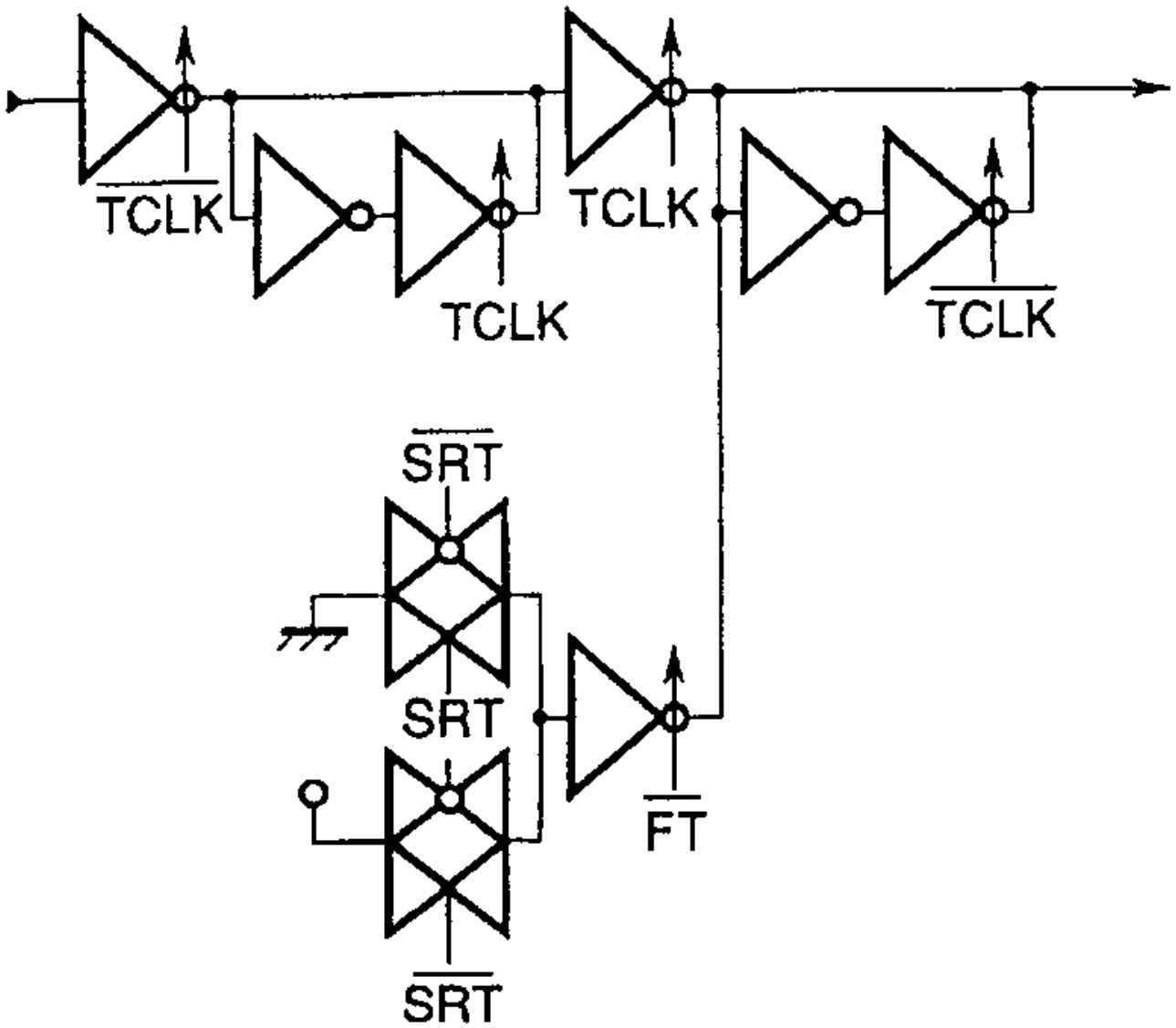
$=C(\text{컬럼}) \text{ for}(i,j) = (1,3)(1,4)(2,2)(2,4)$   
 $(3,2)(3,3)(4,1)(4,4)$   
 $(5,1)(5,3)(6,1)(6,2)$

$l=1\sim 10$

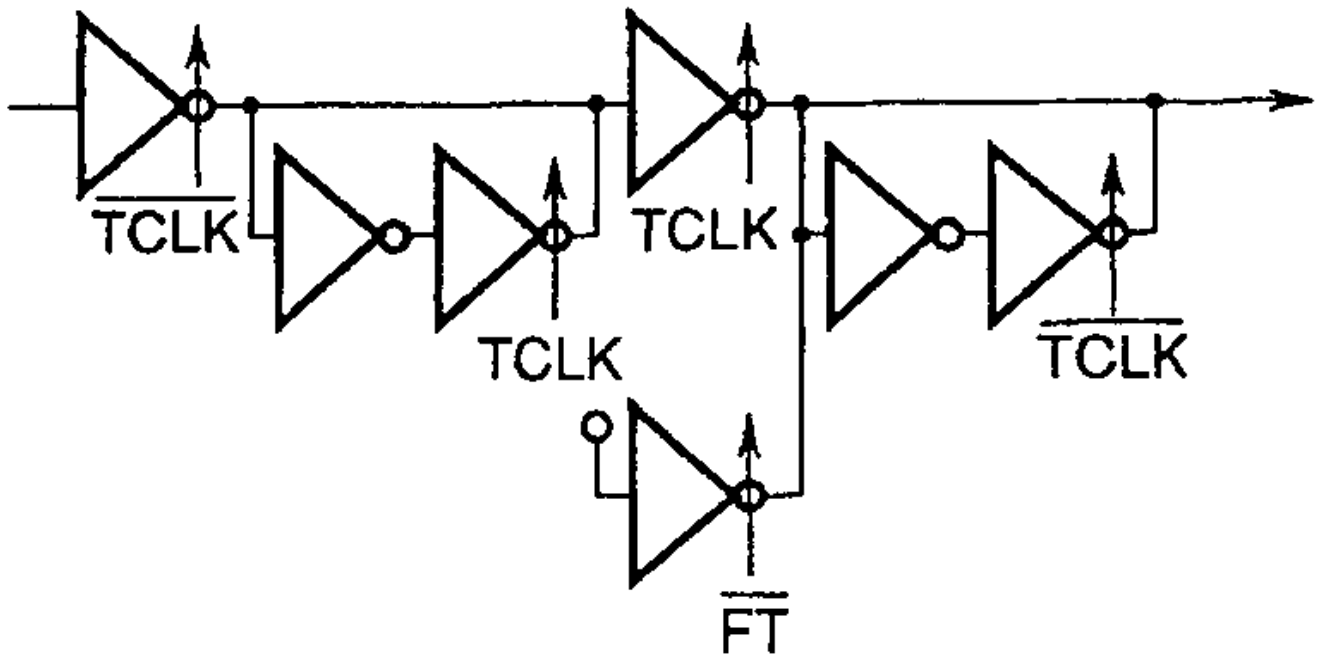


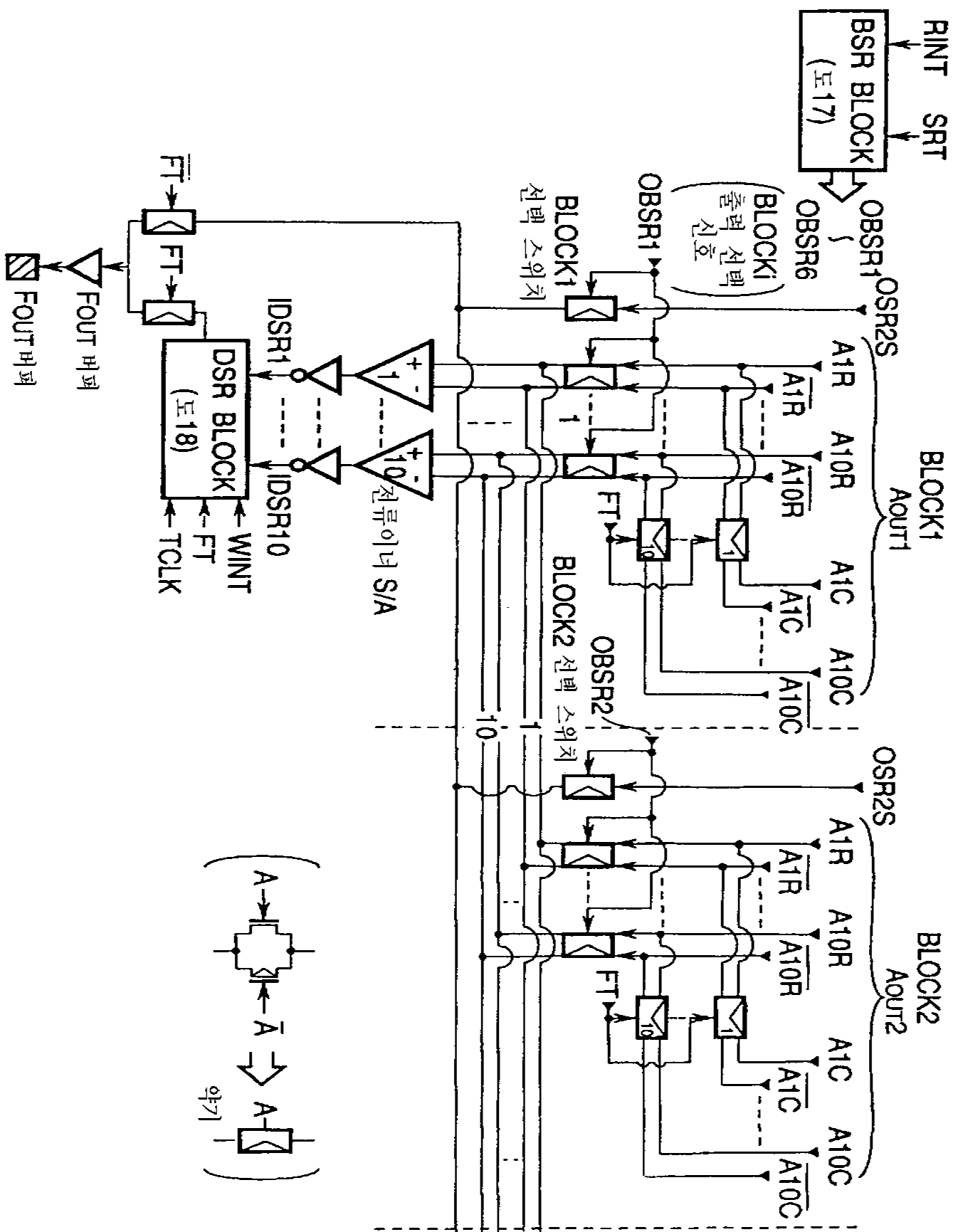


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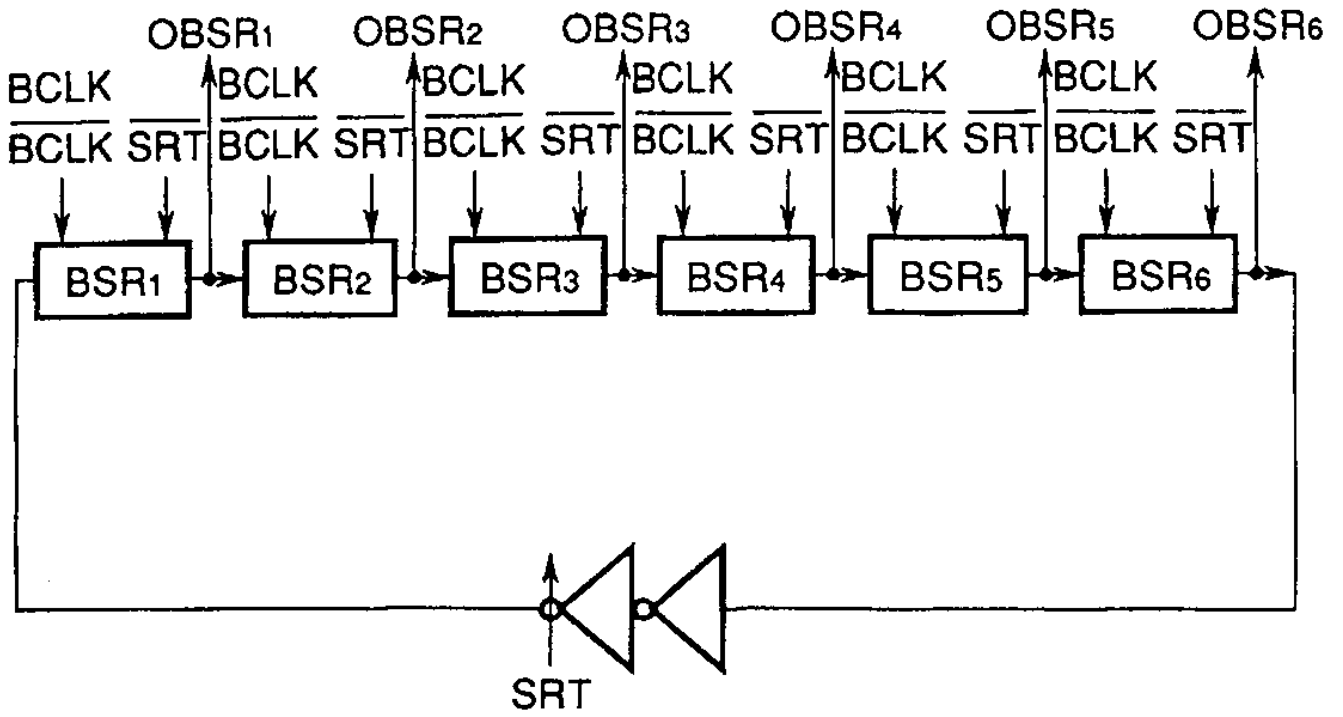


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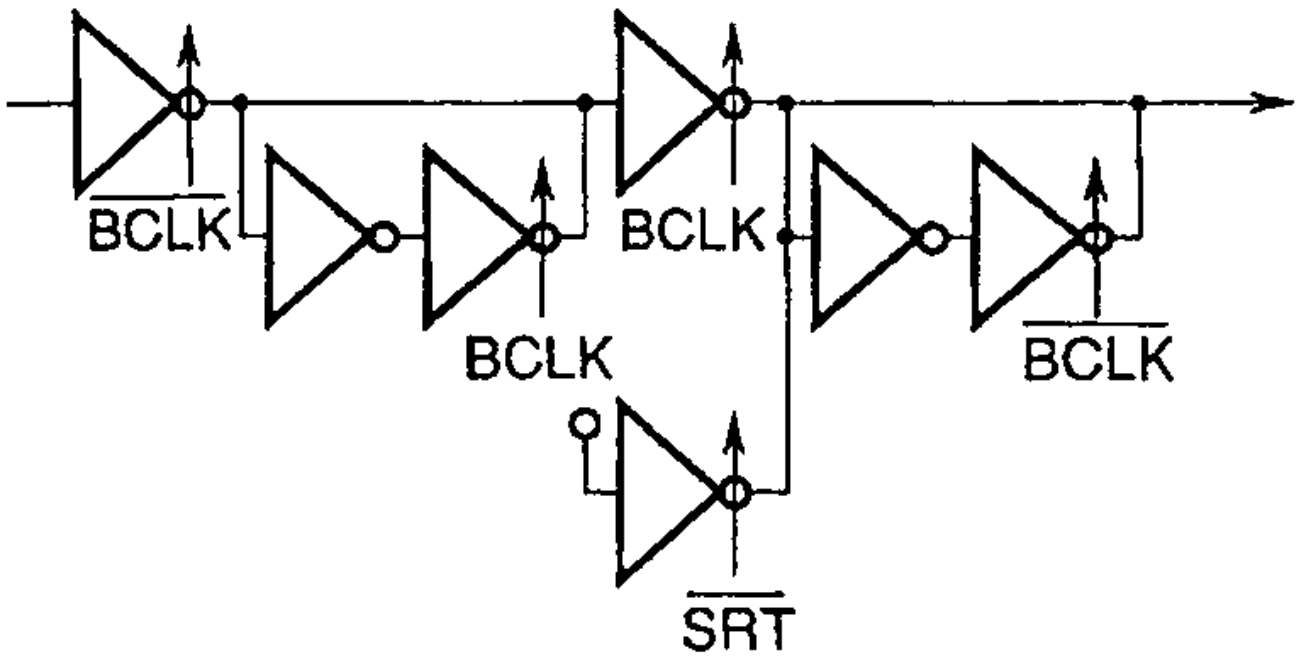
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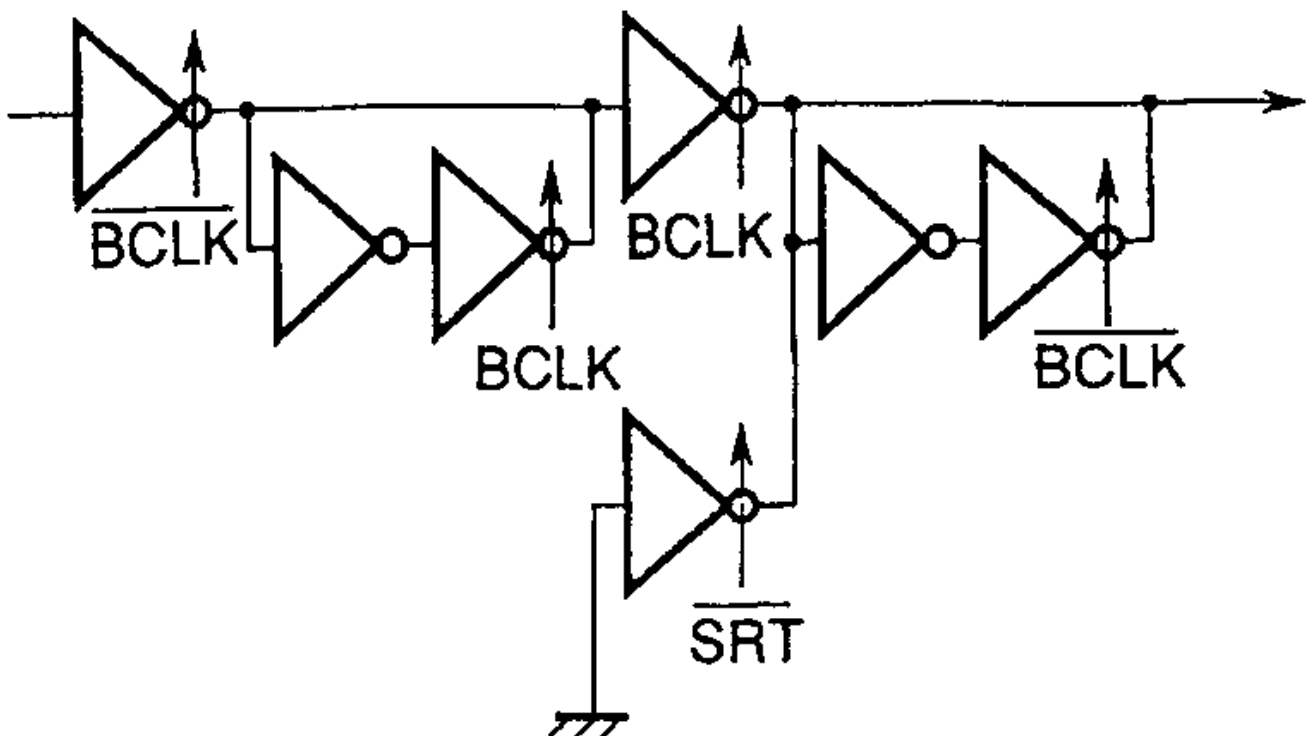
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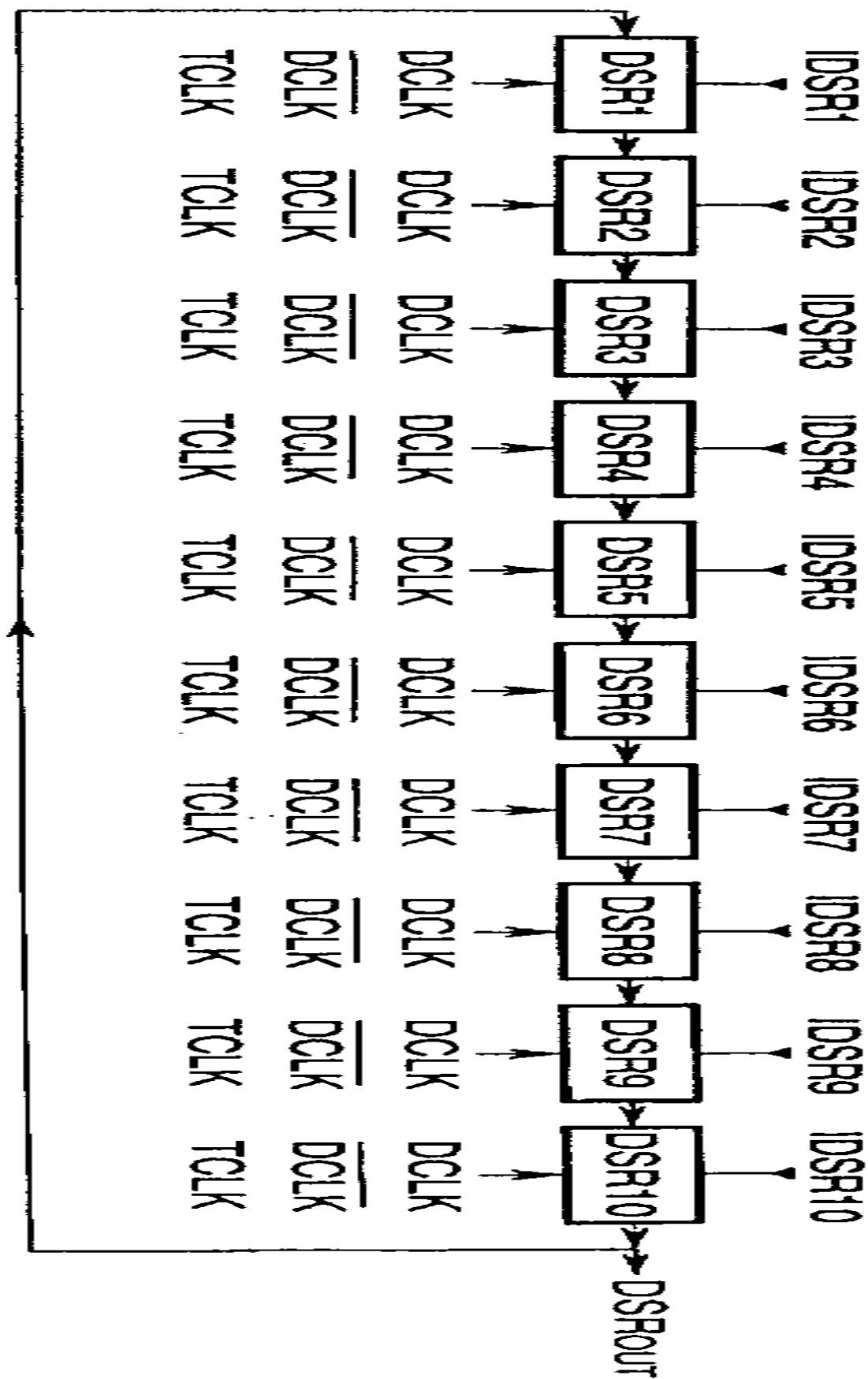


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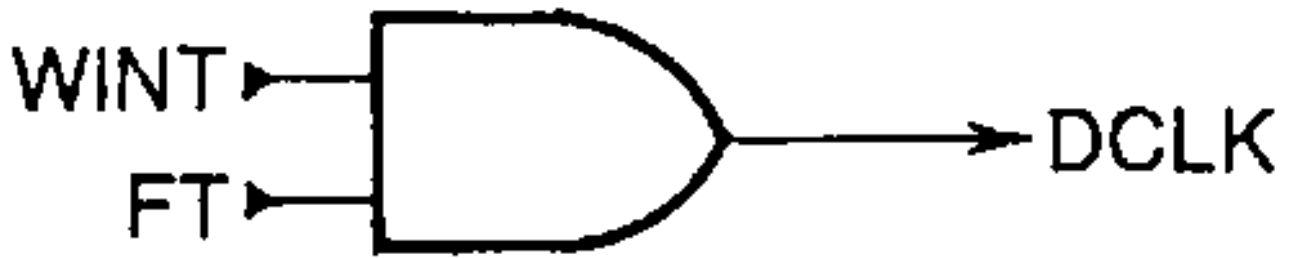


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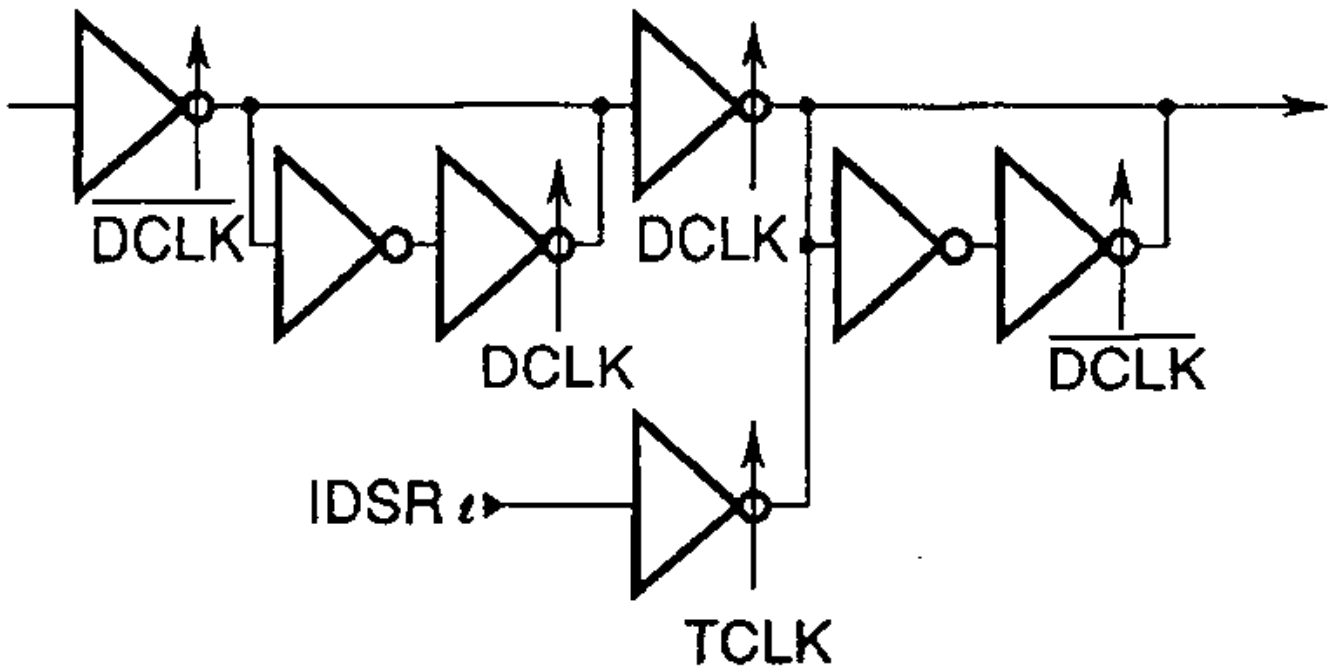


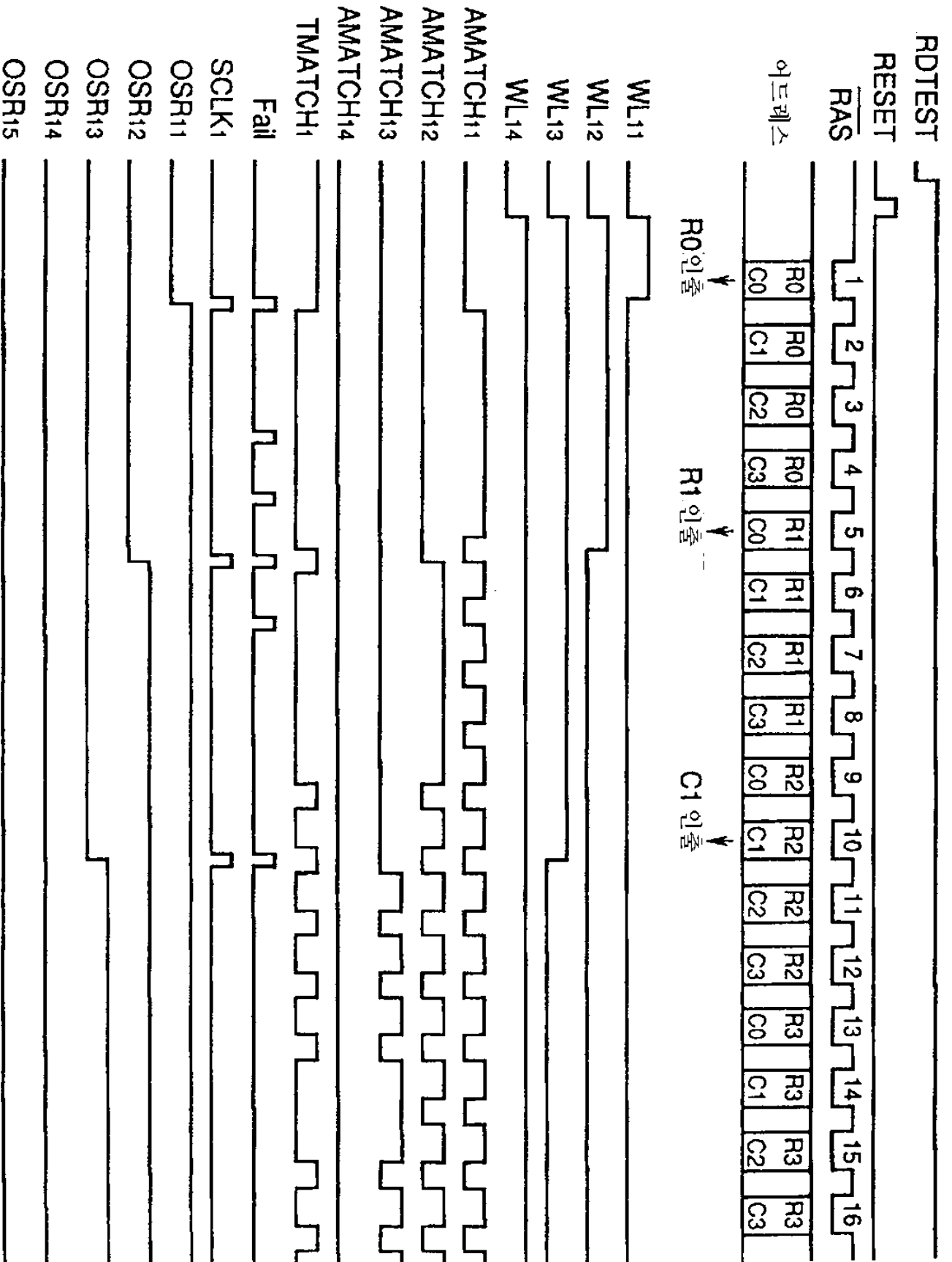


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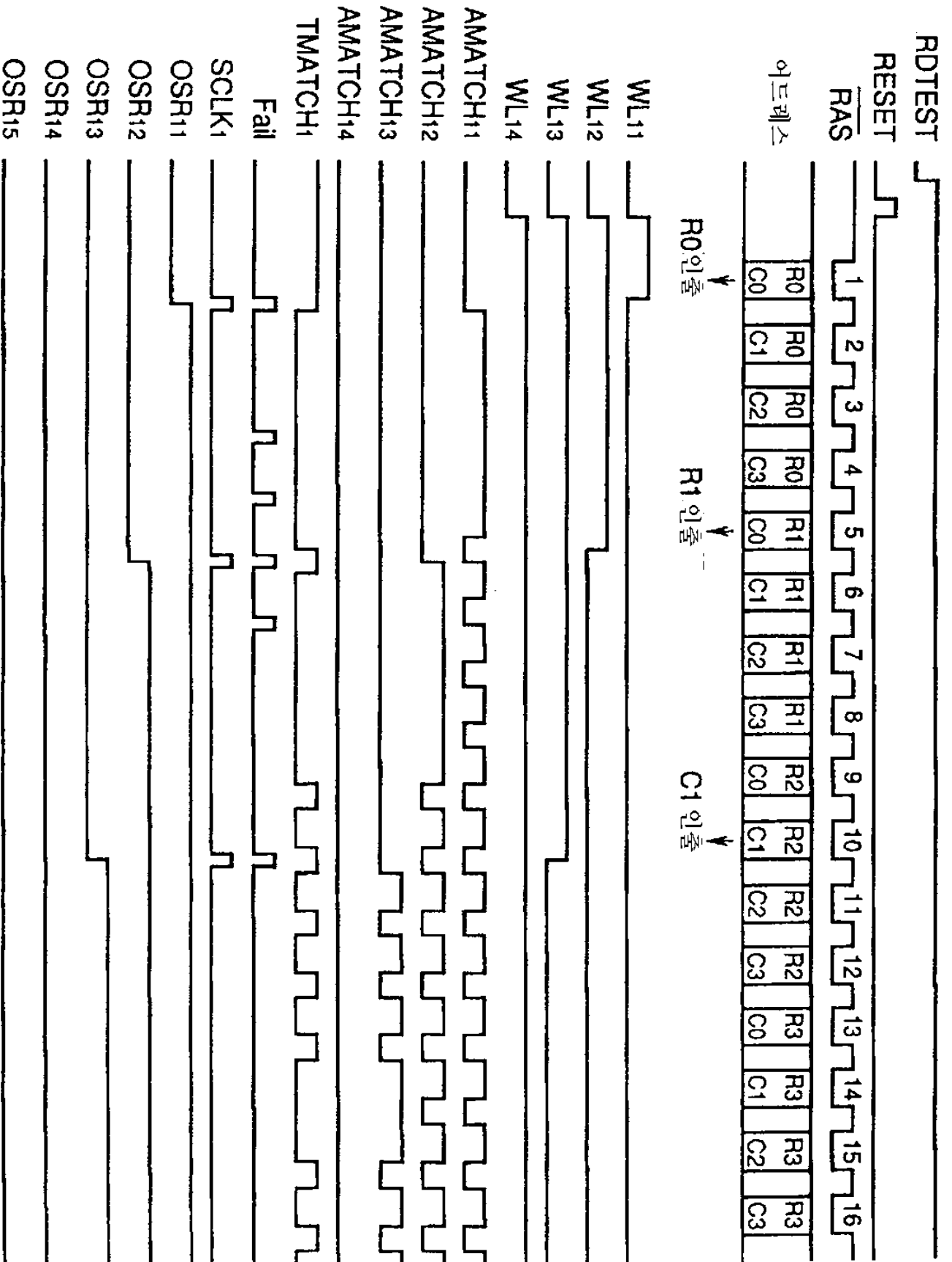


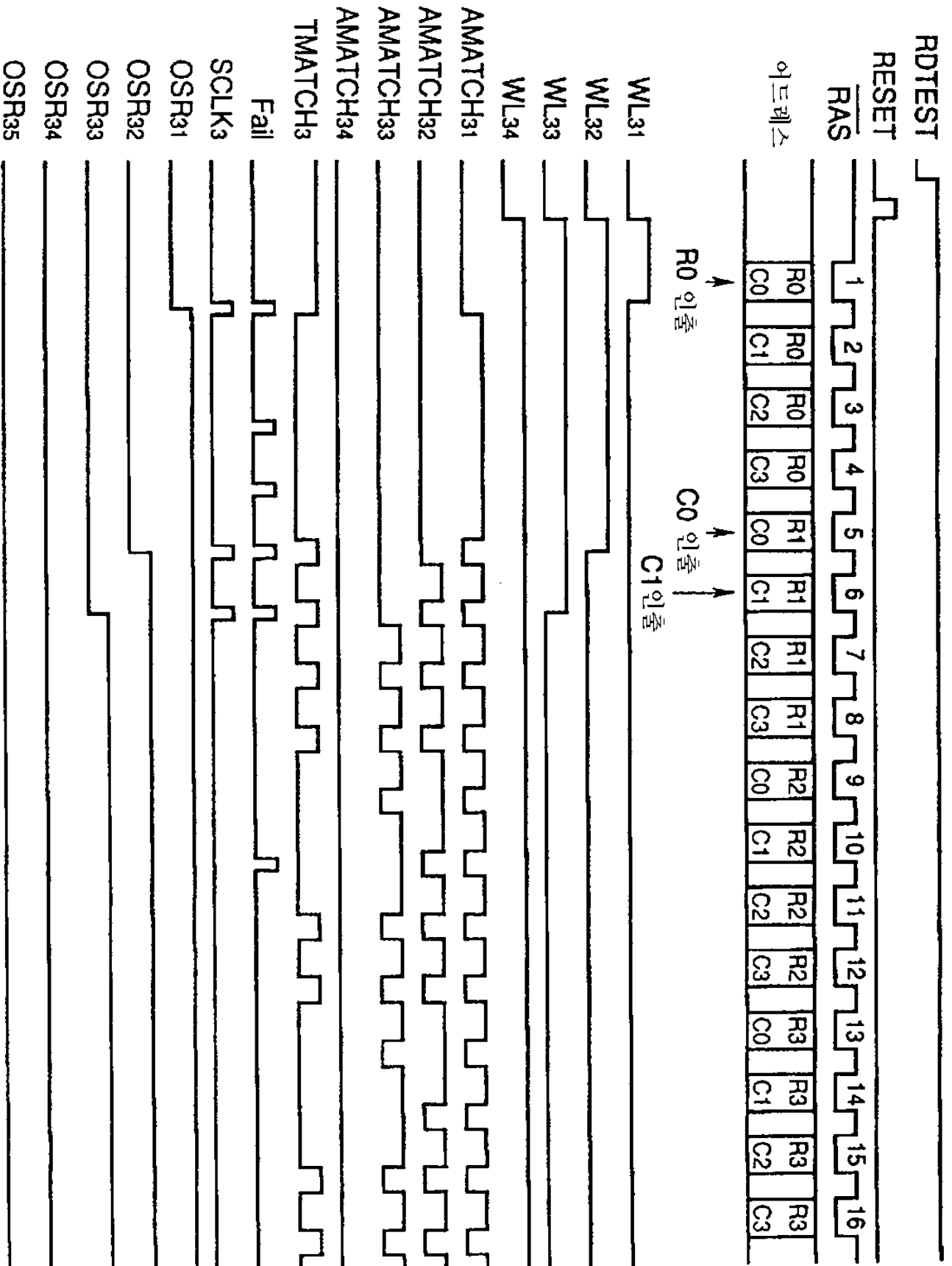
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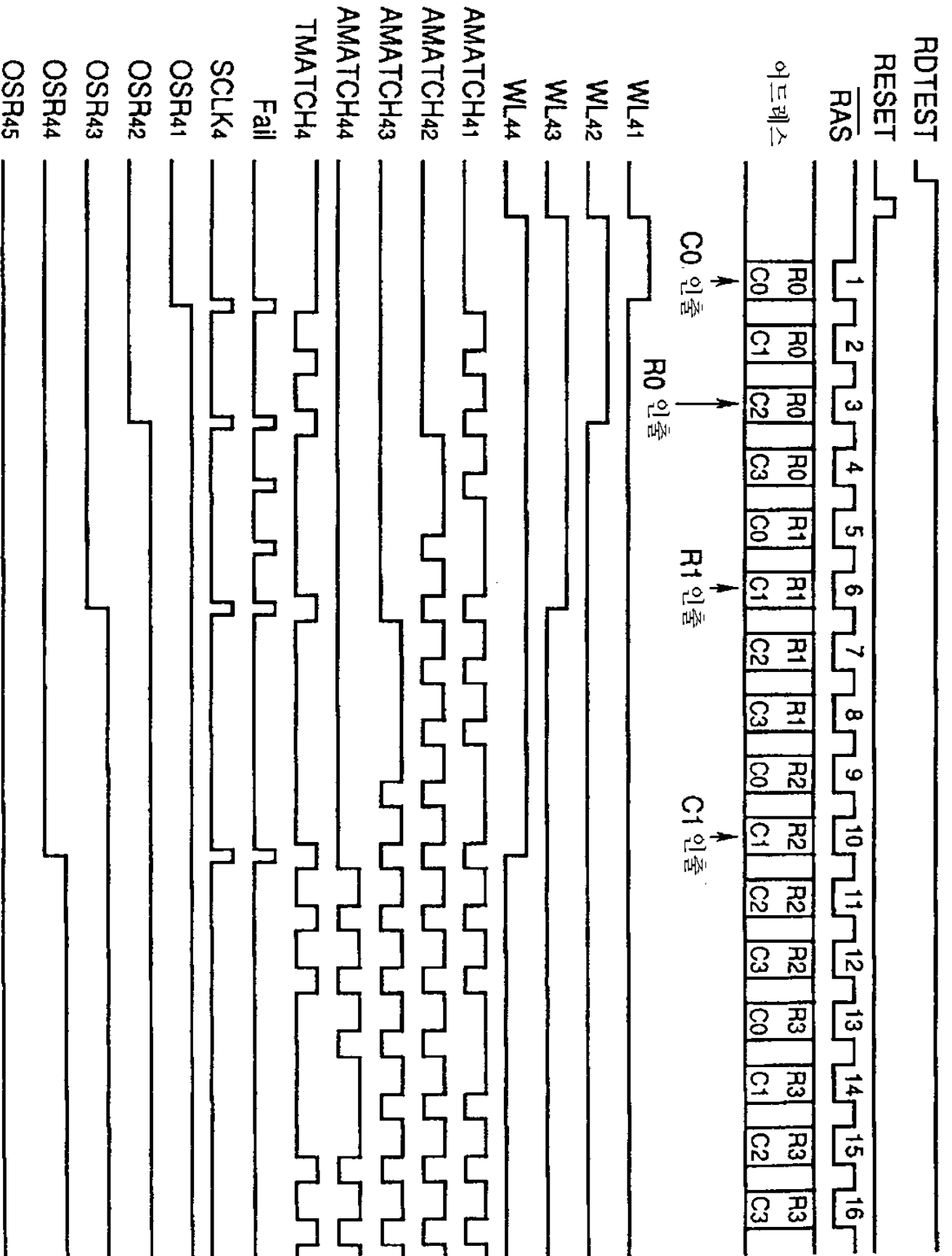


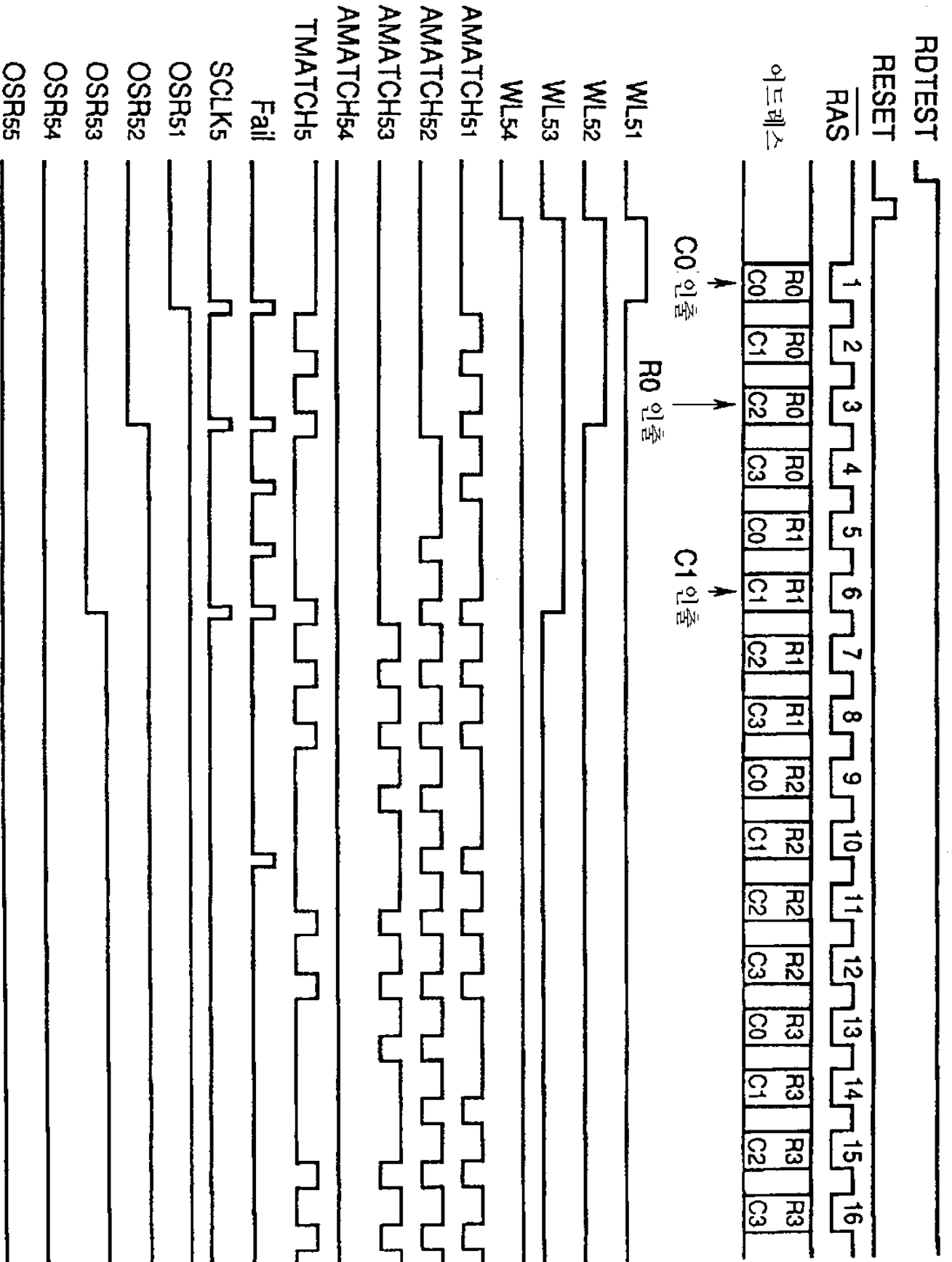


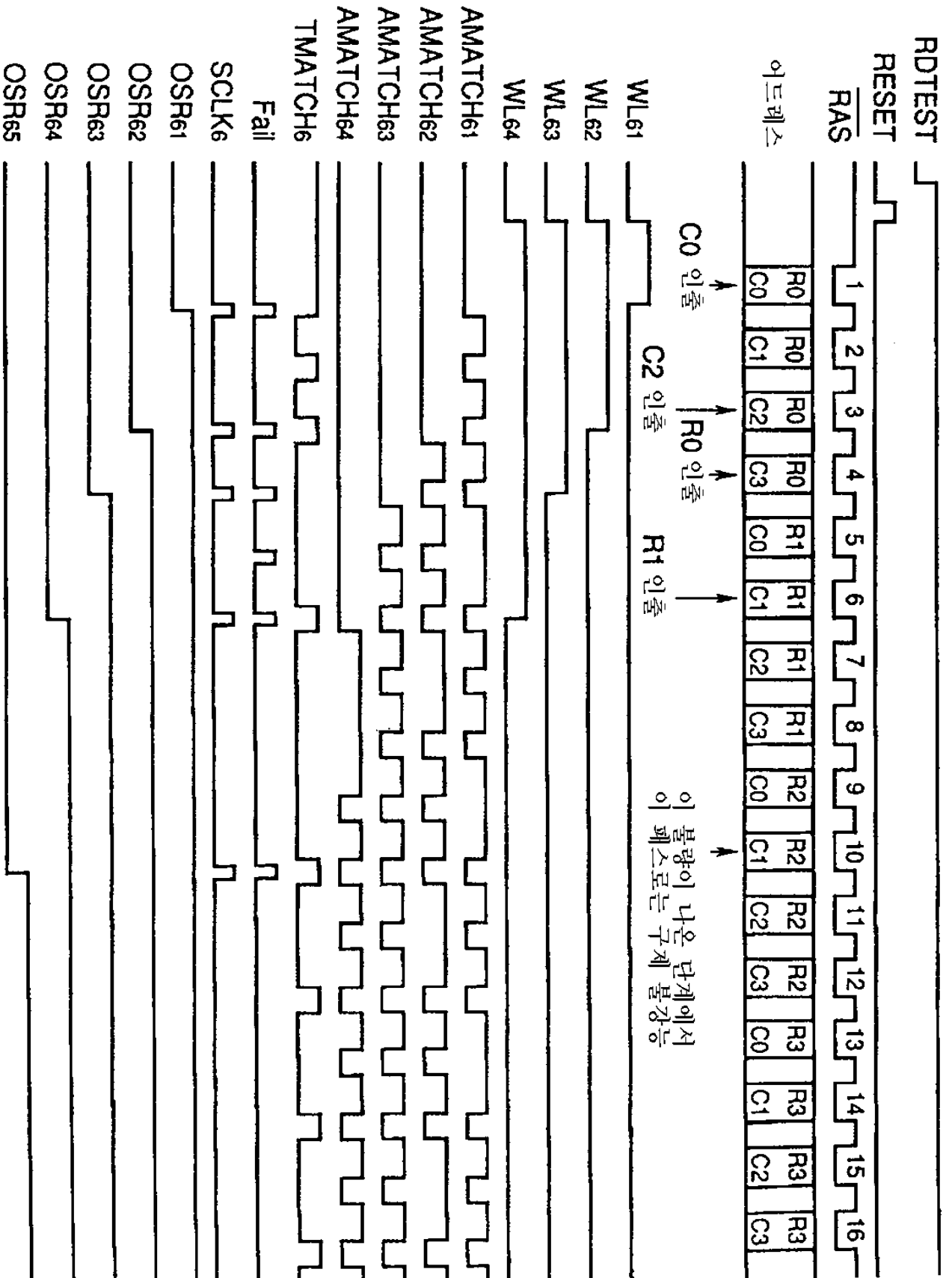


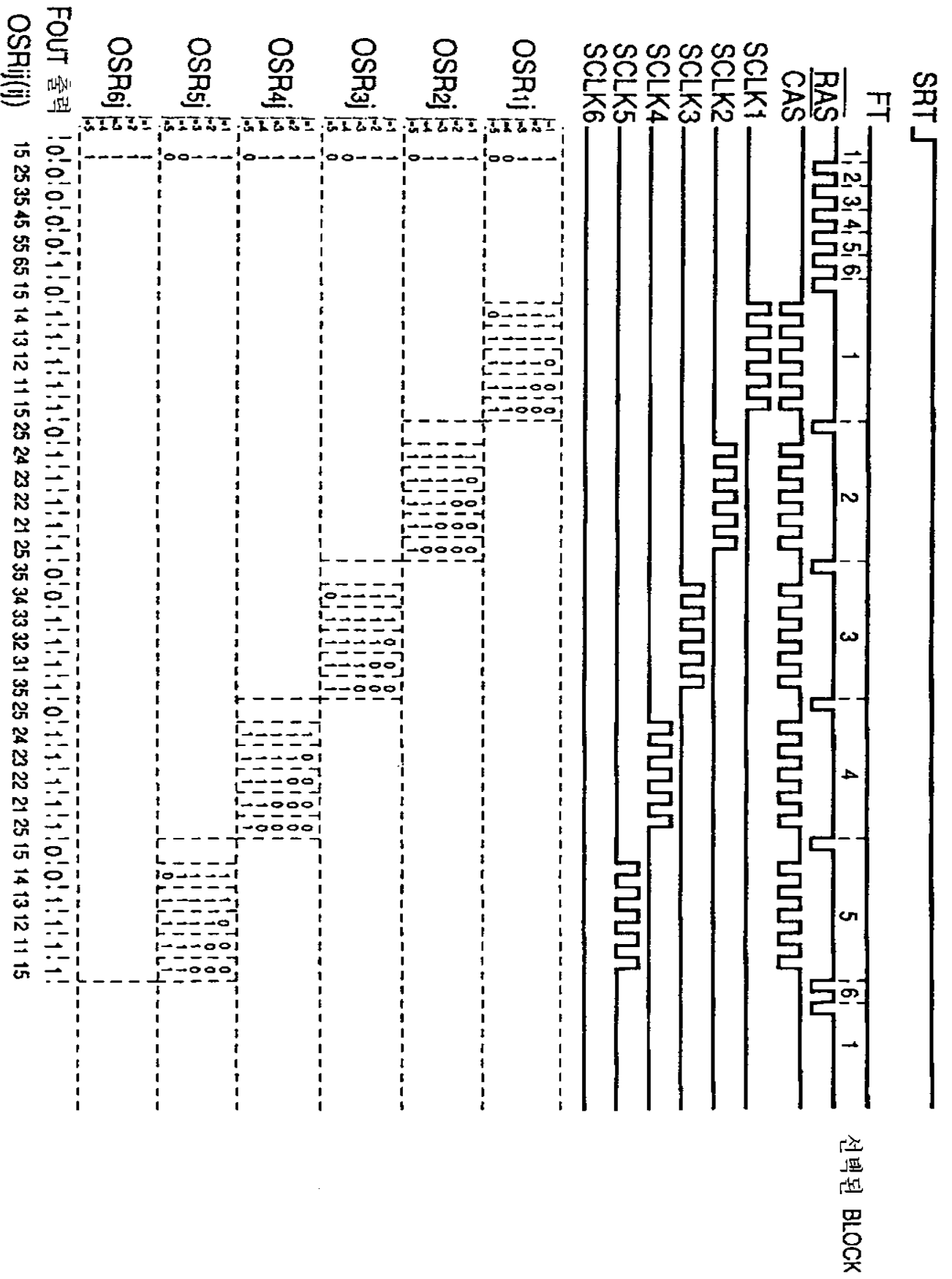


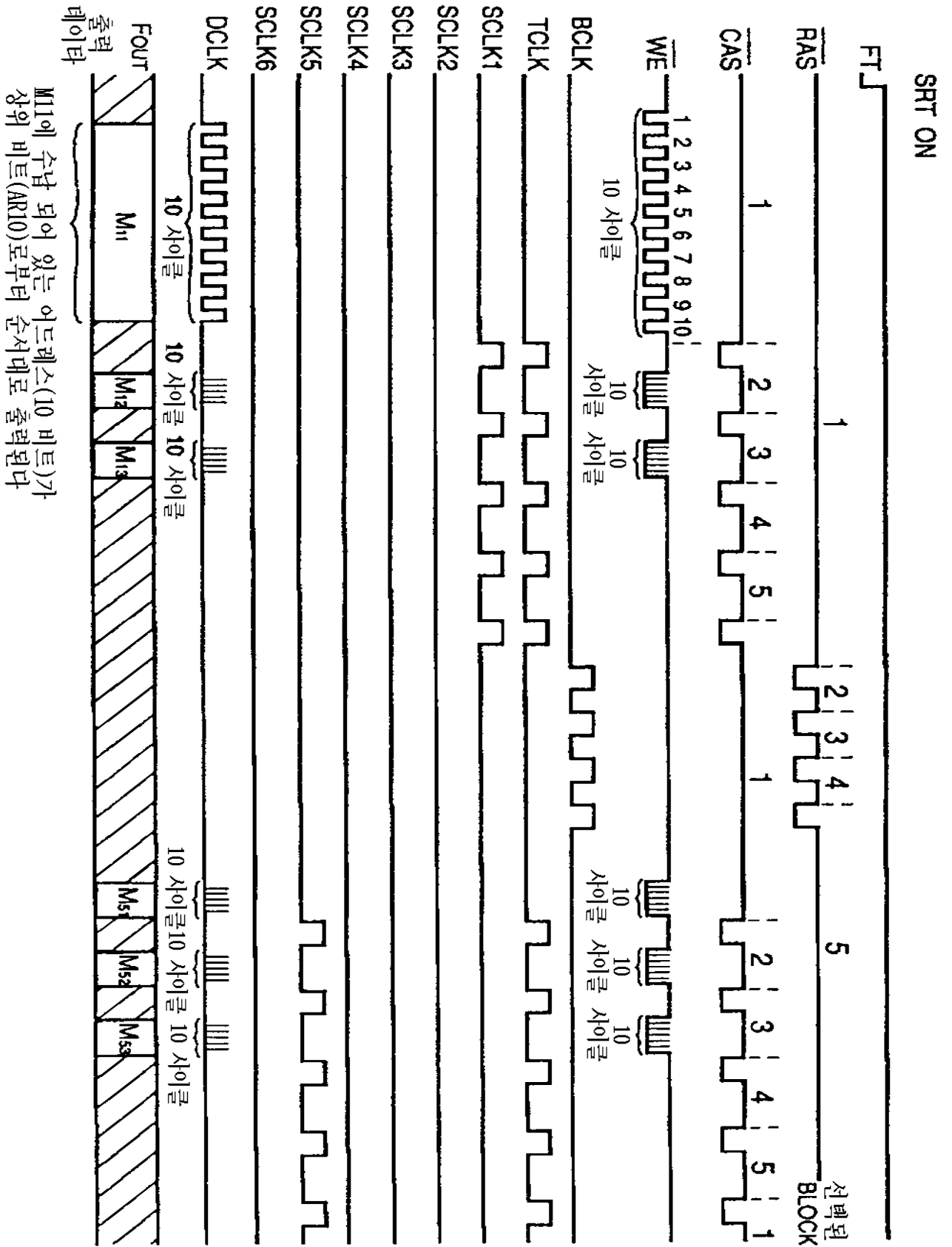




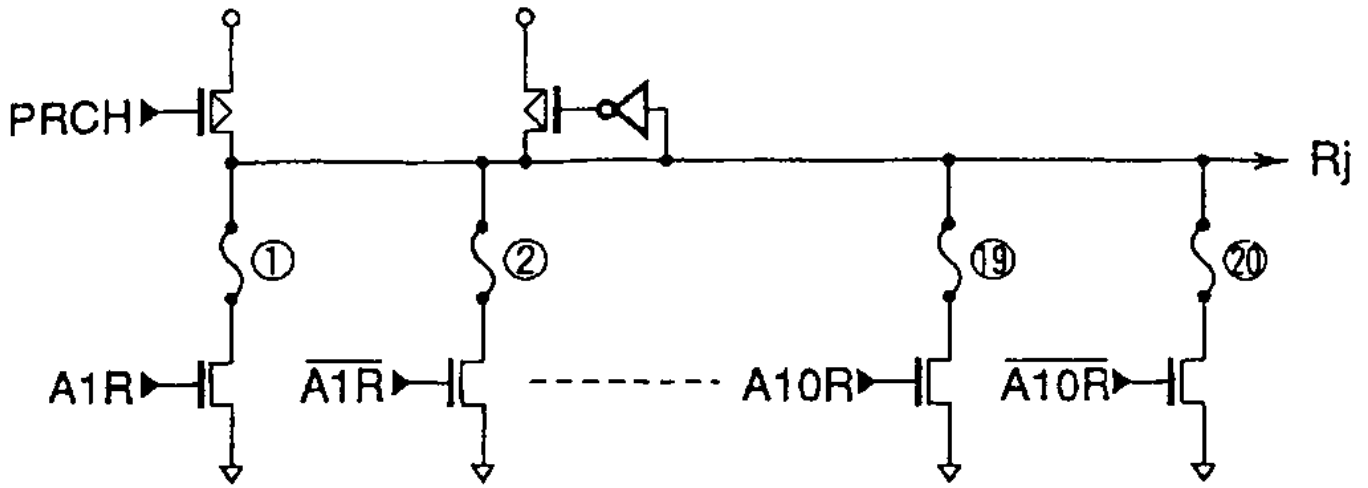






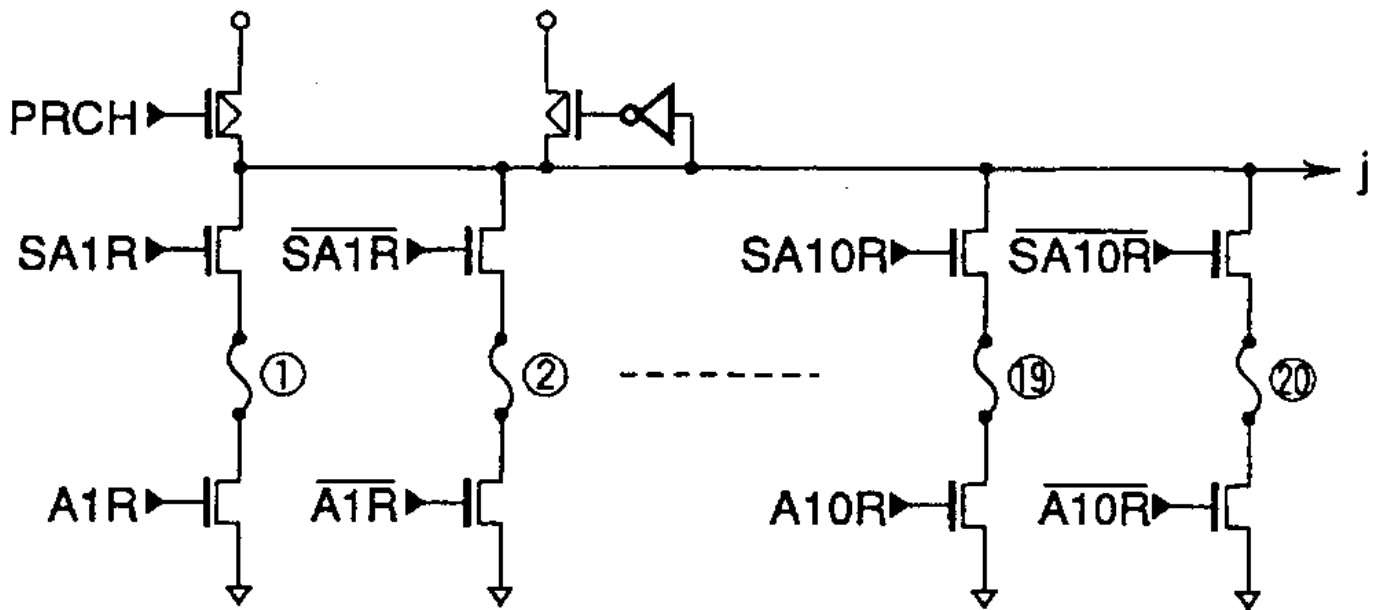


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보통의 퓨즈

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소프트 셋트 가능한 퓨즈



