(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) **World Intellectual Property Organization**
International Bureau

(43) **International Publication Date**
28 March 2024 (28.03.2024)

(10) **International Publication Number**
WO 2024/060046 A1

(51) **International Patent Classification:**
H01L 29/778 (2006.01) *H01L 29/66* (2006.01)

(21) **International Application Number:**
PCT/CN2022/120122

(22) **International Filing Date:**
21 September 2022 (21.09.2022)

(25) **Filing Language:** English

(26) **Publication Language:** English

(71) **Applicant: INNOSCIENCE (SUZHOU) SEMICONDUCTOR CO., LTD.** [CN/CN]; 98 Xinli Rd., FOHO Hi-Tech Zone, Wujiang District, Suzhou, Jiangsu 215211 (CN).

(72) **Inventors: LIU, Yang**; 98 Xinli Rd., FOHO Hi-Tech Zone, Wujiang District, Suzhou, Jiangsu 215211 (CN). **DU, Ziming**; 98 Xinli Rd., FOHO Hi-Tech Zone, Wujiang District, Suzhou, Jiangsu 215211 (CN). **YOU, Jheng-Sheng**; 98 Xinli Rd., FOHO Hi-Tech Zone, Wujiang District, Suzhou, Jiangsu 215211 (CN).

(74) **Agent: BEIJING BESTIPR INTELLECTUAL PROPERTY LAW CORPORATION**; Room 409, Tower B, Ka Wah Building, No. 9 Shangdi 3rd Street, Haidian District, Beijing 100085 (CN).

(81) **Designated States** *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CV, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IQ, IR, IS, IT, JM, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH,

(54) **Title:** NITRIDE-BASED SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

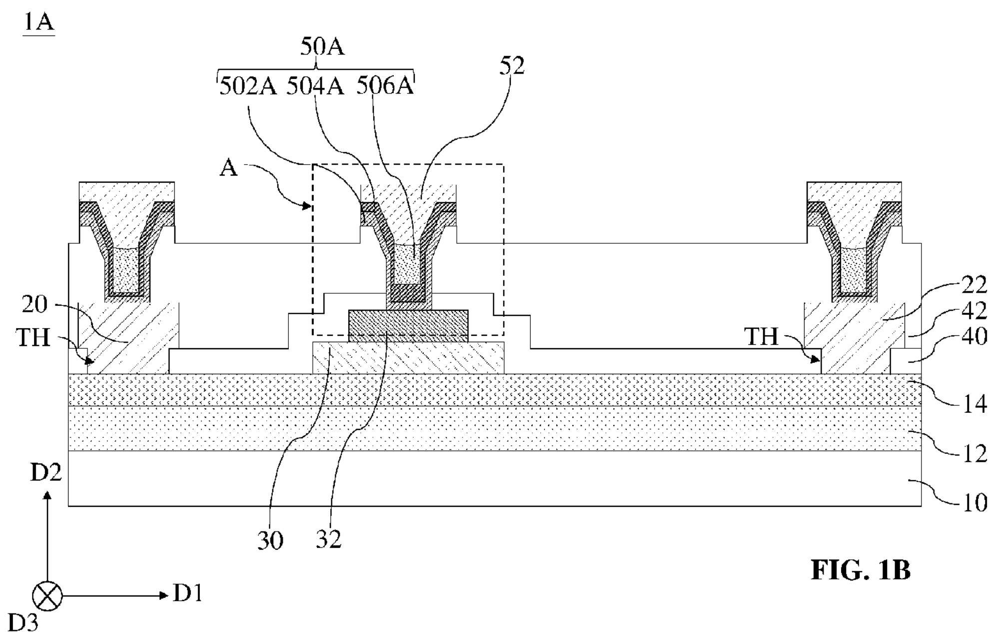

FIG. 1B

(57) **Abstract:** A nitride-based semiconductor device includes a first nitride-based semiconductor layer, a second nitride-based semiconductor layer, a gate electrode, and a first dielectric layer. The second nitride-based semiconductor layer is disposed on the first nitride-based semiconductor layer. The second nitride-based semiconductor layer has a bandgap higher than a bandgap of the first nitride-based semiconductor layer. The gate electrode is disposed above the second nitride-based semiconductor layer. The first dielectric layer is disposed above the gate electrode and has a top surface, a side surface and an inclined surface. The inclined surface connects the top surface to the side surface, and a connection interface between the inclined surface and the side surface is above the gate electrode.

WO 2024/060046 A1

[Continued on next page]

TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SC, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

NITRIDE-BASED SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

Inventors: Liu Yang, Du Ziming, You Jheng-Sheng

Field of the Disclosure:

[0001] The present disclosure generally relates to a nitride-based semiconductor device. More specifically, the present disclosure relates to a nitride-based semiconductor device having a dielectric layer with a chamfer structure.

Background:

[0002] In recent years, intense research on high-electron-mobility transistors (HEMTs) has been prevalent, particularly for high power switching and high frequency applications. III-nitride-based HEMTs utilize a heterojunction interface between two materials with different bandgaps to form a quantum well-like structure, which accommodates a two-dimensional electron gas (2DEG) region, satisfying demands of high power/frequency devices. In addition to HEMTs, examples of devices having heterostructures further include heterojunction bipolar transistors (HBT), heterojunction field effect transistor (HFET), and modulation-doped FETs (MODFET).

Summary of the Disclosure:

[0003] In accordance with one aspect of the present disclosure, a semiconductor device is provided. A nitride-based semiconductor device includes a first nitride-based semiconductor layer, a second nitride-based semiconductor layer, a gate electrode, and a first dielectric layer. The second nitride-based semiconductor layer is disposed on the first nitride-based semiconductor layer. The second nitride-based semiconductor layer has a bandgap higher than a bandgap of the first nitride-based semiconductor layer. The gate electrode is disposed above the second nitride-based semiconductor layer. The first dielectric layer is disposed above the gate electrode and has a top surface, a side surface and an inclined surface. The inclined surface connects the top surface to the side surface, and a connection interface between the inclined surface and the side surface is above the gate electrode.

[0004] In accordance with one aspect of the present disclosure, a semiconductor device is provided. A nitride-based semiconductor device includes a first nitride-based semiconductor layer, a second nitride-based semiconductor layer, a gate electrode, and a first dielectric layer. The second nitride-based semiconductor layer is disposed on the first nitride-based semiconductor layer. The second nitride-based semiconductor layer has a bandgap higher than a bandgap of the first nitride-based semiconductor layer. The gate electrode is disposed above the second nitride-

based semiconductor layer. The first dielectric layer is disposed above the gate electrode and has a chamfer structure that is located immediately over the gate electrode.

[0005] In accordance with one aspect of the present disclosure, a method for manufacturing a semiconductor device is provided. The method includes steps as follows. A first nitride-based semiconductor layer is formed. A second nitride-based semiconductor layer is formed on the first nitride-based semiconductor layer. A gate electrode is formed over the second nitride-based semiconductor layer. A first dielectric layer is formed to cover the gate electrode and the second nitride-based semiconductor layer, in which this step further includes sub-steps as follows. A blanket dielectric layer is formed to cover the gate electrode and the second nitride-based semiconductor layer. A blanket dielectric layer is formed to cover the gate electrode and the second nitride-based semiconductor layer. The blanket dielectric layer is patterned to form a through hole directly over the gate electrode. An ion bombardment process is performed on a portion of the blanket dielectric layer adjacent to the through hole, such that the portion is formed to have an inclined surface, thereby forming the first dielectric layer.

[0006] By the above configuration, in embodiments of the present disclosure, an inclined surface is formed between a top and a side surface of the dielectric layer, such that an accommodating space defined by the top, side and the inclined surfaces can have a funnel shape. The contact via can be formed/disposed in the funnel-shaped accommodating space, so the stress generated by the material difference between the contact via and the dielectric layer can be relieved, thereby avoiding an open circuit issue. Also, the contact resistance of the semiconductor device can be reduced due to the stress relieved. As such, the semiconductor device can have good reliability and good electrical properties.

Brief Description of the Drawings:

[0007] Aspects of the present disclosure are readily understood from the following detailed description when read with the accompanying figures. It should be noted that various features may not be drawn to scale. That is, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion. Embodiments of the present disclosure are described in more detail hereinafter with reference to the drawings, in which:

[0008] FIG. 1A is a top view of a semiconductor device according to some embodiments of the present disclosure;

[0009] FIG. 1B is a vertical cross-sectional view of the semiconductor device along the line I-I' in the FIG. 1A;

[0010] FIG. 1C is a vertical cross-sectional view of an enlarged region A of the semiconductor device 1A;

[0011] FIG. 2A, FIG. 2B, FIG. 2C, and FIG. 2D show different stages of a method for manufacturing a nitride-based semiconductor device according to some embodiments of the present disclosure;

[0012] FIG. 3 is a vertical cross-sectional view of an enlarged region of a semiconductor device according to some embodiment of the present disclosure; and

[0013] FIG. 4 is a vertical cross-sectional view of an enlarged region of a semiconductor device according to some embodiment of the present disclosure.

Detailed Description:

[0014] Common reference numerals are used throughout the drawings and the detailed description to indicate the same or similar components. Embodiments of the present disclosure will be readily understood from the following detailed description taken in conjunction with the accompanying drawings.

[0015] Spatial descriptions, such as "on," "above," "below," "up," "left," "right," "down," "top," "bottom," "vertical," "horizontal," "side," "higher," "lower," "upper," "over," "under," and so forth, are specified with respect to a certain component or group of components, or a certain plane of a component or group of components, for the orientation of the component(s) as shown in the associated figure. It should be understood that the spatial descriptions used herein are for purposes of illustration only, and that practical implementations of the structures described herein can be spatially arranged in any orientation or manner, provided that the merits of embodiments of this disclosure are not deviated from by such arrangement.

[0016] Further, it is noted that the actual shapes of the various structures depicted as approximately rectangular may, in actual device, be curved, have rounded edges, have somewhat uneven thicknesses, etc. due to device fabrication conditions. The straight lines and right angles are used solely for convenience of representation of layers and features.

[0017] In the following description, semiconductor devices/dies/packages, methods for manufacturing the same, and the likes are set forth as preferred examples. It will be apparent to those skilled in the art that modifications, including additions and/or substitutions may be made without departing from the scope and spirit of the present disclosure. Specific details may be omitted so as not to obscure the present disclosure; however, the disclosure is written to enable one skilled in the art to practice the teachings herein without undue experimentation.

[0018] FIG. 1A is a top view of a semiconductor device 1A according to some embodiments of the present disclosure. FIG. 1B is a vertical cross-sectional view of the semiconductor device 1A along the line I-I’ in the FIG. 1A. The directions D1, D2 and D3 are labeled in the FIGS. 1A and

1B, in which the directions D1, D2 and D3 are different from each other. The directions D1 to D3 are perpendicular to each other.

[0019] The semiconductor device 1A includes a substrate 10, nitride-based semiconductor layers 12, 14, electrodes 20, 22, a doped nitride-based layer 30, a gate electrode 32, a plurality of
5 dielectric layers 40,42, a plurality of contact vias 50A, and a circuit layer 52.

[0020] The substrate 10 may be a semiconductor substrate. The exemplary materials of the substrate 10 can include, for example but are not limited to, Si, SiGe, SiC, gallium arsenide, p-doped Si, n-doped Si, sapphire, semiconductor on insulator, such as silicon on insulator (SOI), or other suitable substrate materials. In some embodiments, the substrate 10 can include, for
10 example, but is not limited to, group III elements, group IV elements, group V elements, or combinations thereof (e.g., III-V compounds). In other embodiments, the substrate 10 can include, for example but is not limited to, one or more other features, such as a doped region, a buried layer, an epitaxial (epi) layer, or combinations thereof.

[0021] A buffer layer (not shown) can be disposed on/over/above the substrate 10. The buffer
15 layer can be disposed between the substrate 10 and the nitride-based semiconductor layer 12. The buffer layer can be configured to reduce lattice and thermal mismatches between the substrate 10 and the nitride-based semiconductor layer 12, thereby curing defects due to the mismatches/difference. The buffer layer may include a III-V compound. The III-V compound can include, for example but are not limited to, aluminum, gallium, indium, nitrogen, or
20 combinations thereof. Accordingly, the exemplary materials of the buffer layer can further include, for example but are not limited to, GaN, AlN, AlGaN, InAlGaN, or combinations thereof.

[0022] In some embodiments, the semiconductor device 1A may further include a nucleation layer (not shown). The nucleation layer may be formed between the substrate 10 and the buffer layer. The nucleation layer can be configured to provide a transition to accommodate a
25 mismatch/difference between the substrate 10 and a III-nitride layer of the buffer layer. The exemplary material of the nucleation layer can include, for example but is not limited to AlN or any of its alloys.

[0023] The nitride-based semiconductor layer 12 can be disposed on/over/above the substrate 10. The nitride-based semiconductor layer 14 can be disposed on/over/above the nitride-based
30 semiconductor layer 12. The exemplary materials of the nitride-based semiconductor layer 12 can include, for example but are not limited to, nitrides or group III-V compounds, such as GaN, AlN, InN, $In_xAl_yGa_{(1-x-y)}N$ where $x+y \leq 1$, $Al_xGa_{(1-x)}N$, where $x \leq 1$. The exemplary materials of the nitride-based semiconductor layer 14 can include, for example but are not limited to, nitrides or group III-V compounds, such as GaN, AlN, InN, $In_xAl_yGa_{(1-x-y)}N$ where $x+y \leq 1$, $Al_yGa_{(1-y)}N$,
35 where $y \leq 1$.

[0024] The exemplary materials of the nitride-based semiconductor layers 12 and 14 are selected such that the nitride-based semiconductor layer 14 has a bandgap (i.e., forbidden band width) greater/higher than a bandgap of the nitride-based semiconductor layer 12, which causes electron affinities thereof different from each other and forms a heterojunction therebetween. For example, when the nitride-based semiconductor layer 14 is an AlGaN layer having bandgap of approximately 4.0 eV, the nitride-based semiconductor layer 12 can be selected as an undoped GaN layer having a bandgap of approximately 3.4 eV. As such, the nitride-based semiconductor layers 12 and 14 can serve as a channel layer and a barrier layer, respectively. A triangular well potential is generated at a bonded interface between the channel and barrier layers, so that electrons accumulate in the triangular well, thereby generating a two-dimensional electron gas (2DEG) region adjacent to the heterojunction. Accordingly, the semiconductor device 1A is available to include at least one GaN-based high-electron-mobility transistor (HEMT).

[0025] The electrodes 20 and 22 can be disposed on/over/above the nitride-based semiconductor layer 14. The electrodes 20 and 22 are directly in contact with the nitride-based semiconductor layer 14. Referring to the FIG. 1A, the electrodes 20 and 22 can extend along the direction D3, such that each of the electrodes 20 and 22 can have a strip profile. In some embodiments, the electrode 20 can serve as a source electrode. In some embodiments, the electrode 20 can serve as a drain electrode. In some embodiments, the electrode 22 can serve as a source electrode. In some embodiments, the electrode 22 can serve as a drain electrode. The role of the electrodes 20 and 22 depends on the device design.

[0026] In some embodiments, the electrodes 20 and 22 can include, for example but are not limited to, metals, alloys, doped semiconductor materials (such as doped crystalline silicon), compounds such as silicides and nitrides, other conductor materials, or combinations thereof. The exemplary materials of the electrodes 20 and 22 can include, for example but are not limited to, Ti, AlSi, TiN, or combinations thereof.

[0027] Each of the electrodes 20 and 22 may be a single layer, or plural layers of the same or different composition. The electrodes 20 and 22 form ohmic contacts with the nitride-based semiconductor layer 14. Furthermore, the ohmic contacts can be achieved by applying Ti, Al, or other suitable materials to the electrodes 20 and 22. In some embodiments, each of the electrodes 20 and 22 is formed by at least one conformal layer and a conductive filling. The conformal layer can wrap the conductive filling. The exemplary materials of the conformal layer, for example but are not limited to, Ti, Ta, TiN, Al, Au, AlSi, Ni, Pt, or combinations thereof. The exemplary materials of the conductive filling can include, for example but are not limited to, AlSi, AlCu, or combinations thereof.

[0028] The doped nitride-based semiconductor layer 30 is disposed on/over/above the nitride-based semiconductor layer 14. The doped nitride-based semiconductor layer 30 is in contact with the nitride-based semiconductor layer 14. The gate electrode 32 is disposed on/over/above the doped nitride-based semiconductor layer 30 and the nitride-based semiconductor layer 14. The gate electrode 32 is in contact with the doped nitride-based semiconductor layer 30. The doped nitride-based semiconductor layer 30 is disposed between the gate electrode 32 and the nitride-based semiconductor layer 14. Each of the nitride-based layers 20 and 22 extends along the direction D3 to have a strip profile.

[0029] The gate electrode 32 is narrower than the doped nitride-based semiconductor layer 30. In some embodiments, a width of the doped nitride-based semiconductor layer 30 is substantially the same as a width of the gate electrode 32. The profiles of the doped nitride-based semiconductor layer 30 and the gate electrode 32 are the same, for example, both of them are rectangular profiles. In other embodiments, the profiles of the doped nitride-based semiconductor layer 30 and the gate electrode 32 can be different from each other. For example, the profile of the doped nitride-based semiconductor layer 30 can be a trapezoid profile, the profile of the gate electrode 32 can be a rectangular profile.

[0030] In the exemplary illustration of FIG. 1B, the semiconductor device 1A is an enhancement mode device, which is in a normally-off state when the gate electrode 32 is at approximately zero bias. Specifically, the doped nitride-based semiconductor layer 30 may create at least one p-n junction with the nitride-based semiconductor layer 14 to deplete the 2DEG region, such that at least one zone of the 2DEG region corresponding to a position below the corresponding the gate electrode 32 has different characteristics (e.g., different electron concentrations) than the rest of the 2DEG region and thus is blocked. Due to such mechanism, the semiconductor device 1A has a normally-off characteristic. In other words, when no voltage is applied to the gate electrode 32 or a voltage applied to the gate electrode 32 is less than a threshold voltage (i.e., a minimum voltage required to form an inversion layer below the gate electrode 32), the zone of the 2DEG region below the gate electrode 32 is kept blocked, and thus no current flows therethrough.

[0031] In some embodiments, the doped nitride-based semiconductor layer 30 can be omitted, such that the semiconductor device 1A is a depletion-mode device, which means the semiconductor device 1A in a normally-on state at zero gate-source voltage.

[0032] The doped nitride-based semiconductor layer 30 can be a p-type doped III-V semiconductor layer. The exemplary materials of the doped nitride-based semiconductor layer 30 can include, for example but are not limited to, p-doped group III-V nitride semiconductor materials, such as p-type GaN, p-type AlGaN, p-type InN, p-type AlInN, p-type InGaN, p-type AlInGaN, or combinations thereof. In some embodiments, the p-doped materials are achieved by

using a p-type impurity, such as Be, Zn, Cd, and Mg. In some embodiments, the nitride-based semiconductor layer 14 includes undoped GaN and the nitride-based semiconductor layer 12 includes AlGaN, and the doped nitride-based semiconductor layer 30 is a p-type GaN layer which can bend the underlying band structure upwards and to deplete the corresponding zone of the 2DEG region, so as to place the semiconductor device 1A into an off-state condition.

[0033] The exemplary materials of the gate electrode 32 may include metals or metal compounds. The gate electrode 32 may be formed as a single layer, or plural layers of the same or different compositions. The exemplary materials of the metals or metal compounds can include, for example but are not limited to, W, Au, Pd, Ti, Ta, Co, Ni, Pt, Mo, TiN, TaN, metal alloys or compounds thereof, or other metallic compounds.

[0034] The dielectric layer 40 is disposed on/over/above the nitride-based semiconductor layer 14, the doped nitride-based semiconductor layer 30 and the gate electrode 32. The dielectric layer 40 covers the doped nitride-based semiconductor layer 30 and the gate electrode 32 to form a protruding portion. The dielectric layer 40 has a plurality of through holes TH. The electrodes 20 and 22 can penetrate the dielectric layer 40 via the through holes TH to make contact with the nitride-based semiconductor layer 14.

[0035] In general, with respect to a semiconductor device, a through hole within a dielectric layer is usually filled with a conductive material to achieve electrical connection between layers. However, since thermal expansion coefficients of the conductive material and the dielectric material are different, a thermal stress might be generated at an interface therebetween, resulting in uneven stress distribution in the conductive material. The affection is more obvious at a condition that the dielectric layer has a right angle for defining the through hole. Accordingly, cracks can be generated inside the conductive material, resulting in an opening circuit issue

[0036] At least to avoid the afore-mentioned issues, the present disclosure is to provide a novel structure for the nitride-based semiconductor devices.

[0037] FIG. 1C is a vertical view of an enlarged region A of the semiconductor device 1A. Referring to FIG. 1B and FIG. 1C, during the formation of the dielectric layer 42, first of all, a patterning process is performed on a blanket dielectric layer for forming a through hole with a right angle. The patterning process can include a dry etching process. After that, an ion bombardment process is performed on a portion of the blanket dielectric layer adjacent to the through hole, such that the portion is formed to have an inclined surface (i.e., chamfer structure).

[0038] The dielectric layer 42 is formed to be disposed on/over/above the gate electrode 32. The dielectric layer 42 is formed to be disposed on/over/above the electrodes 20 and 22. The dielectric layer 42 is formed to cover the dielectric layer 40. The dielectric layer 40 is located between the dielectric layer 42 and the nitride-based semiconductor layer 14.

[0039] The dielectric layer 42 is formed to have a side surface 420, an inclined surface 422, a top surface 424, and a bottom surface 426. The inclined surface 422 is located immediately over the gate electrode 32. The inclined surface 422 and the side surface 420 are located between the top surface 424 and the bottom surface 426. The inclined surface 422 connects the top surface 424 to the side surface 420. The side surface 420 connects the inclined surface 422 to the bottom surface 426. The side surface 420 and the inclined surface 422 have different surface roughnesses due to different manufacturing processes thereof (i.e., dry etching process and ion bombardment process). In some embodiments, the side surface 420 is formed by an etching process, and the inclined surface 422 is formed by an etching process in combination with an ion bombardment process.

[0040] A connection interface CI1 is formed between the inclined surface 422 and the side surface 420. The connection interface CI1 is directly above the gate electrode 32. Orthogonal/vertical projections of the side surface 420 and the inclined surface 422 on the nitride-based semiconductor layer 14 are within an orthogonal/vertical projection of the gate electrode 32 on the nitride-based semiconductor layer 14.

[0041] The side surface 420 defines the sub-accommodating space AS1, and the inclined surface 422 defines the accommodating space AS2. The accommodating space AS2 communicates with the accommodating space AS1. The side surface 420 and the inclined surface 422 have different extending depths. Specifically, the extending depth of the side surface 420 is greater than that of the inclined surface 422, such that the depth of the accommodating space AS1 is greater than that of the accommodating space AS2. A width of the accommodating space AS2 gradually decreases along a direction from the top surface 424 toward the bottom surface 426 of the dielectric layer 42. A width of the accommodating space AS1 is constant.

[0042] Overall, the two accommodating spaces AS1 and AS2 can be viewed as an accommodating space AS. The accommodating space AS, which is defined by the top, side and the inclined surfaces 424, 422 and 420 of the dielectric layer 42, can have a funnel shape (i.e., Y-shaped).

[0043] The profile of the accommodating space AS of the dielectric layer 42 can serve as a buffer to accommodate the difference between the thermal expansion coefficients of the conductive material and the dielectric material, improving the opening circuit issue.

[0044] The conductive via 50A can be formed/disposed in the afore-mentioned funnel-shaped accommodating space AS to penetrate the dielectric layer 42. The conductive via 50A can further penetrate the dielectric layer 40, thereby making a contact with the gate electrode 32. The conductive via 50A covers the side surface 420 of the dielectric layer 42. The conductive via

50A covers the inclined surface 422 of the dielectric layer 42. The conductive via 50A covers top surface 424 of the dielectric layer 42.

[0045] The conductive via 50A includes two conductive layers 502A, 504A and a conductive filling 506A. The conductive layers 502A, 504A are conformal with a profile constructed by the top surface 424, the inclined surface 422, and the side surface 420 of the dielectric layer 42. Each of the conductive layers 502A and 504A extends from the top surface 424 to the side surface 420 along the inclined surface 422.

[0046] Due to conformal configuration, each of the conductive layers 502A and 504A can also have an inclined surface (i.e., chamfer structure) corresponding to the inclined surface 422 of the dielectric layer 42. The inclined surfaces of the conductive layer 502A and 504A are above the gate electrode 32. The conductive filling 506A is wrapped by the conductive layers 502A, 504A. The conductive filling 506A is located at a position lower than the inclined surface of the conductive layer 504A.

[0047] With the profile of the dielectric layer 42, even though the stress is generated due to the material differences between the dielectric layer 42 and the conductive via 50A, the stress can be dispersed along an extending direction of the inclined surface 422. As such, the intensity of the stress at the interface between the conductive via 50A and the dielectric layer 42 can be reduced, and thus the phenomenon of the uneven stress distribution would be relieved. As such, the probability of generating cracks in the conductive via 50A can be reduced, thereby avoiding the opening circuit issue. Therefore, the reliability of the semiconductor device 1A can be improved, and the contact resistance thereof can be reduced.

[0048] Moreover, with respect to the configuration of the conductive via 50A, at least one of conductive layer 502A/504A is conformal with the profile constructed by the top, the inclined, and the side surfaces 420, 422 and 424 of the dielectric layer 42. Therefore, the stress generated by the conductive layer 502A/504A itself can be adapted to the morphology of the dielectric layer 42. Thus, the negative impacts of the stress can be further reduced. In this regard, since stress accumulation is enhanced as more layers are formed. With respect to the conductive via 50A, as a multiple-layers structure, since the layers formed from different materials might let the stress accumulation worse, the inclined surface 422 can serve as a key point to relieve the stress distribution.

[0049] The material of the dielectric layers 40 and 42 can include, for example but are not limited to, dielectric materials. For example, the dielectric layers 40 and 42 can include, for example but are not limited to, SiN_x, SiO_x, Si_3N_4, SiON, SiC, SiBN, SiCBN, oxides, nitrides, plasma enhanced oxide (PEOX), or combinations thereof. In some embodiments, each of the

dielectric layers 40 and 42 can be a multi-layered structure, such as a composite dielectric layer of Al_2O_3/SiN, Al_2O_3/SiO_2, AlN/SiN, AlN/SiO_2, or combinations thereof.

[0050] The exemplary materials of the conductive layers 502A, 504A and conductive filling 506A can include, for example but are not limited to, conductive materials, such as metals or alloys. In some embodiments, the material of the conductive layer 502A can include, for example but are not limited to, titanium (Ti), titanium nitride (TiN), or combinations thereof. In some embodiments, the material of the conductive layer 504A can include, for example but are not limited to, titanium (Ti), titanium nitride (TiN). In some embodiments, the material of the conductive filling 506A can include, for example but are not limited to tungsten (Wu), molybdenum (Mo), copper (Cu), or combinations thereof.

[0051] The circuit layer 52 can be disposed on/over/above the conductive via 50A. The circuit layer 52 makes a contact with the inclined surface of the conductive layer 504A. The circuit layer 52 has a bottom portion in contact with the conductive filling 506A. The bottom portion of the circuit layer 52 has a pair of inclined surfaces in contact with the conductive layer 504A and the conductive filling 506A of the conductive via 50A. A contact interface CI2 formed between the bottom portion of the circuit layer 52 and the conductive filling 506A is located at a position lower than the inclined surface of the conductive layer 504A. In some embodiments, the contact interface CI2 can be formed to be a curved surface, such that the curved contact interface CI2 can evenly distribute the stress from the circuit layer 52.

[0052] The circuit layer 52 may have metal lines, pads, traces, or combinations thereof, such that the circuit layer 52 can form at least one circuit. The circuit layer 52 can be connected with the gate electrode 32, electrodes 20 and 22 by the contact vias 50A. An external electronic device can send at least one electronic signal to the semiconductor device 1A by the circuit layer 52, and vice versa.

[0053] The exemplary materials of the circuit layer 52 can include, for example but are not limited to, conductive materials. The circuit layer 52 may include a single film or multilayered film having Ag, Al, Cu, Mo, Ni, Ti, alloys thereof, oxides thereof, nitrides thereof, or combinations thereof.

[0054] Different stages of a method for manufacturing the semiconductor device 1A are shown in FIG. 2A, FIG. 2B, FIG. 2C, and FIG. 2D, as described below. In the following, deposition techniques can include, for example but are not limited to, atomic layer deposition (ALD), physical vapor deposition (PVD), chemical vapor deposition (CVD), metal organic CVD (MOCVD), plasma enhanced CVD (PECVD), low-pressure CVD (LPCVD), plasma-assisted vapor deposition, epitaxial growth, or other suitable processes.

[0055] Referring to FIG. 2A, a nitride-based semiconductor layer 12 is formed on/over/above a substrate 10 by using deposition techniques. A nitride-based semiconductor layer 14 is formed on/over/above the nitride-based semiconductor layer 12 by using deposition techniques, so that a heterojunction is formed therebetween. A doped nitride-based semiconductor layer 30 can be formed on the nitride-based semiconductor layer 14. A gate electrode 32 can be formed on the doped nitride-based semiconductor layer 30.

[0056] A blanket dielectric layer (not shown) is formed to cover the nitride-based semiconductor layer 14, the doped nitride-based semiconductor layer 30, and the gate electrode 32. A patterning process is performed on the blanket dielectric layer to form an intermediate dielectric layer 52 with a plurality of through holes TH to expose the nitride-based semiconductor layer 14. The electrodes 20 and 22 can be formed in the through holes TH to make contact with the nitride-based semiconductor layer 14. A blanket dielectric layer 54 is formed over the nitride-based semiconductor layer 14. The blanket dielectric layer 54 is formed to cover the electrodes 20, 22, the gate electrode 32 and the intermediate dielectric layer 52.

[0057] The formation of the doped nitride-based semiconductor layer 30, the gate electrode 32, the electrodes 20, 22, and the intermediate dielectric layer 52 includes deposition techniques and a patterning process. In some embodiments, the deposition techniques can be performed for forming a blanket layer, and the patterning process can be performed for removing excess portions thereof. In some embodiments, the patterning process can include photolithography, exposure and development, etching, other suitable processes, or combinations thereof.

[0058] Referring to FIG. 2B, a patterning process is performed on the blanket dielectric layer 54 and the intermediate dielectric layer 52, such that a plurality of the through holes can be formed to expose the electrodes 20, 22 and the gate electrode 32. The formed through holes in this stage are directly above the electrodes 20, 22 and the gate electrode 30. After the formation of the through holes, an intermediate dielectric layer 56 and a dielectric layer 40 are formed.

[0059] Referring to FIG. 2C, an ion bombardment process is performed on portions P of the intermediate dielectric layer 56 adjacent to the through holes, such that each of the portions P is formed to have an inclined surface, thereby forming a dielectric layer 42. The step of the ion bombardment process includes emission of inert element ions, for example, argon (Ar) ions.

[0060] Referring to FIG. 2D, a plurality of conductive layers 502A and 504A are formed to conformally cover the portions P of the dielectric layer 42. In some embodiments, the materials of the conductive layers 502A and 504A can be different from each other as afore mentioned. A conductive filling 506A is formed on the conductive layers 502A and 504A, such that the conductive filling 506A is wrapped by the conductive layers 502A and 504A. Thereafter, the

circuit layer 52 can be formed, obtaining the configuration of the semiconductor device 1A as shown in FIGS. 1A, 1B and 1C.

[0061] FIG. 3 is a vertical cross-sectional view of an enlarged region of a semiconductor device according to some embodiment of the present disclosure. The semiconductor device 1B is similar to the semiconductor device 1A as described and illustrated with reference to FIGS. 1A,1B and 1C, except that the dielectric layer 42 is replaced by a dielectric layer 42B. The dielectric layer 42B has a side surface 420B, an inclined surface 422B, and a top surface 424B. The inclined surface 422B connects the side surface 420B to the top surface 424B. The side surface 420B of the dielectric layer 42B is inclined. The slope of the side surface 420B is different from that of the inclined surface 422B. The slope of the side surface 420B is greater than that of the inclined surface 422B. The slope of the side surface 402B of the dielectric layer 40 is greater than that of the side surface 420B of the dielectric layer 42. With the multistage slope design, the stress at the interface between the conductive layer 502B and the dielectric layer 42B can be more evenly distributed.

[0062] FIG. 4 is a vertical cross-sectional view of an enlarged region of a semiconductor device 1C according to some embodiment of the present disclosure. The semiconductor device 1C is similar to the semiconductor device 1A as described and illustrated with reference to FIGS. 1A,1B and 1C, except that the conductive filling 506A is replaced by a conductive filling 506C. The conductive filling 506C is located at a position higher than the inclined surface 422C of the conductive layer 42C. That is, at least one portion of the inclined surface 422C of the conductive layer 42C is located at a position lower than the conductive filling 506C.

[0063] Based on the above description, in embodiments of the present disclosure, a portion of the dielectric layer is formed to have a chamfer structure. The chamfer structure can be conductive to alleviate the stress at the interface between the dielectric layer and the conductive via. As such, the stress distribution in the conductive via can be more uniform, and the probability of generating cracks can be reduced. Thus, the reliability of the semiconductor device can be enhanced, and the contact resistance thereof can be reduced.

[0064] The embodiments were chosen and described in order to best explain the principles of the disclosure and its practical application, thereby enabling others skilled in the art to understand the disclosure for various embodiments and with various modifications that are suited to the particular use contemplated.

[0065] As used herein and not otherwise defined, the terms "substantially," "substantial," "approximately" and "about" are used to describe and account for small variations. When used in conjunction with an event or circumstance, the terms can encompass instances in which the event or circumstance occurs precisely as well as instances in which the event or circumstance

occurs to a close approximation. For example, when used in conjunction with a numerical value, the terms can encompass a range of variation of less than or equal to ±10% of that numerical value, such as less than or equal to ±5%, less than or equal to ±4%, less than or equal to ±3%, less than or equal to ±2%, less than or equal to ±1%, less than or equal to ±0.5%, less than or equal to ±0.1%, or less than or equal to ±0.05%. The term "substantially coplanar" can refer to two surfaces within micrometers of lying along a same plane, such as within 40 μm, within 30 μm, within 20 μm, within 10 μm, or within 1 μm of lying along the same plane.

[0066] As used herein, the singular terms "a," "an," and "the" may include plural referents unless the context clearly dictates otherwise. In the description of some embodiments, a component provided "on" or "over" another component can encompass cases where the former component is directly on (e.g., in physical contact with) the latter component, as well as cases where one or more intervening components are located between the former component and the latter component.

[0067] While the present disclosure has been described and illustrated with reference to specific embodiments thereof, these descriptions and illustrations are not limiting. It should be understood by those skilled in the art that various changes may be made and equivalents may be substituted without departing from the true spirit and scope of the present disclosure as defined by the appended claims. The illustrations may not necessarily be drawn to scale. There may be distinctions between the artistic renditions in the present disclosure and the actual apparatus due to manufacturing processes and tolerances. Further, it is understood that actual devices and layers may deviate from the rectangular layer depictions of the FIGS. and may include angles surfaces or edges, rounded corners, etc. due to manufacturing processes such as conformal deposition, etching, etc. There may be other embodiments of the present disclosure which are not specifically illustrated. The specification and the drawings are to be regarded as illustrative rather than restrictive. Modifications may be made to adapt a particular situation, material, composition of matter, method, or process to the objective, spirit and scope of the present disclosure. All such modifications are intended to be within the scope of the claims appended hereto. While the methods disclosed herein have been described with reference to particular operations performed in a particular order, it will be understood that these operations may be combined, sub-divided, or re-ordered to form an equivalent method without departing from the teachings of the present disclosure. Accordingly, unless specifically indicated herein, the order and grouping of the operations are not limitations.

Claims

1. A nitride-based semiconductor device, comprising:

a first nitride-based semiconductor layer;

a second nitride-based semiconductor layer disposed on the first nitride-based semiconductor layer, wherein the second nitride-based semiconductor layer has a bandgap higher than a bandgap of the first nitride-based semiconductor layer;

a gate electrode disposed above the second nitride-based semiconductor layer; and

a first dielectric layer disposed above the gate electrode and having a top surface, a side surface and an inclined surface, wherein the inclined surface connects the top surface to the side surface, and a connection interface between the inclined surface and the side surface is above the gate electrode.

2. The semiconductor device of any one of the proceeding claims, further comprising:

a conductive via penetrating the first dielectric layer to make contact with the gate electrode, wherein the conductive via covers the inclined surface of the first dielectric layer.

3. The semiconductor device of any one of the proceeding claims, wherein the conductive via comprises at least one conductive layer conformal with a profile constructed by the top surface, the inclined surface, and the side surface of the first dielectric layer.

4. The semiconductor device of any one of the proceeding claims, wherein the conductive layer has an inclined surface above the gate electrode.

5. The semiconductor device of any one of the proceeding claims, wherein the conductive via further comprises a conductive filling wrapped by the conductive layer and located at a position lower than the inclined surface of the conductive layer.

6. The semiconductor device of any one of the proceeding claims, further comprising a circuit layer disposed over the conductive via and making contact with the inclined surface of the conductive layer.

5 7. The semiconductor device of any one of the proceeding claims, wherein a contact interface formed between the circuit layer and the conductive filling is located at a position lower than the inclined surface of the conductive layer.

8. The semiconductor device of any one of the proceeding claims, wherein the conductive 10 via further comprises a conductive filling wrapped by the conductive layer, wherein the semiconductor device further comprises a circuit layer disposed over the conductive via and having a bottom portion in contact with the conductive filling.

9. The semiconductor device of any one of the proceeding claims, wherein the bottom 15 portion has a pair of inclined surfaces in contact with the conductive via.

10. The semiconductor device of any one of the proceeding claims, wherein the side surface and the inclined surface have different extending depths.

20 11. The semiconductor device of any one of the proceeding claims, wherein the side surface and the inclined surface have different surface roughnesses.

12. The semiconductor device of any one of the proceeding claims, further comprising:

a second dielectric layer, disposed on the second nitride-based semiconductor layer and the 25 gate electrode and located between the first dielectric layer and the second nitride-based semiconductor layer.

13. The semiconductor device of any one of the proceeding claims, wherein orthogonal projections of the side surface and the inclined surface on the second nitride-based semiconductor layer are within an orthogonal projection of the gate electrode on the second nitride-based semiconductor layer.

14. The semiconductor device of any one of the proceeding claims, wherein the inclined surface defines a first accommodating space, and a width of the first accommodating space gradually decreases along a direction from the top surface toward a bottom surface of the first dielectric layer.

15. The semiconductor device of any one of the proceeding claims, wherein the side surface defines a second accommodating space communicating with the first accommodating space, and a width of the second accommodating space is constant.

16. A method for manufacturing a semiconductor device, comprising:

forming a first nitride-based semiconductor layer;

forming a second nitride-based semiconductor layer on the first nitride-based semiconductor layer;

forming a gate electrode over the second nitride-based semiconductor layer; and

forming a first dielectric layer to cover the gate electrode and the second nitride-based semiconductor layer, wherein forming the first dielectric layer comprises:

forming a blanket dielectric layer to cover the gate electrode and the second nitride-based semiconductor layer;

patterning the blanket dielectric layer to form a through hole directly over the gate electrode; and

performing an ion bombardment process on a portion of the blanket dielectric layer adjacent to the through hole, such that the portion is formed to have an inclined surface, thereby forming the first dielectric layer.

5 17. The method of any one of the proceeding claims, wherein performing the ion bombardment process comprises emission of argon ions.

18. The method of any one of the proceeding claims, further comprises:

forming a plurality of conductive layers to conformally cover the portion of the first dielectric

10 layer.

19. The method of any one of the proceeding claims, wherein materials of the first and second conductive layers are different from each other.

15 20. The method of any one of the proceeding claims, wherein the first conductive layer comprises titanium, and the second conductive layer comprises titanium nitride.

21. A nitride-based semiconductor device, comprising:

a first nitride-based semiconductor layer;

20 a second nitride-based semiconductor layer disposed on the first nitride-based semiconductor layer, wherein the second nitride-based semiconductor layer has a bandgap higher than a bandgap of the first nitride-based semiconductor layer;

a gate electrode disposed above the second nitride-based semiconductor layer and between the source and drain electrodes; and

25 a first dielectric layer disposed above the gate electrode and having a chamfer structure that is located immediately over the gate electrode.

22. The semiconductor device of any one of the proceeding claims, further comprising:

a conductive via penetrating the first dielectric layer to make contact with the gate electrode, wherein the conductive via covers the chamfer structure of the first dielectric layer.

23. The semiconductor device of any one of the proceeding claims, wherein the conductive via comprises at least one conductive layer conformal with a profile of the chamfer structure of the first dielectric layer such that the conductive layer has a chamfer structure.

24. The semiconductor device of any one of the proceeding claims, wherein the conductive layer extends from a top surface to a side surface of the first dielectric layer along the chamfer structure of the first dielectric layer.

25. The semiconductor device of any one of the proceeding claims, wherein the conductive via further comprises at least one conductive filling wrapped by the conductive layer and located at a position lower than the chamfer structure of the conductive layer.

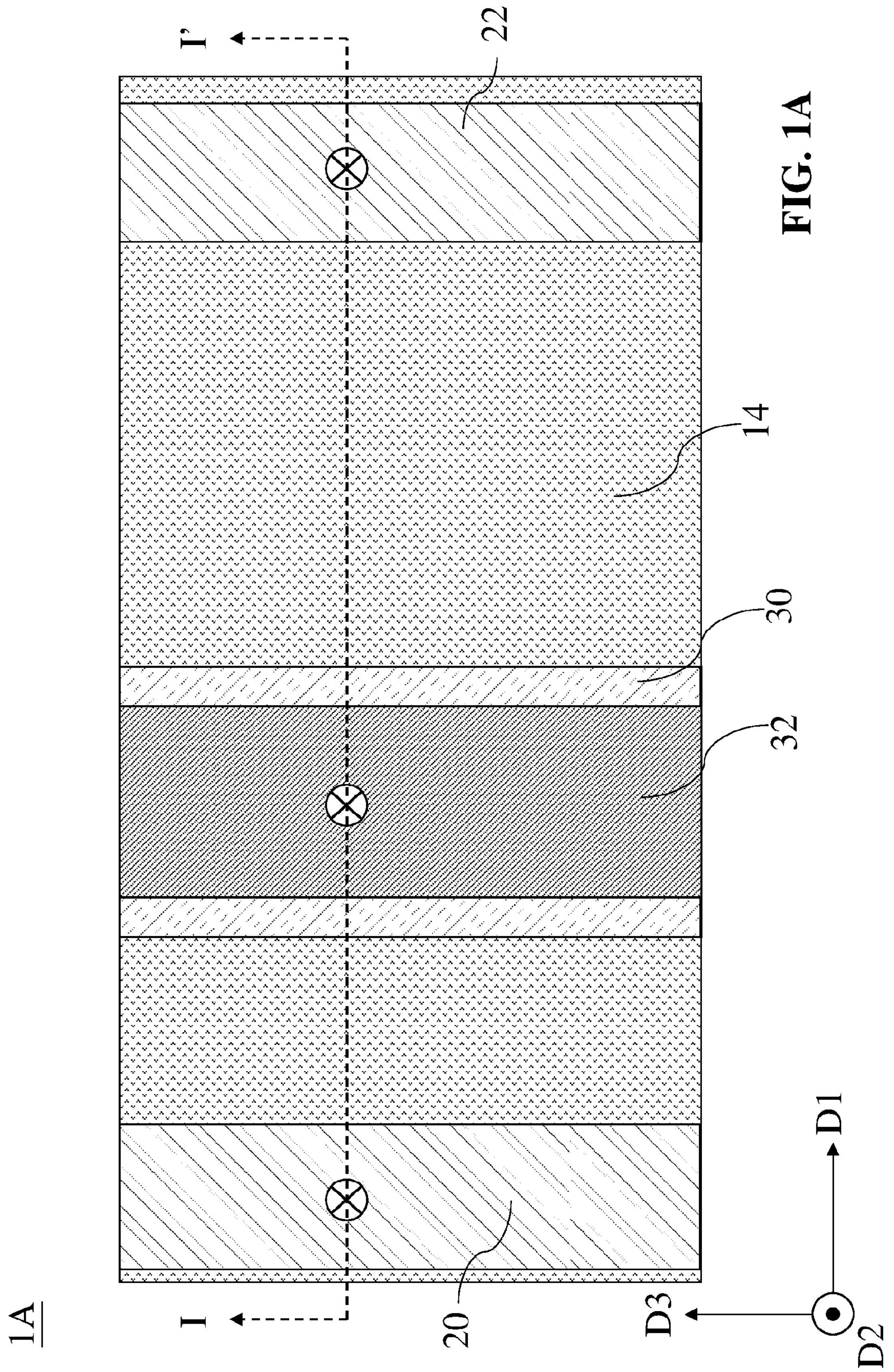

FIG. 1A

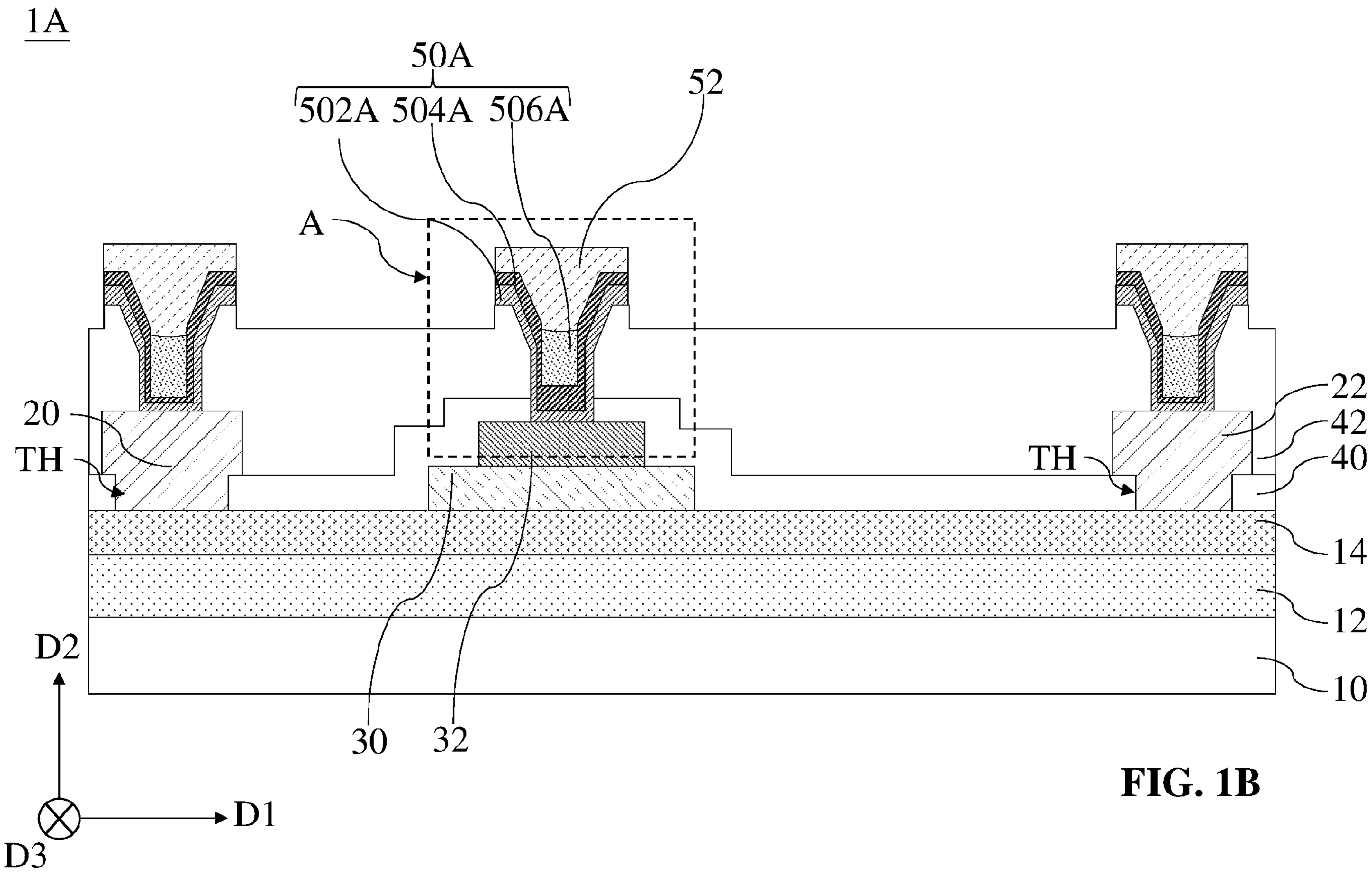

FIG. 1B

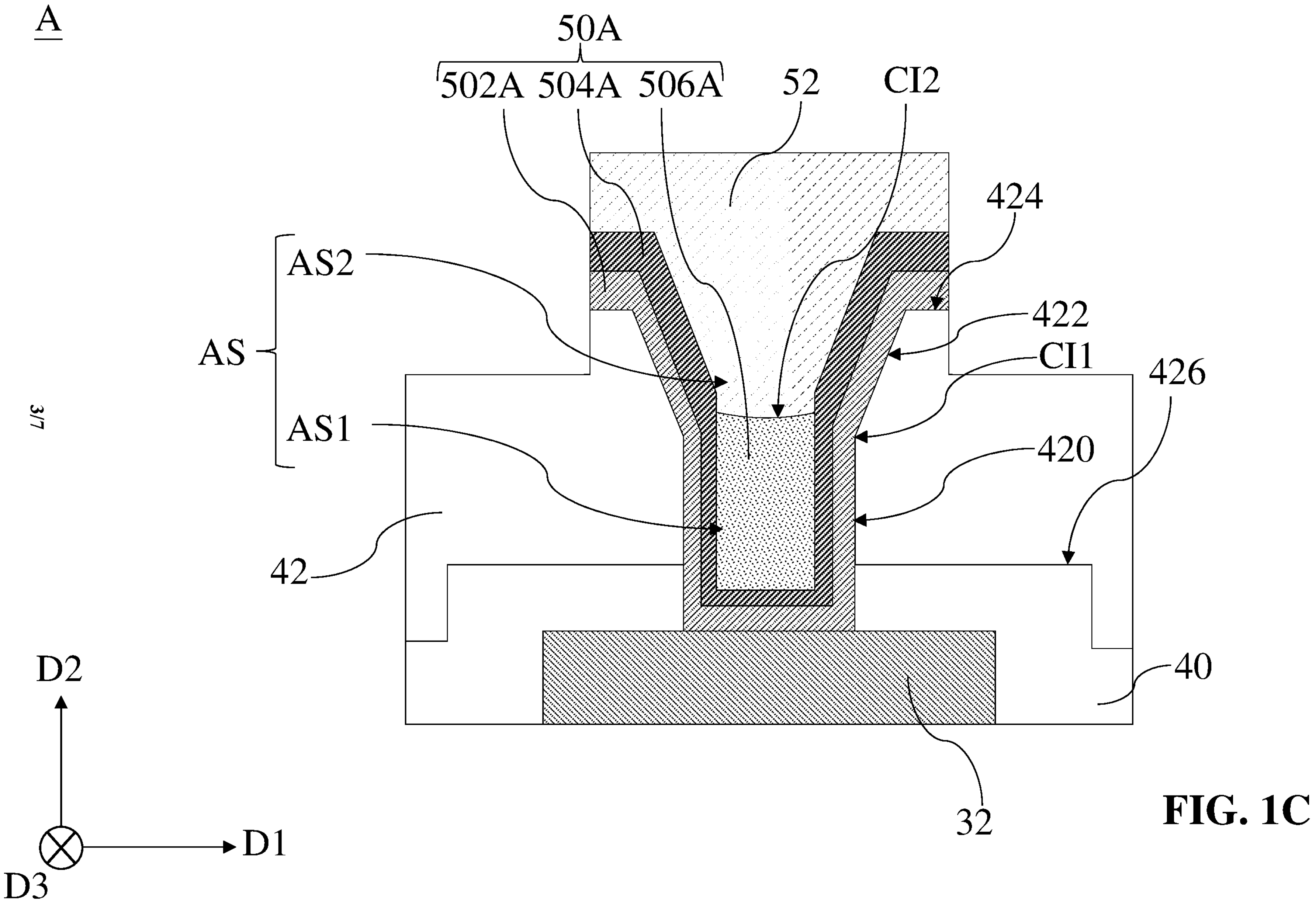

FIG. 1C

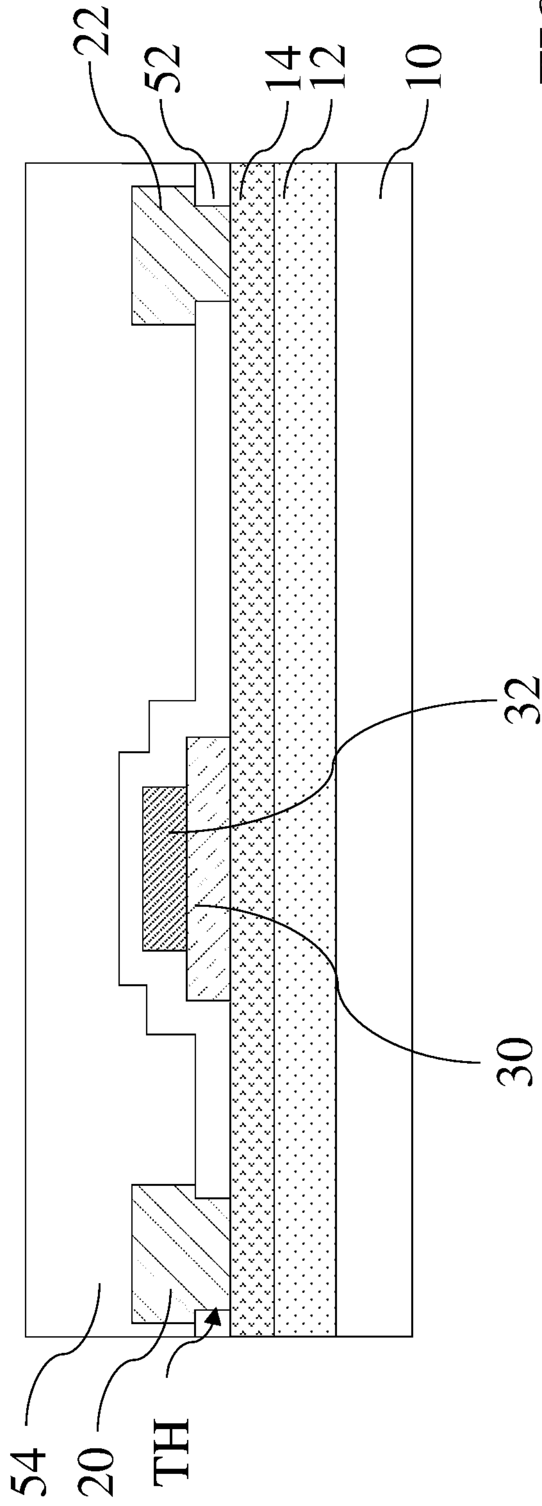

FIG. 2A

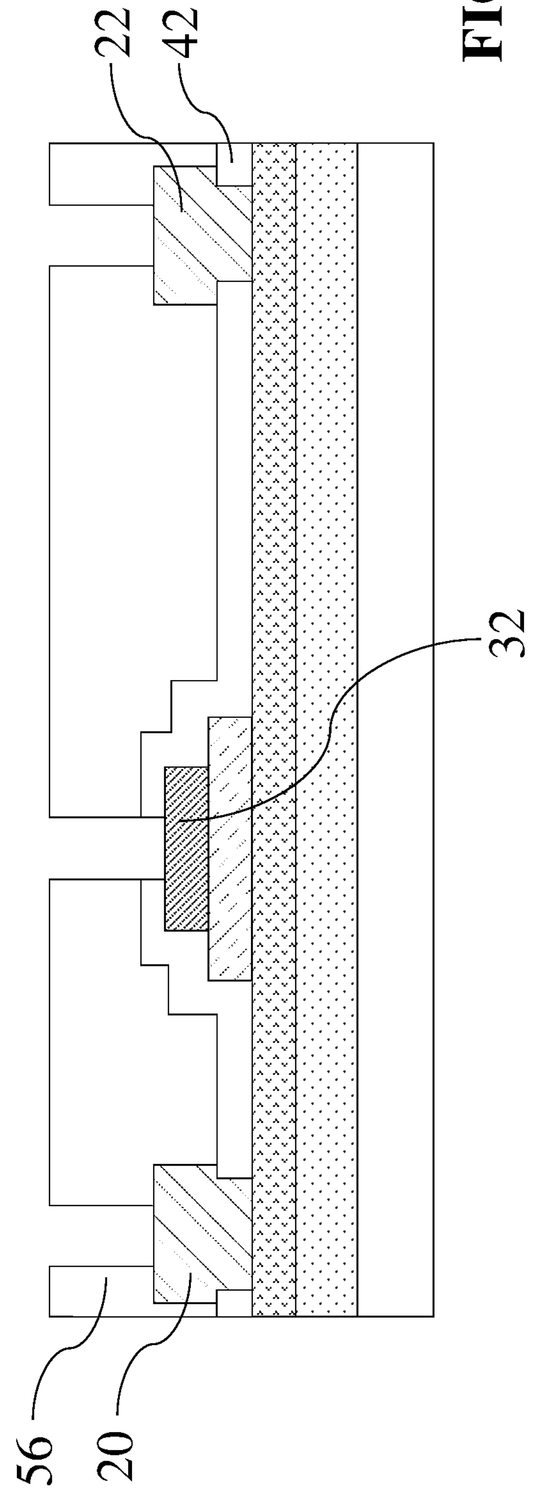

FIG. 2B

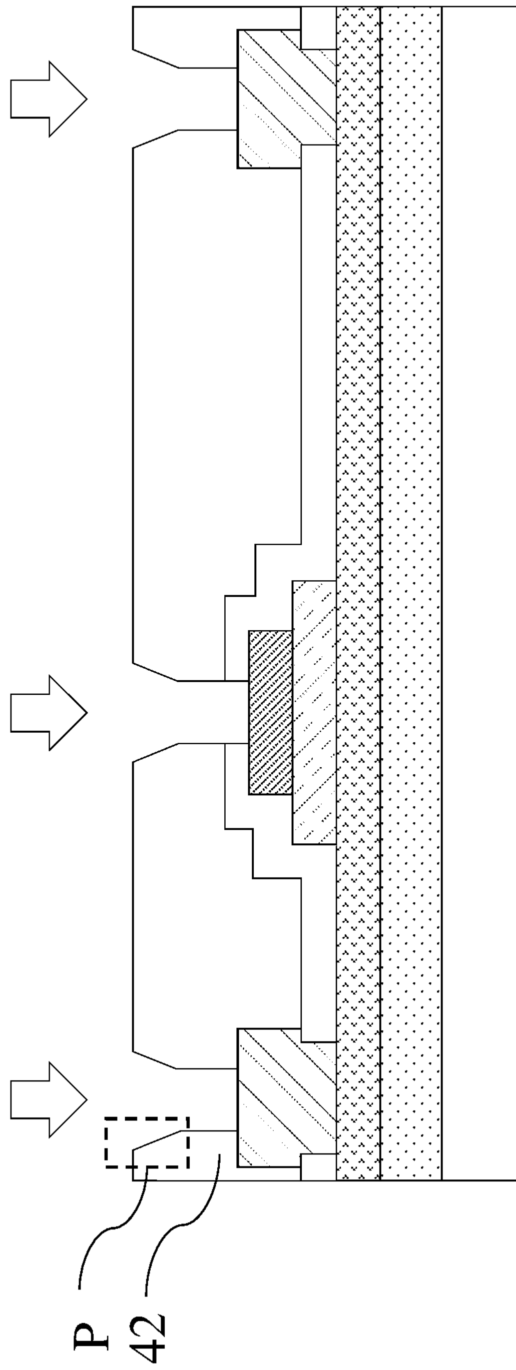

FIG. 2C

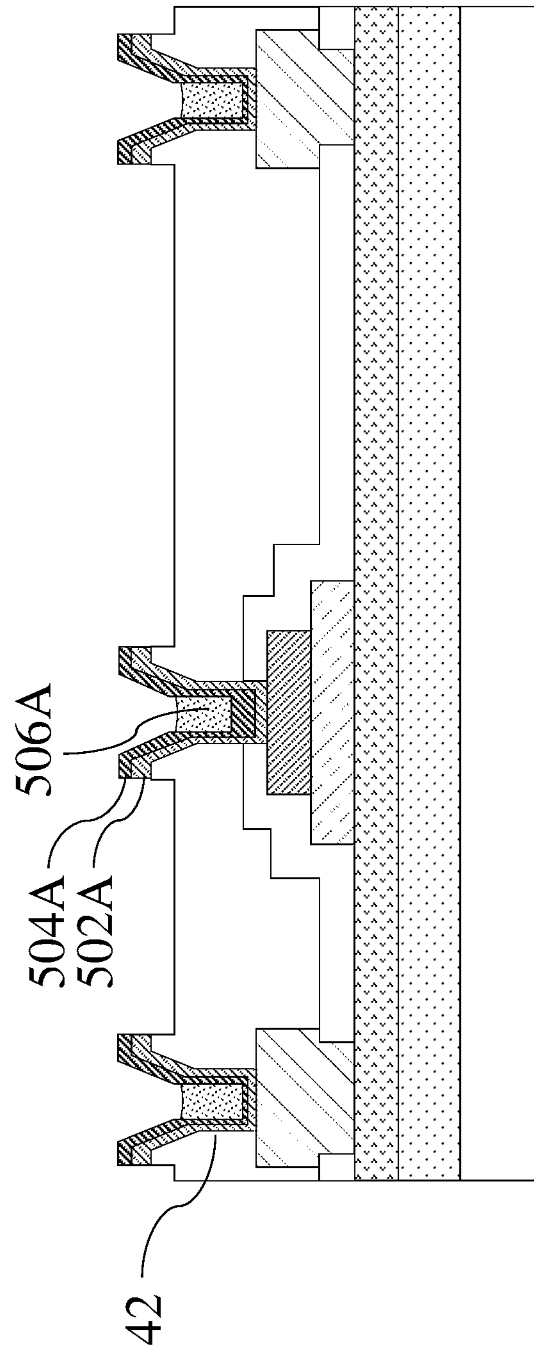

FIG. 2D

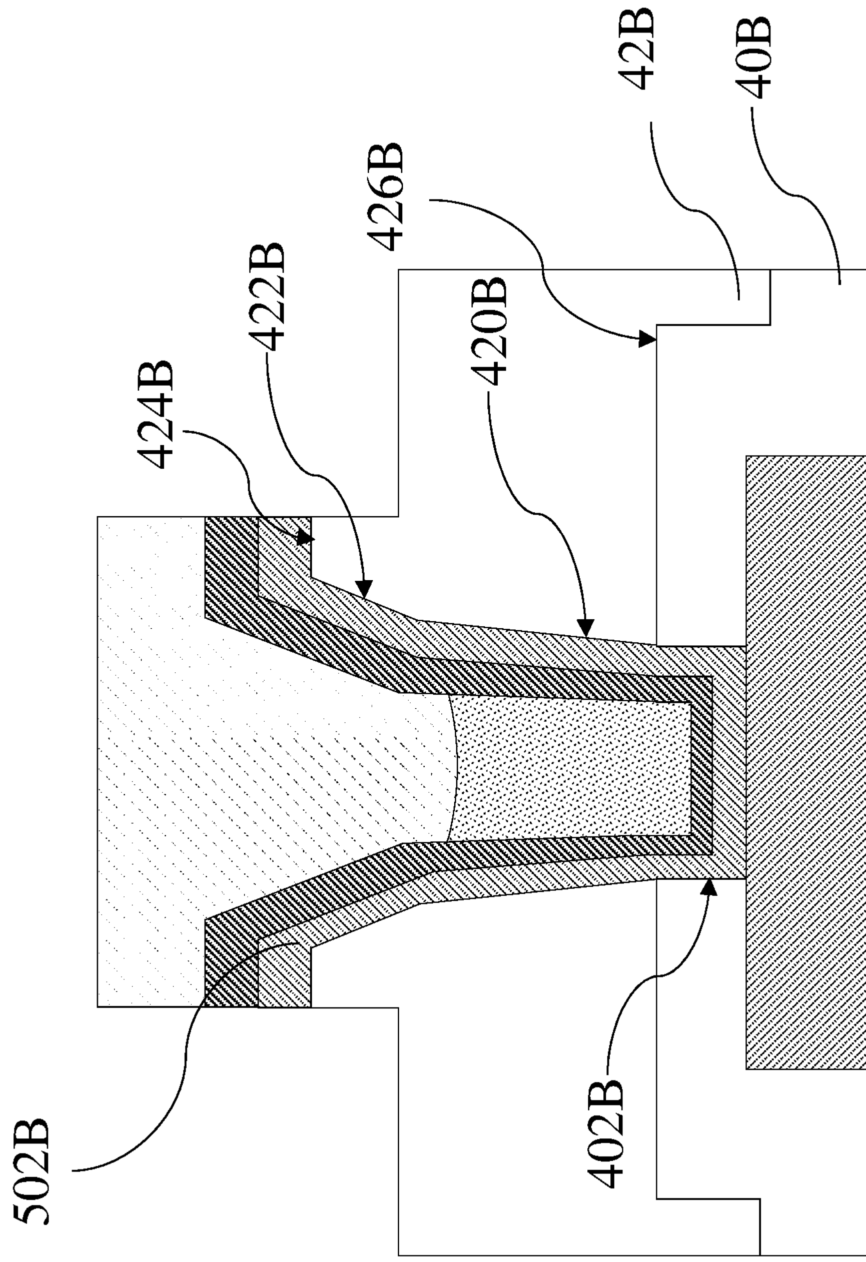

FIG. 3

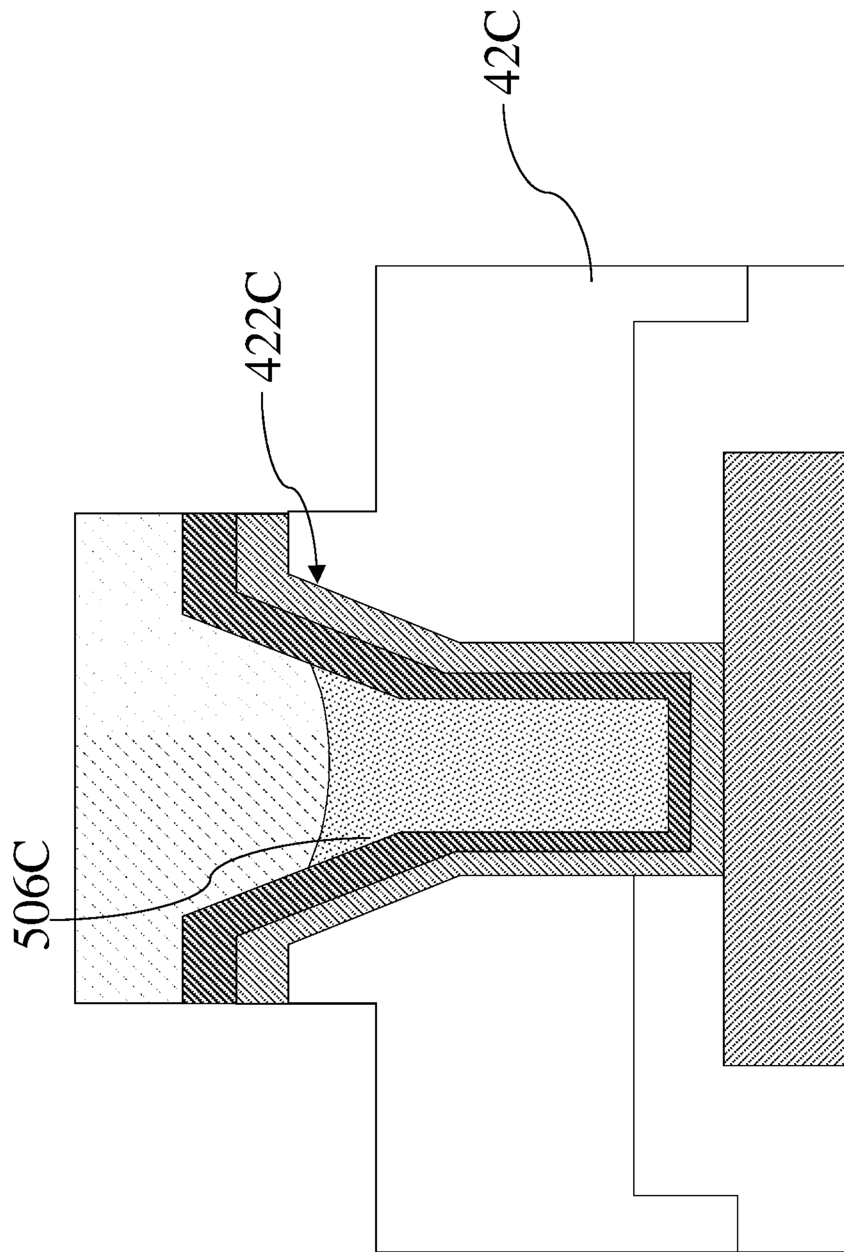

FIG. 4

1C

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2022/120122

A. CLASSIFICATION OF SUBJECT MATTER

H01L29/778(2006.01)i； H01L29/66(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

USTXT,VEN,WPABS,CNTXT:HEMT,gate,contact,taper+,chamfer,funnel,inclin+,slant,via?,hole?,opening?,groove?,recess+,stress,thermal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2021336016 A1 (VANGUARD INTERNATIONAL SEMICONDUCT CORP.) 28 October 2021 (2021-10-28) description paragraphs [0025]-[0042] and figures 1-9	1-25
Y	JP 2012033580 A (SUMITOMO ELECTRIC DEVICE INNOVATIONS INC.) 16 February 2012 (2012-02-16) description paragraphs [0031]-[0043] and figures 2-3	1-25
A	US 2012211891 A1 (INFINEON TECHNOLOGIES AG.) 23 August 2012 (2012-08-23) the whole document	1-25
A	JP 2015002299 A (ZYCUBE K.K.) 05 January 2015 (2015-01-05) the whole document	1-25
A	US 2014061725 A1 (SAMSUNG ELECTRONICS CO., LTD.) 06 March 2014 (2014-03-06) the whole document	1-25

☐ Further documents are listed in the continuation of Box C.　　☑ See patent family annex.

* Special categories of cited documents:
- "A" document defining the general state of the art which is not considered to be of particular relevance
- "D" document cited by the applicant in the international application
- "E" earlier application or patent but published on or after the international filing date
- "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- "O" document referring to an oral disclosure, use, exhibition or other means
- "P" document published prior to the international filing date but later than the priority date claimed
- "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
- "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
- "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
- "&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
17 May 2023	**23 May 2023**

Name and mailing address of the ISA/CN

CHINA NATIONAL INTELLECTUAL PROPERTY ADMINISTRATION
6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing 100088, China

Authorized officer

ZHANG,SiMi

Telephone No. **(+86) 010-53961227**

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2022/120122

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
US	2021336016	A1	28 October 2021	US	11380767	B2	05 July 2022
				US	2022293747	A1	15 September 2022
JP	2012033580	A	16 February 2012	JP	5649355	B2	07 January 2015
US	2012211891	A1	23 August 2012	US	9076821	B2	07 July 2015
				US	2015311163	A1	29 October 2015
				DE	102012222651	A1	13 June 2013
				DE	102012222651	B4	29 August 2019
				CN	105070747	A	18 November 2015
				CN	105070747	B	09 November 2018
				CN	103165663	A	19 June 2013
JP	2015002299	A	05 January 2015		None		
US	2014061725	A1	06 March 2014	KR	20140031001	A	12 March 2014
				KR	101980197	B1	20 May 2019
				US	8860089	B2	14 October 2014