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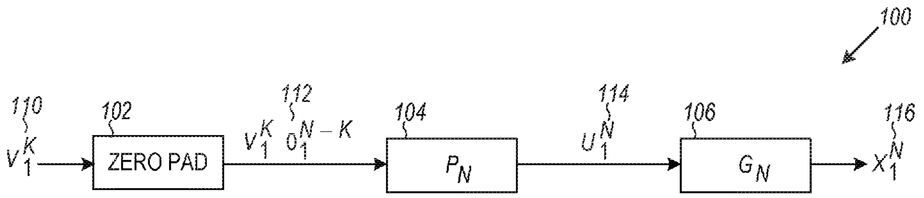

FIG. 1

(57) Abstract: Disclosed herein are user equipment (UE) and base station (eNB) apparatus and methodology for polar code construction, representation and encoding/decoding. An apparatus of a UE may include memory and processing circuitry coupled to the memory. The processing circuitry is configured to generate input vectors by adding zeros to a set of input bits. A polar code permutation vector is generated based on estimates of channel reliability of a transmission channel. The estimates are determined using a pre-defined range of signal-to-noise ratios (SNRs) of the transmission channel. The polar code permutation vector is applied to the input vectors to obtain a output permuted vectors. The output permuted vectors are polar coded using a generator matrix, to generate an encoded information block for transmission to an evolved Node-B (eNB) via the transmission channel.

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CONSTRUCTING, REPRESENTING, AND ENCODING POLAR CODES

PRIORITY CLAIM

[0001] This application claims the benefit of priority to United States Provisional Patent Application Serial No. 62/335,261, filed May 12, 2016, and entitled "CONSTRUCTING, REPRESENTING, AND ENCODING POLAR CODES," and United States Provisional Patent Application Serial No. 62/336,402, filed May 13, 2016, and entitled "POLAR CODE CONSTRUCTION," which applications are incorporated herein by reference in their entireties.

TECHNICAL FIELD

[0002] Embodiments pertain to wireless communications. Some embodiments relate to constructing, representing and encoding polar codes.

BACKGROUND

[0003] With the increase in different types of devices communicating with various network devices, usage of 3GPP LTE systems has increased. The penetration of mobile devices (user equipment or UEs) in modern society has continued to drive demand for a wide variety of networked devices in a number of disparate environments. The use of networked UEs using 3GPP LTE systems has increased in all areas of home and work life. Fifth generation (5G) wireless systems are forthcoming, and are expected to enable even greater speed, connectivity, and usability.

[0004] One concern with wireless communications is using reliable error correction techniques. Polar coding is a new error correction coding technique with theoretical guarantees to achieve the capacity of communication channels. One of the main drawbacks of known polar codes is that their performance under successive cancellation (SC) decoding is inferior to that of turbo and low-density parity-check (LDPC) codes. More involved decoders like list decoders and maximum likelihood (ML) decoders improve known polar codes' performance only marginally. Known polar code constructions become efficient only when aided by an additional cyclic redundancy check (CRC), which contributes to increased system complexity and processing times.

BRIEF DESCRIPTION OF THE FIGURES

[0005] In the figures, which are not necessarily drawn to scale, like numerals may describe similar components in different views. Like numerals having different letter suffixes may represent different instances of similar components. Some embodiments are illustrated by way of example, and not limitation, in the following figures of the accompanying drawings.

[0006] FIG. 1 is a diagram of a polar code encoder in accordance with some embodiments.

[0007] FIG. 2 is a flow diagram of a method to encode input bits using a polar code in accordance with some embodiments.

[0008] FIG. 3 is a flow diagram of a method to generate a polar code in accordance with some embodiments.

[0009] FIG. 4 is a functional diagram of a User Equipment (UE) using a polar encoder in accordance with some embodiments.

[0010] FIG. 5 is a diagram of a size N polar code generator in accordance with some embodiments.

[0011] FIG. 6 is a flow diagram of a method for generating a representation of a polar code permutation vector using a smaller size polar code permutation vector and a bit sequence in accordance with some embodiments.

[0012] FIG. 7 is a flow diagram illustrating example functionalities for generating a polar code permutation vector, in accordance with an example embodiment.

[0013] FIG. 8 illustrates a block diagram of a communication device such as an Evolved Node-B (eNB) or a user equipment (UE), in accordance with some embodiments.

DETAILED DESCRIPTION

[0014] The following description and the drawings sufficiently illustrate specific embodiments to enable those skilled in the art to practice them. A number of examples are described in the context of 3GPP communication systems and components thereof. It will be understood that principles of the embodiments are applicable in other types of communication systems, such as Wi-Fi or Wi-Max networks, Bluetooth or other personal-area networks, Zigbee or other home-area networks, wireless mesh networks, and the like, without limitation, unless expressly limited by a corresponding claim. Given the benefit of the present disclosure, persons skilled in the relevant technologies will be able to engineer suitable variations to implement principles of the embodiments in other types of communication systems. Various diverse embodiments may incorporate structural, logical, electrical, process, and other differences. Portions and features of some embodiments may be included in, or substituted for, those of other embodiments. Embodiments set forth in the claims encompass all presently-known, and after-arising, equivalents of those claims.

[0015] FIG. 1 is a diagram of a polar code encoder in accordance with some embodiments. Referring to FIG. 1, the polar code encoder 100 may include a zero padding block 102, a polar code permutation block 104 and a generator matrix G_N 106, where N is the size of the polar code encoder and the number of generated output bits.

[0016] Polar codes belong to a class of affine codes that can be generated by subsets of the rows of the generator matrix 106:

[0017] $$G_N = \begin{bmatrix} 1 & 0 \\ 1 & 1 \end{bmatrix}^{\otimes log_2 N},$$

where "$\otimes$" denotes a Kronecker power. In some embodiments, a rate K/N code (which may or may not be used as a polar code) may be generated by picking any K rows of G_N as a generator matrix. One or more codes in this class can be encoded by the matrix multiplication $U_1^N G_N$, where U_i is set to a data bit if the i^th row of G_N is in the code's generator matrix, and otherwise

U_i is set to a predetermined value, e.g., zeros. Such a code can be referred to as a polar code if its generator matrix includes K rows of G_N that satisfy $Z(W_i) \leq Z(W_j)$ if i^{th} row is in the matrix and j^{th} row is not. Here, W_i is the channel associated with bit i, with input U_i and output $Y_1^N U_1^{i-1}$, where Y_1^N denotes the output of the channel with input $U_1^N G_N$. Z denotes the Bhattacharyya parameter, which is the reliability associated with communicating the i^{th} bit on the W(i) channel. The order of $Z(W_i)$'s depends on the underlying channel and thus polar codes are channel-specific designs. These codes may have good performance under successive cancellation (SC) decoding and indeed achieve channel capacity. Although very few codes are true polar codes according to this strict definition (in particular, if the order of $Z(W_i)$s is unique for a given W, there is a unique polar code for that channel and given rate), many codes that do not necessarily adhere to the above rule may be called polar codes. In some embodiments, all of these codes share the property that $Z(W_i)$ be "small" if the i^th row is included in the generator matrix. Embodiments of the present disclosure also follow this practice and thus the codes here will also be called polar codes.

[0018] Embodiments of the present disclosure are directed to a class of polar codes that have excellent performance under list decoding, without the aid of an external CRC. This simplifies their decoding, and eliminates CRC overhead. In addition, a single "permutation" is used to represent codes of arbitrary rates. That is, for a given code length, codes of all rates can be encoded using the same mechanism.

[0019] The reliability of each bit U_i under SC decoding can be estimated closely by a recursive "polarize--quantize" technique. A linear-time algorithm may be used to estimate $Z(W_i)$ values very closely and one or more of the most reliable bits may be selected. However, this bit selection only optimizes performance under SC decoder, but this performance itself is may not be compatible with other alternatives like Turbo and LDPC codes. In contrast, embodiments of the code constructions in the present disclosure may be only slightly less optimal under SC decoding, but are significantly superior to other constructions under list decoding. Additionally, unlike other constructions, these codes do not need the CRC to improve decoding performance.

[0020] Referring to FIG. 1, K input data bits 110 (V_1, ..., V_k) are to be encoded by a rate K/N code. In order to do so, the zero padding block 102 may be used to zero pad the input bits 110 V_1, ..., V_k with (N-K) bits of predetermined values (for example, zero bits) to obtain the length N vector 112 $(V_1,\ldots V_K,0,\ldots,0)$. This vector is then permuted by the polar code permutation vector P_N 104, and the permuted N-bit vector 114 is communicated as input to the generator matrix 106, which generates the polar coded data bits 116. The selection of the polar code permutation vector 104 may depend on N, but not on K. Therefore, codes of all rates at a given length N may be encoded by the same encoder 100.

[0021] FIG. 2 is a flow diagram of a method to encode input bits using a polar code in accordance with some embodiments. Referring to FIGS. 1 and 2, the example method 200 may start at 202, when a length N input vector (e.g., 112) may be generated based on K input data bits (e.g., 110), where K and N may be integers with K being less than or equal to than N. In an example, the input data bits 110 may be zero-padded so that the input vector 112 of length N is generated, which may include the K input bits and (N-K) zeros (or other predetermined bits). At 204, the input vector 112 is permuted by the polar code permutation vector 104 to generate the permuted N-bit vector 114. At 206, the permuted N-bit vector 114 is encoded by the generator matrix G_N 106 to generate coded data bits X_N 116 as output. At 208, the coded data bits X_N 116 can be transmitted.

[0022] Example polar code permutation vectors (that is, permutations) for code lengths 2^n for $n = 5,\ldots,13$ are given in Listing A below. One or more other permutation vectors may be derived from the permutations listed in Listing A. For example, if system requirements dictate that data be encoded at rates $K\_1/N, K\_2/N,\ldots K\_m/N$ for a given N, then any permutation derived from P_N by permuting the first K_1 numbers $P_N(1),\ldots P_N(K_1)$ among themselves can be used. Similarly, the numbers $P_N(K_1 + 1), \ldots, P_N(K_1 + K_2)$ can be permuted among themselves, and so can the numbers $P_N(K_1 + K_2 + 1), \ldots P_N(K_1 + K_2 + K_3)$, and so on. Alternatively, any other permutation that can be derived from P_N may be used as well. One suitable class of such permutations is defined by setting a threshold α, with all numbers in the derived permutation being at most α positions away from their positions in P_N. In other words, if R_N is the derived permutation, the following condition is satisfied $R_N(i) = P_N(j)$ for some $i - \alpha \leq j \leq i + \alpha$. Such a derived permutation may be preferred if, for instance, it can be more efficiently represented in memory. In this regard, there may be a trade-off between how large α is and how robust a performance the derived permutation will have. Thus the choice of the derived permutation may be based on error performance versus implementation efficiency considerations.

[0023] Design of the polar code permutation vectors (or permutations) listed in Listing A.

[0024] Approximately optimal polar codes for SC decoding may be constructed using the "polarize--quantize" technique. However, bit selection using this technique may not lead to codes that are competitive with the state-of-the-art LDPC or Turbo codes unless the decoding of these polar codes is augmented by a CRC stage. The quantization technique used in embodiments of the present disclosure to estimate the bit reliabilities leads to only slight performance loss under SC decoding (which in many cases may not be the decoder of choice), but dramatically improves performance under list decoding.

[0025] In some embodiments, generation of the permutations listed in Listing A may start by estimating the bit-channel reliabilities for all channel signal-to-noise ratios (SNRs) from, e.g., -8dB to 11dB, with 0.5dB increments. These constructions are then tested at different rates and channel conditions. In some examples, the construction SNR that achieves optimal performance may be between 0dB and 2dB above the true channel SNR.

[0026] The permutations may be generated using the technique described below and illustrated in the flow diagram of FIG. 3. FIG. 3 is a flow diagram of a method 300 to generate a polar code in accordance with some embodiments.

[0027] At 302, the permutation vector length may be fixed at length N. Bit-channel estimation may be performed with underlying transmission channel SNRs ranging from snr_{min} to snr_{max}, with increments of snr_{inc}. In this regard, a plurality of estimates of channel reliability (e.g., Z(Wi)) may be generated for a transmission channel W(i). For example, to derive the permutations in Listing A, the following SNR values may be used: $snr_{min} = -8dB$, $snr_{max} = 11dB$, and $snr_{inc} = 0.5dB$. In the description below, the underlying channel SNR may be referred to as snr_{target}.

[0028] At 304, the polar code permutation vector is initialized as an empty permutation vector. At the end of the flow diagram in FIG. 3 this vector will have length N.

[0029] At 306, an iteration loop may be performed with SNR values of $snr_{channel} = snr_{min}$, till $snr_{channel} = snr_{max}$ with increments at SNR_{inc}. At 308, for construction rules at $snr_{target} = snr_{channel} + \{0, 0.5, 1, 1.5, 2\}dB$, the rate may be found, at which each construction rule achieves a target block error rate (BLER) (e.g., BLER=1% or another predetermined rate). At 310, the construction rule with the highest rate may be selected. At 312, it may be determined for the selected construction rule and its rate, whether the data bits associated with the rule are a superset of a previous permutation vector (e.g., a permutation vector generated during a previous iteration cycle). At 316, when the data bits associated with the rule are a superset of the previous permutation vector, then the new bit positions are appended to the permutation vector. At 314, when the data bits associated with the rule are not a superset of the previous permutation vector, then the next best construction rule is selected and processing may resume at 308. In instances when no construction rule passes the test in 308, then an error notification may be presented and no permutation vector is generated. At 318, the permutation vector may be appended with any missing bit positions so that a total of N positions are included in the permutation vector.

[0030] In some embodiments, the above technique may simultaneously provide that the constructed codes are nested so that codes of lower rate are sub-codes of those at higher rates, and that codes of all rates have error performance that satisfies a pre-determined error rate. Many refinements and variations on the above technique are possible. For example, a more finely nested construction may be obtained by considering construction and channel SNRs at smaller SNR increments.

[0031] FIG. 4 is a functional diagram of a User Equipment (UE) using a polar encoder in accordance with some embodiments. In some embodiments, the UE 400 may include application circuitry 402, baseband circuitry 404, Radio Frequency (RF) circuitry 406, front-end module (FEM) circuitry 408, and multiple antennas 410A-410D, coupled together at least as shown. In some embodiments, other circuitry or arrangements may include one or more elements or components of the application circuitry 402, the baseband circuitry 404, the RF circuitry 406 or the FEM circuitry 408, and may also include other elements or components in some cases. As an example, “processing circuitry” may include one or more elements or components, some or all of which may be included in the application circuitry 402 or the baseband circuitry 404. As another example, “transceiver circuitry” may include one or more elements or components, some or all of which may be included in the RF circuitry 406 or the FEM circuitry 408. These examples are not limiting, however, as the processing circuitry or the transceiver circuitry may also include other elements or components in some cases.

[0032] The application circuitry 402 may include one or more application processors. For example, the application circuitry 402 may include circuitry such as, but not limited to, one or more single-core or multi-core processors. The processor(s) may include any combination of general-purpose processors and dedicated processors (e.g., graphics processors, application processors, etc.). The processors may be coupled with or may include memory/storage and may be configured to execute instructions stored in the memory/storage to enable various applications or operating systems to run on the system to perform one or more of the functionalities described herein.

[0033] The baseband circuitry 404 may include circuitry such as, but not limited to, one or more single-core or multi-core processors. The baseband circuitry 404 may include one or more baseband processors or control logic to process baseband signals received from a receive signal path of the RF circuitry 406 and to generate baseband signals for a transmit signal path of the RF circuitry 406. Baseband processing circuity 404 may interface with the application circuitry 402 for generation and processing of the baseband signals and for controlling operations of the RF circuitry 406. For example, in some embodiments, the baseband circuitry 404 may include a second generation (2G) baseband processor 404a, third generation (3G) baseband processor 404b, fourth generation (4G) baseband processor 404c, or other baseband processor(s) 404d for other existing generations, generations in development or to be developed in the future (e.g., fifth generation (5G), 6G, etc.). The baseband circuitry 404 (e.g., one or more of baseband processors 404a-d) may handle various radio control functions that enable communication with one or more radio networks via the RF circuitry 406.

[0034] The radio control functions may include, but are not limited to, signal modulation/demodulation, encoding/decoding, radio frequency shifting, etc. In some embodiments, modulation/demodulation circuitry of the baseband circuitry 404 may include Fast-Fourier Transform (FFT), precoding, or constellation mapping/demapping functionality. In some embodiments, encoding/decoding circuitry of the baseband circuitry 404 may include Low Density Parity Check (LDPC) encoder/decoder functionality, optionally along-side other techniques such as, for example, block codes, convolutional codes, turbo codes, or the like, which may be used to support legacy protocols. Embodiments of modulation/demodulation and encoder/decoder functionality are not limited to these examples and may include other suitable functionality in other embodiments.

[0035] In some embodiments, the baseband circuitry 404 may include elements of a protocol stack such as, for example, elements of an evolved universal terrestrial radio access network (EUTRAN) protocol including, for example, physical (PHY) 405a, media access control (MAC) 405b, radio link control (RLC) 405c, packet data convergence protocol (PDCP) 405d, and/or radio resource control (RRC) 405e elements.

[0036] A central processing unit (CPU) 404e of the baseband circuitry 404 may be configured to run elements of the protocol stack for signaling of the PHY, MAC, RLC, PDCP or RRC layers. In some embodiments, the baseband circuitry may include one or more audio digital signal processor(s) (DSP) 404f. The audio DSP(s) 404f may be include elements for compression/decompression and echo cancellation and may include other suitable processing elements in other embodiments. Components of the baseband circuitry may be suitably combined in a single chip, a single chipset, or disposed on a same circuit board in some embodiments. In some embodiments, some or all of the constituent components of the baseband circuitry 404 and the application circuitry 402 may be implemented together such as, for example, on a system on chip (SOC).

[0037] In some embodiments, the baseband circuitry 404 may provide for communication compatible with one or more radio technologies. For example, in some embodiments, the baseband circuitry 404 may support communication with an evolved universal terrestrial radio access network (EUTRAN) or other wireless metropolitan area networks (WMAN), a wireless local area network (WLAN), a wireless personal area network (WPAN). Embodiments in which the baseband circuitry 404 is configured to support radio communications of more than one wireless protocol may be referred to as multi-mode baseband circuitry.

[0038] In some embodiment, the baseband circuitry 204 may include a polar code encoder 404g, which may be configured to perform one or more of the functionalities disclosed herein in connection with construction, representation and encoding of polar codes, including polar code permutation vectors. In an example, the encoder 404g may be similar to the polar code encoder 100 of FIG. 1, and performing one or more of the functions described herein and also illustrated in one or more of the flow diagrams in the attached figures.

[0039] RF circuitry 406 may enable communication with wireless networks using modulated electromagnetic radiation through a non-solid medium. In various embodiments, the RF circuitry 406 may include switches, filters, amplifiers, etc. to facilitate the communication with the wireless network. RF circuitry 406 may include a receive signal path which may include circuitry to down-convert RF signals received from the FEM circuitry 408 and provide baseband signals to the baseband circuitry 404. RF circuitry 406 may also include a transmit signal path which may include circuitry to up-convert baseband signals provided by the baseband circuitry 404 and provide RF output signals to the FEM circuitry 408 for transmission.

[0040] In some embodiments, the RF circuitry 406 may include a receive signal path and a transmit signal path. The receive signal path of the RF circuitry 406 may include mixer circuitry 406a, amplifier circuitry 406b and filter circuitry 406c. The transmit signal path of the RF circuitry 406 may include filter circuitry 406c and mixer circuitry 406a. RF circuitry 406 may also include synthesizer circuitry 406d for synthesizing a frequency for use by the mixer circuitry 406a of the receive signal path and the transmit signal path. In some embodiments, the mixer circuitry 406a of the receive signal path may be configured to down-convert RF signals received from the FEM circuitry 408 based on the synthesized frequency provided by synthesizer circuitry 406d. The amplifier circuitry 406b may be configured to amplify the down-converted signals and the filter circuitry 406c may be a low-pass filter (LPF) or band-pass filter (BPF) configured to remove unwanted signals from the down-converted signals to generate output baseband signals. Output baseband signals may be provided to the baseband circuitry 404 for further processing. In some embodiments, the output baseband signals may be zero-frequency baseband signals, although this is not a requirement. In some embodiments, mixer circuitry 406a of the receive signal path may comprise passive mixers, although the scope of the embodiments is not limited in this respect. In some embodiments, the mixer circuitry 406a of the transmit signal path may be configured to up-convert input baseband signals based on the synthesized frequency provided by the synthesizer circuitry 406d to generate RF output signals for the FEM circuitry 408. The baseband signals may be provided by the baseband circuitry 404 and may be filtered by filter circuitry 406c. The filter circuitry 406c may include a low-pass filter (LPF), although the scope of the embodiments is not limited in this respect.

[0041] In some embodiments, the mixer circuitry 406a of the receive signal path and the mixer circuitry 406a of the transmit signal path may include two or more mixers and may be arranged for quadrature downconversion or upconversion respectively. In some embodiments, the mixer circuitry 406a of the receive signal path and the mixer circuitry 406a of the transmit signal path may include two or more mixers and may be arranged for image rejection (e.g., Hartley image rejection). In some embodiments, the mixer circuitry 406a of the receive signal path and the mixer circuitry 406a may be arranged for direct downconversion or direct upconversion, respectively. In some embodiments, the mixer circuitry 406a of the receive signal path and the mixer circuitry 406a of the transmit signal path may be configured for super-heterodyne operation.

[0042] In some embodiments, the output baseband signals and the input baseband signals may be analog baseband signals, although the scope of the embodiments is not limited in this respect. In some alternate embodiments, the output baseband signals and the input baseband signals may be digital baseband signals. In these alternate embodiments, the RF circuitry 406 may include analog-to-digital converter (ADC) and digital-to-analog converter (DAC) circuitry and the baseband circuitry 404 may include a digital baseband interface to communicate with the RF circuitry 406. In some dual-mode embodiments, a separate radio IC circuitry may be provided for processing signals for each spectrum, although the scope of the embodiments is not limited in this respect.

[0043] In some embodiments, the synthesizer circuitry 406d may be a fractional-N synthesizer or a fractional N/N+1 synthesizer, although the scope of the embodiments is not limited in this respect as other types of frequency synthesizers may be suitable. For example, synthesizer circuitry 406d may be a delta-sigma synthesizer, a frequency multiplier, or a synthesizer comprising a phase-locked loop with a frequency divider. The synthesizer circuitry 406d may be configured to synthesize an output frequency for use by the mixer circuitry 406a of the RF circuitry 406 based on a frequency input and a divider control input. In some embodiments, the synthesizer circuitry 406d may be a fractional N/N+1 synthesizer. In some embodiments, frequency input may be provided by a voltage controlled oscillator (VCO), although that is not a requirement. Divider control input may be provided by either the baseband circuitry 404 or the applications processor 402 depending on the desired output frequency. In some embodiments, a divider control input (e.g., N) may be determined from a look-up table based on a channel indicated by the applications processor 402.

[0044] Synthesizer circuitry 406d of the RF circuitry 406 may include a divider, a delay-locked loop (DLL), a multiplexer and a phase accumulator. In some embodiments, the divider may be a dual modulus divider (DMD) and the phase accumulator may be a digital phase accumulator (DPA). In some embodiments, the DMD may be configured to divide the input signal by either N or N+1 (e.g., based on a carry out) to provide a fractional division ratio. In some example embodiments, the DLL may include a set of cascaded, tunable, delay elements, a phase detector, a charge pump and a D-type flip-flop. In these embodiments, the delay elements may be configured to break a VCO period up into Nd equal packets of phase, where Nd is the number of delay elements in the delay line. In this way, the DLL provides negative feedback to help ensure that the total delay through the delay line is one VCO cycle.

[0045] In some embodiments, synthesizer circuitry 406d may be configured to generate a carrier frequency as the output frequency, while in other embodiments, the output frequency may be a multiple of the carrier frequency (e.g., twice the carrier frequency, four times the carrier frequency) and used in conjunction with quadrature generator and divider circuitry to generate multiple signals at the carrier frequency with multiple different phases with respect to each other. In some embodiments, the output frequency may be a LO frequency (fLO). In some embodiments, the RF circuitry 406 may include an IQ/polar converter.

[0046] FEM circuitry 408 may include a receive signal path, which may include circuitry configured to operate on RF signals received from one or more of the antennas 410A-D, amplify the received signals and provide the amplified versions of the received signals to the RF circuitry 406 for further processing. FEM circuitry 408 may also include a transmit signal path which may include circuitry configured to amplify signals for transmission provided by the RF circuitry 406 for transmission by one or more of the one or more antennas 410A-D.

[0047] In some embodiments, the FEM circuitry 408 may include a TX/RX switch to switch between transmit mode and receive mode operation. The FEM circuitry may include a receive signal path and a transmit signal path. The receive signal path of the FEM circuitry may include a low-noise amplifier (LNA) to amplify received RF signals and provide the amplified received RF signals as an output (e.g., to the RF circuitry 406). The transmit signal path of the FEM circuitry 408 may include a power amplifier (PA) to amplify input RF signals (e.g., provided by RF circuitry 406), and one or more filters to generate RF signals for subsequent transmission (e.g., by one or more of the one or more antennas 410. In some embodiments, the UE 400 may include additional elements such as, for example, memory/storage, display, camera, sensor, or input/output (I/O) interface.

[0048] In an example, a single "permutation" technique for generating a polar code permutation vector may provide optimal performance with relatively low processing resource requirements. However, in instances when a large polar code permutation vector is used for polar coding, a large memory may be required during processing. For example, in order to represent a polar code permutation vector of codeword length N = 8192, 13 x 8192 = 106496 bits are required, which is 13KB (this large codeword is listed in Listing A). Using various techniques, an approximation of the "permutation" (or permutation vector) may be utilized with smaller memory requirement with marginal performance degradation.

[0049] For example, a polar code permutation vector of a large codeword size may be represented using a permutation vector of a smaller size and a bit sequence. More specifically, two sets of small codeword permutation vectors may be generated. One is the small codeword permutation vector and the other may be prepared from the small codeword permutation vector and a value that represents the size of the permutation vector. The two smaller permutation vectors may then be compared with the long codeword (optimal) permutation. More specifically, indices from both small codeword permutation vectors are compared with a corresponding index in the optimal permutation to determine which one provides less offset from the optimal permutation. A corresponding position in the bit sequence is then marked with 1, if less offset is provided from the second permutation vector, otherwise the corresponding position in the bit sequence is marked with 0. In some examples, the bit sequence can be represented by a binary run-length code, as further explained below.

[0050] In embodiments, the device 400 of FIG. 4, and/or circuitry of the device 400 such as the RF circuitry 406, the baseband circuitry 404, and/or other circuitry may be configured to: receive an indication of a codeword to be represented using polar codes, where the codeword size is larger than a small codeword size used to represent the codeword; generate a small codeword permutation and a bit sequence to represent the codeword; and send the represented codeword. In other embodiments, the device 400 such as the RF circuitry 406, the baseband circuitry 404, and/or other circuitry may be configured to: generate a first polar code permutation of a first size and a first binary sequence; determine a permutation replica based on the first polar code permutation; and output indices from the first polar code permutation and the permutation replica based on the first binary sequence to form a second polar code permutation for the second size

[0051] In some embodiments, the electronic device 400 such as the RF circuitry 406, the baseband circuitry 404, and/or other circuitry may be configured to perform one or more processes, techniques, and/or methods as described herein, or portions thereof. One such process may include identifying or causing to identify a large codeword to be represented using polar codes; representing or causing to represent the large codeword using a small codeword permutation and a bit sequence; and transmitting or causing to transmit the represented codeword. Another such process may include acquiring or causing to acquire a first polar code permutation of a first size and a first binary sequence; obtaining or causing to obtain a permutation replica based on the first polar code permutation; and reading or causing to read out indices from the first polar code permutation and the permutation replica based on the first binary sequence to form a second polar code permutation for the second size.

[0052] Even though the components of FIG. 4 are discussed in reference to a UE, the same components and functionalities may also be associated with an evolved Node B (eNB).

[0053] FIG. 5 is a diagram of a size N polar code generator in accordance with some embodiments. Referring to FIG. 5, the generator 500 may include two polar code generators (502 and 504) for polar codes of size N/2. The two polar codes generated by polar code generators 502 and 504 may be combined with a polarization operation $(\oplus)$ 506. For example, after the polarization 506, the channel of the N/2 polar code generator block 502 may be degraded, while the channel of the lower N/2 polar code generator block 504 may be upgraded. Using this property, size N polar code construction rule may be represented using size N/2 polar code construction rule. The order of bit positions within the permutation vector contains information of ordering of a bit channel at the information bit position where information bits are loaded in the order of permutation and according to the coding rate. Remaining bits may be filled with predetermined values, e.g. zeros.

[0054] In an example, the optimal polar code permutation vector is of size N and the polar code construction rule is based on size N/2 polar code permutation vector. A size N permutation vector may be generated based on the following techniques described in FIG. 6. FIG. 6 is a flow diagram of a method for generating a representation of a polar code permutation vector using a smaller size polar code permutation vector and a bit sequence in accordance with some embodiments.

[0055] At 602, during initialization, the optimal permutation vector of size N is designated as "Opt" (ultimately, Opt will be represented by a polar code permutation vector of size N/2, Approx_Perm, and a bit sequence, BitSequence). The first smaller permutation vector of size N/2 is designated as Set1. A second polar code permutation vector is designated as Set2 and is generated by adding the size of the smaller permutation vector (i.e., N/2) to the first smaller permutation vector Set1. The initialization, therefore, may be represented as follows:

[0056] Set1 = Permutation_N/2

[0057] Set2 = Permutation_N/2 + N/2

[0058] Opt = Permutation_N

[0059] IDX = [0:1:N-1]

[0060] Approx_Perm = []

[0061] BitSequence = []

[0062] Count1 = Count2 = 0

[0063] The Permutation_N/2 indicates the permutation vector for size N/2, and it contains information of ordering of bit channel at the information bit position where information bits are loaded in the order of permutation and according to coding rate, and remaining bits are filled with predetermined values (frozen), e.g. zeros. The Approx_Perm is the polar code construction (or polar code permutation vector) for size N polar code obtained using the N/2 polar code permutation vector and BitSequence is the bit index which indicates which of the two smaller permutations supplies each position in the larger permuatation. Put another way, Approx_Perm is the smaller polar code permutation vector (of size N/2) which can be used with the BitSequence to represent the optimal (size N) polar code permutation vector (i.e., Opt).

[0064] At 604, an iteration may be performed for values of K from 0 to (N-1), with K being increased by 1 at every iteration. At 606, it is determined whether Count1 $\geq$ N/2. If it is, then processing continues at 612-614 by performing the following functions: at 612, BitSequence = [BitSequence 1] (i.e., 1 is added to BitSequence); at 614, Approx_Perm = [Approx_Perm Set2(Count2)] (i.e., Set2(Count2) is added to Approx_Perm); and at 616, Count2 is increased by 1.

[0065] At 608, if the condition at 606 is not satisfied, it is determined whether Count2 $\geq$ N/2. If it is, then processing continues at 618-622 by performing the following functions: at 618, BitSequence = [BitSequence 0] (i.e., 0 is added to BitSequence); at 620, Approx_Perm = [Approx_Perm Set1(Count1)] (i.e., Set1(Count1) is added to Approx_Perm); and at 622, Count1 is increased by 1.

[0066] At 610, if the condition at 608 is not satisfied, it may be determined whether (IDX(Opt==Set1(Count1)) > IDX(Opt==Set2(Count2))), which is equivalent to determining that the number Set1(Count1) occurs in Opt after the number Set2(Count2). If Set1(Count1) occurs in Opt after the number Set2(Count2), then processing resumes at 612. If Set1(Count1) does not occur in Opt after the number Set2(Count2), then processing resumes at 618. The following pseudo code may represent the flow diagram in FIG. 6:

```
For k = 0:N-1
    if (Count1 ≥ N/2)
        BitSequence = [BitSequence 1]
        Approx_Perm = [Approx_Perm Set2(Count2)]
        Count2 += 1
    elseif (Count2 ≥ N/2)
        BitSequence = [BitSequence 0]
        Approx_Perm = [Approx_Perm Set1(Count1)]
        Count1 += 1
    else
        if (IDX(Opt==Set1(Count1)) > IDX(Opt==Set2(Count2)))
            BitSequence = [BitSequence 1]
            Approx_Perm = [Approx_Perm Set2(Count2)]
            Count2 += 1
        else
            BitSequence = [BitSequence 0]
            Approx_Perm = [Approx_Perm Set1(Count1)]
            Count1 += 1
        end
    end
```

[0067] Recursive Construction

[0068] In case of recursive construction, i.e. starting from a certain size M, and creating permutations of size 2·M, 4·M, 8·M, etc, the Approx_Perm may replace the new size of Permutation_N/2 for a next size.

[0069] As an example, take M = 64, N = 2·M =128 and N/2 = 64. After initialization, there is no Approx_Perm, and Set1, Set2 and Opt indicate

Set1 = Permutation_N/2, Set2 = Permutation_N/2+N/2 and Opt = Permutation_N as follows:

[0070] Set1 = [63 62 61 59 55 47 60 31 58 57 54 53 46 51 45 43 30 29 39 27 …];

[0071] Set2 = [63 62 61 59 55 47 60 31 58 57 …] + 64 = [127 126 125 123 119 111 124 95 122 121 118 117 110 115 109 107 94 93 103 91 …]; and

[0072] Opt = [127 126 125 123 119 111 124 95 122 121 118 117 63 110 115 109 107 94 93 103 91 62 …].

[0073] Using the techniques disclosed in FIG. 6, the following may be generated:

[0074] Approx_Perm = [127 126 125 123 119 111 124 95 122 121 118 117 63 110 115 109 107 94 93 103 91 62 …] and BitSequence = [1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 1 0 …].

[0075] Now for next size, i.e. 4·M = 256 and N = 256 in this case, the Approx_Perm may replace Permutation_N/2 = Permutation_128, and processing flow in FIG. 6 may be repeated to obtain Approx_Perm for size N = 256.

[0076] Run-Length Representation

[0077] The generated short codeword permutation vector with length N/2 may be used with BitSequence to construct size N permutation vector. In an example, the BitSequence can be represented by binary run-length code as follows:

[0078] BitSequence = [1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 1 0 …] may be represented as [12A1A8A…] or [12, 1, 8, …], where 'A' or ',' represents the switching point of 1 or 0, and the number in front of that symbol is length of the run of 1s or 0s.

[0079] Using the run-length notation, the permutation for size N may be described as follows;

$$\text{BitSequence\_RL} = [12, 1, 8, \ldots] = [i_{2,0}, i_{1,0}, i_{2,1}, i_{1,0}, \ldots, i_{2,K-1}, i_{1,K-1}]$$

$$\text{Approx\_Perm} = [\text{Set2}(1{:}\,i_{2,0})\ \text{Set1}(1{:}i_{1,0})\ \text{Set2}(i_{2,0}+1{:}\textstyle\sum_{k=0}^{1} i_{2,k})\ \text{Set1}(i_{1,0}+1{:}\textstyle\sum_{k=0}^{1} i_{1,k})\ \ldots\ \text{Set2}(\textstyle\sum_{k=0}^{K-2} i_{2,k}+1{:}\textstyle\sum_{k=0}^{K-1} i_{2,k})\ \ \text{Set1}(\textstyle\sum_{k=0}^{K-2} i_{1,k}+1{:}\textstyle\sum_{k=0}^{K-1} i_{1,k})]$$

$$\text{And N} = \textstyle\sum_{k=0}^{K-1} i_{1,k} + \textstyle\sum_{k=0}^{K-1} i_{2,k}.$$

[0080] Rule for Non-power of 2

[0081] In case of construction for $N \neq 2^n$, legacy shortening techniques may be used. In that instance, the shortened index may be excluded from the Set1/Set2, and therefore, also from Approx_Perm and BitSequence. The shortened index may be predetermined, e.g. last S bits, where S is the number of bits to be shortened.

[0082] Examples of generating size 128, 256, 512, 1024, 2048, 4096, 8192 codeword (i.e., polar code permutation vector) from a size 64 permutation vector (i.e., permutation vector with 64 values) are provided in Listing B.

[0083] FIG. 7 is a flow diagram illustrating example functionalities for generating a polar code permutation vector, in accordance with an example embodiment. Referring to FIG. 7, the example method 700 may start at 702, when a plurality of input vectors may be generated by adding zeros to a set of input bits. For example, the input vectors 112 may be generated by zero-padding the input bits 110 (FIG. 1). At 704, a polar code permutation vector may be generated based on a plurality of estimates of channel reliability of a transmission channel. The plurality of estimates may be determined using a pre-defined range of signal-to-noise ratios (SNRs) of the transmission channel (e.g., 302 at FIG. 3). At 706, the permutation vector may be applied to the plurality of input vectors to obtain a plurality of output permuted vectors. For example, the permutation vector 104 may be applied to the input vectors 112 to obtain a plurality of output permuted vectors 114. The plurality of output permuted vectors may be polar coded using a generator matrix, to generate an encoded information block for transmission to an evolved Node-B (eNB) via the transmission channel. For example, the permuted vectors 114 may be polar coded using the generator matrix 106. The permutation vector (e.g., 104) may indicate positions of the input bits within the output vectors associated with a block error rate (BLER) below a threshold level.

[0084] FIG. 8 illustrates a block diagram of a communication device such as an eNB or a UE, in accordance with some embodiments. In alternative embodiments, the communication device 800 may operate as a standalone device or may be connected (e.g., networked) to other communication devices. In a networked deployment, the communication device 800 may operate in the capacity of a server communication device, a client communication device, or both in server-client network environments. In an example, the communication device 800 may act as a peer communication device in peer-to-peer (P2P) (or other distributed) network environment. The communication device 800 may be a UE, eNB, PC, a tablet PC, a STB, a PDA, a mobile telephone, a smart phone, a web appliance, a network router, switch or bridge, or any communication device capable of executing instructions (sequential or otherwise) that specify actions to be taken by that communication device. Further, while only a single communication device is illustrated, the term "communication device" shall also be taken to include any collection of communication devices that individually or jointly execute a set (or multiple sets) of instructions to perform any one or more of the methodologies discussed herein, such as cloud computing, software as a service (SaaS), other computer cluster configurations.

[0085] Examples, as described herein, may include, or may operate on, logic or a number of components, modules, or mechanisms. Modules are tangible entities (e.g., hardware) capable of performing specified operations and may be configured or arranged in a certain manner. In an example, circuits may be arranged (e.g., internally or with respect to external entities such as other circuits) in a specified manner as a module. In an example, the whole or part of one or more computer systems (e.g., a standalone, client or server computer system) or one or more hardware processors may be configured by firmware or software (e.g., instructions, an application portion, or an application) as a module that operates to perform specified operations. In an example, the software may reside on a communication device readable medium. In an example, the software, when executed by the underlying hardware of the module, causes the hardware to perform the specified operations.

[0086] Accordingly, the term "module" is understood to encompass a tangible entity, be that an entity that is physically constructed, specifically configured (e.g., hardwired), or temporarily (e.g., transitorily) configured (e.g., programmed) to operate in a specified manner or to perform part or all of any operation described herein. Considering examples in which modules are temporarily configured, each of the modules need not be instantiated at any one moment in time. For example, where the modules comprise a general-purpose hardware processor configured using software, the general-purpose hardware processor may be configured as respective different modules at different times. Software may accordingly configure a hardware processor, for example, to constitute a particular module at one instance of time and to constitute a different module at a different instance of time.

[0087] Communication device (e.g., UE) 800 may include a hardware processor 802 (e.g., a central processing unit (CPU), a graphics processing unit (GPU), a hardware processor core, or any combination thereof), a main memory 804 and a static memory 806, some or all of which may communicate with each other via an interlink (e.g., bus) 808. The communication device 800 may further include a display unit 810, an alphanumeric input device 812 (e.g., a keyboard), and a user interface (UI) navigation device 814 (e.g., a mouse). In an example, the display unit 810, input device 812 and UI navigation device 814 may be a touch screen display. The communication device 800 may additionally include a storage device (e.g., drive unit) 816, a signal generation device 818 (e.g., a speaker), a network interface device 820, and one or more sensors 821, such as a global positioning system (GPS) sensor, compass, accelerometer, or other sensor. The communication device 800 may include an output controller 828, such as a serial (e.g., universal serial bus (USB), parallel, or other wired or wireless (e.g., infrared (IR), near field communication (NFC), etc.) connection to communicate or control one or more peripheral devices (e.g., a printer, card reader, etc.).

[0088] The storage device 816 may include a communication device readable medium 822 on which is stored one or more sets of data structures or instructions 824 (e.g., software) embodying or utilized by any one or more of the techniques or functions described herein. The instructions 824 may also reside, completely or at least partially, within the main memory 804, within static memory 806, or within the hardware processor 802 during execution thereof by the communication device 800. In an example, one or any combination of the hardware processor 802, the main memory 804, the static memory 806, or the storage device 816 may constitute communication device readable media.

[0089] While the communication device readable medium 822 is illustrated as a single medium, the term "communication device readable medium" may include a single medium or multiple media (e.g., a centralized or distributed database, and/or associated caches and servers) configured to store the one or more instructions 824.

[0090] The term "communication device readable medium" may include any medium that is capable of storing, encoding, or carrying instructions for execution by the communication device 800 and that cause the communication device 800 to perform any one or more of the techniques of the present disclosure, or that is capable of storing, encoding or carrying data structures used by or associated with such instructions. Non-limiting communication device readable medium examples may include solid-state memories, and optical and magnetic media. Specific examples of communication device readable media may include: non-volatile memory, such as semiconductor memory devices (e.g., Electrically Programmable Read-Only Memory (EPROM), Electrically Erasable Programmable Read-Only Memory (EEPROM)) and flash memory devices; magnetic disks, such as internal hard disks and removable disks; magneto-optical disks; Random Access Memory (RAM); and CD-ROM and DVD-ROM disks. In some examples, communication device readable media may include non-transitory communication device readable media. In some examples, communication device readable media may include communication device readable media that is not a transitory propagating signal.

[0091] The instructions 824 may further be transmitted or received over a communications network 826 using a transmission medium via the network interface device 820 utilizing any one of a number of transfer protocols (e.g., frame relay, internet protocol (IP), transmission control protocol (TCP), user datagram protocol (UDP), hypertext transfer protocol (HTTP), etc.). Example communication networks may include a local area network (LAN), a wide area network (WAN), a packet data network (e.g., the Internet), mobile telephone networks (e.g., cellular networks), Plain Old

Telephone (POTS) networks, and wireless data networks (e.g., Institute of Electrical and Electronics Engineers (IEEE) 802.11 family of standards known as Wi-Fi®, IEEE 802.16 family of standards known as WiMax®), IEEE 802.15.4 family of standards, a Long Term Evolution (LTE) family of standards, a Universal Mobile Telecommunications System (UMTS) family of standards, peer-to-peer (P2P) networks, among others. In an example, the network interface device 820 may include one or more physical jacks (e.g., Ethernet, coaxial, or phone jacks) or one or more antennas to connect to the communications network 826. In an example, the network interface device 820 may include a plurality of antennas to wirelessly communicate using at least one of single-input multiple-output (SIMO), MIMO, or multiple-input single-output (MISO) techniques. In some examples, the network interface device 820 may wirelessly communicate using Multiple User MIMO techniques. The term "transmission medium" shall be taken to include any intangible medium that is capable of storing, encoding or carrying instructions for execution by the communication device 800, and includes digital or analog communications signals or other intangible medium to facilitate communication of such software.

[0092] Even though certain techniques are described herein and are associated with a user equipment (UE) or Evolved Node-B (eNB), the disclosure is not limited in this regard and other devices may be used as well. Additionally, functionalities described herein as being performed by the UE may be performed by the eNB, and vice versa (i.e., the polar code construction, representation and encoding techniques described herein are interchangeable between devices).

[0093] Additional notes and examples:

[0094] Example 1 is an apparatus of a user equipment (UE), the apparatus comprising: memory; and processing circuitry coupled to the memory, the processing circuitry configured to: generate input vectors by adding zeros to a set of input bits; generate a polar code permutation vector based on estimates of channel reliability of a transmission channel, the estimates determined using a pre-defined range of signal-to-noise ratios (SNRs) of the transmission channel; apply the polar code permutation vector to the input vectors to obtain output permuted vectors; and polar code the output permuted vectors using a generator matrix, to generate an encoded information block for transmission to an evolved Node-B (eNB) via the transmission channel, wherein the polar code permutation vector indicates positions of the input bits within the output permuted vectors associated with a block error rate (BLER) below a threshold level.

[0095] In Example 2, the subject matter of Example 1 optionally includes wherein to generate the polar code permutation vector, the processing circuitry is further configured to: initialize the polar code permutation vector as an empty vector.

[0096] In Example 3, the subject matter of Example 2 optionally includes wherein to generate the polar code permutation vector, the processing circuitry is further configured to: iterate between a minimum SNR and a maximum SNR at a pre-determined SNR increment value, to generate the estimates of channel reliability, wherein each estimate of channel reliability is associated with one or more construction codes indicating output bit positions with the BLER below the threshold level.

[0097] In Example 4, the subject matter of Example 3 optionally includes wherein to generate the polar code permutation vector, the processing circuitry is further configured to: for SNR values between the minimum SNR and the maximum SNR, iterate with increments at the pre-determined SNR increment value: for a particular one of the input vectors, select a corresponding channel reliability estimate of the estimates of channel reliability; and determine channel rates at which the one or more construction codes associated with the channel reliability estimate satisfy the BLER being below the threshold level.

[0098] In Example 5, the subject matter of Example 4 optionally includes wherein to generate the polar code permutation vector, the processing circuitry is further configured to, during the iteration: select a construction code from the one or more construction codes, associated with a highest channel rate among the determined channel rates; and append new bit positions associated with the selected construction code to the polar code permutation vector.

[0099] In Example 6, the subject matter of Example 5 optionally includes wherein to generate the polar code permutation vector, the processing circuitry is further configured to, during the iteration: determine for the selected construction code and the highest channel rate, whether the new bit positions are a superset of a previous polar code permutation vector generated during a previous iteration; and append the new bit positions to the polar code permutation vector upon determining that the new bit positions are a superset of the previous polar code permutation vector.

[00100] In Example 7, the subject matter of Example 6 optionally includes wherein to generate the polar code permutation vector, the processing circuitry is further configured to, subsequent to the iteration: determine whether a number of bit positions within the polar code permutation vector matches a number of inputs to the generator matrix; and upon determining one or more bit positions are missing, add the missing bit positions to the polar code permutation vector.

[00101] In Example 8, the subject matter of any one or more of Examples 1–7 optionally include wherein the generator matrix is of a type

$$G_N = \begin{bmatrix} 1 & 0 \\ 1 & 1 \end{bmatrix}^{\otimes log_2 N}$$

, where operation "$\otimes$" denotes a Kronecker power and N denotes a size of the output permuted vectors.

[00102] In Example 9, the subject matter of any one or more of Examples 1–8 optionally include wherein a number of the input vectors matches a number of bit positions within the polar code permutation vector.

[00103] In Example 10, the subject matter of any one or more of Examples 1–9 optionally include wherein the processing circuitry is further configured to: generate a second polar code permutation vector based on the estimates of channel reliability of a transmission channel, wherein the second polar code permutation vector is smaller than the polar code permutation vector.

[00104] In Example 11, the subject matter of Example 10 optionally includes wherein the second polar code permutation vector is half the size of the polar code permutation vector.

[00105] In Example 12, the subject matter of any one or more of Examples 10–11 optionally include wherein the processing circuitry is further configured to: generate a third polar code permutation vector using the second polar code permutation vector and a size of the second polar code permutation vector; generate a bit sequence of size equal to the size of the polar code permutation vector, wherein a bit at a bit position in the bit sequence indicates whether a value at the bit position within the polar code permutation vector is the same as a value at the bit position within the polar code permutation vector or a value at the bit position within the second polar code permutation vector.

[00106] In Example 13, the subject matter of Example 12 optionally includes wherein the processing circuitry is further configured to: encode the third polar code permutation vector and the bit sequence as a representation of the polar code permutation vector, for transmission to the eNB.

[00107] In Example 14, the subject matter of any one or more of Examples 1–13 optionally include a transceiver coupled to an antenna, the transceiver configured to transmit the encoded information block to the eNB.

[00108] Example 15 is an apparatus of an evolved Node B (eNB) configured to communicate with a user equipment (UE), the apparatus comprising: memory; and processing circuitry, the processing circuitry configured to: acquire a bit sequence and a first polar code permutation vector from the memory; generate using the bit sequence and the first polar code permutation vector, a second polar code permutation vector, the second polar code permutation vector having a number of bit positions that is a multiple of a number of bit positions within the first polar code permutation vector; apply the second polar code permutation vector to input vectors to obtain output permuted vectors; and polar code the output permuted vectors using a generator matrix, to generate an encoded information block for transmission to the UE via a transmission channel.

[00109] In Example 16, the subject matter of Example 15 optionally includes wherein the processing circuitry is further configured to: generate a third polar code permutation vector using the first polar code permutation vector and the number of bit positions within the first polar code permutation vector.

[00110] In Example 17, the subject matter of Example 16 optionally includes wherein the processing circuitry is further configured to: add the number of bit positions within the first polar code permutation vector to each vector value within the first polar code permutation vector to generate the third polar code permutation vector.

[00111] In Example 18, the subject matter of any one or more of Examples 16–17 optionally include wherein: the bit sequence comprises a plurality of bits at a corresponding plurality of bit positions; and a bit at a bit position of the plurality of bit positions indicates whether a value at the bit position within the second polar code permutation vector is determined based on a value at the bit position within the first polar code permutation vector or a value at the bit position within the third polar code permutation vector.

[00112] Example 19 is a computer-readable storage medium that stores instructions for execution by one or more processors of a user equipment (UE), the one or more processors to configure the UE to: generate input vectors by adding zeros to a set of input bits; iterate between a minimum SNR and a maximum SNR at a pre-determined SNR increment value, to generate estimates of channel reliability of a transmission channel; generate a polar code permutation vector based on estimates of channel reliability of the transmission channel; apply the polar code permutation vector to the input vectors to obtain output permuted vectors; and polar code the output permuted vectors using a generator matrix, to generate an encoded information block for transmission to an evolved Node-B (eNB) via the transmission channel, wherein each estimate of channel reliability is associated with one or more construction codes indicating output bit positions with the BLER below the threshold level, and wherein the polar code permutation vector indicates positions of the input bits within the output vectors associated with a block error rate (BLER) below a threshold level.

[00113] In Example 20, the subject matter of Example 19 optionally includes wherein to generate the polar code permutation vector, the one or more processors further configure the UE to: initialize the polar code permutation vector as an empty vector.

[00114] In Example 21, the subject matter of Example 20 optionally includes wherein to generate the permutation vector, the one or more processors further configure the UE to: select a construction code from the one or more construction codes, associated with a highest channel rate among the determined plurality of channel rates; and append new bit positions associated with the selected construction code to the permutation vector.

[00115] In Example 22, the subject matter of Example 21 optionally includes wherein to generate the permutation vector, the one or more processors further configure the UE to: determine for the selected construction code and the highest channel rate, whether the new bit positions are a superset of a previous polar code permutation vector generated during a previous iteration; and append the new bit positions to the polar code permutation vector upon determining that the new bit positions are a superset of the previous permutation vector.

[00116] In Example 23, the subject matter of Example 22 optionally includes wherein to generate the permutation vector, the one or more processors further configure the UE to: determine whether a number of bit positions within the polar code permutation vector matches a number of inputs to the generator matrix; and upon determining the number of bit positions within the polar code permutation vector does not match a number of inputs to the generator matrix and one or more bit positions are missing, add the missing bit positions to the polar code permutation vector.

[00117] In Example 24, the subject matter of any one or more of Examples 19–23 optionally include wherein the one or more processors further configure the UE to: generate a second polar code permutation vector based on the plurality estimates of channel reliability of a transmission channel, wherein the second polar code permutation vector comprises a number of values that is smaller than a number of values within the polar code permutation vector.

[00118] In Example 25, the subject matter of Example 24 optionally includes wherein the one or more processors further configure the UE to: generate a third polar code permutation vector using the second polar code permutation vector and the number of values within the second polar code permutation vector.

[00119] In Example 26, the subject matter of Example 25 optionally includes wherein the one or more processors further configure the UE to: generate a bit sequence comprising a plurality of bits, wherein a number of the plurality of bits within the bit sequence is equal to the number of values within the polar code permutation vector, wherein a bit at a bit position in the bit sequence indicates whether a value at the bit position within the polar code permutation vector is the same as a value at the bit position within the polar code permutation vector or a value at the bit position within the second polar code permutation vector.

[00120] In Example 27, the subject matter of Example 26 optionally includes wherein the one or more processors further configure the UE to: generate a binary run-length code based on the bit sequence; and encode the second polar code permutation vector and the binary run-length code as a representation of the polar code permutation vector, for transmission to the eNB.

[00121] Example 28 is an apparatus of a user equipment (UE), the apparatus comprising: means for generating input vectors by adding zeros to a set of input bits; means for generating a polar code permutation vector based on estimates of channel reliability of a transmission channel, the estimates determined using a pre-defined range of signal-to-noise ratios (SNRs) of the transmission channel; means for applying the polar code permutation vector to the input vectors to obtain output permuted vectors; and means for polar coding the output permuted vectors using a generator matrix, to generate an encoded information block for transmission to an evolved Node-B (eNB) via the transmission channel, wherein the polar code permutation vector indicates positions of the input bits within the output permuted vectors associated with a block error rate (BLER) below a threshold level.

[00122] In Example 29, the subject matter of Example 28 optionally includes means for initializing the polar code permutation vector as an empty vector.

[00123] In Example 30, the subject matter of Example 29 optionally includes means for iterating between a minimum SNR and a maximum SNR at a pre-determined SNR increment value, to generate the estimates of channel reliability, wherein each estimate of channel reliability is associated with one or more construction codes indicating output bit positions with the BLER below the threshold level.

[00124] In Example 31, the subject matter of Example 30 optionally includes for SNR values between the minimum SNR and the maximum SNR, with increments at the pre-determined SNR increment value: means for selecting a corresponding channel reliability estimate of the estimates of channel reliability, for a particular one of the input vectors; and means for determining channel rates at which the one or more construction codes associated with the channel reliability estimate satisfy the BLER being below the threshold level.

[00125] In Example 32, the subject matter of Example 31 optionally includes means for selecting a construction code from the one or more construction codes, associated with a highest channel rate among the determined channel rates; and means for appending new bit positions associated with the selected construction code to the polar code permutation vector.

[00126] In Example 33, the subject matter of Example 32 optionally includes means for determining for the selected construction code and the highest channel rate, whether the new bit positions are a superset of a previous polar code permutation vector generated during a previous iteration; and means for appending the new bit positions to the polar code permutation vector upon determining that the new bit positions are a superset of the previous polar code permutation vector.The above detailed description includes references to the accompanying drawings, which form a part of the detailed description. The drawings show, by way of illustration, specific embodiments that may be practiced. These embodiments are also referred to herein as "examples." Such examples may include elements in addition to those shown or described. However, also contemplated are examples that include the elements shown or described. Moreover, also contemplated are examples using any combination or permutation of those elements shown or described (or one or more aspects thereof), either with respect to a particular example (or one or more aspects thereof), or with respect to other examples (or one or more aspects thereof) shown or described herein.

[00127] Publications, patents, and patent documents referred to in this document are incorporated by reference herein in their entirety, as though individually incorporated by reference. In the event of inconsistent usages between this document and those documents so incorporated by reference, the usage in the incorporated reference(s) are supplementary to that of this document; for irreconcilable inconsistencies, the usage in this document controls.

[00128] The above description is intended to be illustrative, and not restrictive. For example, the above-described examples (or one or more aspects thereof) may be used in combination with others. Other embodiments may be used, such as by one of ordinary skill in the art upon reviewing the above description. The Abstract is to allow the reader to quickly ascertain the nature of the technical disclosure. It is submitted with the understanding that it will not be used to interpret or limit the scope or meaning of the claims. Also, in the above Detailed Description, various features may be grouped together to streamline the disclosure. However, the claims may not set forth every feature disclosed herein as embodiments may feature a subset of said features. Further, embodiments may include fewer features than those disclosed in a particular example. Thus, the following claims are hereby incorporated into the Detailed Description, with a claim standing on its own as a separate embodiment. The scope of the embodiments disclosed herein is to be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.

Listing A: Permutations for lengths 64, 128, 256, 512, 1024, 2048, 4096, 8192.

Notation:

$P_N(i) = j$ means P_N maps the i^{th} bit to the j^{th} position

P_{64}=[64 63 62 60 56 48 61 32 59 58 55 54 47 52 46 44 31 30 40 28 57 53 24 51 16 45 50 43 42 29 39 27 38 26 23 36 22 15 20 14 12 49 41 8 37 25 21 35 34 19 13 11 18 7 10 6 4 33 17 9 5 3 2 1]

P_{128}=[128 127 126 124 120 112 125 96 123 122 119 118 64 111 116 110 108 95 94 104 92 63 121 117 62 88 115 60 109 114 80 107 56 106 93 103 91 102 48 90 100 87 61 86 32 59 79 84 58 78 55 54 76 52 47 46 72 113 105 44 101 31 89 99 30 85 98 40 83 28 57 77 24 82 53 75 51 16 74 50 45 71 43 70 42 29 39 68 27 38 26 97 23 36 22 15 20 14 81 73 12 49 69 41 8 25 37 67 21 35 66 13 19 34 11 18 7 10 6 4 65 33 17 9 5 3 2 1]

P_{256}=[256 255 254 252 248 240 253 224 251 250 247 192 246 239 244 238 236 128 223 222 232 220 191 216 190 249 245 188 243 208 242 237 127 184 235 126 234 231 221 124 176 230 219 218 120 228 215 160 214 189 112 187 207 212 186 206 183 182 125 204 96 180 175 200 174 123 122 119 172 64 118 159 158 168 116 241 111 156 110 233 229 227 108 226 217 213 152 211 205 210 95 185 203 181 94 179 202 104 199 173 178 92 121 144 198 171 63 117 170 157 62 88 60 196 80 167 115 166 56 155 114 109 154 107 164 151 106 150 103 93 48 91 102 143 148 90 142 100 32 87 86 140 61 59 79 84 225 58 209 201 55 78 197 136 177 54 76 52 47 46 195 72 169 165 194 113 153 163 105 149 162 101 147 89 141 44 31 30 40 28 99 146 24 98 85 139 83 138 57 77 82 53 135 75 16 51 134 74 45 50 71 43 42 70 29 132 39 27 38 68 26 23 36 22 193 161 15 145 14 20 12 8 97 81 49 137 73 133 41 69 25 37 131 67 21 35 130 13 19 66 34 11 18 7 129 65 33 17 10 9 6 5 4 3 2 1]

P_{512}=[512 511 510 508 504 496 480 509 507 506 503 448 502 500 495 494 492 384 479 478 488 505 476 447 256 472 446 501 499 444 464 440 498 383 493 382 491 490 380 487 432 477 486 475 474 376 484 471 255 445 470 254 416 443 463 368 468 252 442 462 439 438 381 248 460 352 436 431

379 430 456 378 240 497 375 428 320 374 415 489 485 414 224 424 372 367 483 253 412 366 251 482 364 250 473 469 408 467 192 351 247 350 246 360 466 461 459 348 244 441 400 239 458 437 435 455 429 434 377 238 454 427 319 373 426 413 344 318 236 128 223 452 423 371 222 316 411 422 365 232 370 336 410 363 220 312 420 216 191 407 190 362 406 304 359 188 349 358 249 404 399 347 245 208 243 346 398 184 356 242 288 343 127 237 396 342 126 235 317 234 315 340 335 176 124 392 231 314 334 230 221 311 219 218 120 481 310 465 332 228 160 215 308 214 457 303 453 451 112 302 328 189 450 433 425 187 421 212 207 419 186 409 300 206 418 405 183 369 287 361 403 96 182 204 286 296 180 284 175 200 125 174 123 402 122 357 397 355 395 354 172 119 394 345 64 280 341 241 339 233 391 313 333 229 338 390 309 217 331 227 159 118 307 213 330 226 388 301 158 111 116 168 110 272 156 108 327 306 211 326 95 152 299 210 205 94 298 185 203 324 181 104 285 295 202 179 283 92 144 294 199 63 178 173 282 198 88 62 171 292 279 121 117 170 278 196 157 60 80 167 115 166 155 114 271 109 276 56 154 449 107 417 270 401 393 164 48 106 151 150 103 268 102 93 91 148 143 90 32 100 142 87 389 264 387 353 337 329 325 386 305 225 61 323 297 209 86 201 293 59 322 140 197 177 58 84 79 55 78 54 136 76 291 281 47 195 52 169 277 290 165 194 46 275 113 153 163 72 105 269 274 149 162 31 101 44 267 147 89 99 30 141 266 85 146 263 98 40 139 57 28 83 24 77 53 82 138 262 75 135 51 16 45 74 50 134 260 71 43 385 321 29 132 70 42 289 193 39 27 161 273 68 38 26 97 145 23 265 36 22 15 81 137 20 14 49 73 261 133 12 41 8 69 25 37 259 21 13 131 67 35 19 11 258 130 66 34 7 18 10 6 4 257 129 65 33 17 9 5 3 2 1]

P_{1024}=[1024 1023 1022 1020 1016 1008 992 960 1021 1019 1018 1015 1014 1012 1007 1006 896 1004 991 990 1000 988 984 768 959 958 956 1017 976 1013 1011 1010 952 1005 895 1003 894 1002 999 989 512 892 944 987 998 986 983 996 767 888 957 982 766 955 928 975 954 880 764 980 974 951 760 950 972 864 948 893 943 511 891 942 968 510 890 752 1009 940 832 508 887 886 927 926 736 936 884 504 879 1001 997 995 765 878 924 985 876 763 496 762 920 994 704 863 759 981 862 979 758 872 978 973 971 860 756 953 912 751 970 949 947 967 941 509 946 889 750 966 939 480 507 831 885 856 830 748 938 640 506 735 964 925 935 503 883 828 734 923 934

877 502 744 882 448 848 922 875 732 761 495 824 500 932 919 703 494 874 728 918 702 871 861 757 816 492 870 859 911 384 916 755 479 700 858 720 478 910 488 868 696 800 754 855 639 476 908 749 854 638 747 829 746 827 688 636 852 472 447 847 904 256 446 826 743 846 742 733 823 731 444 822 993 730 632 977 969 505 844 464 740 672 727 820 501 726 440 499 815 965 498 963 840 814 383 624 701 962 493 945 937 382 699 491 933 724 719 931 698 490 812 921 930 718 917 695 487 380 881 799 477 432 694 716 798 486 608 808 475 915 376 474 914 873 692 869 909 637 484 687 796 867 471 907 635 857 255 866 686 712 416 853 906 470 634 445 851 753 745 903 825 845 850 741 254 443 631 902 821 843 729 463 739 684 792 671 468 442 630 368 819 576 252 725 842 439 900 738 462 497 670 680 628 623 438 784 460 248 622 839 668 818 352 813 381 723 838 431 436 811 379 717 620 722 697 430 489 810 607 456 378 715 693 664 836 797 807 485 240 375 606 691 428 616 320 374 415 604 656 714 414 806 795 424 224 372 367 711 794 690 483 575 685 253 710 804 366 412 473 791 600 482 683 251 574 469 633 790 467 682 250 364 572 408 708 351 247 679 592 192 629 466 669 246 350 788 783 461 627 678 667 360 459 441 626 782 621 437 568 666 458 435 239 961 244 619 929 348 913 400 676 238 663 780 455 618 319 434 662 344 454 560 429 236 318 615 427 128 605 905 614 901 426 223 603 660 655 377 452 776 899 865 849 373 841 423 316 602 222 413 654 898 837 371 612 232 817 599 422 411 835 336 809 365 370 737 573 721 805 834 410 598 220 544 652 713 312 216 420 191 190 363 407 596 304 571 362 406 591 570 648 590 188 359 567 358 349 404 399 249 208 347 566 245 803 588 243 398 346 793 802 709 789 356 242 707 184 343 237 787 689 564 127 559 681 706 288 235 677 396 786 342 781 317 126 558 675 584 234 665 481 779 465 315 625 457 674 661 231 221 335 617 778 453 340 314 659 556 124 433 613 775 392 219 176 543 230 451 425 334 311 653 601 658 611 421 774 120 218 310 542 228 332 160 552 215 214 308 540 303 112 189 302 328 187 450 651 212 610 207 186 597 650 419 772 595 206 536 409 300 418 183 647 405 594 369 589 287 361 403 569 646 182 357 587 96 204 286 296 180 125 175 528 123 402 284 565 397 174 200 355 586 122 563 395 644 345 354 583 341 562 119 394 557 339 582 172 241 64 555 391 118 233 280 159 333 338 229 158 116 111 168 390 554 110 331 580 313 156 227 551 309 272 541 330 217 226 307 388 213 550 539 327 108 306 211 301 538 95 326 299 205 210 897 152 185 833 535 548 801 785 94

203 181 298 777 705 534 285 104 673 324 773 295 179 657 202 649 283 92 771 199 173 527 609 294 178 144 63 88 62 198 60 532 282 171 121 292 170 117 279 526 80 196 115 167 157 278 56 114 109 155 166 524 645 107 770 271 593 449 154 417 276 643 401 585 393 106 151 164 581 270 642 561 353 93 389 103 337 553 520 579 48 150 329 387 91 549 102 225 268 578 305 325 143 386 209 537 90 547 148 297 323 61 201 87 100 533 142 546 293 177 264 322 32 197 59 86 281 531 169 291 525 140 195 79 58 277 530 113 84 55 290 165 523 194 78 153 275 136 105 54 47 76 52 46 163 149 269 101 72 31 162 274 44 89 522 147 99 267 519 30 141 85 769 146 98 266 641 57 40 518 263 139 28 83 577 385 77 53 138 262 82 321 545 516 135 24 51 75 16 45 50 74 43 71 134 29 193 42 260 289 70 27 39 132 161 529 26 38 273 97 68 23 145 521 36 81 22 265 15 137 49 14 20 12 73 8 41 517 25 261 133 69 37 21 515 259 131 67 13 35 19 514 258 130 66 11 34 513 257 129 65 33 18 17 10 9 7 6 5 4 3 2 1]

P_{2048}=[2048 2047 2046 2044 2040 2032 2016 1984 1920 2045 2043 2042 2039 2038 2036 2031 2030 2028 1792 2015 2014 2024 2012 2008 1983 1982 2000 1980 1976 1968 1536 1919 1918 1916 1912 1952 2041 2037 2035 2034 1904 2029 2027 2026 1791 1790 2023 2022 2013 2011 2010 2020 1788 2007 2006 1024 1888 1784 2004 1999 1998 1981 1979 1978 1996 1975 1974 1776 1972 1992 1967 1966 1535 1534 1856 1917 1964 1915 1532 1914 1911 1910 1760 1951 1950 1960 1528 1908 1948 1903 1902 1900 1789 1787 2033 2025 1520 2021 1786 1944 2019 2018 1728 1023 1887 1783 2009 2005 1022 1886 2003 1782 1896 2002 1997 1995 1020 1884 1780 1977 1936 1775 1994 1973 1971 1504 1774 1991 1970 1965 1533 1855 1990 1963 1531 1016 1880 1854 1772 1913 1962 1664 1530 1909 1759 1988 1949 1959 1527 1907 1852 1758 1947 1958 1901 1526 1768 1906 1472 1008 1872 1946 1899 1756 1785 1519 1943 1848 1524 1752 1956 1518 1727 992 1726 1840 1942 1898 1516 1408 1724 1895 1940 1894 1744 1503 1885 1935 1883 1021 1502 1934 1019 1882 1512 1781 1018 1892 1720 1779 1824 1778 1879 1663 1015 1500 1932 1773 960 1878 1662 1771 1014 1853 1770 1851 1471 1712 1660 1496 1876 1280 1012 1470 1928 1871 1850 1007 1870 1767 1006 1766 1656 1468 1847 1757 1846 1755 1868 1488 1004 1754 896 1764 1696 1751 1844 1529 1525 991 2017 1750 1464 2001 1993 1523 1839 1989 990 1987 1522 1864 1838

1407 1648 1000 1725 1986 1517 1969 1961 1723 1406 1957 1515 1748 1743 1955 1722 1514 988 1836 1945 1954 1742 1941 1719 1511 1905 1823 1404 1501 1939 1456 1897 1893 1718 959 1510 1499 1938 1933 1822 1740 1891 1881 1017 1661 984 1832 958 1931 1632 1498 768 1890 1877 1013 1711 1508 1716 1659 1495 1400 1777 1930 1820 1875 1279 1011 1469 1769 1927 1710 956 1440 1736 976 1494 1658 1278 1392 1816 1708 1655 1600 952 1492 1467 1654 1010 1276 1487 895 1695 1874 1466 1005 1926 1869 1486 1003 894 1694 1867 1463 1849 1765 1704 1002 1652 1845 1647 1866 1763 1462 1924 1843 1808 1753 999 1484 1272 1646 989 1762 1863 1692 892 512 1749 944 1842 1837 1376 1405 998 987 1747 1862 1455 1835 1460 1403 1741 1521 986 1644 1746 1721 1454 1834 1513 1631 1480 1402 996 983 1688 1739 888 1717 1860 1821 767 1831 1264 928 1630 1452 1640 1344 1399 982 766 1398 1628 1439 880 1680 957 1738 1830 1438 955 980 1819 764 975 1715 1448 1396 1248 954 1735 1391 1509 1818 1714 974 1599 1507 1709 1828 1734 1277 1390 951 1436 1815 1624 1497 1707 1506 1598 1275 1493 950 1657 1814 1706 1491 972 760 1274 1732 1653 1388 893 864 1703 1693 1485 1490 1985 1271 1596 1651 1465 1953 1375 1807 943 1937 1432 948 891 1812 1691 511 1483 1702 1929 1009 1461 1645 1650 1270 1616 1889 1374 1925 1001 1806 942 1216 968 1384 890 752 510 1592 1690 1482 887 1643 1459 1268 1263 1372 1700 940 1687 1424 1479 1804 1642 1458 1453 508 886 927 997 832 1262 1686 1873 1478 1923 1343 1639 1629 1451 995 1865 985 1401 926 1861 1922 765 879 1584 1368 736 936 1260 884 1342 1152 504 924 878 1340 1684 1638 1247 1800 1450 1246 1679 1476 1256 1627 1360 1678 1626 876 763 1636 1447 994 762 1568 920 1446 1397 1244 1623 1437 496 981 1395 1336 1435 1676 979 863 759 1622 1394 704 1434 978 862 758 1389 1597 973 1444 872 1859 1387 1431 1595 971 1841 1215 953 1833 1620 1858 1615 1386 949 1829 1240 970 1594 1430 1214 756 1672 860 1761 751 947 1827 1745 912 1383 1614 1737 1817 1273 967 1373 1591 1733 1328 1826 946 941 1813 750 1269 1713 1382 480 509 1731 1371 1423 966 1428 831 1705 1590 1811 939 1267 1212 889 1612 1730 1701 507 1370 1805 1422 856 1261 1810 1505 830 1232 748 640 1380 938 1588 735 1266 506 1583 1367 964 1208 1151 828 1312 935 885 1420 734 1582 503 1259 1366 925 1608 1341 883 1699 744 1150 1803 934 1689 848 923 1258 502 448 1339 1698 1489 882 1685 877 1649 1481 1802 1359 1255 1641 922

732 1245 1364 1580 1477 1683 1338 875 1799 824 1637 1567 1416 1457 1148 932 919 495 1200 1243 1475 1254 1358 1677 500 1335 1449 1682 1635 703 1625 494 1566 728 874 918 702 1334 1242 1576 1144 1356 871 1252 1798 816 861 761 1239 1675 492 1564 870 757 1474 911 859 916 1634 1445 1327 1621 700 1332 384 1184 1238 1213 755 479 1674 1443 1796 858 1619 1433 910 1326 1211 1671 749 720 1352 1393 754 1429 868 1442 478 855 993 1613 1593 1618 1231 1385 977 1136 1236 488 747 1560 1210 1670 829 639 1427 969 696 800 908 1324 476 854 1230 638 1207 1311 746 827 1611 1206 1589 847 852 1381 447 743 1310 1228 1426 733 1421 1610 826 1587 636 904 1379 1668 1120 688 965 1552 1149 1320 1369 472 505 846 742 1419 446 1607 731 823 945 256 1581 1586 1199 963 1378 1365 1204 501 1147 937 1308 1418 1265 730 1606 1579 822 962 933 1363 499 1198 1257 444 632 1224 844 740 1146 464 727 672 1143 820 815 1196 726 1304 1415 498 1578 701 493 1362 1088 1142 1357 440 1604 1183 814 383 931 1414 840 1337 491 699 1575 1565 921 1253 1355 624 1333 719 930 917 724 881 1182 382 1251 1563 490 698 1574 1241 873 1135 1354 1331 1140 915 1192 1412 812 718 869 477 1921 487 1237 1250 1857 695 1825 1351 1562 799 1325 1809 1296 909 1330 1134 914 867 380 432 1180 694 486 798 716 475 608 808 1572 1132 1559 1350 474 1235 637 1323 376 692 687 907 484 1119 857 1176 1558 796 1234 471 635 866 1229 853 1322 255 1209 906 686 712 1348 1118 1227 1801 634 851 445 470 1205 1319 1309 416 753 903 1551 1797 1729 1128 1697 254 745 1556 1681 845 631 1226 1203 850 443 825 1307 1795 1673 1318 741 902 1550 684 368 576 792 252 1116 1168 468 630 463 671 442 462 670 680 628 248 1112 439 1087 352 784 438 460 623 1086 668 622 1223 1306 1202 1316 1222 843 842 1548 900 436 1197 1303 1084 1195 821 739 620 819 1302 431 1194 839 738 381 1220 818 456 430 379 729 1104 664 838 240 725 813 1145 1191 378 607 1141 723 811 1300 1181 1544 1139 1295 1190 722 606 810 1179 375 1669 1080 717 428 1138 1794 836 1294 616 1133 1667 715 1178 1633 697 807 320 1617 374 1609 797 497 415 693 1131 1188 489 1666 1605 714 1175 1473 806 1441 604 485 795 691 1425 1585 1603 1130 656 1417 414 1292 1577 711 483 1413 1174 367 690 685 473 794 372 1573 1377 1602 424 1127 253 1117 224 1361 1411 575 482 469 710 1353 804 791 1571 1072 683 1561 633 366 251 1115 1126 1349 412 1167 1410 467 1329 961 1557 600 1172 574 929 629 1570 682 790 1288

1249 913 1347 1321 250 1114 461 441 708 669 1233 1166 1555 466 905 679 627 1317 364 1111 247 865 1124 1225 1346 1549 783 437 351 1085 459 901 849 667 572 621 1554 1305 788 408 678 1201 626 1315 1221 1110 246 841 1547 1164 899 435 1056 782 350 458 1083 192 592 1301 666 619 1193 1219 817 1314 429 737 455 837 360 663 1103 898 239 1546 377 676 434 1082 568 348 244 400 238 1108 319 780 618 344 454 662 236 1160 318 560 1102 128 427 615 1079 605 223 426 614 1078 603 452 655 660 373 776 316 222 1100 423 413 602 371 654 1299 232 1543 1218 1189 411 422 612 1071 336 599 1076 835 365 1293 370 1298 809 1187 1177 220 1542 573 721 410 805 1137 1070 834 1291 544 363 598 652 713 1096 312 1173 1129 1186 407 420 793 571 803 249 191 709 1290 689 362 1125 1540 216 190 406 596 591 1068 570 359 304 349 648 1055 590 245 188 567 358 347 399 1171 404 243 802 789 1287 1054 707 566 1165 208 346 1170 681 1123 398 237 242 787 1113 1064 588 1286 677 706 356 343 1163 481 127 1109 781 1122 235 465 786 559 184 317 1052 665 675 564 457 625 1162 1107 342 779 396 288 126 1284 234 661 617 453 1081 1159 674 315 433 558 1101 221 584 231 1106 778 613 1793 425 335 659 1665 451 1077 1601 775 1158 314 1099 340 1048 219 1569 653 124 601 230 421 611 392 556 311 176 1553 543 1409 450 658 334 1075 1345 369 774 1098 409 218 597 651 1545 1069 1313 1156 419 610 1095 310 542 215 1074 228 189 361 1297 1217 405 120 897 1541 332 552 214 303 160 308 1040 187 650 540 595 418 772 1067 302 569 207 1094 647 112 589 328 357 186 212 403 594 565 183 1066 397 345 1053 206 646 587 355 241 402 1063 1092 300 1289 1185 287 536 833 125 1539 563 341 182 395 801 1051 1169 586 233 354 1285 644 557 1062 204 286 583 123 96 180 175 296 122 174 200 284 119 528 64 394 172 118 339 562 159 391 229 333 582 338 313 555 280 1050 111 227 390 158 217 116 309 331 1047 1060 554 213 168 541 226 110 580 307 551 330 1046 388 785 211 156 301 327 1161 1538 539 1283 306 1121 705 185 777 550 272 205 673 1105 1039 1157 108 210 95 299 326 538 657 773 1282 1044 181 1097 203 449 535 1155 609 649 548 1038 152 298 94 285 771 417 1073 179 1093 324 295 593 202 1154 104 645 534 121 401 173 199 1065 770 283 178 1036 1091 585 92 353 294 527 643 63 393 117 171 561 144 198 1061 532 282 1090 337 581 1049 279 526 62 88 115 170 157 292 196 167 60 109 114 389 278 642 155 1032 553 166 80 225 107 329 1059 579 524 271 387 154 56 305 276 1045 549 209 93 151 106 325 1058 578 164

386 270 537 103 297 520 1043 547 201 150 91 323 1037 48 1537 102 177 268 533 143 90 61 87 32 100 148 59 142 86 197 293 58 322 79 169 55 281 546 264 140 84 195 291 113 78 531 165 1042 54 277 194 290 153 105 525 1281 47 1035 136 530 163 76 275 52 769 1153 101 149 523 269 46 1034 162 89 641 274 1031 31 72 1089 99 147 522 267 44 385 141 577 30 85 57 98 40 146 28 83 519 266 139 53 77 263 321 1030 82 24 1057 518 138 51 75 545 193 135 45 262 289 1028 50 16 74 43 29 71 42 134 27 39 70 161 26 516 97 38 260 23 1041 132 529 273 68 145 22 15 36 81 1033 20 14 49 521 265 137 73 12 41 1029 517 8 261 133 25 69 1027 1026 1025 515 514 513 259 258 257 131 130 129 67 66 65 37 35 34 33 21 19 18 17 13 11 10 9 7 6 5 4 3 2 1]

P_{4096}=[4096 4095 4094 4092 4088 4080 4064 4032 3968 3840 4090 4091 4093 4086 4087 4084 4078 4079 4076 4072 4062 4063 4060 4056 4030 4031 3584 4048 4028 4024 4016 3967 3966 3964 4000 3960 3952 3839 3838 3936 3072 3836 3832 3824 4089 4085 4083 4082 4077 4075 4074 3904 4071 4070 4061 4059 4058 4068 4055 4054 3808 3583 3582 4052 4029 4027 4026 4047 4046 3580 4023 4022 4044 3576 4020 4015 4014 4040 4012 3965 3963 3962 2048 3776 3568 3999 3998 4008 3959 3958 3996 3956 3951 3950 3992 3948 3552 3935 3934 3944 3071 3070 3837 3835 3834 3984 3932 3068 3831 3830 3712 3828 3928 3064 3823 3822 3820 3903 3902 3520 4081 4073 4069 4067 4066 3900 3056 3920 3816 3807 3806 4057 4053 4051 4050 3896 3804 3581 3579 3578 4045 4043 4042 4025 4021 4019 4039 4018 4038 3575 3574 3800 4036 4013 4011 3572 4010 3040 3888 2047 2046 3775 3774 3567 4007 3566 4006 3456 2044 3564 3772 3997 3995 3994 4004 3961 3957 3955 3954 3792 3991 3990 3949 3947 3946 2040 3551 3560 3550 3768 3988 3943 3942 3872 3983 3982 3008 3548 3933 3931 3940 3930 3069 3067 3066 3711 3710 3980 3833 3927 3829 3063 3827 3926 3062 3826 2032 3760 3708 3544 3821 3924 3819 3328 3060 3818 3519 3518 3976 3901 3899 3919 3898 3055 3918 3815 3054 3814 3704 3516 3895 3805 3803 3894 3916 3802 3052 3536 3812 2944 2016 3744 3799 3577 3892 3573 4065 4049 3039 3798 4041 3571 3512 3887 4037 4035 3570 3038 3912 3886 3455 3696 2045 3048 4034 3773 3454 3796 3036 3771 3565 2043 3884 3791 3563 3770 2042 3790 3562 3504 3452 4017 4009 4005 1984 4003 3767 2039 3871 3559 4002 3766 2038 3870 3788 3993 3558 3007 3680 3549 3989 3032 3880 3987 3547 2816 3006 3953 3945

3986 3546 3448 3941 3764 3981 2036 3709 3759 3556 3868 3939 2031 3979 3543 3707 3065 3929 3938 3758 3327 3004 3784 3061 2030 3925 3978 3488 3706 3542 3024 3326 3440 3864 3648 3756 3000 2028 1920 3324 3540 3703 3702 3517 3515 3059 3535 3743 2943 3514 3058 3534 3742 2942 2015 3923 3752 3975 2014 3700 3922 3974 3053 2024 3511 3051 3856 3320 3695 3917 3510 3050 3532 3915 2992 3740 2940 3424 3694 2560 3914 2012 3825 3817 3897 3972 3813 3047 3893 3811 3891 3046 3508 3911 3037 3810 3890 3503 3692 3801 3453 3035 3797 3910 3885 3451 3528 3502 3795 3034 1983 3883 3736 2936 3679 3044 3450 3312 2008 3794 3882 3789 3031 1792 1982 3908 2815 3678 3769 3447 3787 2041 3879 3569 2976 3500 3869 3030 3765 3392 3688 2928 1980 2814 3676 3728 3296 2000 3446 2812 3487 3496 3486 3444 3028 1976 3672 3484 3439 3023 3438 3005 3022 3003 3002 3878 3647 3646 3786 2808 2912 1919 3867 2999 1918 3020 3436 3866 2998 3876 3783 3763 2037 2035 3644 3782 3762 2034 3480 3325 3323 3322 1968 3863 3664 3264 1916 3862 2996 1536 3757 3561 3755 3557 2029 3555 2027 3754 3780 2026 3554 3423 3422 3319 2991 3432 3016 2800 3318 2990 3860 3640 3751 3545 3541 2559 2023 2941 3539 3750 2939 2558 2022 3538 3855 3705 2938 3701 3420 3741 3854 1912 3699 3472 3739 2013 3316 3533 2988 2011 3698 3738 3531 2880 2010 3311 2935 3748 3530 2556 2020 3693 3310 3513 2934 3691 3509 3735 3852 1952 2975 2007 3507 1791 3690 3527 3734 3506 3391 2006 2974 3632 3416 3526 1790 3501 2984 3687 3390 3057 3308 2932 2784 3049 1981 4033 3499 2927 4001 3985 3045 3677 3977 1904 3200 3686 2552 1979 3043 3973 3732 3727 3675 3498 3848 2813 2004 2926 3295 2972 1788 3388 3294 1999 3524 3304 1978 3408 3726 1998 3674 2924 2811 3684 3495 3042 2810 3616 1975 3449 2968 3494 1024 3445 3292 3671 3033 3485 2544 3029 1784 3443 1974 3384 3483 3724 3971 1996 2911 3027 2807 3670 1888 3442 3937 2752 3482 3921 3970 3026 3913 2910 2806 3437 3909 3645 3492 3021 2920 3907 3435 3479 3643 1972 3019 1917 3288 3263 2908 3668 2960 1967 3262 2804 1992 1966 3376 1776 3720 1535 3478 3434 3663 3642 2799 1915 1534 3662 2528 3018 2798 1914 3001 3431 3260 2997 3639 3906 2995 1964 3015 3430 3476 3889 3881 3638 2879 1911 3421 2904 2994 3877 1856 3471 1532 3660 3280 3014 3419 3875 3321 2878 1910 2796 2989 2557 3317 3470 3809 3793 1951 3418 3874 3785 2987 3865 2688 3315 2555 3781 3861 3428 3636 3779 1950 2986 3314 2783 2033 3631 3859 3415 2554 3256 3012 2025

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3593 2822 759 2498 6211 1256 971 3361 2440 4296 3143 4434 5201 2278 876 1813 1434 2359 2172 1387 1505 1622 5253 863 1273 4650 1676 1360 1705 2417 2645 2699 2382 4637 4873 4215 3122 4769 4313 2457 4405 1826 1731 2224 1595 4486 2658 5378 6181 3345 1568 5135 1431 4676 4323 920 496 1244 1336 704 758 862 1444 872 2590 2266 1215 3088 2358 1615 1386 970 1620 2168 4268 2600 2276 947 2380 1594 1430 4376 2263 751 1240 4214 756 4160 860 1214 1672 967 1383 4255 1373 912 1614 941 1591 946 1269 4427 4647 2237 2588 2351 3142 509 2467 3115 2262 750 2356 2698 2208 6152 1328 1371 5140 1811 966 2820 1382 1423 2643 4254 480 939 831 889 4635 1267 4207 1428 1701 4403 2235 1730 1590 2453 4426 2695 4646 4212 4309 2466 507 2409 4322 2350 1805 5134 3114 4484 2617 1212 2637 4264 2376 1489 1810 1612 3101 1370 1261 2642 885 4423 2255 4397 1689 1422 1699 3140 938 1649 1266 4634 3111 830 856 2451 4402 2160 2405 4206 2260 6210 2234 4307 1481 748 2694 2613 5193 4368 3589 925 964 1803 1367 506 1380 1583 5251 2635 1232 735 4252 2584 6169 935 4869 4631 640 4753 1641 1685 2445 4281 3099 883 1259 3265 1341 1588 4644 6179 4395 2393 2231 4422 4301 2254 1698 3337 1457 5169 1151 1477 5132 503 2403 2348 5189 2450 3233 3110 3587 2335 4306 2611 4745 2945 923 1802 4705 5250 877 6165 2289 1366 4867 1420 2634 1582 2881 1637 734 1208 3217 934 1683 4545 828 4277 3333 4630 2692 4204 2443 5161 2173 882 1449 1608 2389 3098 6178 1258 4191 1339 1799 4394 2605 1312 4299 2230 1475 2849 4381 2631 5187 1245 4689 2402 1150 502 4513 4741 3586 1625 1677 744 2610 4420 3169 2334 3095 2281 1255 3209 4391 993 6163 448 4866 922 2252 761 875 4248 1359 2833 1635 3108 848 3331 4623 5157 1682 2753 4275 1445 2442 4497 2387 6157 2171 4681 5128 1338 1798 2576 1474 4190 4298 2603 1364 2223 919 5186 2344 2144 2361 1580 2630 1567 3153 4379 4739 932 1243 732 495 1393 4628 5145 977 2439 1621 3205 1675 4269 2721 1416 2825 1433 2277 824 1148 500 1200 2228 703 1254 1358 1335 874 494 2332 918 4200 728 1566 2222 702 871 1242 2248 861 2170 1334 757 1576 1252 3094 1356 1239 1144 2167 4390 4188 1634 859 816 2381 4295 870 911 492 2386 755 2602 4622 916 4274 1443 4240 1213 479 384 1674 1564 2589 2438 2220 1327 4378 700 1796 1619 2628 4217 2357 2328 1238 2599 3087 4159 2379 2166 1332 2207 749 858 2265 4294 2275 1429 4267 910 1184 1671 2112 1385 754 1593 1442 4375 3092 1613 1211

969 4388 2587 478 855 4213 868 6162 720 1618 1326 2355 5155 2261 2378 3330 1352 2598 4620 4657 3086 747 4158 829 1381 1427 4677 2206 1231 2274 4489 4184 2436 2159 4266 1589 945 1670 965 3145 639 6155 4449 4738 488 4253 4374 1611 2349 3203 1236 5141 2375 1210 2164 1136 4292 2705 2821 1421 4211 2586 1369 4263 4649 854 908 1560 2216 2354 1921 5154 696 2259 505 4433 3121 4485 4675 1379 937 1857 746 1207 1426 3141 827 800 1230 963 2233 1587 2583 476 733 2158 1265 4205 2657 6154 2697 1324 638 2320 1311 3202 4367 2596 5139 4251 1610 2253 2347 1825 2819 3084 2497 2374 4156 743 2204 4645 1668 4425 4210 1419 6151 1365 3113 847 1581 4262 447 4616 1149 4483 4372 2258 501 5133 1607 4674 933 1378 2641 3139 2465 1809 1206 962 826 4321 4633 2693 852 1257 1586 1729 2229 2582 4401 731 4203 881 5138 2818 4176 4366 1310 4250 2346 2333 2251 921 904 1228 4421 4643 742 823 2143 3109 2156 1418 6150 1363 636 472 688 446 256 846 1120 1320 1552 1199 1204 730 1147 822 2200 499 444 1308 740 632 844 727 1606 1198 1579 2372 2142 1146 1224 493 4152 2343 498 1415 931 701 464 2575 1357 815 1337 4247 4260 2152 2227 1143 2250 3080 726 1253 1362 820 2580 1578 2331 491 4202 917 672 383 873 1565 2342 930 1414 2247 699 2221 4189 1604 1333 1575 4364 1355 1241 1196 2574 4199 440 2140 2226 4246 814 1304 1251 1183 1142 2169 840 3138 4482 2633 2330 869 719 915 5131 490 2192 2691 1088 1801 2449 382 1563 4629 3097 477 1697 2219 2246 724 1331 2111 698 4187 4393 4305 624 1237 3107 2327 4642 1574 1354 909 4419 487 2609 857 4198 1250 2340 4239 1412 2629 2165 4144 2441 1182 1681 2401 1797 1135 867 695 1325 914 2690 5130 1351 718 2572 3093 4297 4244 4627 753 812 1562 4389 799 1140 475 1330 2218 2601 5127 4360 4186 6148 1235 2110 3106 2205 2385 1192 4418 1633 2326 907 1673 2136 853 2437 486 4621 380 2627 7169 1209 637 1473 1559 6657 2244 1795 4238 2163 4273 4377 6401 2215 866 4183 1572 1134 432 1229 694 4157 1323 1296 4293 6273 4196 3091 1350 745 4626 4387 1617 1441 1180 2597 798 2157 2377 474 6209 5126 1234 2319 1669 716 3085 2203 2435 906 2626 851 4619 5633 1794 4265 1205 1558 2273 2568 2162 825 635 5377 4373 2585 2108 471 2214 2324 687 445 6177 608 808 376 484 692 255 1132 796 1119 470 686 416 634 254 712 1176 1322 903 1227 2128 443 1309 1348 845 631 1118 1319 850 741 4182 1551 2318 463 4128 2202 2155 4236 1203 902 368 1226 468 821 4155 1128 1556 442 684

1307 843 729 2104 792 252 739 630 671 2199 1318 2212 1223 1197 576 439 1550 3090 462 4175 2154 1202 2595 1609 4291 2353 819 1116 1145 2141 4386 2373 725 4154 1667 1425 842 4180 1306 2316 2434 3083 738 2151 900 1168 497 2198 670 623 4618 2581 1195 1222 381 1585 813 4151 1087 839 4261 4371 1303 2257 2345 4232 1605 438 1417 5124 4174 1377 628 1316 2594 4290 1141 2371 4615 818 1666 4209 723 2139 680 1548 4365 489 248 3082 460 4249 697 2150 2191 1577 961 2249 2579 1361 622 1194 2096 784 717 379 811 4259 2341 3079 1181 1413 4370 5249 1603 838 4150 1086 352 1302 431 2196 1112 668 2370 1220 4201 1139 2573 4614 2312 5185 929 6161 722 1191 2138 2225 436 2329 485 4363 4172 4245 1573 693 1353 2190 2245 4865 2578 5153 1133 2135 4258 1411 2109 1295 1602 4143 2339 810 797 3585 378 3078 715 2148 1179 4737 473 1249 913 430 3329 1561 1544 6153 607 620 1138 4197 456 836 1329 2571 4148 1190 240 375 1084 664 428 606 807 374 1300 415 320 1104 483 691 616 714 795 1294 253 1178 1131 806 711 414 685 469 2134 367 482 2188 1080 2080 690 1175 604 224 1188 372 2107 633 794 251 424 656 1130 1571 2325 1349 467 2217 1117 4142 710 683 575 1410 2243 791 1292 2127 4362 366 2338 4168 4243 1127 804 441 4612 1174 905 1557 629 865 2106 461 412 1233 2132 1321 4359 250 2570 1570 4185 4237 1347 2213 2323 3076 466 2103 682 1115 2242 4195 2567 849 574 2184 669 247 2161 790 901 2126 4242 600 437 1167 1126 2317 1555 1225 708 627 2201 4140 5137 679 4127 1317 3201 4673 1072 459 4358 364 351 4181 1346 1172 1549 2211 4235 2322 3137 1288 841 621 1201 4194 1114 1305 2102 783 4641 6149 2566 2153 899 667 246 5129 1221 1554 4481 408 435 2817 1166 737 2315 192 626 3105 2197 1315 572 1111 678 788 1085 817 4126 458 2124 2689 1124 350 4179 2210 4234 4417 4153 4625 1547 429 4356 837 2095 377 1193 455 898 619 239 782 1301 6147 4136 2149 2625 666 3089 4231 5125 4173 592 360 721 1219 434 2564 2314 2100 1314 2195 244 1110 4385 809 1083 663 348 238 400 568 319 676 454 427 1164 1056 618 373 605 780 236 128 615 662 223 318 426 344 1103 413 2094 1082 452 835 371 1108 2120 603 423 1546 2311 1299 1189 614 655 222 2137 1079 1543 1218 2189 560 1160 713 365 4124 1137 1102 805 411 4178 1293 660 2147 1177 316 834 776 2194 370 602 422 4149 232 249 689 793 4230 2092 1298 1187 2079 2310 481 654 4171 2133 709 1542 1078 2187 599 1129 573 4617 363 803 2593 612 336 2146 410 1793 1291 220

3081 2433 1173 1100 1665 4147 191 681 465 5123 245 1186 407 789 6146 4289 4369 2078 4170 4120 1071 2369 420 2577 707 2131 2186 4228 2105 2308 312 4613 598 802 1601 349 1125 362 571 4141 652 1540 1290 3077 4167 1076 544 2088 2183 1171 2125 4257 359 4146 2337 1287 190 1113 457 677 5122 406 4361 243 787 625 1409 1569 2569 706 1165 591 1070 216 2130 4611 1096 2076 1123 2101 570 347 781 665 237 4139 433 4166 2241 3075 596 1170 2182 399 4241 2123 358 1345 2321 567 1286 648 786 242 675 453 1553 4112 4357 1109 304 590 188 2565 617 1163 404 1055 4610 1122 1068 346 4193 2099 4125 127 208 235 398 343 317 356 184 566 126 234 221 779 661 425 588 342 231 315 451 674 396 559 288 1054 613 564 1107 1162 219 778 1081 1284 124 2122 2072 335 659 421 2180 369 450 1064 230 1159 2093 775 314 601 4138 1101 2119 558 176 340 653 1313 409 2209 897 4164 584 3074 2098 1545 311 611 2313 1106 4135 218 392 1052 658 334 1077 419 4233 2563 189 1217 361 1158 774 4355 833 215 2091 2118 597 1099 120 1297 228 651 2193 543 4123 556 610 405 310 1541 2309 4134 2064 4177 418 2562 1075 4229 1185 332 2145 187 801 214 4354 2077 2090 1098 357 569 772 160 1156 303 1048 595 650 241 542 1289 4122 2116 1069 2185 403 1095 1539 2087 2307 647 308 345 705 589 207 1074 112 552 4119 4132 4169 186 397 4227 302 594 1169 212 355 183 125 328 206 233 402 540 182 565 341 287 123 96 646 300 395 587 354 204 1067 1094 785 175 229 2075 1285 563 1040 313 122 286 180 339 2086 2129 394 1538 673 586 217 536 644 1121 1066 2181 1053 119 557 2306 333 391 777 174 296 583 1092 1161 227 449 200 2074 1063 562 1283 4145 338 4118 64 309 284 2121 2071 2084 657 118 4165 4226 213 390 2179 159 1051 555 1105 582 331 773 6145 226 172 1062 528 1282 1157 609 417 2097 111 4111 307 5121 185 2070 4137 541 158 4116 116 554 1050 2178 280 211 330 388 2117 649 4163 580 771 301 1097 551 110 327 1047 168 1060 205 156 210 306 95 181 108 203 299 401 326 539 593 94 272 121 1155 550 179 353 152 645 770 1073 285 202 298 104 173 2063 538 1046 324 393 199 3073 2089 1154 295 63 178 92 1093 2068 4110 117 2115 585 4609 535 548 643 337 283 1039 4162 4133 171 2062 144 198 561 62 2561 294 1065 225 1044 389 534 1091 88 115 2114 642 2085 157 581 4121 282 4108 170 1038 4353 1537 109 196 60 527 279 114 167 107 80 155 56 292 166 329 93 209 106 387 154 305 103 278 151 48 553 164 532 91 325 201 386 579 271 102 61 177 526 150 276

1061 1090 297 90 323 87 32 549 2073 578 270 197 2060 143 100 2305 1049 1036 4131 59 148 2083 1281 524 169 537 1059 86 293 322 113 142 58 195 268 547 769 79 4117 281 55 4130 2069 4104 2082 2056 84 1045 1032 4225 1058 165 291 140 194 2177 520 78 533 105 54 546 1153 153 264 47 4115 277 641 290 2067 76 163 52 1043 136 46 101 531 4109 2061 385 149 1037 89 162 4114 72 2066 31 4161 275 525 1042 2113 44 99 1089 530 269 30 577 147 4107 274 85 2059 40 1035 98 57 141 523 28 321 146 267 4106 83 4129 4113 4105 4103 4102 4101 4100 4099 4098 4097 2081 2065 2058 2057 2055 2054 2053 2052 2051 2050 2049 1057 1041 1034 1033 1031 1030 1029 1028 1027 1026 1025 545 529 522 521 519 518 517 516 515 514 513 289 273 266 265 263 262 261 260 259 258 257 193 161 145 139 138 137 135 134 133 132 131 130 129 97 82 81 77 75 74 73 71 70 69 68 67 66 65 53 51 50 49 45 43 42 41 39 38 37 36 35 34 33 29 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1]

Listing B: **Examples of generating size (length) 128, 256, 512, 1024, 2048, 4096, 8192 codeword (i.e., polar code permutation vector) from a size 64 permutation vector (i.e., permutation vector with 64 values):**

Permutation_64 = [63 62 61 59 55 47 60 31 58 57 54 53 46 51 45 43 30 29 39 27 56 52 23 50 15 44 49 42 41 28 38 26 37 25 22 35 21 14 19 13 11 48 40 7 36 24 20 34 33 18 12 10 17 6 9 5 3 32 16 8 4 2 1 0]

BitSequence_128 = [1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 1 0 1 1 0 1 1 0 1 1 1 1 0 1 1 1 1 1 0 1 1 1 0 1 0 0 1 1 0 1 0 0 1 0 0 0 1 1 1 0 1 0 1 0 1 1 1 0 1 0 0 1 0 0 1 1 0 0 0 0 1 1 0 1 0 0 0 1 0 0 0 1 0 0 0 0 0 0 1 1 0 0 1 0 0 0 0 1 0 0 1 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0]

BitSequence_RL_128 = [12, 1, 8, 1, 2, 1, 2, 1, 4, 1, 5, 1, 3, 1, 1, 2, 2, 1, 1, 2, 1, 3, 3, 1, 1, 1, 1, 1, 3, 1, 1, 2, 1, 2, 2, 4, 2, 1, 1, 3, 1, 3, 1, 6, 2, 2, 1, 4, 1, 2, 1, 9, 1, 7]

BitSequence_256 = [1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 0 1 1 1 0 1 1 1 1 0 1 1 1 1 1 0 1 1 1 1 1 1 1 0 1 0 1 1 1 0 0 0 0 0 1 0 0 0 1 1 1 1 1 0 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 0 1 0 0 1 1 1 1 1 1 1 0 0 0 1 1 0 0 1 1 0 0 0 1 1 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 0 1 1 1 0 0 1 1 0 0 0 0 0 1 1 1 0 1 1 0 0 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 1 1 0 0 0 0 0 0 1 1 0 0 0 0 1 0 0 0 0 0 0 0 0 1 0 0 0 0 0 1 1 1 0 0 0 0 0 0 0 0 1 0 0 0 1 0 0 0 0 0 1 0 0 0 1 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0]

BitSequence_RL_256 = [17 , 1 , 14 , 1 , 2 , 1 , 3 , 1 , 4 , 1 , 5 , 1 , 7 , 1 , 1 , 1 , 3 , 5 , 1 , 3 , 5 , 1 , 8 , 1 , 6 , 1 , 1 , 2 , 7 , 3 , 2 , 2 , 2 , 3 , 2 , 2 , 1 , 17 , 7 , 1 , 3 , 2 , 2 , 5 , 3 , 1 , 2 , 2 , 6 , 9 , 2 , 6 , 2 , 4 , 1 , 8 , 1 , 5 , 3 , 8 , 1 , 3 , 1 , 5 , 1 , 3 , 1 , 7 , 1 , 11]

BitSequence_512 = [1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 0 1 1 1 1 1 0 1 1 1 1 1 0 1 1 1 1 1 1 1 0 1 1 1 1 1 1 0 0 1 1 1 1 1 1 0 1 0 1 1 1 1 1 1 1 1 1 0 0 0 1 1 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 1 1 0 0 0 1 1 1 0 1 0 1 1 1 1 1 1 1 0 1 0 1 1 1 0 1 1 1 0 0 0 0 0 0 1 1 1 0 0 0 0 0 0 1 1 1 0 1 1 1 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 0 0 1 1 1 1 0 0 0 0 1 1 1 1 1 1 1 1 1 0 1 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 1 1 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 1 0 0 0 0 0 0 0 0 1 1 1 0 0 0 0 0 0 0 1 1 1 0 0 0 1 1 1 0 0 0 0 0 0 0 1 1 1 1 0 0 1 0 0 1 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 1 1 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1

1 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 0 0 1 1 1 1 1 0 0 0 0 1 0 0 0 0 0 1 0 0 0 0 1 1 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 0 0 0 0 1 0 1 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 1 0 0 0 0 1 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0]

BitSequence_RL_512 = [24 , 1 , 23 , 1 , 2 , 1 , 5 , 1 , 5 , 1 , 7 , 1 , 6 , 2 , 6 , 1 , 1 , 1 , 9 , 3 , 2 , 2 , 13 , 1 , 9 , 3 , 3 , 1 , 1 , 1 , 7 , 1 , 1 , 1 , 3 , 1 , 3 , 6 , 3 , 6 , 3 , 1 , 3 , 8 , 9 , 2 , 4 , 4 , 9 , 1 , 1 , 5 , 10 , 9 , 4 , 1 , 18 , 3 , 1 , 8 , 3 , 7 , 3 , 3 , 3 , 7 , 4 , 2 , 1 , 2 , 1 , 4 , 1 , 19 , 1 , 2 , 2 , 9 , 14 , 1 , 2 , 2 , 1 , 20 , 3 , 2 , 5 , 4 , 1 , 5 , 1 , 4 , 2 , 9 , 1 , 22 , 5 , 4 , 1 , 1 , 1 , 9 , 1 , 8 , 1 , 8 , 1 , 4 , 1 , 8 , 1 , 12]

BitSequence_1024 = [1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 0 1 1 0 1 1 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 0 0 1 1 1 1 0 1 1 1 1 1 1 1 1 0 1 1 1 0 1 0 1 1 1 1 1 1 1 1 0 1 0 1 0 1 1 1 1 0 1 1 1 1 1 1 0 1 0 1 1 1 0 0 1 1 0 1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 1 1 1 1 1 1 0 0 0 0 0 0 1 1 1 1 0 0 0 1 1 1 1 1 1 1 1 1 1 0 0 0 1 1 1 1 0 1 1 1 1 1 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 1 1 1 1 1 1 1 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 1 1 1 0 0 0 0 1 1 0 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 0 0 1 1 1 1 1 1 0 1 1 1 1 0 0 1 1 1 1 1 1 1 0 0 0 1 1 1 1 0 0 1 1 1 1 1 0 0 0 0 0 0 0 0 1 1 1 0 1 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 0 0 1 1 1 1 1 0 0 1 1 1 0 1 0 0 0 0 0 0 0 0 1 1 1 0 1 0 1 0 0 0 0 0 0 0 0 1 1 1 1 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 1 1 1 0 1 1 1 0 0 0 0 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 0 0 0 0 0 0 1 1 1 1 1 0 0 1 1 1 0 1 1 1 1 1 1 1 1 1 0 0 0 1 0 0 0 0 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 1 1 0 0 0 0 0 0 1 1 1 1 1 1 0 0 0 0 0 0 0 1 1 1 0 0 0 0 0 0 0 0 0 1 1 1 1 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0 1 0 0 1 0 0 0 0 1 0 0 1 1 1 1 1 1 0 0 0 0 0 0 1 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 1 1 0 0 0 0 0 0 1 1 1 0 1 1 1 0 0 1 1 0 1 0 0 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 0 0 0 0 0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 1 1 1 1 0 0 0 0 0 0 0 0 0 0 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 1 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0]

BitSequence_RL_1024 = [40 , 1 , 28 , 1 , 2 , 1 , 2 , 1 , 4 , 1 , 12 , 1 , 27 , 1 , 6 , 2 , 4 , 1 , 8 , 1 , 3 , 1 , 1 , 1 , 8 , 1 , 1 , 1 , 1 , 1 , 4 , 1 , 6 , 1 , 1 , 1 , 3 , 2 , 2 , 1 , 11 , 1 , 19 , 2 , 6 , 6 , 4 , 3 , 10 , 3 , 4 , 1 , 5 , 8 , 13 , 3 , 7 , 4 , 20 , 4 , 3 , 4 , 2 , 1 , 9 , 6 , 12 , 2 , 6 , 1 , 4 , 2 , 7 , 3 , 4 , 2 , 5 , 8 , 3 , 1 , 1 , 12 , 7 , 2 , 5 , 2 , 3 , 1 , 1 , 8 , 3 , 1 , 1 , 1 , 1 , 8 , 5 , 3 , 1 , 12 , 16 , 5 , 3 , 1 , 3 , 4 , 1 , 1 , 15 , 17 , 7 , 1 , 7 , 6 , 5 , 2 , 3 , 1 , 9 , 3 , 1 , 4 , 5 , 11 , 1 , 24 , 9 , 12 , 2 , 6 , 6 , 7 , 3 , 9 , 4 , 2 , 1 , 38 , 16 , 8 , 1 , 2 , 1 , 4 , 1 , 2 , 6 , 6 , 1 , 7 , 1 , 12 , 2 , 6 , 3 , 1 , 3 , 2 , 2 , 1 , 1 , 2 , 4 , 19 , 6 , 5 , 2 , 13 , 2 , 34 , 1 , 8 , 4 , 10 , 3 , 24 , 1 , 10 , 1 , 9 , 1 , 9 , 1 , 5 , 1 , 7 , 1 , 15]

BitSequence_2048 = [1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 0 1 1 1 1 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 1 1 1 1 0 1 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 0 0 1 1 1 1 1 1 1 1 0 0 0 1 1 1 1 1 1 0 1 1 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 1 0 1 1 1 0 1 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 1 1 1 1 1 0 0 0 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 1 1 1 1 0 1 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 0 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 1 0 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 1 1 1 1 1 1 1 1 1 0 0 0 1 0 0 1 1 1 1 1 1 1 1 1 1 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 0 0 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 1 0 1 1 1 1 1 1 1 0 0 0 0 0 0 1 1 1 1 1 1 0 0 0 1 1 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 1 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 1 0 0 1 0 0 1 1 1 1 1 1 1 0 0 1 0 0 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 1 1 1 1 1 1 0 0 0 0 0 0 0 0 1 1 1 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 1 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 1 0 0 0 0 0 0 1 1 1 0 0 0 1 1 1 1 1 1 1 1 0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 1 1 1 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

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BitSequence_RL_2048 = [50 , 1 , 45 , 1 , 6 , 1 , 6 , 1 , 24 , 1 , 19 , 1 , 21 , 3 , 4 , 1 , 9 , 1 , 7 , 2 , 8 , 3 , 6 , 1 , 2 , 2 , 23 , 2 , 25 , 1 , 8 , 1 , 3 , 1 , 1 , 4 , 17 , 1 , 2 , 2 , 20 , 6 , 2 , 1 , 29 , 4 , 5 , 3 , 2 , 1 , 21 , 3 , 4 , 1 , 7 , 9 , 9 , 1 , 2 , 1 , 13 , 1 , 4 , 1 , 11 , 4 , 9 , 3 , 1 , 2 , 10 , 3 , 22 , 5 , 6 , 11 , 4 , 2 , 11 , 8 , 17 , 6 , 9 , 2 , 22 , 10 , 1 , 1 , 7 , 6 , 6 , 3 , 2 , 3 , 21 , 3 , 2 , 12 , 10 , 6 , 1 , 2 , 13 , 1 , 4 , 2 , 1 , 2 , 7 , 2 , 1 , 2 , 12 , 3 , 6 , 8 , 3 , 6 , 14 , 3 , 10 , 6 , 1 , 4 , 13 , 2 , 1 , 6 , 3 , 3 , 8 , 1 , 2 , 12 , 8 , 12 , 16 , 3 , 2 , 16 , 9 , 6 , 3 , 7 , 9 , 4 , 10 , 1 , 2 , 14 , 19 , 2 , 1 , 1 , 2 , 9 , 11 , 13 , 3 , 2 , 2 , 54 , 33 , 3 , 3 , 11 , 4 , 7 , 8 , 10 , 4 , 12 , 9 , 10 , 16 , 9 , 10 , 1 , 5 , 11 , 1 , 16 , 14 , 6 , 1 , 3 , 3 , 2 , 1 , 6 , 4 , 13 , 1 , 19 , 6 ,

6 , 8 , 6 , 9 , 27 , 2 , 2 , 4 , 2 , 2 , 12 , 2 , 23 , 1 , 10 , 15 , 4 , 6 , 9 , 1 , 21 , 13 ,
24 , 4 , 14 , 4 , 2 , 2 , 38 , 4 , 18 , 6 , 3 , 1 , 31 , 7 , 18 , 5 , 29 , 7 , 16 , 6 , 5 , 1 ,
3 , 1 , 2 , 1 , 51 , 3 , 27 , 4 , 21 , 1 , 11 , 3 , 24 , 1 , 14 , 1 , 10 , 1 , 8 , 3 , 32]

BitSequence_4096 = [1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 1 1 1 1 1 1 1 1 0 0 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 0 0 0 1 1 1 1 1 1 1 1 1 1 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 0 1 1 1 0 1
1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
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1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 0 0 0 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0
0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 1 1 1 1 1 1 1 0 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0
0 0 0 0 0 0 0 0 0 0 1 1 1 0 1 1 1 0 0 0 0 0 0 1 1 1 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1
1 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
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1 1 1 1 1 0 0 0 1 1 1 0 0 1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1
1 1 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 1 1 0 0 0 0 0 0 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 0
0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 1 1 1 0 0 1 1 1 1 1 1 1 1 1 1 0 0 0
0 0 0 1 1 1 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 1 1 1
1 1 1 1 1 1 1 1 1 1 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0 1 1 1

1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 1 1 1 1 1 0 0 0 0 0 0

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1 1 1 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0

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0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

```
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0
0 0 0 0 0 0 0 0 0 1 1 1 1 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 1 1 1 1 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 1 1 1 1 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1
1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
```

0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0]

BitSequence_RL_8192 = [81 , 1 , 121 , 2 , 19 , 1 , 11 , 2 , 133 , 7 , 66 , 5 , 73 , 1 , 1 , 2 , 19 , 1 , 26 , 1 , 60 , 2 , 16 , 3 , 23 , 3 , 17 , 6 , 8 , 1 , 29 , 4 , 4 , 3 , 46 , 2 , 15 , 2 , 8 , 1 , 84 , 12 , 13 , 11 , 52 , 3 , 42 , 1 , 101 , 18 , 11 , 2 , 20 , 14 , 6 , 1 , 44 , 9 , 5 , 4 , 46 , 1 , 5 , 5 , 4 , 3 , 18 , 3 , 74 , 1 , 16 , 1 , 73 , 35 , 64 , 23 , 2 , 2 , 6 , 1 , 14 , 1 , 81 , 18 , 9 , 1 , 13 , 7 , 71 , 3 , 10 , 24 , 6 , 1 , 24 , 3 , 28 , 9 , 29 , 19 , 9 , 3 , 16 , 1 , 15 , 12 , 14 , 1 , 15 , 24 , 51 , 1 , 53 , 1 , 14 , 27 , 20 , 4 , 14 , 4 , 24 , 45 , 6 , 2 , 20 , 13 , 10 , 2 , 2 , 12 , 31 , 15 , 29 , 2 , 28 , 4 , 1 , 13 , 29 , 14 , 33 , 10 , 2 , 1 , 17 , 6 , 13 , 3 , 8 , 13 , 15 , 1 , 4 , 9 , 7 , 1 , 2 , 1 , 2 , 1 , 18 , 1 , 14 , 15 , 31 , 1 , 12 , 10 , 1 , 29 , 34 , 5 , 42 , 16 , 64 , 25 , 10 , 30 , 7 , 6 , 17 , 2 , 5 , 1 , 26 , 4 , 7 , 26 , 66 , 3 , 1 , 62 , 11 , 12 , 24 , 10 , 2 , 17 , 31 , 20 , 8 , 10 , 16 , 5 , 13 , 9 , 4 , 9 , 34 , 6 , 3 , 31 , 22 , 7 , 3 , 17 , 9 , 9 , 7 , 1 , 16 , 35 , 36 , 9 , 17 , 17 , 5 , 2 , 10 , 21 , 29 , 4 , 15 , 2 , 2 , 20 , 14 , 4 , 1 , 2 , 3 , 31 , 10 , 4 , 27 , 19 , 2 , 6 , 19 , 31 , 2 , 9 , 39 , 5 , 3 , 5 , 8 , 9 , 8 , 14 , 20 , 94 , 64 , 31 , 35 , 12 , 24 , 89 , 80 , 60 , 22 , 25 , 12 , 26 , 27 , 11 , 2 , 27 , 17 , 2 , 2 , 9 , 1 , 10 , 10 , 3 , 2 , 1 , 8 , 49 , 18 , 19 , 5 , 2 , 2 , 10 , 8 , 23 , 5 , 7 , 4 , 52 , 11 , 8 , 25 , 24 , 9 , 1 , 6 , 12 , 29 , 37 , 21 , 29 , 1 , 30 , 23 , 38 , 16 , 32 , 12 , 10 , 2 , 24 , 16 , 5 , 3 , 6 , 23 , 20 , 1 , 11 , 4 , 1 , 2 , 31 , 8 , 35 , 10 , 15 , 25 , 82 , 3 , 18 , 5 , 40 , 10 , 17 , 12 , 15 , 4 , 43 , 47 , 31 , 3 , 9 , 8 , 38 , 8 , 31 , 7 , 5 , 9 , 322 , 81 , 3 , 1 , 13 , 24 , 28 , 3 , 42 , 3 , 20 , 1 , 49 , 20 , 11 , 4 , 12 , 1 , 13 , 4 , 1 , 1 , 27 , 6 , 84 , 17 , 1 , 10 , 29 , 1 , 29 , 4 , 7 , 11 , 6 , 4 , 129 , 14 , 30 , 6 , 102 , 13 , 44 , 12 , 185 , 16 , 40 , 1 , 17 , 7 , 56 , 5 , 47 , 17 , 67 , 1 , 8 , 1 , 53 , 3 , 33 , 14 , 148]

CLAIMS

What is claimed is:

1. An apparatus of a user equipment (UE), the apparatus comprising:

memory; and

processing circuitry coupled to the memory, the processing circuitry configured to:

generate input vectors by adding zeros to a set of input bits;

generate a polar code permutation vector based on estimates of channel reliability of a transmission channel, the estimates determined using a pre-defined range of signal-to-noise ratios (SNRs) of the transmission channel;

apply the polar code permutation vector to the input vectors to obtain output permuted vectors; and

polar code the output permuted vectors using a generator matrix, to generate an encoded information block for transmission to an evolved Node-B (eNB) via the transmission channel,

wherein the polar code permutation vector indicates positions of the input bits within the output permuted vectors associated with a block error rate (BLER) below a threshold level.

2. The apparatus of claim 1, wherein to generate the polar code permutation vector, the processing circuitry is further configured to:

initialize the polar code permutation vector as an empty vector.

3. The apparatus of claim 2, wherein to generate the polar code permutation vector, the processing circuitry is further configured to:

iterate between a minimum SNR and a maximum SNR at a predetermined SNR increment value, to generate the estimates of channel reliability,

wherein each estimate of channel reliability is associated with one or more construction codes indicating output bit positions with the BLER below the threshold level.

4. The apparatus of claim 3, wherein to generate the polar code permutation vector, the processing circuitry is further configured to:

for SNR values between the minimum SNR and the maximum SNR, iterate with increments at the pre-determined SNR increment value:

for a particular one of the input vectors, select a corresponding channel reliability estimate of the estimates of channel reliability; and

determine channel rates at which the one or more construction codes associated with the channel reliability estimate satisfy the BLER being below the threshold level.

5. The apparatus of claim 4, wherein to generate the polar code permutation vector, the processing circuitry is further configured to, during the iteration:

select a construction code from the one or more construction codes, associated with a highest channel rate among the determined channel rates; and

append new bit positions associated with the selected construction code to the polar code permutation vector.

6. The apparatus of claim 5, wherein to generate the polar code permutation vector, the processing circuitry is further configured to, during the iteration:

determine for the selected construction code and the highest channel rate, whether the new bit positions are a superset of a previous polar code permutation vector generated during a previous iteration; and

append the new bit positions to the polar code permutation vector upon determining that the new bit positions are a superset of the previous polar code permutation vector.

7. The apparatus of claim 6, wherein to generate the polar code permutation vector, the processing circuitry is further configured to, subsequent to the iteration:

determine whether a number of bit positions within the polar code permutation vector matches a number of inputs to the generator matrix; and

upon determining one or more bit positions are missing, add the missing bit positions to the polar code permutation vector.

8. The apparatus of any of claims 1-7, wherein the generator matrix is of a type $G_N = \begin{bmatrix} 1 & 0 \\ 1 & 1 \end{bmatrix}^{\otimes log_2 N}$, where operation "$\otimes$" denotes a Kronecker power and N denotes a size of the output permuted vectors.

9. The apparatus of any of claims 1-7, wherein a number of the input vectors matches a number of bit positions within the polar code permutation vector.

10. The apparatus of any of claims 1-7, wherein the processing circuitry is further configured to:

generate a second polar code permutation vector based on the estimates of channel reliability of a transmission channel, wherein the second polar code permutation vector is smaller than the polar code permutation vector.

11. The apparatus of claim 10, wherein the second polar code permutation vector is half the size of the polar code permutation vector.

12. The apparatus of claim 10, wherein the processing circuitry is further configured to:

generate a third polar code permutation vector using the second polar code permutation vector and a size of the second polar code permutation vector;

generate a bit sequence of size equal to the size of the polar code permutation vector,

wherein a bit at a bit position in the bit sequence indicates whether a value at the bit position within the polar code permutation vector is the same as a value at the bit position within the polar code permutation vector or a value at the bit position within the second polar code permutation vector.

13. The apparatus of claim 12, wherein the processing circuitry is further configured to:

encode the third polar code permutation vector and the bit sequence as a representation of the polar code permutation vector, for transmission to the eNB.

14. The apparatus of any of claims 1-7, further comprising:

a transceiver coupled to an antenna, the transceiver configured to transmit the encoded information block to the eNB.

15. An apparatus of an evolved Node B (eNB) configured to communicate with a user equipment (UE), the apparatus comprising:

memory; and

processing circuitry, the processing circuitry configured to:

acquire a bit sequence and a first polar code permutation vector from the memory;

generate using the bit sequence and the first polar code permutation vector, a second polar code permutation vector, the second polar code permutation vector having a number of bit positions that is a multiple of a number of bit positions within the first polar code permutation vector;

apply the second polar code permutation vector to input vectors to obtain output permuted vectors; and

polar code the output permuted vectors using a generator matrix, to generate an encoded information block for transmission to the UE via a transmission channel.

16. The apparatus of claim 15, wherein the processing circuitry is further configured to:

generate a third polar code permutation vector using the first polar code permutation vector and the number of bit positions within the first polar code permutation vector.

17. The apparatus of claim 16, wherein the processing circuitry is further configured to:

add the number of bit positions within the first polar code permutation vector to each vector value within the first polar code permutation vector to generate the third polar code permutation vector.

18. The apparatus of any of claims 16-17, wherein:

the bit sequence comprises a plurality of bits at a corresponding plurality of bit positions; and

a bit at a bit position of the plurality of bit positions indicates whether a value at the bit position within the second polar code permutation vector is determined based on a value at the bit position within the first polar code permutation vector or a value at the bit position within the third polar code permutation vector.

19. A computer-readable storage medium that stores instructions for execution by one or more processors of a user equipment (UE), the one or more processors to configure the UE to:

generate input vectors by adding zeros to a set of input bits;

iterate between a minimum SNR and a maximum SNR at a pre-determined SNR increment value, to generate estimates of channel reliability of a transmission channel;

generate a polar code permutation vector based on estimates of channel reliability of the transmission channel;

apply the polar code permutation vector to the input vectors to obtain output permuted vectors; and

polar code the output permuted vectors using a generator matrix, to generate an encoded information block for transmission to an evolved Node-B (eNB) via the transmission channel,

wherein each estimate of channel reliability is associated with one or more construction codes indicating output bit positions with the BLER below the threshold level, and

wherein the polar code permutation vector indicates positions of the input bits within the output vectors associated with a block error rate (BLER) below a threshold level.

20. The computer-readable storage medium of claim 19, wherein to generate the polar code permutation vector, the one or more processors further configure the UE to:

initialize the polar code permutation vector as an empty vector.

21. The computer-readable storage medium of claim 20, wherein to generate the permutation vector, the one or more processors further configure the UE to:

select a construction code from the one or more construction codes, associated with a highest channel rate among the determined plurality of channel rates; and

append new bit positions associated with the selected construction code to the permutation vector.

22. The computer-readable storage medium of claim 21, wherein to generate the permutation vector, the one or more processors further configure the UE to:

determine for the selected construction code and the highest channel rate, whether the new bit positions are a superset of a previous polar code permutation vector generated during a previous iteration; and

append the new bit positions to the polar code permutation vector upon determining that the new bit positions are a superset of the previous permutation vector.

23. The computer-readable storage medium of claim 22, wherein to generate the permutation vector, the one or more processors further configure the UE to:

determine whether a number of bit positions within the polar code permutation vector matches a number of inputs to the generator matrix; and

upon determining the number of bit positions within the polar code permutation vector does not match a number of inputs to the generator matrix and one or more bit positions are missing, add the missing bit positions to the polar code permutation vector.

24. The computer-readable storage medium of any of claims 19-23, wherein the one or more processors further configure the UE to:

generate a second polar code permutation vector based on the plurality estimates of channel reliability of a transmission channel, wherein the second polar code permutation vector comprises a number of values that is smaller than a number of values within the polar code permutation vector.

25. The computer-readable storage medium of claim 24, wherein the one or more processors further configure the UE to:

generate a third polar code permutation vector using the second polar code permutation vector and the number of values within the second polar code permutation vector.

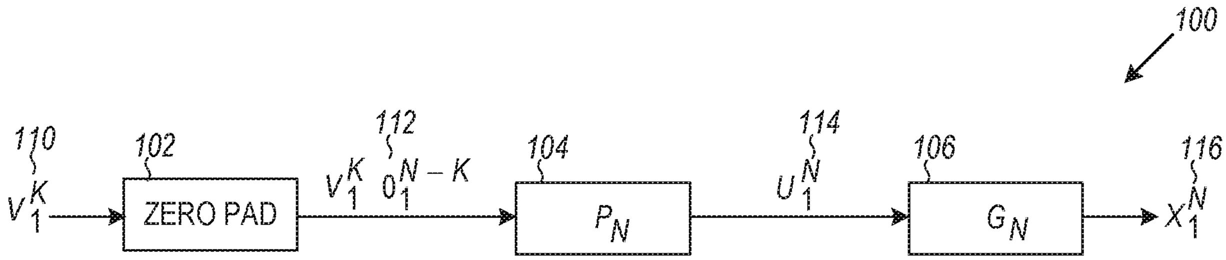
100
110
V_1^K
102
ZERO PAD
112
$V_1^K \ 0_1^{N-K}$
104
P_N
114
U_1^N
106
G_N
116
X_1^N

FIG. 1

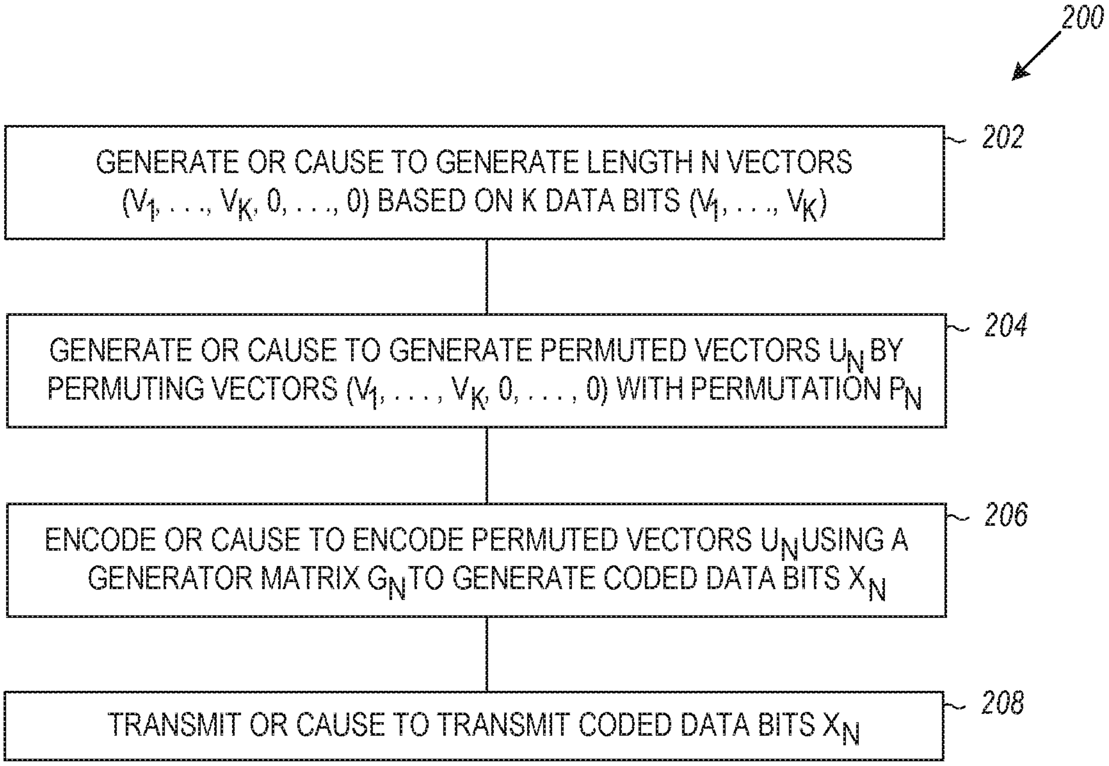
200
GENERATE OR CAUSE TO GENERATE LENGTH N VECTORS $(V_1, \ldots, V_K, 0, \ldots, 0)$ BASED ON K DATA BITS $(V_1, \ldots, V_K)$
202
GENERATE OR CAUSE TO GENERATE PERMUTED VECTORS U_N BY PERMUTING VECTORS $(V_1, \ldots, V_K, 0, \ldots, 0)$ WITH PERMUTATION P_N
204
ENCODE OR CAUSE TO ENCODE PERMUTED VECTORS U_N USING A GENERATOR MATRIX G_N TO GENERATE CODED DATA BITS X_N
206
TRANSMIT OR CAUSE TO TRANSMIT CODED DATA BITS X_N
208

FIG. 2

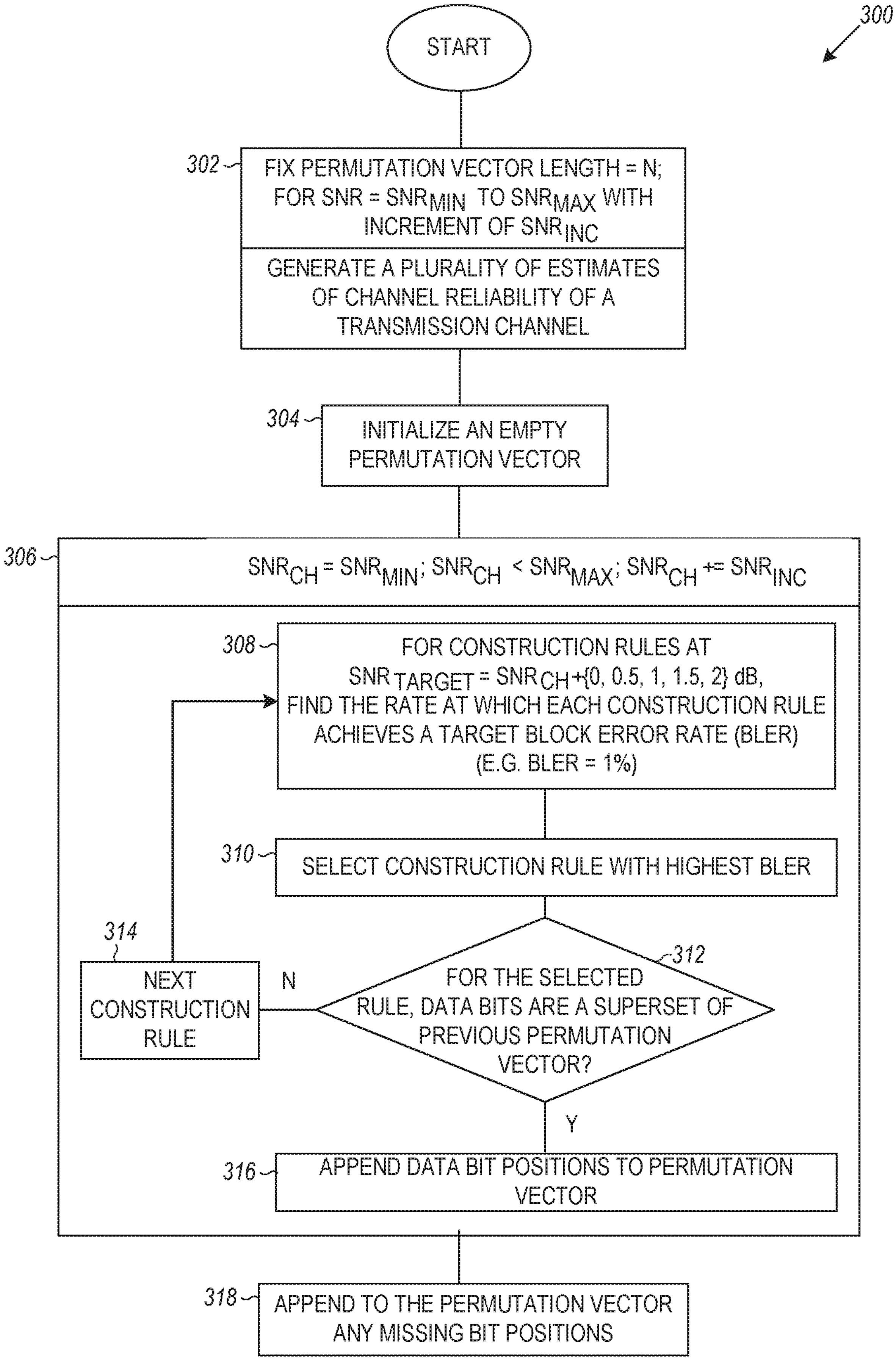
300
START
302
FIX PERMUTATION VECTOR LENGTH = N; FOR SNR = SNR$_{MIN}$ TO SNR$_{MAX}$ WITH INCREMENT OF SNR$_{INC}$
GENERATE A PLURALITY OF ESTIMATES OF CHANNEL RELIABILITY OF A TRANSMISSION CHANNEL
304
INITIALIZE AN EMPTY PERMUTATION VECTOR
306
SNR$_{CH}$ = SNR$_{MIN}$; SNR$_{CH}$ < SNR$_{MAX}$; SNR$_{CH}$ += SNR$_{INC}$
308
FOR CONSTRUCTION RULES AT SNR$_{TARGET}$ = SNR$_{CH}$+{0, 0.5, 1, 1.5, 2} dB, FIND THE RATE AT WHICH EACH CONSTRUCTION RULE ACHIEVES A TARGET BLOCK ERROR RATE (BLER) (E.G. BLER = 1%)
310
SELECT CONSTRUCTION RULE WITH HIGHEST BLER
312
FOR THE SELECTED RULE, DATA BITS ARE A SUPERSET OF PREVIOUS PERMUTATION VECTOR?
N
314
NEXT CONSTRUCTION RULE
Y
316
APPEND DATA BIT POSITIONS TO PERMUTATION VECTOR
318
APPEND TO THE PERMUTATION VECTOR ANY MISSING BIT POSITIONS

FIG. 3

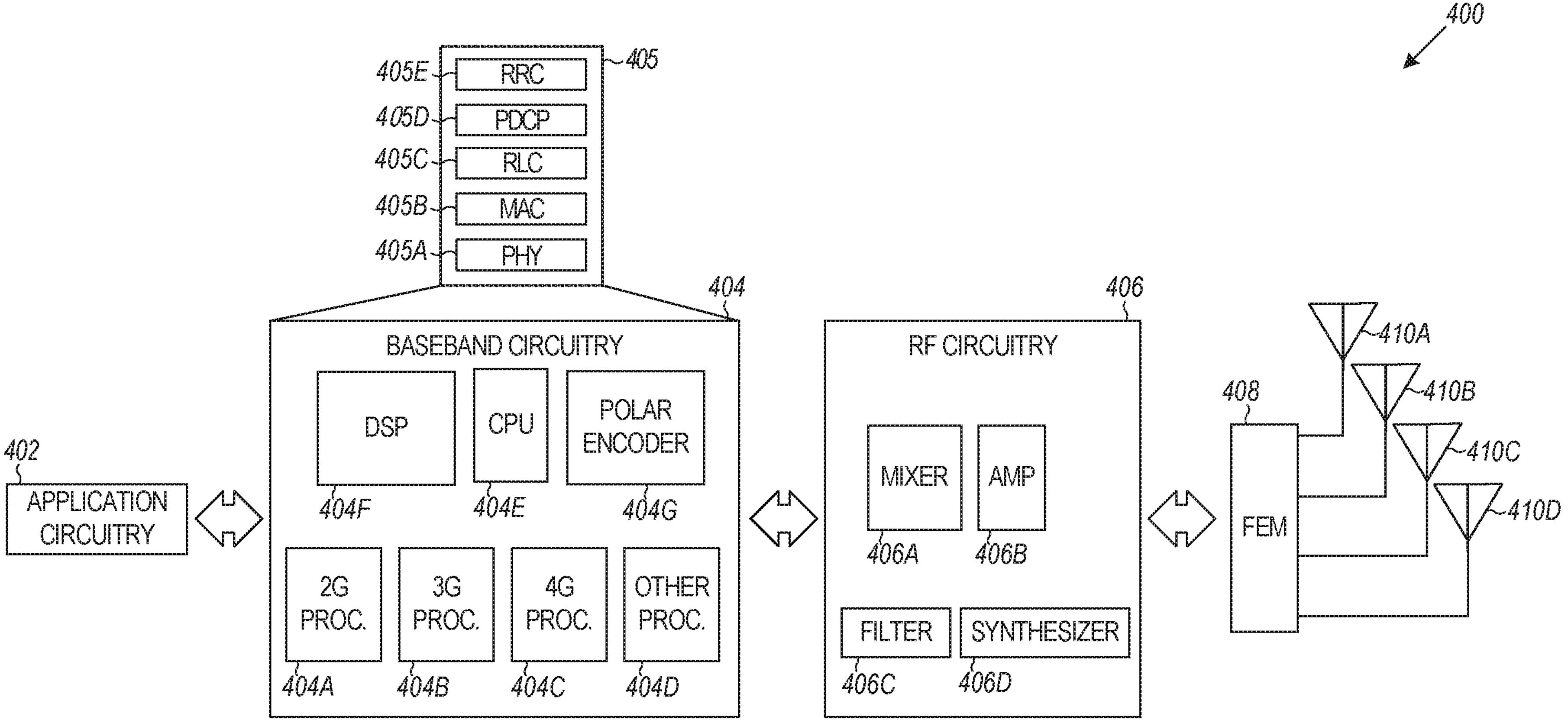
400
405
405E
RRC
405D
PDCP
405C
RLC
405B
MAC
405A
PHY
404
BASEBAND CIRCUITRY
DSP
404F
CPU
404E
POLAR ENCODER
404G
2G PROC.
404A
3G PROC.
404B
4G PROC.
404C
OTHER PROC.
404D
402
APPLICATION CIRCUITRY
406
RF CIRCUITRY
MIXER
406A
AMP
406B
FILTER
406C
SYNTHESIZER
406D
408
FEM
410A
410B
410C
410D

FIG. 4

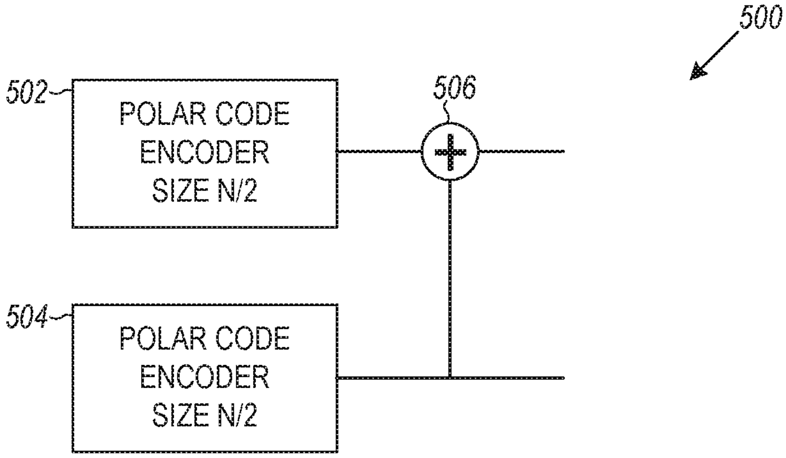
500
502
POLAR CODE ENCODER SIZE N/2
506
504
POLAR CODE ENCODER SIZE N/2

FIG. 5

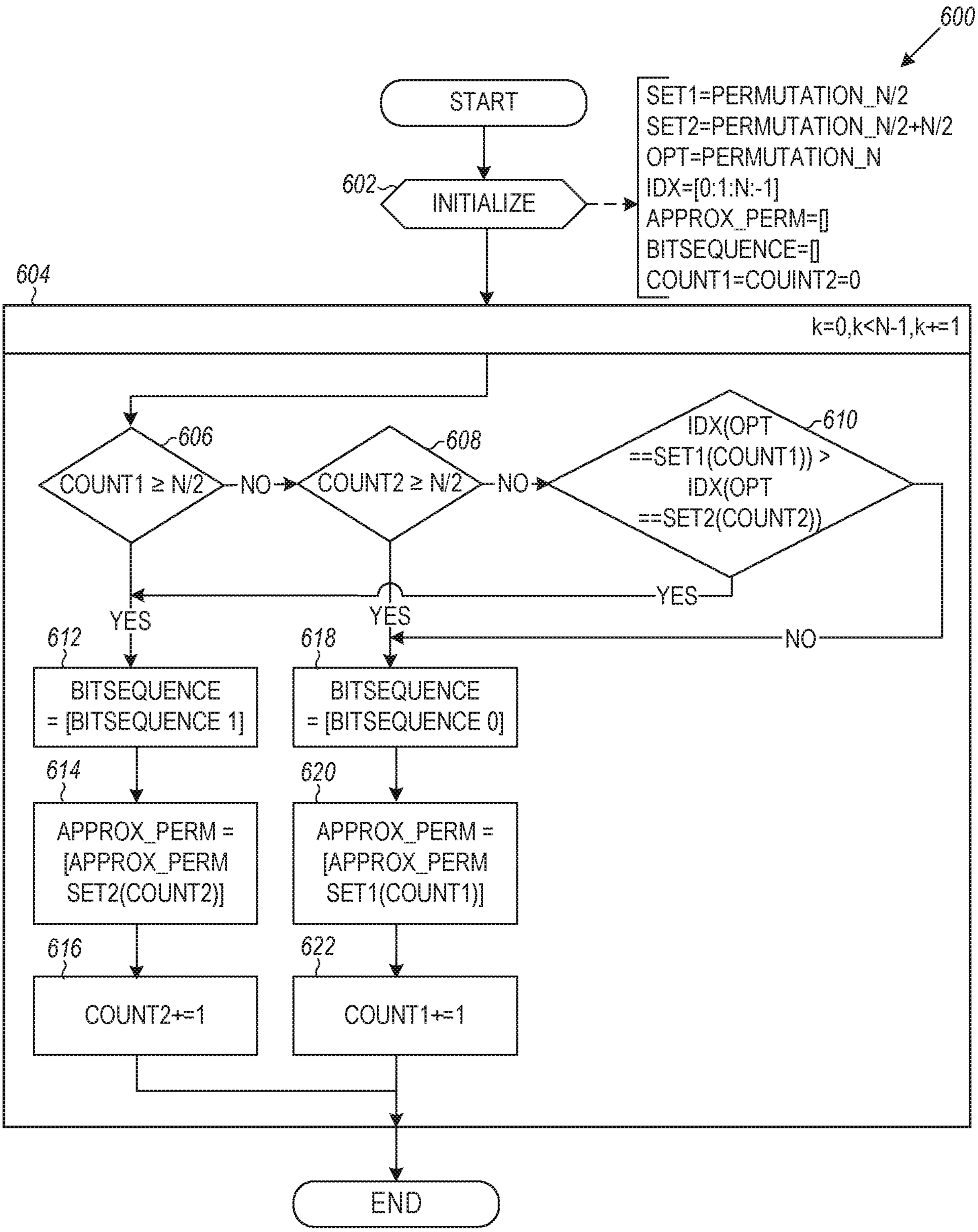
600
START
602
INITIALIZE
SET1=PERMUTATION_N/2
SET2=PERMUTATION_N/2+N/2
OPT=PERMUTATION_N
IDX=[0:1:N:-1]
APPROX_PERM=[]
BITSEQUENCE=[]
COUNT1=COUINT2=0
604
k=0,k<N-1,k+=1
606
COUNT1 ≥ N/2
NO
608
COUNT2 ≥ N/2
NO
610
IDX(OPT ==SET1(COUNT1)) > IDX(OPT ==SET2(COUNT2))
YES
YES
YES
NO
612
BITSEQUENCE = [BITSEQUENCE 1]
614
APPROX_PERM = [APPROX_PERM SET2(COUNT2)]
616
COUNT2+=1
618
BITSEQUENCE = [BITSEQUENCE 0]
620
APPROX_PERM = [APPROX_PERM SET1(COUNT1)]
622
COUNT1+=1
END

FIG. 6

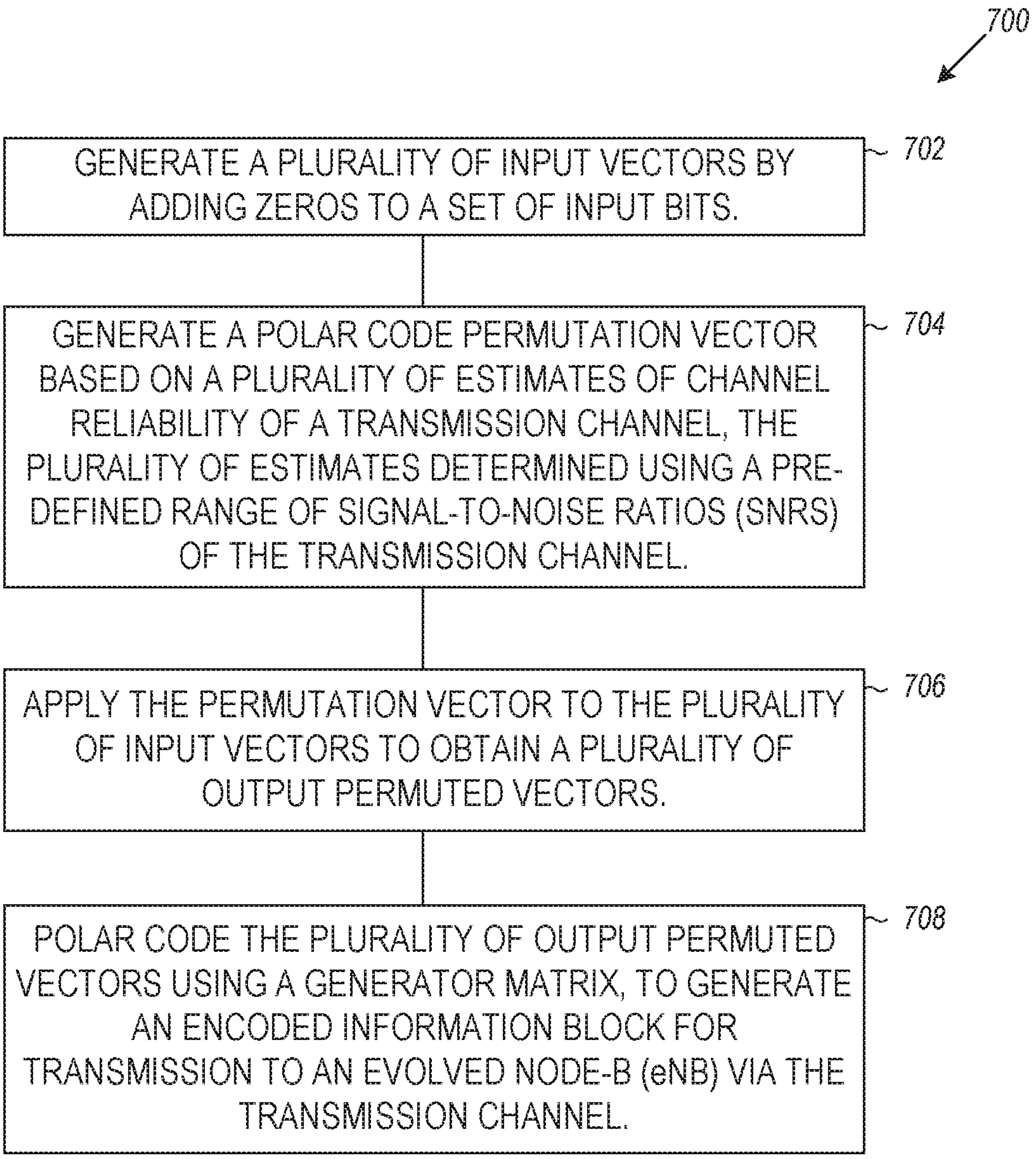
700
GENERATE A PLURALITY OF INPUT VECTORS BY ADDING ZEROS TO A SET OF INPUT BITS.
702
GENERATE A POLAR CODE PERMUTATION VECTOR BASED ON A PLURALITY OF ESTIMATES OF CHANNEL RELIABILITY OF A TRANSMISSION CHANNEL, THE PLURALITY OF ESTIMATES DETERMINED USING A PRE-DEFINED RANGE OF SIGNAL-TO-NOISE RATIOS (SNRS) OF THE TRANSMISSION CHANNEL.
704
APPLY THE PERMUTATION VECTOR TO THE PLURALITY OF INPUT VECTORS TO OBTAIN A PLURALITY OF OUTPUT PERMUTED VECTORS.
706
POLAR CODE THE PLURALITY OF OUTPUT PERMUTED VECTORS USING A GENERATOR MATRIX, TO GENERATE AN ENCODED INFORMATION BLOCK FOR TRANSMISSION TO AN EVOLVED NODE-B (eNB) VIA THE TRANSMISSION CHANNEL.
708

FIG. 7

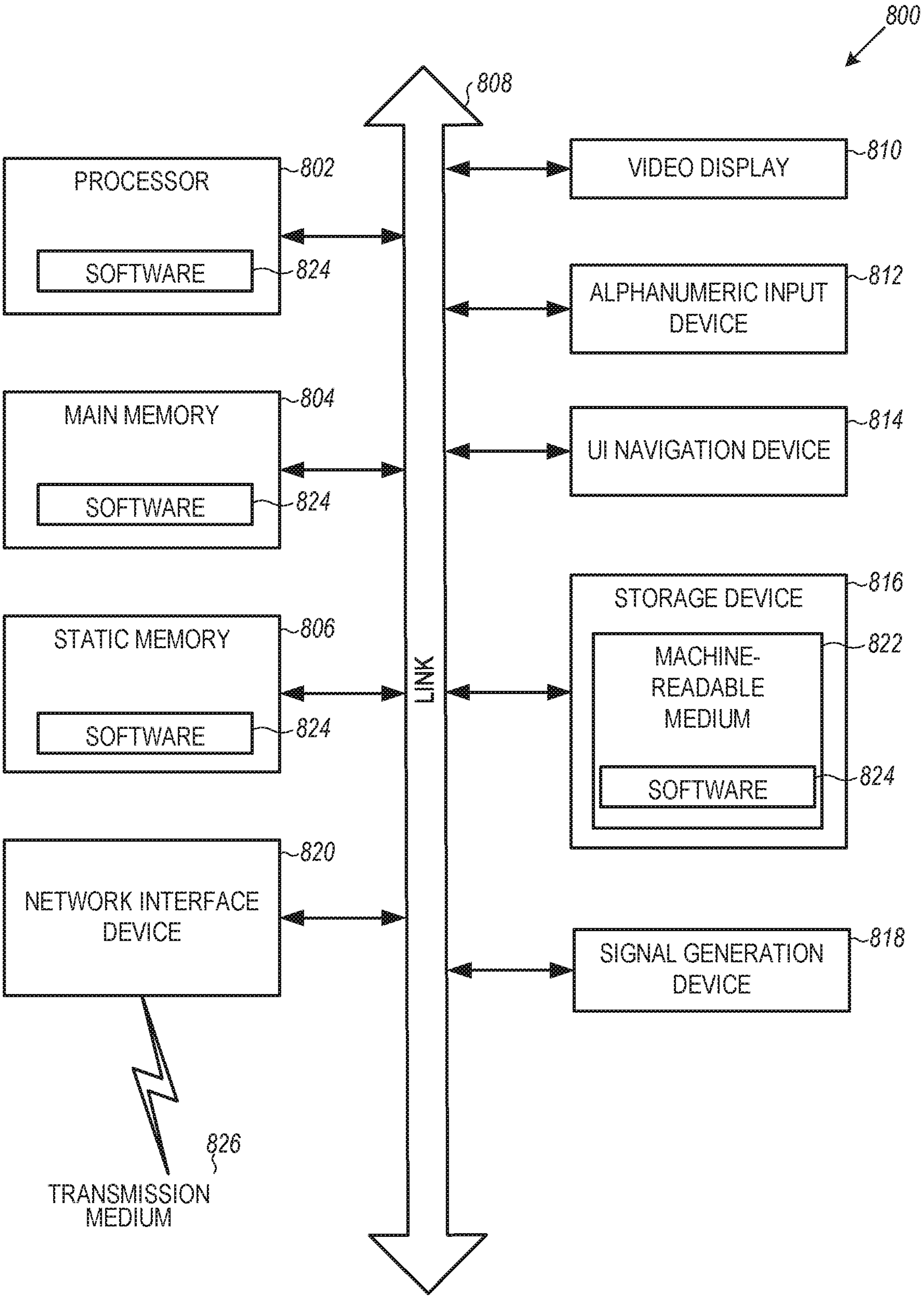
800
808
PROCESSOR
802
SOFTWARE
824
VIDEO DISPLAY
810
ALPHANUMERIC INPUT DEVICE
812
MAIN MEMORY
804
SOFTWARE
824
UI NAVIGATION DEVICE
814
STATIC MEMORY
806
SOFTWARE
824
LINK
STORAGE DEVICE
816
MACHINE-READABLE MEDIUM
822
SOFTWARE
824
NETWORK INTERFACE DEVICE
820
SIGNAL GENERATION DEVICE
818
826
TRANSMISSION MEDIUM

FIG. 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/063650

A. CLASSIFICATION OF SUBJECT MATTER

H04L 1/00(2006.01)i, H03M 13/00(2006.01)i, H03M 13/05(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04L 1/00; H03M 13/15; H03M 13/00; H03M 13/05

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & keywords: polar code, polar code permutation vector, generator matrix, SNR, BLER

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	BO YUAN et al., `Low-Latency Successive-Cancellation List Decoders for Polar Codes With Multibit Decision`, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Volume: 23, Issue: 10, October 2015 See sections II-A - IV-E.	1-9,14,19-23
A		10-13,15-18,24-25
Y	HARISH VANGALA et al., `A Comparative Study of Polar Code Constructions for the AWGN Channel`, arXiv:1501.02473v1, 11 January 2015 See sections II-V.	1-9,14,19-23
Y	US 2016-0013810 A1 (THE ROYAL INSTITUTION FOR THE ADVANCEMENT OF LEARNING / MCGILL UNIVERSITY) 14 January 2016 See paragraph [0042].	8
Y	WO 2015-026148 A1 (LG ELECTRONICS INC.) 26 February 2015 See paragraphs [0279]-[0283], [0340].	14
A	US 2016-0013887 A1 (HUAWEI TECHNOLOGIES CO., LTD.) 14 January 2016 See paragraphs [0120]-[0163]; and figures 1-4.	1-25

☐ Further documents are listed in the continuation of Box C.   ☒ See patent family annex.

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