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(54) EMBEDDED DRAM GAIN MEMORY CELL

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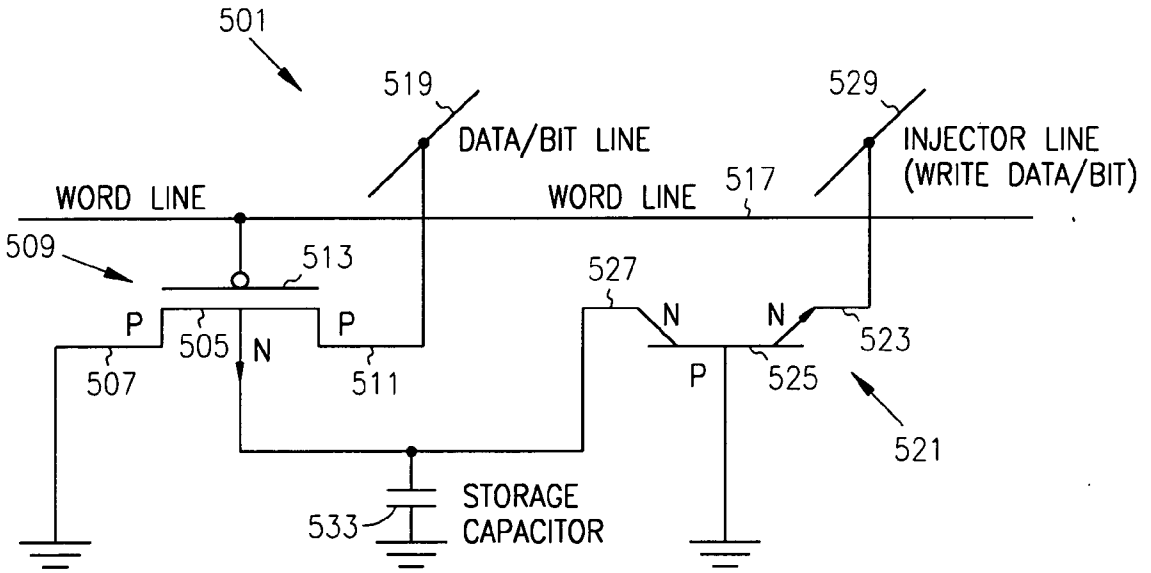
(52) **U.S. Cl.** **365/149**

(57) **ABSTRACT**

A high density horizontal merged MOS-bipolar gain memory cell is realized for DRAM operation. The gain cell includes a horizontal MOS transistor having a source region, a drain region, and a floating body region therebetween. The gain cell includes a horizontal bi-polar transistor having an emitter region, a base region and a collector region. The collector region for the horizontal bi-polar transistor serves as the floating body region for the horizontal MOS transistor. A gate opposes the floating body region and is separated therefrom by a gate oxide. The emitter region for the horizontal bi-polar transistor is coupled to a write data line.



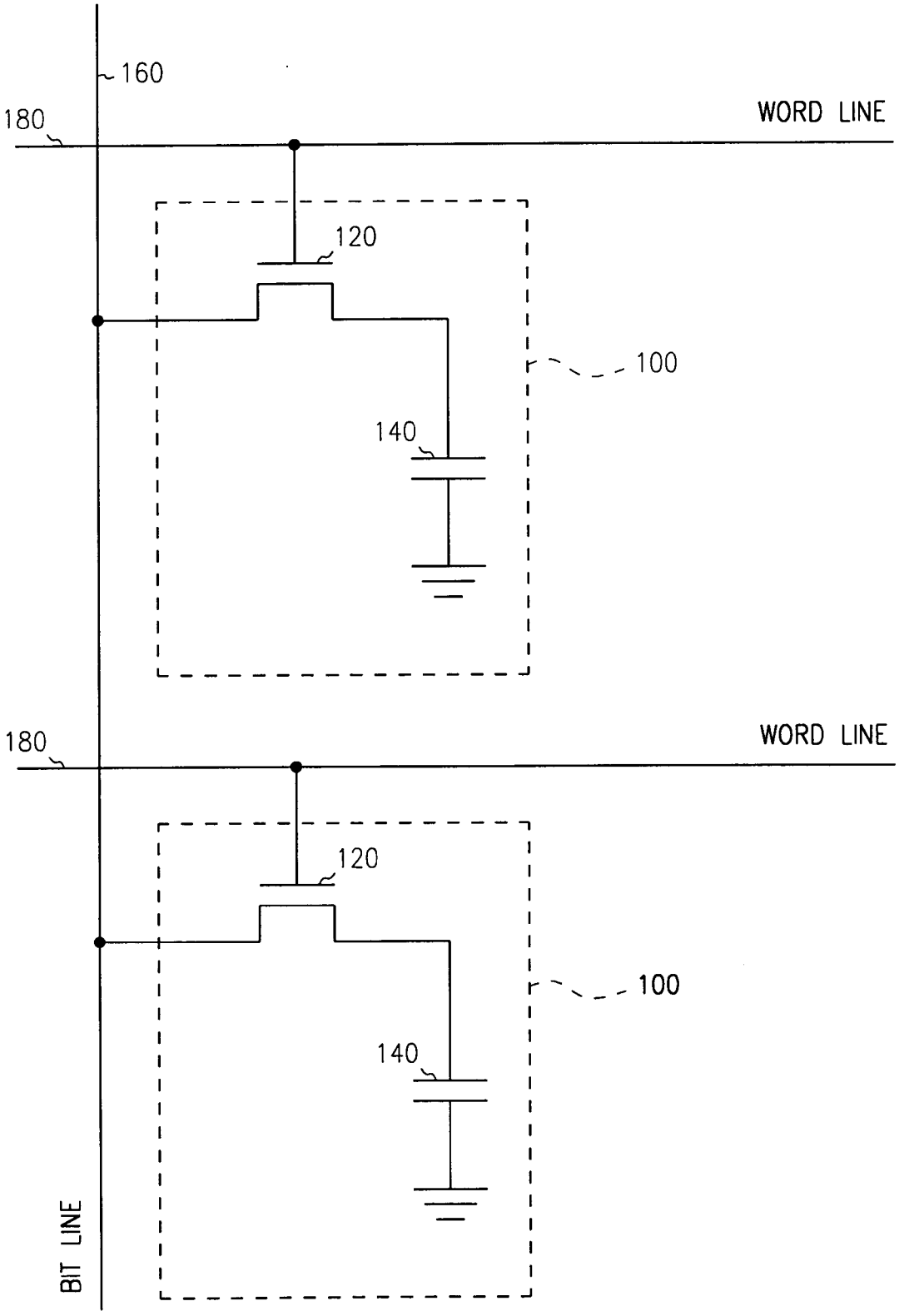


FIG. 1
(PRIOR ART)

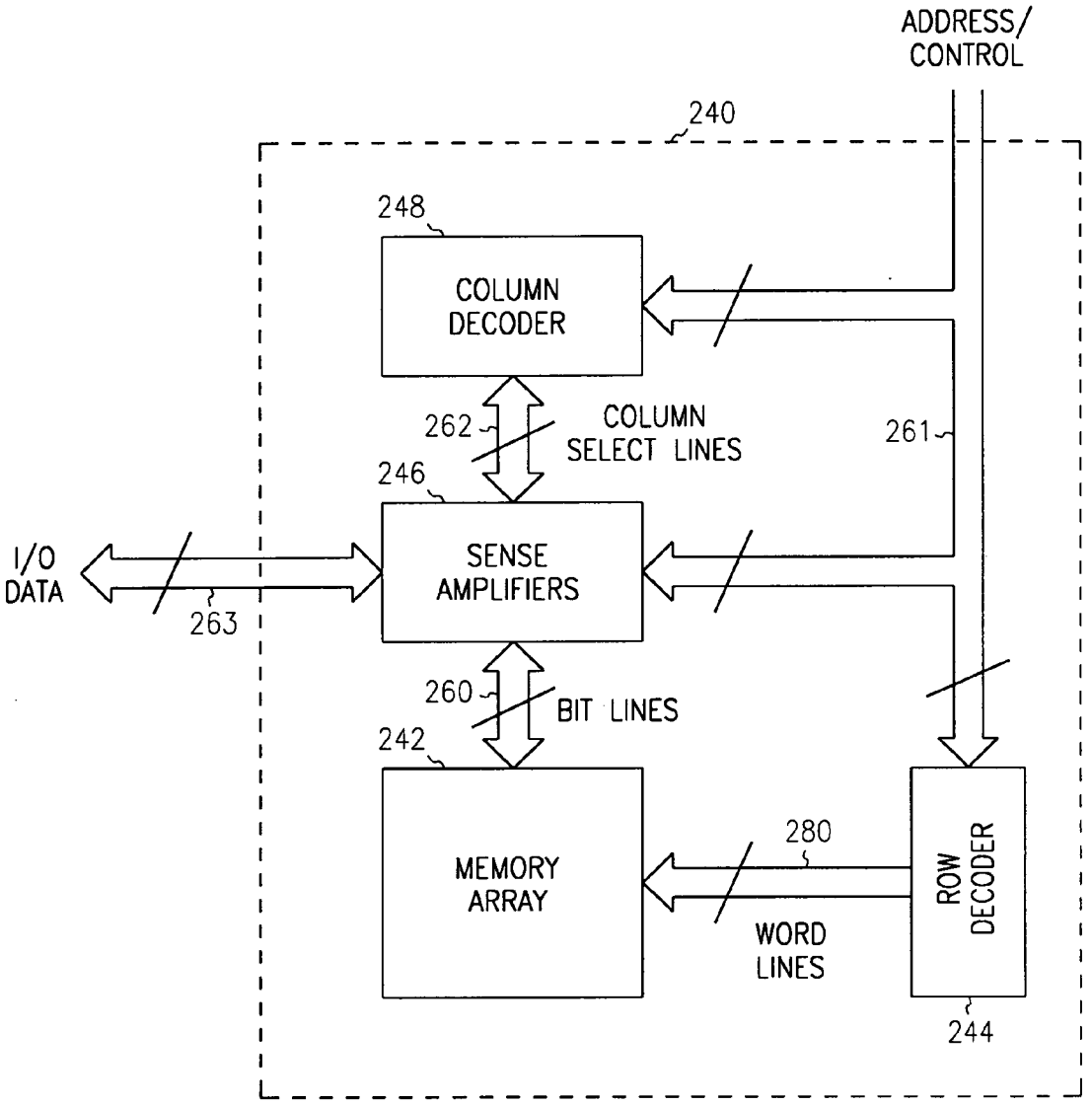

ADDRESS/
CONTROL
240
248
COLUMN
DECODER
262
COLUMN
SELECT LINES
261
246
I/O
DATA
SENSE
AMPLIFIERS
263
260
BIT LINES
242
MEMORY
ARRAY
280
WORD
LINES
ROW
DECODER
244

FIG. 2

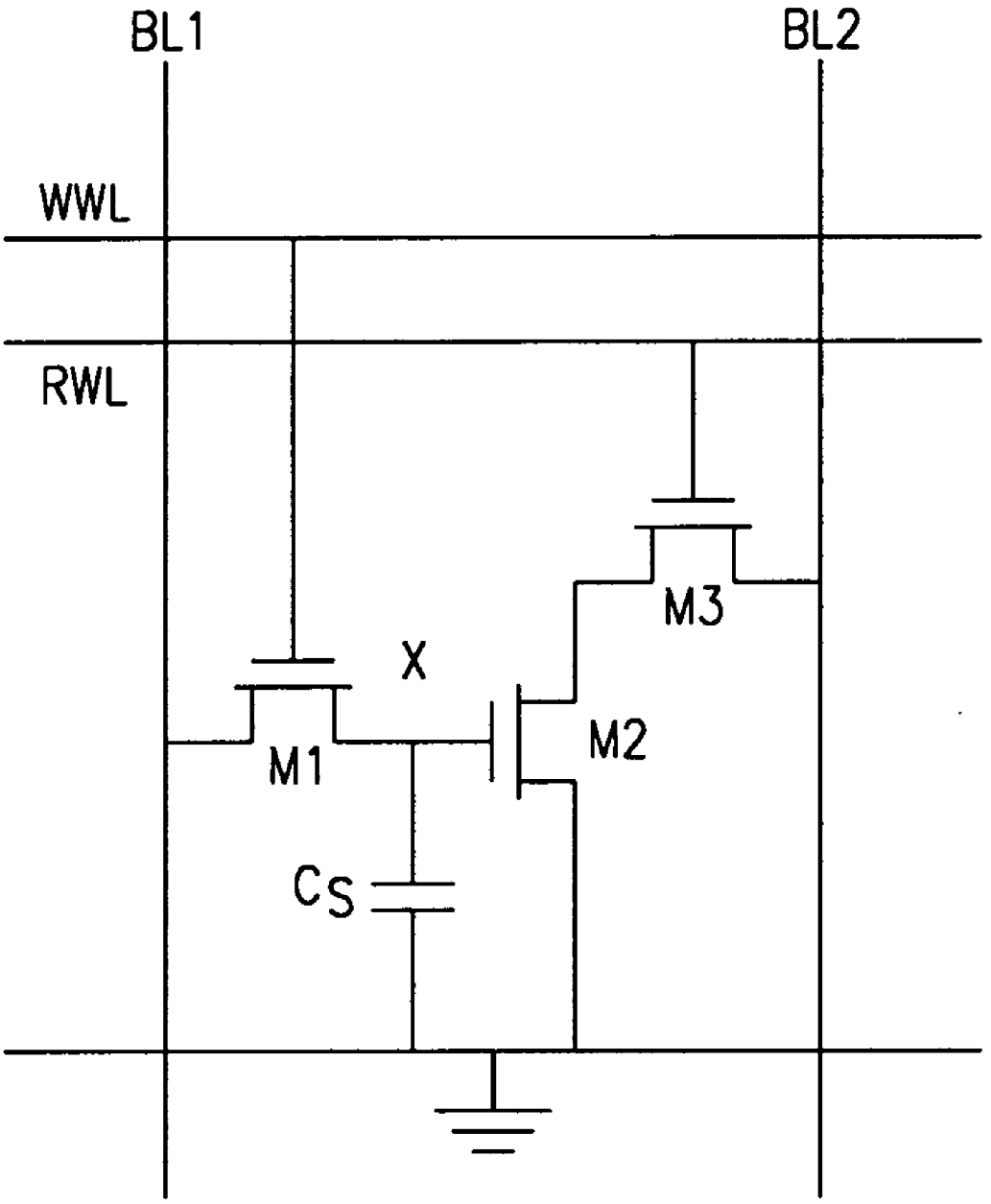


FIG. 3
(PRIOR ART)

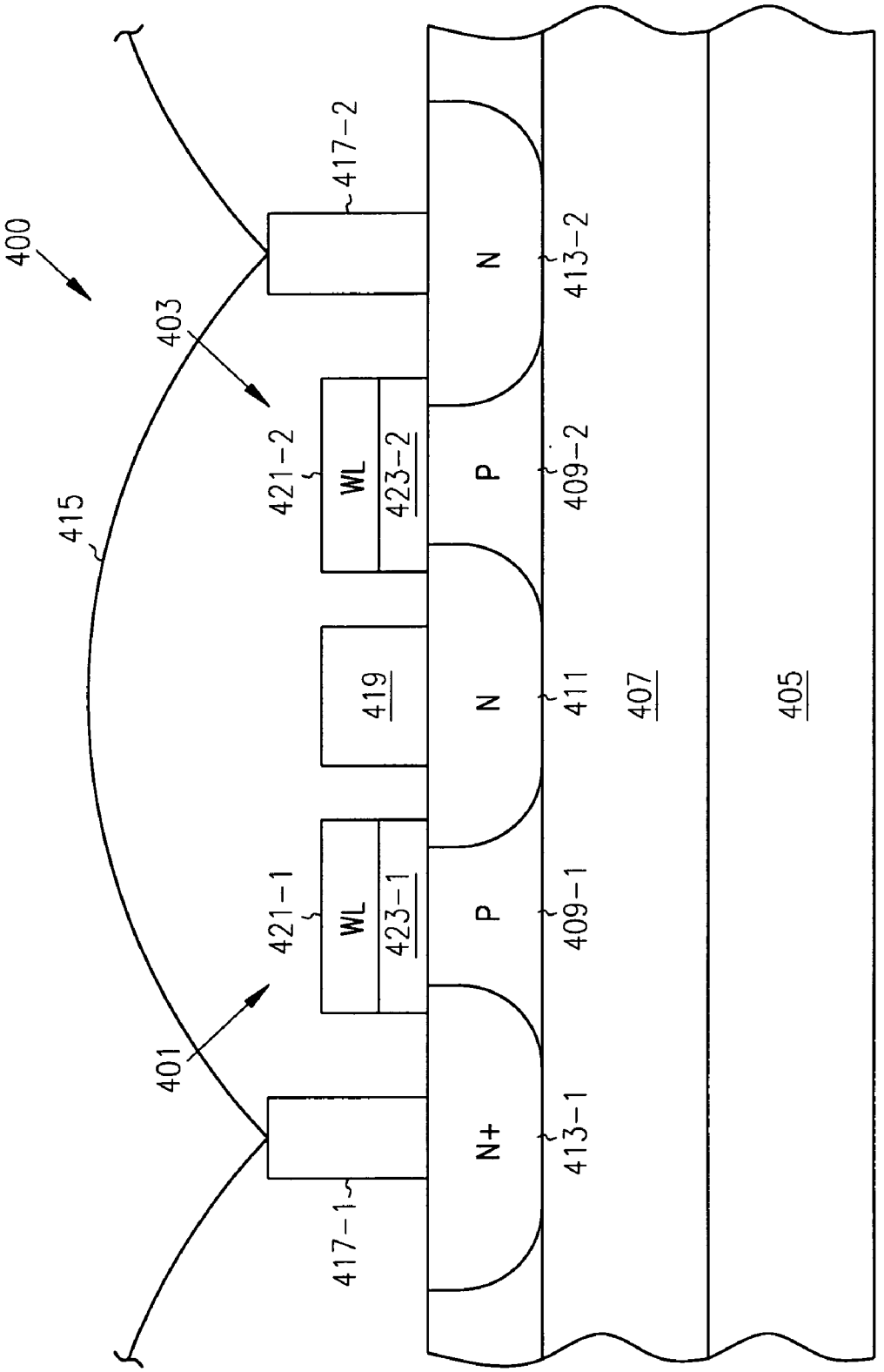

400
401
403
415
417-1
417-2
421-1
421-2
WL
423-1
423-2
419
N+
P
N
P
N
413-1
409-1
411
409-2
413-2
407
405

FIG. 4

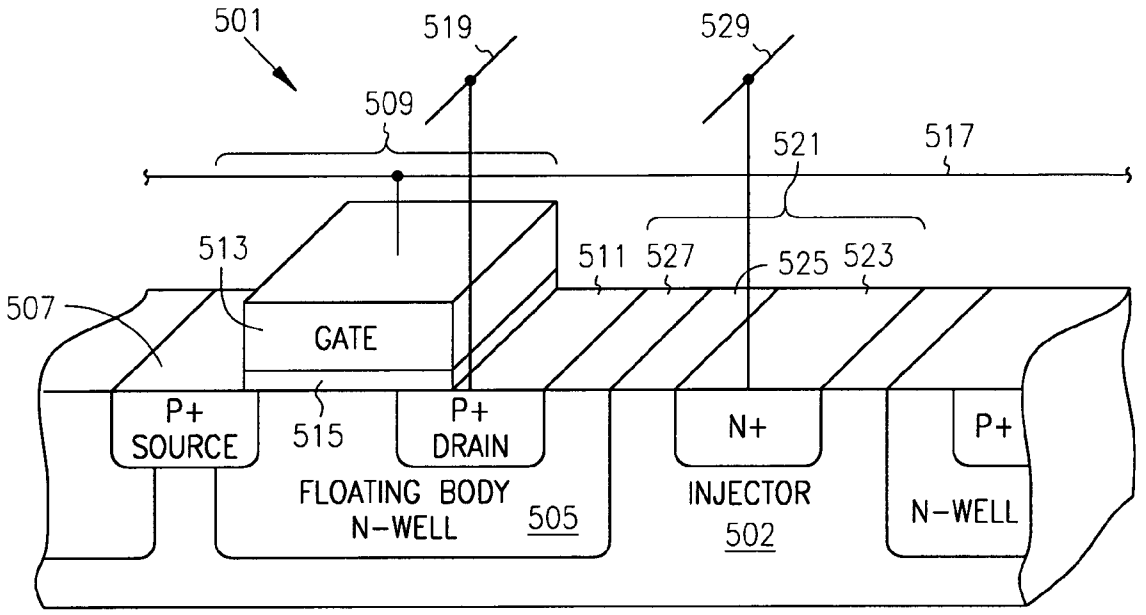

501
519
529
509
521
517
513
511
527
525
523
507
GATE
P+
SOURCE
515
P+
DRAIN
N+
P+
FLOATING BODY
N-WELL
505
INJECTOR
502
N-WELL

FIG. 5A

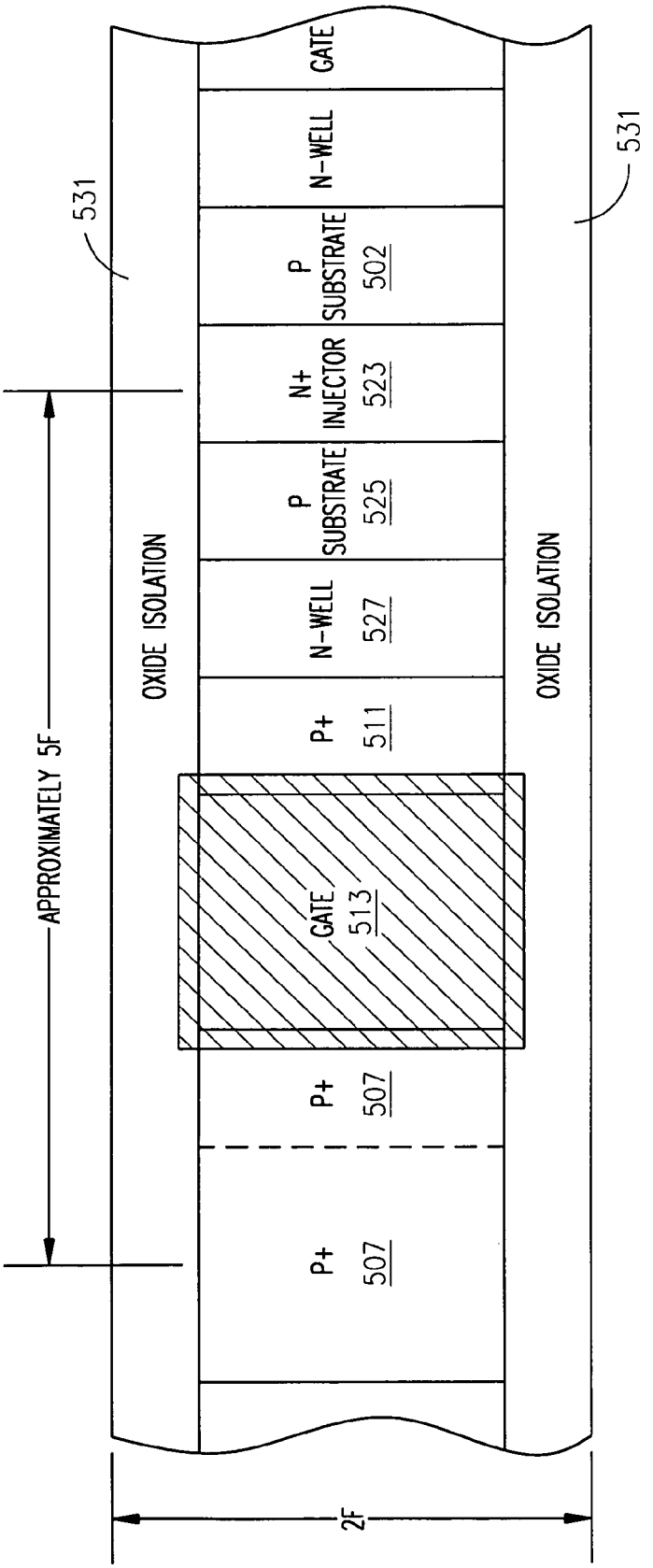

GATE
N-WELL
P SUBSTRATE 502
N+ INJECTOR 523
P SUBSTRATE 525
N-WELL 527
P+ 511
GATE 513
P+ 507
P+ 507
531
531
OXIDE ISOLATION
OXIDE ISOLATION
APPROXIMATELY 5F
2F

FIG. 5B

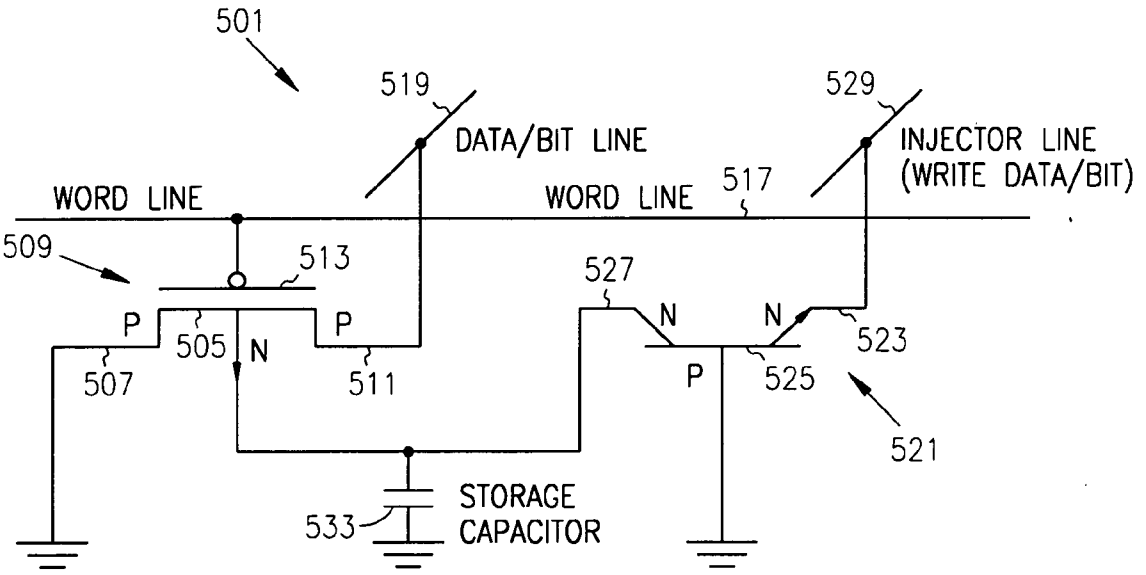

501
519
529
DATA/BIT LINE
INJECTOR LINE
(WRITE DATA/BIT)
WORD LINE
WORD LINE
517
509
513
527
P
505
N
P
N
N
523
507
511
P
525
521
533
STORAGE
CAPACITOR

FIG. 5C

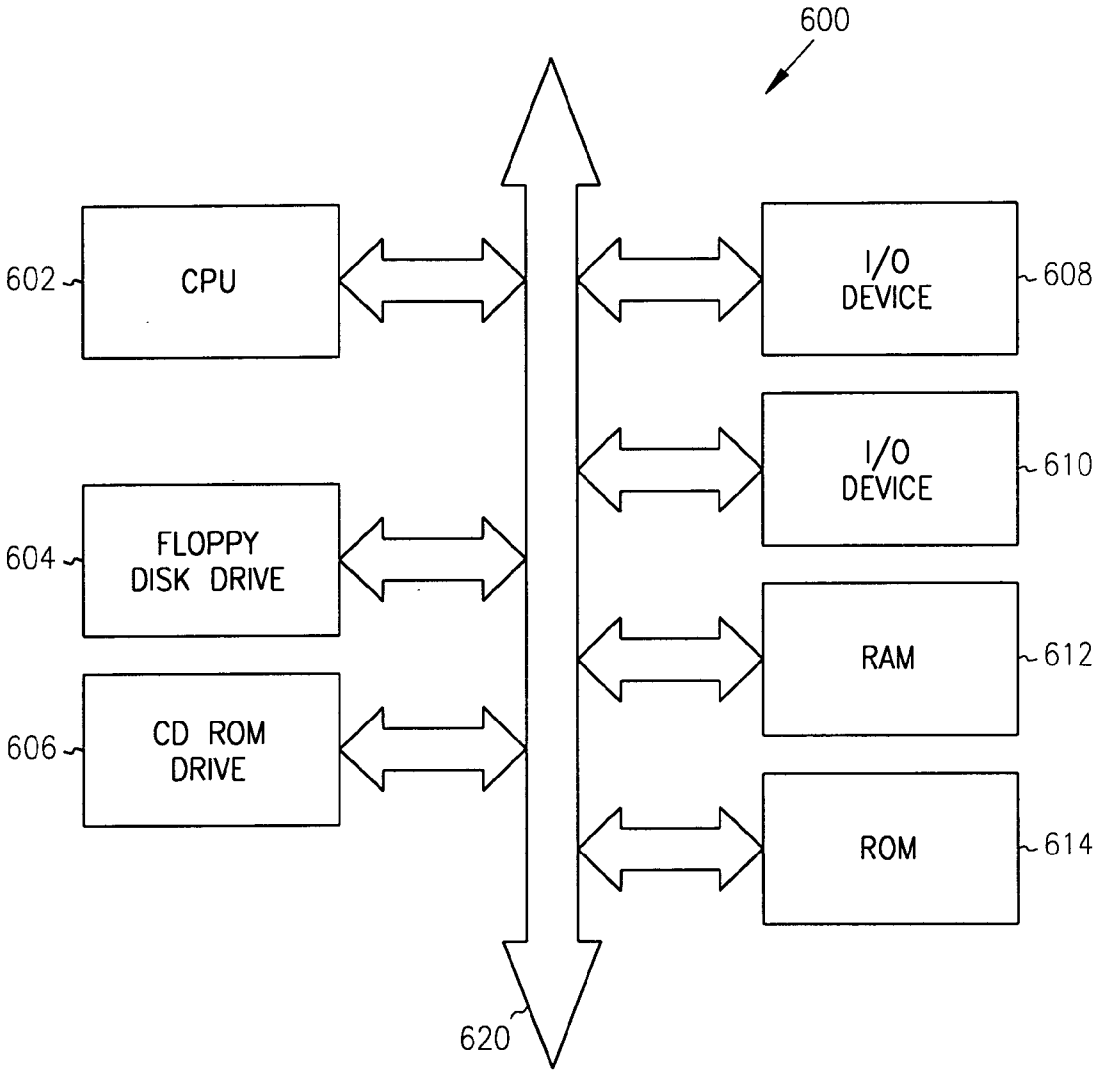

600
602
CPU
604
FLOPPY DISK DRIVE
606
CD ROM DRIVE
608
I/O DEVICE
610
I/O DEVICE
612
RAM
614
ROM
620

FIG. 6

EMBEDDED DRAM GAIN MEMORY CELL

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of U.S. application Ser. No. 10/309,873, filed Dec. 4, 2002, which is incorporated herein by reference.

[0002] This application is also related to the following commonly assigned U.S. patent applications: "Single Transistor Vertical Memory Gain Cell," Ser. No. 10/231,397, filed Aug. 29, 2002, "Merged MOS-Bipolar Capacitor Memory Cell," Ser. No. 10/230,929, filed Aug. 29, 2002, each of which disclosure is herein incorporated by reference.

FIELD OF THE INVENTION

[0003] The present invention relates generally to integrated circuits, and in particular to an embedded DRAM gain memory cell.

BACKGROUND OF THE INVENTION

[0004] An essential semiconductor device is semiconductor memory, such as a random access memory (RAM) device. A RAM device allows the user to execute both read and write operations on its memory cells. Typical examples of RAM devices include dynamic random access memory (DRAM) and static random access memory (SRAM).

[0005] DRAM is a specific category of RAM containing an array of individual memory cells, where each cell includes a capacitor for holding a charge and a transistor for accessing the charge held in the capacitor. The transistor is often referred to as the access transistor or the transfer device of the DRAM cell.

[0006] **FIG. 1** illustrates a portion of a DRAM memory circuit containing two neighboring DRAM cells **100**. Each cell **100** contains a storage capacitor **140** and an access field effect transistor or transfer device **120**. For each cell, one side of the storage capacitor **140** is connected to a reference voltage (illustrated as a ground potential for convenience purposes). The other side of the storage capacitor **140** is connected to the drain of the transfer device **120**. The gate of the transfer device **120** is connected to a signal known in the art as a word line **180**. The source of the transfer device **120** is connected to a signal known in the art as a bit line **160** (also known in the art as a digit line). With the memory cell **100** components connected in this manner, it is apparent that the word line **180** controls access to the storage capacitor **140** by allowing or preventing the signal (representing a logic "0" or a logic "1") carried on the bit line **160** to be written to or read from the storage capacitor **140**. Thus, each cell **100** contains one bit of data (i.e., a logic "0" or logic "1").

[0007] In **FIG. 2 a** DRAM circuit **240** is illustrated. The DRAM **240** contains a memory array **242**, row and column decoders **244**, **248** and a sense amplifier circuit **246**. The memory array **242** consists of a plurality of memory cells **200** (constructed as illustrated in **FIG. 1**) whose word lines **280** and bit lines **260** are commonly arranged into rows and columns, respectively. The bit lines **260** of the memory array **242** are connected to the sense amplifier circuit **246**, while its word lines **280** are connected to the row decoder **244**. Address and control signals are input on address/control lines **261** into the DRAM **240** and connected to the column decoder **248**, sense amplifier circuit **246** and row decoder **244** and are used to gain read and write access, among other things, to the memory array **242**.

[0008] The column decoder **248** is connected to the sense amplifier circuit **246** via control and column select signals on column select lines **262**. The sense amplifier circuit **246** receives input data destined for the memory array **242** and outputs data read from the memory array **242** over input/output (I/O) data lines **263**. Data is read from the cells of the memory array **242** by activating a word line **280** (via the row decoder **244**), which couples all of the memory cells corresponding to that word line to respective bit lines **260**, which define the columns of the array. One or more bit lines **260** are also activated. When a particular word line **280** and bit lines **260** are activated, the sense amplifier circuit **246** connected to a bit line column detects and amplifies the data bit transferred from the storage capacitor of the memory cell to its bit line **260** by measuring the potential difference between the activated bit line **260** and a reference line which may be an inactive bit line. The operation of DRAM sense amplifiers is described, for example, in U.S. Pat. Nos. 5,627,785; 5,280,205; and 5,042,011, all assigned to Micron Technology Inc., and incorporated by reference herein.

[0009] The memory cells of dynamic random access memories (DRAMs) are comprised of two main components, a field-effect transistor (FET) and a capacitor which functions as a storage element. The need to increase the storage capability of semiconductor memory devices has led to the development of very large scale integrated (VLSI) cells which provides a substantial increase in component density. As component density has increased, cell capacitance has had to be decreased because of the need to maintain isolation between adjacent devices in the memory array. However, reduction in memory cell capacitance reduces the electrical signal output from the memory cells, making detection of the memory cell output signal more difficult. Thus, as the density of DRAM devices increases, it becomes more and more difficult to obtain reasonable storage capacity.

[0010] As DRAM devices are projected as operating in the gigabit range, the ability to form such a large number of storage capacitors requires smaller areas. However, this conflicts with the requirement for larger capacitance because capacitance is proportional to area. Moreover, the trend for reduction in power supply voltages results in stored charge reduction and leads to degradation of immunity to alpha particle induced soft errors, both of which require that the storage capacitance be even larger.

[0011] By using embedded memory rather than external memory, designers can maximize memory throughput to achieve higher system performance, introduce innovative architectures with customized memory sizes, and reduce power consumption in their systems. (See generallly, H. Takato et al., _Process Integration Trends for Embedded DRAM,__ *Proceedings of U1SI Process Integration, Electrochemical Society Proceedings,* 99-18, 107-19 (1999); M. Mukai et al., _Proposal of a Logic Compatible Merged-Type Gain Cell for High Density Embedded.,__ *IEEE Trans. on Electron Devices,* 46-6, 1201-1206 (1999)). Designers will also benefit from less expensive packaging, by removing the extra pins that drive external memory and by eliminating

board space otherwise required by external memory chips. Both of these benefits can lower production costs. In addition, using embedded memory ensures users of a guaranteed supply of this type of memory, without the volatility of the external memory market.

[0012] One approach to embedded memory technology is based on the one transistor DRAM cell structure that utilizes the trench process employed in IBM's and Toshiba's DRAMs. (See generally, W. P. Noble et al., _The evolution of IBM CMOS DRAM Technology,__ *IBM J. Research and Development,* 39-1/2, 167-188 (1995)). With trench technology, logic performance is not compromised. Trench technology provides a planar surface topology that enhances interconnect reliability while providing a DRAM storage capacitor with a large and conventional storage capacitance. However, additional masking levels are required in the logic technology to fabricate the trench capacitors.

[0013] Another approach to embedded memory is based on a three transistor DRAM cell structure, shown in **FIG. 3**. The three transistor DRAM cell structure was developed prior to the use of the trench capacitors or stacked capacitors now used in DRAMs. (See generally, J. Rabaey, Digital Integrated Circuits, Prentice Hall, 585-587 (1996)). A much smaller storage capacitor was utilized and compensated for by the gain of one of the transistors, in other words the first DRAMs developed used gain cells. These type of DRAM cells require only a minor modification of the conventional logic technology processes but occupy a large area due to the use of three transistors.

[0014] The inventors have previously disclosed a DRAM gain cell using two transistors. (See generally, L. Forbes, "Merged Transistor Structure for Gain Memory Cell," U.S. Pat. No. 5,732,014, issued 24 Mar. 1998, continuation granted as U.S. Pat. No. 5,897,351, issued 27 Apr. 1999). A number of other gain cells have also been disclosed. (See generally, Sunouchi et al., "A self-Amplifying (SEA) Cell for Future High Density DRAMs," Ext. Abstracts of IEEE Int. Electron Device Meeting, pp. 465-468 (1991); M. Terauchi et al., "A Surrounding Gate Transistor (SGT) Gain Cell for Ultra High Density DRAMS," VLSI Tech. Symposium, pp. 21-22 (1993); S. Shukuri et al., "Super-Low-Voltage Operation of a Semi-Static Complementary Gain RAM Memory Cell," VLSI Tech. Symposium pp. 23-24 (1993); S. Shukuri et al., "Super-low-voltage operation of a semi-static complementary gain DRAM memory cell," Ext. Abs. of IEEE Int. Electron Device Meeting, pp. 1006-1009 (1992); S. Shukuri et al., "A Semi-Static Complementary Gain Cell Technology for Sub-1 V Supply DRAM's," IEEE Trans. on Electron Devices, Vol. 41, pp. 926-931 (1994); H. Wann and C. Hu, "A Capacitorless DRAM Cell on SOI Substrate," Ext. Abs. IEEE Int. Electron Devices Meeting, pp. 635-638; W. Kim et al., "An Experimental High-Density DRAM Cell with a Built-in Gain Stage," IEEE J. of Solid-State Circuits, Vol. 29, pp. 978-981 (1994); W. H. Krautschneider et al., "Planar Gain Cell for Low Voltage Operation and Gigabit Memories," Proc. VLSI Technology Symposium, pp. 139-140 (1995); D. M. Kenney, "Charge Amplifying trench Memory Cell," U.S. Pat. No. 4,970,689, 13 Nov. 1990; M. Itoh, "Semiconductor memory element and method of fabricating the same," U.S. Pat. No. 5,220, 530, 15 Jun. 1993; W. H. Krautschneider et al., "Process for the Manufacture of a high density Cell Array of Gain Memory Cells," U.S. Pat. No. 5,308,783, 3 May 1994; C. Hu et al., "Capacitorless DRAM device on Silicon on Insulator Substrate," U.S. Pat. No. 5,448,513, 5 Sep. 1995; S. K. Banerjee, "Method of making a Trench DRAM cell with Dynamic Gain," U.S. Pat. No. 5,066,607, 19 Nov. 1991; S. K. Banerjee, "Trench DRAM cell with Dynamic Gain," U.S. Pat. No. 4,999,811, 12 Mar. 1991; Lim et al., "Two transistor DRAM cell," U.S. Pat. No. 5,122,986, 16 Jun. 1992).

[0015] Recently a one transistor gain cell has been reported as shown in **FIG. 4**. (See generally, T. Ohsawa et al., "Memory design using one transistor gain cell on SOI," IEEE Int. Solid State Circuits Conference, San Francisco, 2002, pp. 152-153). **FIG. 4** illustrates a portion of a DRAM memory circuit containing two neighboring gain cells, **401** and **403**. Each gain cell, **401** and **403**, is separated from a substrate **405** by a buried oxide layer **407**. The gain cells, **401** and **403**, are formed on the buried oxide **407** and thus have a floating body, **409-1** and **409-2** respectively, separating a source region **411** (shared for the two cells) and a drain region **413-1** and **413-2**. A bit/data line **415** is coupled to the drain regions **413-1** and **413-2** via bit contacts, **417-1** and **417-2**. A ground source **419** is coupled to the source region **411**. Wordlines or gates, **421-1** and **421-2**, oppose the floating body regions **409-1** and **409-2** and are separated therefrom by a gate oxide, **423-1** and **423-2**.

[0016] In the gain cell shown in **FIG. 4 a** floating body, **409-1** and **409-2**, back gate bias is used to modulate the threshold voltage and consequently the conductivity of the NMOS transistor in each gain cell. The potential of the back gate body, **409-1** and **409-2**, is made more positive by avalanche breakdown in the drain regions, **413-1** and **413-2**, and collection of the holes generated by the body, **409-1** and **409-2**. A more positive potential or forward bias applied to the body, **409-1** and **409-2**, decreases the threshold voltage and makes the transistor more conductive when addressed. Charge storage is accomplished by this additional charge stored on the floating body, **409-1** and **409-2**. Reset is accomplished by forward biasing the drain-body n-p junction diode to remove charge from the body.

[0017] Still, there is a need in the art for improved DRAM cell structures which can be based entirely on conventional CMOS logic technology, without additional masking and process steps, and which have a minimal cell area.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] **FIG. 1** is a circuit diagram illustrating conventional dynamic random access memory (DRAM) cells.

[0019] **FIG. 2** is a block diagram illustrating a DRAM device.

[0020] **FIG. 3** is a schematic for an embedded memory based on a three transistor DRAM cell structure.

[0021] **FIG. 4** illustrates two neighboring one transistor gain cells as a portion of a memory array.

[0022] **FIG. 5A** is a cross-sectional, perspective view illustrating an embodiment of a horizontally merged MOS-bipolar transistor gain memory cell according to the teachings of the present invention.

[0023] **FIG. 5B** illustrates a top view of **FIG. 5A** in planar, CMOS technology with shallow trench oxide isolation.

[0024] **FIG. 5C** illustrates an electrical equivalent circuit embodiment of the horizontally merged MOS-bipolar tran-

sistor gain memory cell indicating that the floating body well of the horizontal MOS transistor and the well to substrate capacitance acts as a storage capacitor.

[0025] **FIG. 6** is a block diagram illustrating an embodiment of an electronic system utilizing the embedded gain memory cells of the present invention.

DETAILED DESCRIPTION

[0026] In the following detailed description of the invention, reference is made to the accompanying drawings which form a part hereof, and in which is shown, by way of illustration, specific embodiments in which the invention may be practiced. The embodiments are intended to describe aspects of the invention in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and changes may be made without departing from the scope of the present invention. In the following description, the terms wafer and substrate are interchangeably used to refer generally to any structure on which integrated circuits are formed, and also to such structures during various stages of integrated circuit fabrication. Both terms include doped and undoped semiconductors, epitaxial layers of a semiconductor on a supporting semiconductor or insulating material, combinations of such layers, as well as other such structures that are known in the art.

[0027] The term "horizontal" as used in this application is defined as a plane parallel to the conventional plane or surface of a wafer or substrate, regardless of the orientation of the wafer or substrate. The term "vertical" refers to a direction perpendicular to the horizontal as defined above. Prepositions, such as "on", "side" (as in "sidewall"), "higher", "lower", "over" and "under" are defined with respect to the conventional plane or surface being on the top surface of the wafer or substrate, regardless of the orientation of the wafer or substrate. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims, along with the full scope of equivalents to which such claims are entitled.

[0028] **FIG. 5A** is a cross-sectional, perspective view illustrating an embodiment of an embedded, horizontally merged MOS-bipolar transistor gain memory cell **501** according to the teachings of the present invention. In the embodiment of **FIG. 5A**, the embedded, horizontally merged MOS-bipolar transistor gain memory cell **501** is formed in a p-type conductivity substrate **502**. An n-type conductivity well **505** is formed in the p-type conductivity substrate **502**. A more heavily doped p-type conductivity region (p+) **507** is formed in a portion of the p-type conductivity substrate **502** and in a portion of the n-type conductivity well **505**. The more heavily doped p-type conductivity region (p+) **507** serves as a source region **507** for a horizontal MOS transistor **509** portion of the horizontally merged MOS-bipolar transistor gain memory cell **501**.

[0029] Another more heavily doped p-type conductivity region (p+) **511** is formed in another portion of the n-type conductivity well **505**. This more heavily doped p-type conductivity region (p+) **511** serves as the drain region **511** for the horizontal MOS transistor **509** portion of the horizontally merged MOS-bipolar transistor gain memory cell **501**. A gate **513** opposes the n-type conductivity well **505** between the source and the drain regions, **507** and **511** respectively. As one of ordinary skill in the art will understand upon reading this disclosure, the n-type conductivity well **505** serves as a body region **505** and, more particularly, as a floating body region **505** for the horizontal MOS transistor **509** portion of the horizontally merged MOS-bipolar transistor gain memory cell **501**. The n-type conductivity well **505** can also be referred to as a floating body n-well **505**.

[0030] The gate **513** is separated from the floating body region **505** by a gate dielectric **515**. As shown in the embodiment of **FIG. 5A**, a read data word line **517** is coupled to the gate **513** along rows of an array. As one of ordinary skill in the art will appreciate upon reading this disclosure, any number of the horizontally merged MOS-bipolar transistor gain memory cell **501** shown in **FIG. 5A** can be arranged in an array on a semiconductor wafer. A read data bit line **519** is coupled to the drain region **511** along columns of such an array.

[0031] As shown in **FIG. 5A**, a horizontal bi-polar transistor **521** completes the horizontally merged MOS-bipolar transistor gain memory cell **501**. The horizontal bi-polar transistor **521** includes an emitter region **523**, a base region **525**, and a collector region **527**. As shown in the embodiment of **FIG. 5A**, the emitter region **523** includes a heavily doped n-type conductivity region **523** (n+) formed in the p-type conductivity substrate **502**. The emitter region can also be referred to as an injector **523**. In **FIG. 5A**, the base region **525** for the horizontal bi-polar transistor **521** portion of the is formed by the p-type conductivity substrate material. In some embodiments, the base region **525** and the p-type conductivity substrate **502** are coupled to a ground potential.

[0032] According to the teachings of the present invention, the collector region **527** for the horizontal bi-polar transistor **521** is formed from a portion of the floating body n-well **505**. In the embodiment shown in **FIG. 5A**, the p+ drain region **511** is formed in the floating body n-well **505** and a portion of the floating body n-well **505** extends and/or wraps around the p+ drain region **511** to a side of the drain region **511** horizontally opposite from the side of the drain region **511** where the gate **513** is located. In this manner, the floating body n-well **505** serves both as a floating body region **505** for the horizontal MOS transistor **509** and a portion of the floating body n-well also serves as the collector region **527** of the horizontal bi-polar transistor **521**.

[0033] As shown in the embodiment of **FIG. 5A**, a write data bit line **529** is coupled to the emitter region **523** for the horizontal bi-polar transistor **521** portion of the horizontally merged MOS-bipolar transistor gain memory cell **501**. The write data bit line **529** can also be referred to as an emitter line **529** and/or an injector line **529**. According to the teachings of the present invention, the horizontal bi-polar transistor **521** is operable to inject a charge on to the floating body **505** of the horizontal MOS transistor **509**. The floating body **505** is operable to store charge by capacitive coupling to the gate **513** and a small stored charge from the same produces a change in the threshold voltage of the horizontal MOS transistor **509**. As one of ordinary skill in the art will appreciate upon reading this disclosure, the horizontally merged MOS-bipolar transistor gain memory cell **501** can be formed or fabricated using planar CMOS processing tech-

niques. As such, the present invention yields a horizontally merged MOS-bipolar transistor gain memory cell **501** which has an area equal to or less than 10 square photolithographic features ($10F^2$).

[**0034**] **FIG. 5B** illustrates a top view of **FIG. 5A** in planar, CMOS technology with shallow trench oxide isolation **531** illustrated alongside the horizontally merged MOS-bipolar transistor gain memory cell **501**. The top view of **FIG. 5A** illustrates the heavily doped p-type conductivity source region **507** (p+). The gate **513** is shown above the floating body region **505** of the horizontal MOS transistor **509** portion of the horizontally merged MOS-bipolar transistor gain memory cell **501**. On the other side of the gate **513** is shown the heavily doped p-type conductivity drain region **511** (p+). The portion of the floating body n-well **505** which serves as the collector region **527** for the horizontal bi-polar transistor **521** is seen from the top view on the opposite side of the drain region **511** from the gate's **513** location. From the top view embodiment of **FIG. 5A**, the p-type conductivity portion of the substrate which serves as the base region **525** for the horizontal bi-polar transistor **521** is viewable adjacent to the collector region **527**. The heavily doped n-type conductivity emitter region, or injector, **523** (n+) is viewable adjacent to the base region **525**. On the other side of the emitter region **523**, another portion of the substrate **502** which serves as the base region **525** for an adjacent horizontal bi-polar transistor **521** portion of a row adjacent horizontally merged MOS-bipolar transistor gain memory cell is viewable as well as another portion of a neighboring floating body n-well.

[**0035**] **FIG. 5C** illustrates an electrical equivalent circuit embodiment of the horizontally merged MOS-bipolar transistor gain memory cell **501** indicating that the floating body well **505** of the horizontal MOS transistor **509** and the floating body well **505** to substrate **502** capacitance acts as a storage capacitor **533**. The embodiment of **FIG. 5C** illustrates the horizontal MOS transistor **509** including the source region **507**, the gate **513** opposing the floating body region **505**, and the drain region **511**. A read data word line **517** is shown coupled to the gate **513** and a read data bit line **519** is coupled to the drain region **511**.

[**0036**] The embodiment of **FIG. 5C** further illustrates the bi-polar transistor **521** including the collector region **527**, which is integrally formed with the floating body region **505**, the base region **525**, and the emitter, or injector, region **523**. As shown in the embodiement of **FIG. 5C**, the emitter region **523** is coupled to a write data bit line, emitter line, or injector line **529**. As shown in the embodiment of **FIG. 5C**, in some embodiments the base region **525** of the bi-polar transistor **521**, which is integrally formed with the substrate **502**, is coupled to a ground potential. And, as indicated above, the floating body well **505** of the horizontal MOS transistor and the floating body well **505** to substrate **502** capacitance acts as a storage capacitor **533**.

[**0037**] In operation, the sense device used to read the horizontally merged MOS-bipolar transistor gain memory cell **501** is the horizontal MOS transistor **509** which is addressed by the read data word line **517**. In the embodiment of a horizontal PMOS transistor **509**, if a negative charge or electrons are stored on the floating body **505**, then the n-type floating body **505** will be slightly forward biased and the horizontal MOS transistor **509** will be more conductive than normal.

[**0038**] According to the teachings of the present invention, charge is injected on to the floating body **505** of the horizontal MOS transistor **509** by the horizontal, or lateral, bi-polar transistor **521**. In the embodiment describe here, the horizontal bi-polar transistor **521** is an npn bi-polar transistor **521**. The horizontal bi-polar transistor **521** need not be a high performance device nor have a high current gain. Accordingly, the horizontal bi-polar transistor **521** can be a high yield structure.

[**0039**] During standby the read data word line **517** is driven positive to drive the floating n-type body **505** to a positive potential by capacitive coupling to the read data word line **517**. This positive potential serves to keep the floating body **505** reverse biased and avoid charge leakage.

[**0040**] The horizontally merged MOS-bipolar transistor gain memory cell **501** can be erased by driving the drain **511** positive and the gate **513** negative to forward bias the drain-body p-n junction (**511-505** junction). (See generally, T. Ohsawa et al., _Memory Design Using One Transistor Gain Cell on SOI,__ *IEEE Int. Solid State Circuits Conv.,* San Francisco, 152-153 (2002); S. Okhonin, M. Nagoga, J. M. Sallese, P. Fazan, _A SOI Capacitor-less 1T-DRAM Cell,__ *Late News* 2001 *IEEE Intl. SOI Conference,* Durango, Colo., 153-154).

[**0041**] The horizontally merged MOS-bipolar transistor gain memory cell **501** can provide a very high gain and amplification of the stored charge on the floating body **505** of the horizontal, or lateral, PMOS sense transistor **509**. A small change in the threshold voltage caused by charge stored on the floating body **505** will result in a large difference in the number of holes conducted between the drain **511** and source of **507** the horizontal PMOS sense transistor **509** during the read data operation.

[**0042**] This amplification allows the small storage capacitance of the sense amplifier floating body **505** to be used instead of a large stacked capacitor storage capacitance. The resulting horizontally merged MOS-bipolar transistor gain memory cell **501** has a very high density with a cell area of approximately 10 F^2, where F is the minimum feature size, and whose vertical extent is far less than the total height of a stacked capacitor or trench capacitor cell and access transistor. The cell can be fabricated without any modification of conventional CMOS logic technology.

[**0043**] While the description here has been given for a p-type substrate an alternative embodiment would work equally well with n-type or silicon-on-insulator substrates. In that case the sense transistor **509** would be an NMOS transistor with a p-type floating body.

System Level

[**0044**] **FIG. 6** is a block diagram of a processor-based system **600** utilizing embedded, horizontally merged MOS-bipolar transistor gain memory cells according to the various embodiments of the present invention. That is, the system **600** utilizes various embodiments of the horizontally merged MOS-bipolar transistor gain memory cell **501** illustrated in **FIGS. 5A-5C**. The processor-based system **600** may be a computer system, a process control system or any other system employing a processor and associated memory. The system **600** includes a central processing unit (CPU) **602**, e.g., a microprocessor, that communicates with the RAM **612** and an I/O device **608** over a bus **620**. It must be noted

that the bus **620** may be a series of buses and bridges commonly used in a processor-based system, but for convenience purposes only, the bus **620** has been illustrated as a single bus. A second I/O device **610** is illustrated, but is not necessary to practice the invention. The processor-based system **600** can further include read-only memory (ROM) **614** and can include peripheral devices such as a floppy disk drive **604** and a compact disk (CD) ROM drive **606** that also communicates with the CPU **602** over the bus **620** as is well known in the art.

[**0045**] It will be appreciated by those skilled in the art that additional circuitry and control signals can be provided, and that the processor-based system **600** has been simplified to help focus on the invention.

[**0046**] It will be understood that the embodiment shown in **FIG. 6** illustrates an embodiment for electronic system circuitry in which the novel embedded, horizontally merged MOS-bipolar transistor gain memory cell **501** of the present invention are used. The illustration of system **600**, as shown in **FIG. 6**, is intended to provide a general understanding of one application for the structure and circuitry of the present invention, and is not intended to serve as a complete description of all the elements and features of an electronic system using the novel horizontally merged MOS-bipolar transistor gain memory cell **501** structures. Further, the invention is equally applicable to any size and type of system **600** using the novel horizontally merged MOS-bipolar transistor gain memory cells of the present invention and is not intended to be limited to that described above. As one of ordinary skill in the art will understand, such an electronic system can be fabricated in single-package processing units, or even on a single semiconductor chip, in order to reduce the communication time between the processor and the memory device.

[**0047**] Applications containing the embedded, horizontally merged MOS-bipolar transistor gain memory cells of the present invention as described in this disclosure include electronic systems for use in memory modules, device drivers, power modules, communication modems, processor modules, and application-specific modules, and may include multilayer, multichip modules. Such circuitry can further be a subcomponent of a variety of electronic systems, such as a clock, a television, a cell phone, a personal computer, an automobile, an industrial control system, an aircraft, and others.

[**0048**] The embedded, horizontally merged MOS-bipolar transistor gain memory cell of the present invention can provide a very high gain and amplification of a stored charge on the floating body of the horizontal MOS sense transistor. A small change in the threshold voltage caused by charge stored on the floating body will result in a large difference in the number of holes conducted between the drain and source of the horizontal MOS sense transistor during the read data operation. This amplification allows the small storage capacitance of the sense amplifier floating body to be used instead of a large stacked capacitor storage capacitance. The resulting cell has a very high density with a cell area of 10 F^2, where F is the minimum feature size, and whose horizontal extent is far less than the total height of a stacked capacitor or trench capacitor cell and access transistor.

[**0049**] It is to be understood that the above description is intended to be illustrative, and not restrictive. Many other embodiments will be apparent to those of skill in the art upon reviewing the above description. The scope of the invention should, therefore, be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.

What is claimed is:

1. A memory cell, comprising:

a bipolar transistor having an emitter region, a base region and a collector region;

a MOS transistor including a first source/drain region and a second source/drain region with a body region therebetween; and

wherein the collector region of the bipolar transistor serves as the body region of the MOS transistor.

2. The memory cell of claim 1, wherein the MOS transistor includes a P-channel MOS transistor.

3. The memory cell of claim 1, wherein the MOS transistor includes an N-channel MOS transistor.

4. The memory cell of claim 1, wherein the memory cell has an area equal to or less than 10 square photolithographic features.

5. The memory cell of claim 1, wherein the MOS transistor includes a horizontal MOS transistor.

6. A memory cell, comprising:

a bipolar transistor having an emitter region, a base region and a collector region;

a MOS transistor including a first source/drain region and a second source/drain region with a floating body region therebetween; and

wherein the collector region of the bipolar transistor is integrated with the floating body region of the MOS transistor.

7. The memory cell of claim 6, wherein the memory cell has an area equal to or less than 10 square photolithographic features.

8. The memory cell of claim 6, wherein the MOS transistor includes a horizontal MOS transistor.

9. The memory cell of claim 6, wherein the bipolar transistor includes a horizontal bipolar transistor.

10. A memory cell, comprising:

a bipolar transistor having an emitter region, a base region and a collector region;

a MOS transistor including a first source/drain region and a second source/drain region with a body region therebetween;

wherein the collector region of the bipolar transistor serves as the body region of the MOS transistor; and

wherein the second source/drain region is formed within the collector region of the bipolar transistor.

11. The memory cell of claim 10, wherein the body region includes a floating body region.

12. The memory cell of claim 10, wherein the MOS transistor includes a P-channel MOS transistor.

13. The memory cell of claim 10, wherein the MOS transistor includes an N-channel MOS transistor.

14. The memory cell of claim 10, wherein a write data line is coupled to an emitter of the bipolar transistor, and a read data line is coupled to the second source/drain region.

15. The memory cell of claim 10, wherein the collector region extends around the second source/drain region to a location horizontrally opposite from a side of the second source/drain region where the body region is located.

16. A memory array, comprising:

an array of memory cells, including:

a bipolar transistor having an emitter region, a base region and a collector region;

a MOS transistor including a first source/drain region and a second source/drain region with a body region therebetween;

wherein the collector region of the bipolar transistor serves as the body region of the MOS transistor; and

data reading and writing circuitry coupled to the array of memory cells.

17. The memory array of claim 16, wherein the body region includes a floating body region.

18. The memory array of claim 16, wherein the second source/drain region is formed within the collector region of the bipolar transistor.

19. The memory array of claim 16, wherein the collector region extends around the second source/drain region to a location horizontrally opposite from a side of the second source/drain region where the body region is located.

20. An electronic system, comprising:

a memory device with a number of memory cells, the memory cells including:

a bipolar transistor having an emitter region, a base region and a collector region;

a MOS transistor including a first source/drain region and a second source/drain region with a body region therebetween;

wherein the collector region of the bipolar transistor serves as the body region of the MOS transistor; and

a logic device coupled to the memory device to manipulate data.

21. The electronic system of claim 20, wherein the memory device and logic device are located on the same chip.

22. The electronic system of claim 20, wherein the memory device includes a dynamic random access memory device.

23. The electronic system of claim 20, wherein the logic device includes a processor chip.

24. The electronic system of claim 20, wherein the body region includes a floating body region.

25. The electronic system of claim 20, wherein the second source/drain region is formed within the collector region of the bipolar transistor.

26. A method of operating a memory cell, comprising:

operating a bipolar transistor to provide a charge at a collector wherein the collector also serves as a floating body region of a MOS transistor;

modulating a threshold voltage of the MOS transistor in response to the charge; and

operating a gate of the MOS transistor and detecting a signal in proportion to the modulated threshold voltage.

27. The method of claim 26, wherein the method includes storing a first state on the floating body region, wherein storing a first state on the floating body region includes forward biasing the floating body region.

28. The method of claim 26, wherein the method further includes providing a standby state, wherein the standby state includes;

applying a positive potential to the gate of the MOS transistor; and

driving the floating body region to a positive potential by capacitive coupling with the gate to keep the floating body region reverse biased.

29. The method of claim 26, wherein method includes storing a second state on the floating body, wherein storing a second state on the floating body includes;

applying a positive potential to a drain region of the MOS transistor; and

applying a negative potential to the gate of the MOS transistor to forward bias a drain-floating body region junction.

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