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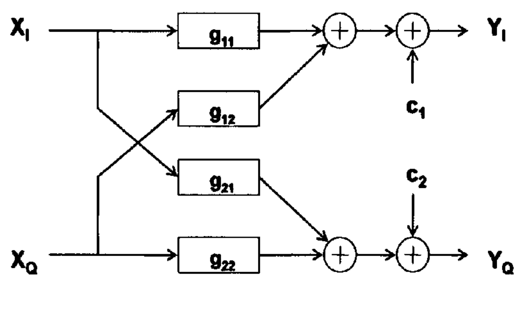

Figure 9 Analog Quadrature Modulator Compensation Block

(57) **Abstract**: A RF-digital hybrid mode power amplifier system for achieving high efficiency and high linearity in wideband communication systems is disclosed. The present invention is based on the method of adaptive digital predistortion to linearize a power amplifier in the RF domain. The present disclosure enables a power amplifier system to be field reconfigurable and support multi-modulation schemes (modulation agnostic), multi-carriers and multi-channels. As a result, the digital hybrid mode power amplifier system is particularly suitable for wireless transmission systems, such as base-stations, repeaters, and indoor signal coverage systems, where baseband I-Q signal information is not readily available.

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MODULATION AGNOSTIC DIGITAL HYBRID MODE POWER AMPLIFIER SYSTEM AND METHOD

SPECIFICATION

RELATED APPLICATIONS

[001] This application claims the benefit of the following applications:

US Patent Appn SN 12/415,676, filed 3/31/2009, and through it U.S. Patent Appn SN 61/041,164, filed 3/31/2008; which also claims the benefit of U.S. Provisional Patent Application S.N. 61/172,642, filed 4/24/2009;

US Patent Application SN 12/603,419, filed 10/21/2009, and through it US Patent Application SN 12/108,507, filed 4/23/2008, and through it U.S. Patent Application SN 60/925,577, filed 4/23/2007;

US Patent Application SN 12/330,451 filed 12/8/2008, and through it US Patent Application SN 61/012,416, filed 12/07/2007;

US Patent Application SN 11/961,969, filed 12/20/2007, and through it US Patent Application SN 60/877,035, filed 12/26/2006, and US Patent Application SN 60/925,603, filed 4/23/2007;

US Patent Application SN 12/108,502, filed 4/23/2008, and through it US Patent Application SN 12/021,241, filed 1/28/2008, and through that to US Patent Application SN 60/897,746, filed 1/26/2007.

US Patent Application S.N. 61/288,838, filed 12/21/2009, entitled MULTI-BAND WIDEBAND POWER AMPLIFIER DIGITAL PREDISTORTION SYSTEM AND

METHOD and naming as inventors Wan-Jong Kim, Kyoung-Joon Cho, and Shawn Patrick Stapleton.

US Patent Application S.N. 61/288,840, filed 12/21/2009, entitled REMOTE RADIO HEAD UNIT SYSTEM WITH WIDEBAND POWER AMPLIFIER AND METHOD and naming as inventors Chengxun Wang and Shawn Patrick Stapleton.

US Patent Application S.N. 61/288,844, filed 12/21/2009, entitled MODULATION AGNOSTIC DIGITAL HYBRID MODE POWER AMPLIFIER SYSTEM AND METHOD and naming as inventors Wan-Jong Kim, Kyoung-Joon Cho, Shawn Patrick Stapleton, Ying Xiao.

US Patent Application S.N. 61/288,847, filed 12/21/2009, entitled HIGH EFFICIENCY, REMOTELY RECONFIGURABLE REMOTE RADIO HEAD UNIT SYSTEM AND METHOD FOR WIRELESS COMMUNICATIONS and naming as inventors Wan-Jong Kim, Kyoung-Joon Cho, and Shawn Patrick Stapleton, and Ying Xiao.

All of the foregoing are incorporated herein by reference for all purposes.

FIELD OF THE INVENTION

[002] The present invention generally relates to wireless communication systems using complex modulation techniques. More specifically, the present invention relates to power amplifier systems for wireless communications.

BACKGROUND OF THE INVENTION

[003] A wideband mobile communication system using complex modulation techniques, such as wideband code division multiple access (WCDMA) and orthogonal frequency division multiplexing (OFDM), has large peak-to-average power ratio (PAPR) specifications and hence requires highly linear power amplifiers for its RF transmissions. The conventional feedforward linear power amplifier (FFLPA) has been widely utilized due to its excellent linearity performance in spite of poor power efficiency.

[004] Conventional FFLPAs are mainly based on the principle of error subtraction and power-matching with dedicated hardware circuitries to realize non-linear corrections to PA. These approaches must use an auxiliary PA and complicated hardware circuitries to match exactly the transmitted power-balance, time-delay and errors generated by the main PA. After a perfect matching is obtained, the non-linear distortion errors from the main PA can then be canceled by those distortion errors from the auxiliary PA. Due to the complexities of the nonlinear predistortion circuits, which among other things involve many variables and parameters, FFLPAs require significant fine tuning and other calibration efforts. In addition, such traditional FFLPA schemes are also vulnerable to fluctuating environmental conditions, such as temperature and humidity changes, since perfect alignment of the main PA's signal and that of the auxiliary PA are vital. As a result, traditional predistortion schemes are costly to implement and are limited in their predistortion accuracy and stability in a commercial wireless system environment.

[005] In order to overcome the FFLPA's poor efficiency, digital baseband predistortion (PD) has been demonstrated due to the recent advances in digital signal processing (DSP) technology. In addition, Doherty power amplifiers (DPA) have also been applied to these linearization systems to improve power efficiency. However, there is still a demand for higher performance of the power amplifier such as more linearity and better efficiency with less expensive architecture.

[006] Conventional DSP-based PD schemes utilize digital microprocessors to compute, calculate and correct the PA's nonlinearities, typically by performing fast tracking and adjustments of signals in the PA system. However, conventional DSP-based PD schemes are challenged by variations of the linearity performance of the amplifier due to changes in the environment such as temperature and the asymmetric distortions of the output signal of the PA resulting from memory effects. All of these variations and distortions have to be compensated for. Conventional PD algorithms are based on a wideband feedback signal, and require a high speed analog-to-digital converter (ADC) in order to capture the necessary information. In addition, time-synchronizations are typically required to capture an error signal between a reference signal and a distorted signal. This time-matching process may result in small

synchronization errors which can further affect conventional PD schemes' linearization performance. Amplitude and phase synchronization is also required in order to align the reference signal and the distorted signal.

[007] Moreover, conventional PD schemes necessitate coded in-phase (I) and quadrature (Q) channel signals in the baseband as the required ideal or reference signals. As a result, conventional PD schemes are often standard or modulation specific and must be closely tailored to each baseband system. Therefore, in order to deploy conventional PD schemes into base-stations, the PD engines must be embedded into the baseband architecture of base-stations. This embedment is a practical implementation challenge since it is frequently inconvenient or impossible to modify the baseband architectures of existing base-stations or base-station designs. Once the PD scheme is set up for a specific base-station design, it is often not reconfigurable and hence not upgradeable to future changes in standards or modulations. Furthermore, since traditional PD approaches require baseband I-Q signal sources to operate, they are inapplicable to certain RF systems that do not possess any baseband I-Q signal sources, such as repeater and indoor signal coverage sub-systems.

SUMMARY OF THE INVENTION

[008] Accordingly, the present invention has been made in view of the above problems, and it is an object of the present invention to provide a high performance and cost effective method of power amplifier systems with high linearity and high efficiency for wideband communication system applications. The present disclosure provides a field-reconfigurable power amplifier system that supports multi-modulation schemes (modulation agnostic), multi-carriers and multi-channels. In multi-channel configurations of the present invention there can be more than one PA for multiple bands.

[009] To achieve the above objects, the present invention is generally based on the method of adaptive digital predistortion to linearize a power amplifier in the RF domain. Various embodiments of the invention are disclosed. In an embodiment, the combination of crest factor reduction, PD, power efficiency boosting techniques as well as coefficient adaptive algorithms are utilized within a PA system. In another embodiment, analog quadrature modulator compensation structure is also utilized to enhance performance.

[0010] Some embodiments of the present invention are able to monitor the fluctuation of the power amplifier characteristics and to self-adjust by means of a self-adaptation algorithm. One such self-adaptation algorithm presently disclosed is called a digital predistortion algorithm, which is implemented in the digital domain.

[0011] Applications of the present invention are suitable for use with all wireless base-stations, access points, mobile equipment and wireless terminals, portable wireless devices, and other wireless communication systems such as microwave and satellite communications.

[0012] A RF-digital hybrid mode power amplifier system for achieving high efficiency and high linearity in wideband communication systems is disclosed. The present invention is based on the method of adaptive digital predistortion to linearize a power amplifier in the RF domain. The power amplifier characteristics such as variation of linearity and asymmetric distortion of the amplifier output signal are sampled in a feedback path and controlled by the adaptation algorithm in a digital module. Therefore, in an embodiment, the present invention is capable of compensating for the nonlinearities as well as memory effects of power amplifier systems and also improves performance, in terms of power added efficiency, adjacent channel leakage ratio (ACLR) and peak-to-average power ratio. The present disclosure enables a power amplifier system to be field reconfigurable and support multi-modulation schemes (modulation agnostic), multi-carriers and multi-channels. As a result, the digital hybrid mode power amplifier system is particularly suitable for wireless transmission systems, such as base-stations, repeaters, and indoor signal coverage systems, where baseband I-Q signal information is not readily available.

THE FIGURES

[0013] Further objects and advantages of the present invention can be more fully understood from the following detailed description taken in conjunction with the accompanying drawings in which:

[0014] Figure 1 is a block diagram showing the basic form of a digital hybrid mode power amplifier system.

[0015] Figure 2 is a block diagram showing a simple digital predistortion block diagram for a power amplifier system according to one embodiment of the present invention.

[0016] Figure 3 is a block diagram showing polynomial-based predistortion in a digital hybrid mode power amplifier system of the present invention.

[0017] Figure 4 is a block diagram of the digital predistortion algorithm applied for self-adaptation in a digital hybrid mode power amplifier system of the present invention.

[0018] Figure 5 is a delay estimation block diagram of the present invention.

[0019] Figure 6 is a block diagram of a fractional delay for the present invention.

[0020] Figure 7 is a block diagram showing a digital hybrid mode power amplifier system implemented with a down converter (DNC) and UPC-based clipping error restoration path according to another embodiment of the present invention..

[0021] Figure 8 is a block diagram showing a digital hybrid mode power amplifier system implemented with a DNC and an analog quadrature modulator (AQM) according to another embodiment of the present invention.

[0022] Figure 9 is a block diagram showing an embodiment of the analog quadrature modulator compensation structure.

GLOSSARY

[0023] The acronyms used herein have the following meanings:

ACLR	Adjacent Channel Leakage Ratio
ACPR	Adjacent Channel Power Ratio

ADC	Analog to Digital Converter
AQDM	Analog Quadrature Demodulator
AQM	Analog Quadrature Modulator
AQDMC	Analog Quadrature Demodulator Corrector
AQMC	Analog Quadrature Modulator Corrector
BPF	Bandpass Filter
CDMA	Code Division Multiple Access
CFR	Crest Factor Reduction
DAC	Digital to Analog Converter
DET	Detector
DHMPA	Digital Hybrid Mode Power Amplifier
DDC	Digital Down Converter
DNC	Down Converter
DPA	Doherty Power Amplifier
DQDM	Digital Quadrature Demodulator
DQM	Digital Quadrature Modulator
DSP	Digital Signal Processing
DUC	Digital Up Converter
EER	Envelope Elimination and Restoration
EF	Envelope Following
ET	Envelope Tracking
EVM	Error Vector Magnitude
FFLPA	Feedforward Linear Power Amplifier
FIR	Finite Impulse Response
FPGA	Field-Programmable Gate Array

GSM	Global System for Mobile communications
I-Q	In-phase / Quadrature
IF	Intermediate Frequency
LINC	Linear Amplification using Nonlinear Components
LO	Local Oscillator
LPF	Low Pass Filter
MCPA	Multi-Carrier Power Amplifier
MDS	Multi-Directional Search
OFDM	Orthogonal Frequency Division Multiplexing
PA	Power Amplifier
PAPR	Peak-to-Average Power Ratio
PD	Digital Baseband Predistortion
PLL	Phase Locked Loop
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
SAW	Surface Acoustic Wave Filter
UMTS	Universal Mobile Telecommunications System
UPC	Up Converter
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network

DETAILED DESCRIPTION OF THE INVENTION

[0024] The present invention is a novel RF-out PA system that utilizes an adaptive digital predistortion algorithm. The present invention is a hybrid system of digital and analog modules. The interplay of the digital and analog modules of the hybrid system both linearize the spectral regrowth and enhance the power efficiency of the PA while maintaining or increasing the wide bandwidth. The present invention, therefore, achieves higher efficiency and higher linearity for wideband complex modulation carriers.

[0025] Figure 1 is a high level block diagram showing the basic system architecture which can be thought of, at least for some embodiments, as comprising digital and analog modules and a feedback path. The digital module is the digital predistortion controller 101 which comprises the PD algorithm, other auxiliary DSP algorithms, and related digital circuitries. The analog module is the main power amplifier 102, other auxiliary analog circuitries such as DPA, and related peripheral analog circuitries of the overall system. The present invention is a "black box", plug-and-play type system because it accepts RF modulated signal 100 as its input, and provides a substantially identical but amplified RF signal 103 as its output, therefore, it is RF-in/RF-out. Baseband input signals can be applied directly to the Digital Predistorter Controller according to one embodiment of the present invention. An Optical input signal can be applied directly to the Digital Predistorter Controller according to one embodiment of the present invention. The feedback path essentially provides a representation of the output signal to the predistortion controller 101. The present invention is sometimes referred to as a digital hybrid mode power amplifier (DHMPA) system hereinafter.

[0026] Digital Predistorter Algorithm

[0027] Digital Predistortion (DPD) is a technique to linearize a power amplifier (PA). Figure 2 shows in block diagram form an embodiment of a linear digitally predistorted PA. In the DPD block, a memory polynomial model is used as the predistortion function (Figure 3), and complies with the formula:

$$z(n) = \sum_{i=0}^{n-1} x_i(n-i)\left(\sum_{j=0}^{k-1} a_{ij}\left|x_i(n-i)\right|^j\right)$$

where a_{ij} are the DPD coefficients.

[0028] In the DPD estimator block, a least square algorithm is utilized to find the DPD coefficients, and then transfer them to DPD block. The detailed DPD algorithm is shown in Figure 4.

[0029] Figure 3 is a block diagram showing a predistortion (PD) part in the DHMPA system of the present invention. The PD in the present invention generally utilizes an adaptive polynomial-based digital predistortion system. Another embodiment of the PD utilizes a LUT-based digital predistortion system. More specifically, the PD illustrated in FIG. 3 and in embodiments disclosed in FIG. 7 and FIG. 8, discussed below, are processed in the digital processor by an adaptive algorithm, presented in U.S. Patent application S.N. 11/961,969, entitled A Method for Baseband Predistortion Linearization in Multi-Channel Wideband Communication Systems. The PD for the DHMPA system in FIG. 3 has multiple finite impulse response (FIR) filters, that is, FIR1 301, FIR2 303, FIR3 305, and FIR4 307. The PD also contains the third order product generation block 302, the fifth order product generation block 304, and the seventh order product generation block 306. The output signals from FIR filters are combined in the summation block 308. Coefficients for multiple FIR filters are updated by the digital predistortion algorithm.

[0030] Delay Estimation Algorithm:

[0031] The DPD estimator compares x(n) and its corresponding feedback signal y(n-Δd) to find the DPD coefficients, where Δd is the delay of the feedback path. As the feedback path delay is different for each PA, this delay should be identified before the signal arrives at the coefficient estimation. In this design, the amplitude difference correlation function of the transmission, x(n), and feedback data, y(n), is applied to find the feedback path delay. The correlation is given by

$$C(m) = \sum_{i=0}^{N-1} sign\big(x(i+1) - x(i)\big) sign\big(y(i+m+1) - y(i+m)\big)$$

$$n(delay) = Max(C(m))$$

The delay n that maximizes the correlation $C(m)$ is the feedback path delay. The delay estimation block is shown in Figure 5.

[0032] Since the feedback path goes through analog circuitry, the delay between the transmission and feedback path could be a fractional sample delay. To synchronize the signals more accurately, fractional delay estimation is necessary. To simplify the design, only a half-sample delay is considered in this design, as shown in Figure 6. It will be appreciated that smaller fractional delays can also be utilized in at least some embodiments.

[0033] To get the half-sample delay data, an upsampling approach is the common choice, but in this design, in order to avoid a very high sampling frequency in the FPGA, an interpolation method is used to get the half-sample delay data. The data with integer delay and fractional delay are transferred in parallel. The interpolation function for fractional delay is

$$y(n) = \sum_{i=0}^{3} c_i x(n+i)$$

in which c_i is the weight coefficient.

[0034] Whether the fractional delay path or the integer delay path will be chosen is decided by the result of the amplitude difference correlator. If the correlation result is odd, the integer path will be chosen, otherwise the fractional delay path will be chosen.

[0035] **Phase offset Estimation and Correction Algorithm**:

[0036] Phase offset between the transmission signal and the feedback signal exists in the circuit. For a better and faster convergence of the DPD coefficient estimation, this phase offset should be removed.

[0037] The transmission signal x(n) and feedback signal y(n) can be expressed as

$$x(n) = |x(n)|e^{j\theta_x} \quad \text{and} \quad y(n) = |y(n)|e^{j\theta_y},$$

The phase offset $e^{j(\theta_x-\theta_y)}$ can be calculated through

$$e^{j(\theta_x-\theta_y)} = \frac{x(n)y(n)^*}{|x(n)||y(n)|}$$

So, the phase offset between the transmission and feedback paths is

$$e^{j\theta o,} = \text{mean}\left(\frac{x(n)y(n)^*}{|x(n)||y(n)|}\right)$$

The feedback signal with the phase offset removed can be calculated by

$$\bar{y}(n) = y(n)e^{j\theta o}$$

[0038] **Magnitude correction:**

[0039] As the gain of the PA may change slightly, the feedback gain should be corrected to avoid the error from the gain mismatch. The feedback signal is corrected according to the function

$$\bar{y}(n) = y(n)\frac{\sum_{i=1}^{N}|x(i)|}{\sum_{i=1}^{N}|y(i)|}$$

In this design, N is chosen to be 4096. The choice of N will depend on the desired accuracy.

[0040] **QR_RLS Adaptive Algorithm:**

[0041] The least square solution for DPD coefficient estimation is formulated as

$$F(x(n)) = y(n)$$

$$F(x(n)) = \sum_{i=1}^{N}\sum_{j=0}^{K} a_{ij}x(n-i)|x(n-i)|^j$$

Define $h_k = x(n-i)|x(n-i)|^j$, $w_k = a_{ij}$, where $k = (i-1)N + j$. The least square formulation can be expressed as:

$$\sum_{k=1}^{N\times K} w_k h_k = y(n)$$

In this design, QR-RLS algorithm (Haykin, 1996) is implemented to solve this problem. The formulas of QR_RLS algorithm are

$$\begin{cases} d(i) \triangleq y(i) - h_i\bar{w} \\ \bar{w}_i \triangleq w_i - \bar{w} \\ q_i \triangleq \phi_i^{*/2}[w_i - \bar{w}] \end{cases}$$

where ϕ_i is a diagonal matrix, and q_i is a vector.

The QR_RLS algorithm gets the ith moment ϕ_i and q_i from its $(i-1)$th moment through a unitary transformation:

$$A = \begin{bmatrix} \phi_i^{1/2} & 0 \\ q_i^* & e_a^*(i)\,\gamma^{\frac{1}{2}}(i) \\ h_i\,\Phi_i^{-\frac{*}{2}} & \gamma^{\frac{1}{2}}(i) \end{bmatrix} = \begin{bmatrix} \lambda^{1/2}\phi_{i-1}^{*/2} & h_i^* \\ \lambda^{1/2} q_{i-1}^* & d(i)^* \\ 0 & 1 \end{bmatrix} \theta_i$$

θ_i is a unitary matrix for unitary transformation.

[0042] To apply QR_RLS algorithm more efficiently in FPGA, a squared-root-free Givens rotation is applied for the unitary transformation process (E.N. Frantzeskakis, 1994)

$$\begin{bmatrix} a_1 & a_2 & \cdots & a_n \\ b_1 & b_2 & \cdots & b_n \end{bmatrix} = \begin{bmatrix} \sqrt{k_a} & 0 \\ 0 & \sqrt{k_b} \end{bmatrix} \begin{bmatrix} a_1' & a_2' & \cdots & a_n' \\ b_1' & b_2' & \cdots & b_n' \end{bmatrix}$$

$$\begin{bmatrix} a_1' & a_2' & \cdots & a_n' \\ b_1' & b_2' & \cdots & b_n' \end{bmatrix} \theta = \begin{bmatrix} \sqrt{k_a'} & 0 \\ 0 & \sqrt{k_b'} \end{bmatrix} \begin{bmatrix} 1 & a_2'' & \cdots & a_n'' \\ 0 & b_2'' & \cdots & b_n'' \end{bmatrix}$$

$$k_a' = k_a a_1^2 + k_b b_1^2$$

$$k_b' = {k_a k_b}/{k_a'}$$

$$a_j' = (k_a a_1 a_j + k_b b_1 b_j)/k_a'$$

$$b_j' = -b_1 a_j + a_1 b_j$$

[0043] For RLS algorithm, the ith moment is achieved as below:

$$\begin{bmatrix} \lambda^{1/2}\phi_{i-1}^{*/2} & h_i^* \\ \lambda^{1/2} q_{i-1}^* & \overline{d(i)^*} \\ 0 & 1 \end{bmatrix} \theta_i = \begin{bmatrix} \overline{\phi_i^{1/2}} & 0 \\ \overline{q_i^*} & \overline{e_a^*(i)\,\gamma^{\frac{1}{2}}(i)} \\ \overline{h_i\,\Phi_i^{-\frac{*}{2}}} & \overline{\gamma^{\frac{1}{2}}(i)} \end{bmatrix} \begin{bmatrix} \sqrt{k_a} & 0 \\ 0 & \sqrt{k_b} \end{bmatrix}$$

w_i can be obtained by solving

$$\overline{\Phi^{\frac{*}{2}}}[w_i - \bar{w}] = \bar{q}_i$$

[0044] In the iterative process, a block of data (in this design, there are 4096 data in one block) is stored in memory, and the algorithm uses all the data in memory to estimate the DPD coefficient. In order to make the DPD performance more stable, the DPD coefficients are only updated after one block of data is processed. The matrix A will be used for the next iteration process, which will make the convergence faster.

[0045] To make sure the performance of the DPD is stable, a weighting factor f is used when updating the DPD coefficients as

$$w_i = f \times w_{i-1} + (1 - f)w_i$$

[0046] The DPD coefficient estimator calculates coefficients w_i by using QR_RLS algorithm. These w_i are copied to the DPD block to linearize the PA.

[0047] Figures 7 and 8 are block diagrams showing more sophisticated embodiments of DHMPA system, where like elements are indicated with like numerals and elements not numbered in Figure 8 have the same reference numerals as shown in Figure 7. The embodiments of Figures 7 and 8 apply crest factor reduction (CFR) prior to the PD with an adaptation algorithm in one digital processor, so as to reduce the PAPR, EVM and ACPR and compensate the memory effects and variation of the linearity due to the temperature changing of the PA. The digital processor can take nearly any form; for convenience, an FPGA implementation is shown as an example, but a general purpose processor is also acceptable in many embodiments. The CFR implemented in the digital module of the embodiments is based on the scaled iterative pulse cancellation presented in patent application US61/041,164, filed March 31, 2008, entitled An Efficient Peak Cancellation Method For Reducing The Peak-To-Average Power Ratio In Wideband Communication Systems, incorporated herein by reference. The CFR is included to enhance performance and hence optional. The CFR can be removed from the embodiments without affecting the overall functionality.

[0048] Figure 7 is a block diagram showing a DHMPA system implemented with DQM in accordance with an embodiment of the present invention. The system shown in Figure 7 has a dual mode of RF-in 700 and/or multi-carrier digital signal 705 at the input, and an RF signal at the output 710. The dual mode of signal input allows maximum flexibility: RF-in (the “RF-in Mode”) or baseband digital-in (the “Baseband-in Mode”). The system shown in Figure 7 comprises three key portions:

a reconfigurable digital (hereinafter referred as "FPGA-based Digital") module 715, a power amplifier module 760 and a feedback path 725.

[0049] The FPGA-based Digital part comprises a digital processor 715 (e.g. FPGA), digital-to-analog converters 735 (DACs), analog-to-digital converters 740 (ADCs), and a phase-locked loop (PLL) 745. Since the embodiment of Figure 7 has a dual input mode, the digital processor has two paths of signal processing. For the RF signal input path, the digital processor has implemented a digital quadrature demodulator (DQDM), a CFR, a PD, and a digital quadrature modulator (DQM). For the baseband digital input path, a digital up-converter (DUC), CFR, PD, and a DQM are implemented.

[0050] The RF-in Mode of the embodiment shown in Figure 7 has implemented a down converter (DNC) 750 prior to the FPGA-based Digital part and an ADC 740 prior to the FPGA. An analog down converted signal is provided to the FPGA-based Digital module and converted to a digital signal by the ADC 740. The digitally converted signal is demodulated by the DQDM to generate both real and imaginary signals and then PAPR of the signal is reduced by CFR. The peak reduced signal is predistorted to linearize the amplifier and is passed through a DQM to generate the real signal and then converted to an intermediate frequency (IF) analog signal by a DAC in the FPGA-based Digital part. However, it is not required in all embodiments to implement DQDM and DQM in the FPGA. If, as shown in Figures 7 and 8, a digital modulator will not be used, then two DAC's 801 behind the FPGA feeding AQM module 800 can be used to generate real and imaginary signals, respectively (the "AQM Implementation").

[0051] The Baseband-in Mode of the system of Figure 7 works slightly differently from the RF-in Mode. Digital data streams from multi-channels as I-Q signals are coming to the FPGA-based Digital module and are digitally up-converted to digital IF signals by the DUC. From this point onwards, the Baseband-in Mode and RF-in Mode proceeds identically. These IF signals are then passed through the CFR block so as to reduce the signal's PAPR. This PAPR suppressed signal is digitally predistorted in order to pre-compensate for nonlinear distortions of the power amplifier.

[0052] In either input mode, the memory effects due to self-heating, bias networks, and frequency dependencies of the active device are compensated by the adaptation algorithm in the PD, as well. The coefficients of the PD are adapted by a synchronizing the wideband captured output signal from the feedback path 725 with the reference signal. The digital predistortion algorithm performs the synchronization and compensation. . The predistorted signal is passed through a DQM in order to generate the real signal and then converted to an IF analog signal by the DAC 740 as shown. As disclosed above, the DQM is not required to be implemented in the FPGA, or at all, in all embodiments. Alternatively, if the DQM is not used in the FPGA, then the AQM Implementation can be implemented with two DACs to generate real and imaginary signals, respectively. The gate bias voltage 753 of the power amplifier is determined by the adaptation algorithm and then adjusted through the DACs 535 in order to stabilize the linearity fluctuations due to the temperature changes in the power amplifier. .

[0053] The power amplifier part comprises a UPC for a real signal (such as illustrated in the embodiment shown in Figures 7), or an AQM for real and complex signals (such as the embodiment of a DHMPA system depicted in Figure 8) from the FPGA-based Digital module, a high power amplifier with multi-stage drive amplifiers, and a temperature sensor. In order to improve the efficiency performance of the DHMPA system, efficiency boosting techniques such as Doherty, Envelope Elimination and Restoration (EER), Envelope Tracking (ET), Envelope Following (EF), and Linear amplification using Nonlinear Components (LINC) can be used, depending upon the embodiment. These power efficiency techniques can be mixed and matched and are optional features to the fundamental DHMPA system. One such Doherty power amplifier technique is presented in commonly assigned U.S. Provisional Patent Application S.N. 60/925,577, filed April 23, 2007, entitled N-Way Doherty Distributed Power Amplifier, incorporated herein by reference, together with U.S. Patent Application S.N. 12/603,419, filed 10/21/2009, entitled N-Way Doherty Distributed Power Amplifier with Power Tracking. To stabilize the linearity performance of the amplifier, the temperature of the amplifier is monitored by the temperature sensor and then the gate bias of the amplifier is controlled by the FPGA-based Digital part.

[0054] The feedback portion comprises a directional coupler, a mixer, a gain amplifier, a band pass filter (BPF), and a Digital to Analog Converter (DAC). Depending upon the embodiment, these analog components can be mixed and matched with other analog components. Part of the RF output signal of the amplifier is sampled by the directional coupler and then down converted to an IF analog signal by the local oscillation signal in the mixer. The IF analog signal is passing through the the gain amplifier, and the BPF (e.g., surface acoustic wave filter) which can capture the out-of-band distortions. The output of the BPF is provided to the ADC of the FPGA-based Digital module in order to determine the dynamic parameters of the digital PD depending on output power levels and asymmetrical distortions due to the memory effects. In addition, temperature is also detected by the detector 580 to calculate the variation of linearity and then adjust gate bias voltage of the PA. More details of the PD algorithm and self-adaptation feedback algorithm can be appreciated from Figure 3, discussed above, which shows a polynomial-based predistortion algorithm and from Figure 4, also discussed above, which shows the block diagram of the digital predistorter synchronization algorithm which can be used in some embodiments of the invention.

[0055] In the case of a strict EVM requirement for broadband wireless access such as WiMAX or other OFDM based schemes (EVM < 2.5%), the CFR in the FPGA-based Digital part is only able to achieve a small reduction of the PAPR in order to meet the strict EVM specification. In general circumstances, this means the CFR's power efficiency enhancement capability is limited. In some embodiments of the present invention, a novel technique is included to compensate the in-band distortions from CFR by use of a "Clipping Error Restoration Path" 790, hence maximizing the DHMPA system power efficiency in those strict EVM environments. As noted above, the Clipping Error Restoration Path has an additional DAC 735 in the FPGA-based Digital portion and an extra UPC 720 in the power amplifier part (see Figures 7 and 8). The Clipping Error Restoration Path can allow compensation of in-band distortions resulting from the CFR at the output of the power amplifier.

Further, any delay mismatch between the main path and the Clipping Error Restoration Path can be aligned using digital delay in the FPGA.

[0056] Referring again to Figure 7, the RF input signal is first down-converted to baseband digital signals, and then digitally up-converted to digital IF signals (-7.5 MHz, -2.5 MHz, 2.5 MHz, 7.5 MHz). If the system of Figure 7 has a Baseband-in Mode, then the digital data streams from multi-channels are digitally up-converted to digital IF signals (-7.5 MHz, -2.5 MHz, 2.5 MHz, 7.5 MHz) directly as they enter the digital processor. The CFR then reduces the PAPR. The peak-reduced signal is predistorted to linearize the DPA and is passing through two DACs for real and imaginary signals and finally through an AQM.

[0057] FIG. 9. is a block diagram showing an embodiment of the analog quadrature modulator compensation structure. The input signal is separated into an in-phase component X_I and a quadrature component X_Q. The analog quadrature modulator compensation structure comprises four real filters {g11, g12, g21, g22} and two DC offset compensation parameters c1, c2. The DC offsets in the AQM will be compensated by the parameters c1, c2. The frequency dependence of the AQM will be compensated by the filters {g11, g12, g21, g22}. The order of the real filters is dependent on the level of compensation required. The output signals YI and YQ will be presented to the AQM's in-phase and quadrature ports.

[0058] The configuration of the power amplifier part and the feedback part of the system shown in Figure 8 are the same as for the system shown in FIG. 7.

[0059] In the system shown in Figure 8, the DNC frequency translates the RF signal into a low IF signal. The IF signal is then presented to the ADC whereupon it is digitally down-converted to baseband followed by CFR and predistortion (PD). The output of the PD is a baseband signal which will then be digitally upconverted to an IF frequency and presented to the DAC. The output of the DAC is then further frequency translated to a RF frequency through the up-converter (UPC.) The configuration of the power amplifier part and the feedback part of system of Figure 8 are the same as for the FIG. 7 System.

[0060] In summary, the DHMPA system of the present invention enhances efficiency and linearity relative to the prior art since the DHMPA system is able to implement CFR, DPD and adaptation algorithms in one digital processor, which consequently saves hardware resources and processing time. The DHMPA system is also reconfigurable and field-programmable since the algorithms and power-efficiency-enhancing features can be adjusted like software in the digital processor at anytime.

[0061] Furthermore, since the DHMPA system accepts RF modulated signal as input, it is not necessary to use coded I and Q channel signals in the baseband. Therefore, the performance of wireless base-station systems can be enhanced simply by replacing the existing PA modules with the DHMPA. The result is that the present invention provides a "plug and play" PA system solution such that the structure of existing base-station systems does not need to be modified or rebuilt for a new set of signal channels in order to benefit from high efficiency and high linearity PA system performance.

[0062] Moreover, the DHMPA system is agnostic to modulation schemes such as quadrature phase shift keying (QPSK), quadrature amplitude modulation (QAM), Orthogonal Frequency Division Multiplexing (OFDM), etc. in code division multiple access (CDMA), global system for wireless communications (GSM), WCDMA, CDMA2000, and wireless LAN systems. This means that the DHMPA system is capable of supporting multi-modulation schemes, multi-carriers and multi-channels. Other benefits of the DHMPA system of the present invention include correction of PA non-linearities in repeater or indoor coverage systems that do not have the necessary baseband signals information readily available.

[0063] Although the present invention has been described with reference to the preferred embodiments, it will be understood that the invention is not limited to the details described thereof. Various substitutions and modifications have been suggested in the foregoing description, and others will occur to those of ordinary skill in the art. Therefore, all such substitutions and modifications are intended to be embraced within the scope of the invention as defined in the appended claims.

We claim:

1. A digital predistortion system for linearizing the output of power amplifiers comprising
   input signal for wireless communications,
   at least one power amplifier for outputting an amplified signal,
   at least one feedback signal derived from the amplified signal including a representation of a noise characteristic of the power amplifier,
   estimator logic responsive to the at least one feedback signal for determining predistortion coefficients at least partly in accordance with the equation

$$z(n) = \sum_{i=0}^{n-1} x_l(n-i)\left(\sum_{j=0}^{k-1} a_{ij}\left|x_l(n-i)\right|^j\right),$$

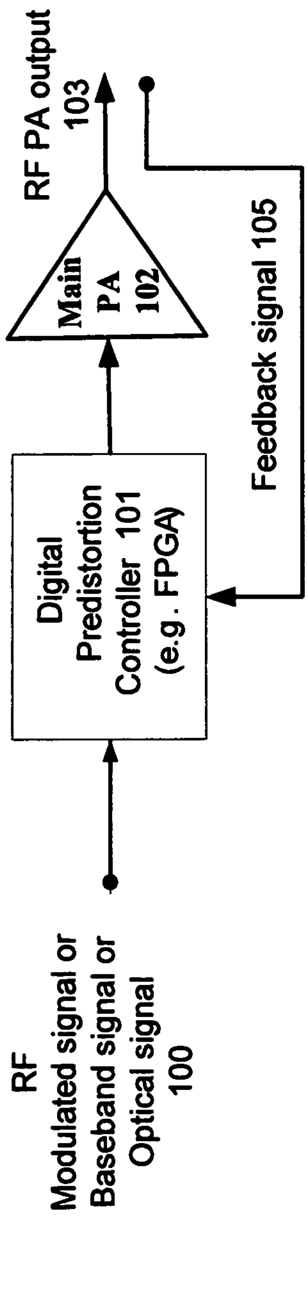
   where a_{ij} are predistortion coefficients, and
   digital predistortion logic for predistorting the input signal and supplying a predistorted signal to the at least one power amplifier.

2. A digital predistortion system for linearizing the output of power amplifiers comprising
   input signal suitable for wireless communications,
   at least one power amplifier for outputting an amplified signal,
   at least one feedback signal derived from the amplified signal including a representation of a noise characteristic of the at least one power amplifier,
   estimator logic responsive to the at least one feedback signal for generating predistortion coefficients based at least in part on feedback path delay determined from the correlation given by the equation

$$C(m) = \sum_{i=0}^{N-1} sign\big(x(i+1) - x(i)\big)sign\big(y(i+m+1) - y(i+m)\big)$$

$$n(delay) = Max(C(m))$$

FIG. 1. Basic Digital Hybrid Mode Power Amplifier System



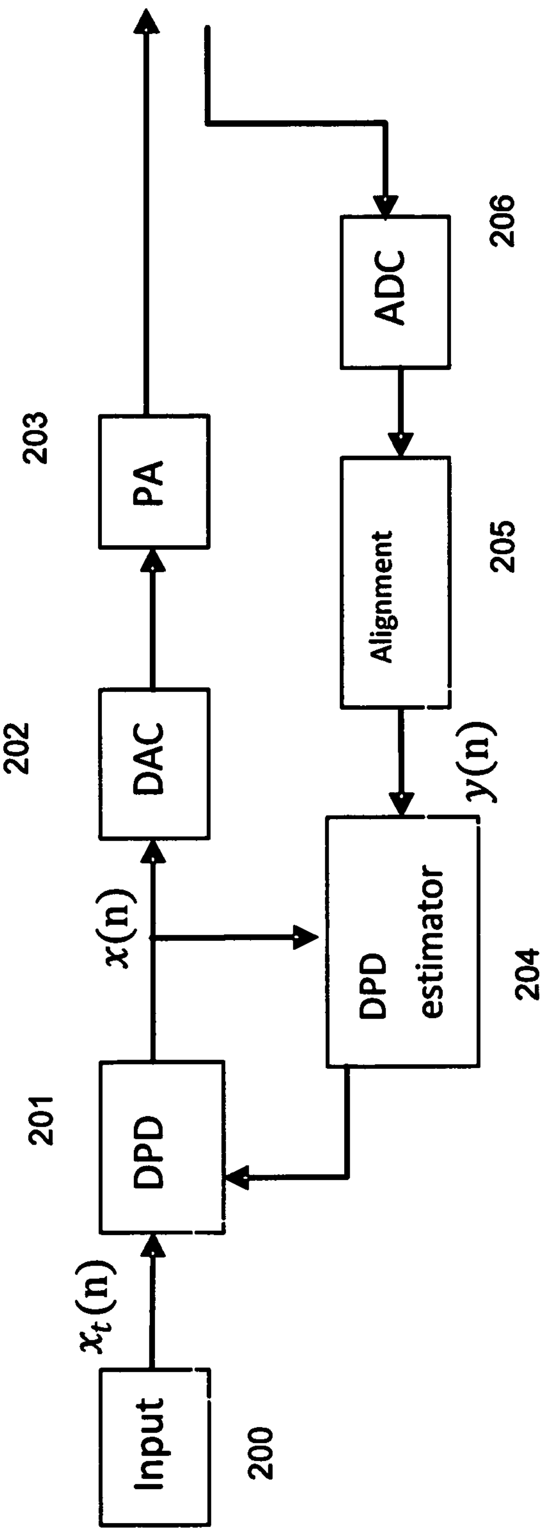


FIG. 2. Digital Predistortion Block Diagram

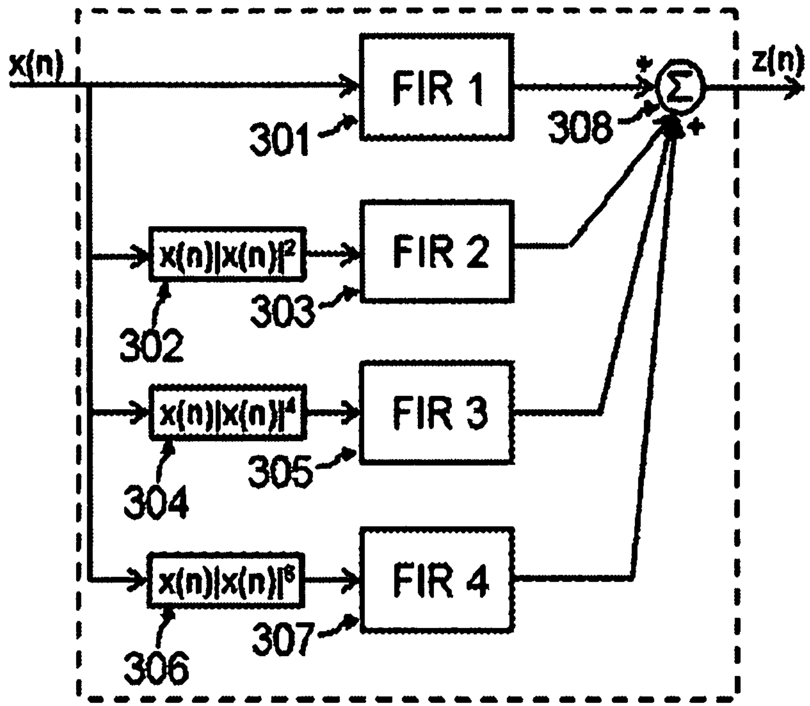


FIG. 3. Polynomial based PD in an embodiment of Digital Hybrid Mode Predistortion PA System

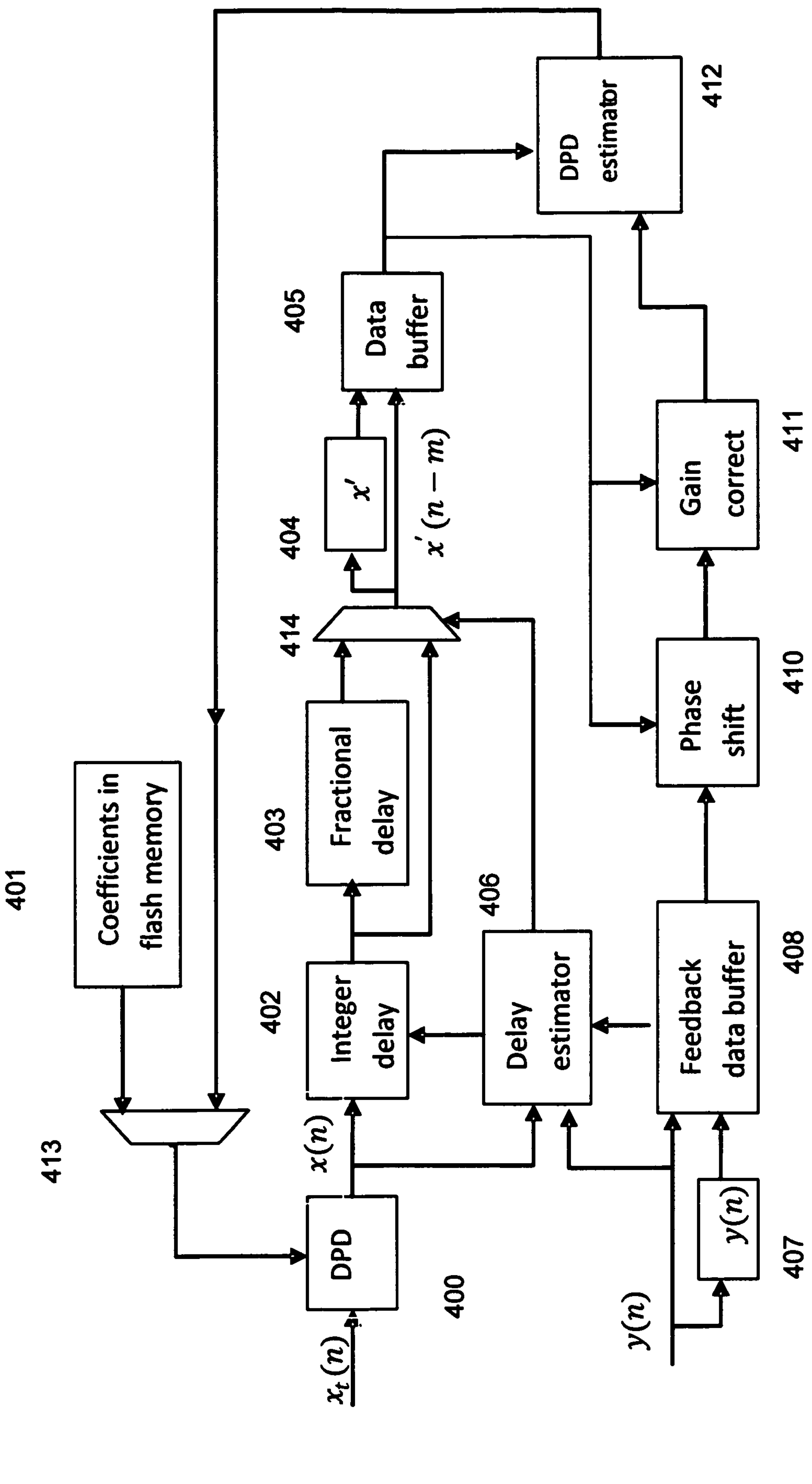


FIG. 4. Digital Predistortion Algorithm

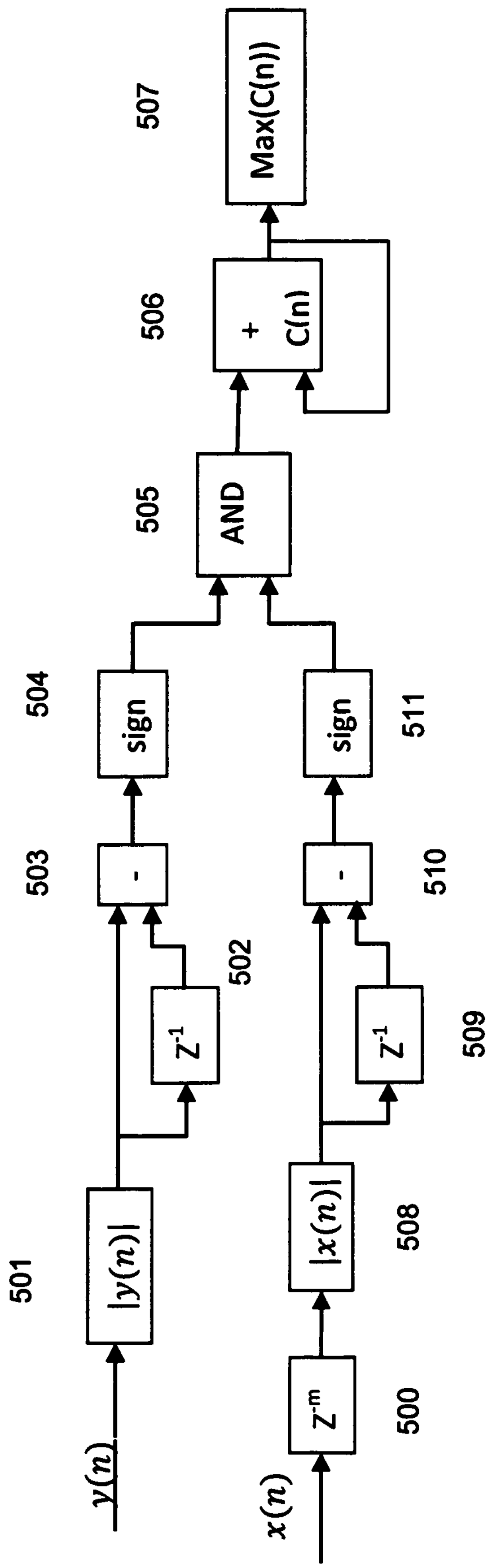


FIG. 5. Delay Estimation Block

600

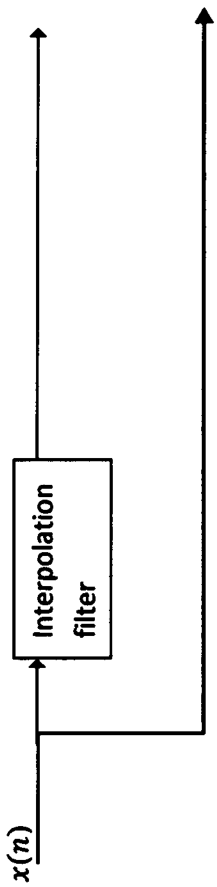


Figure 6 Fractional Delay Block

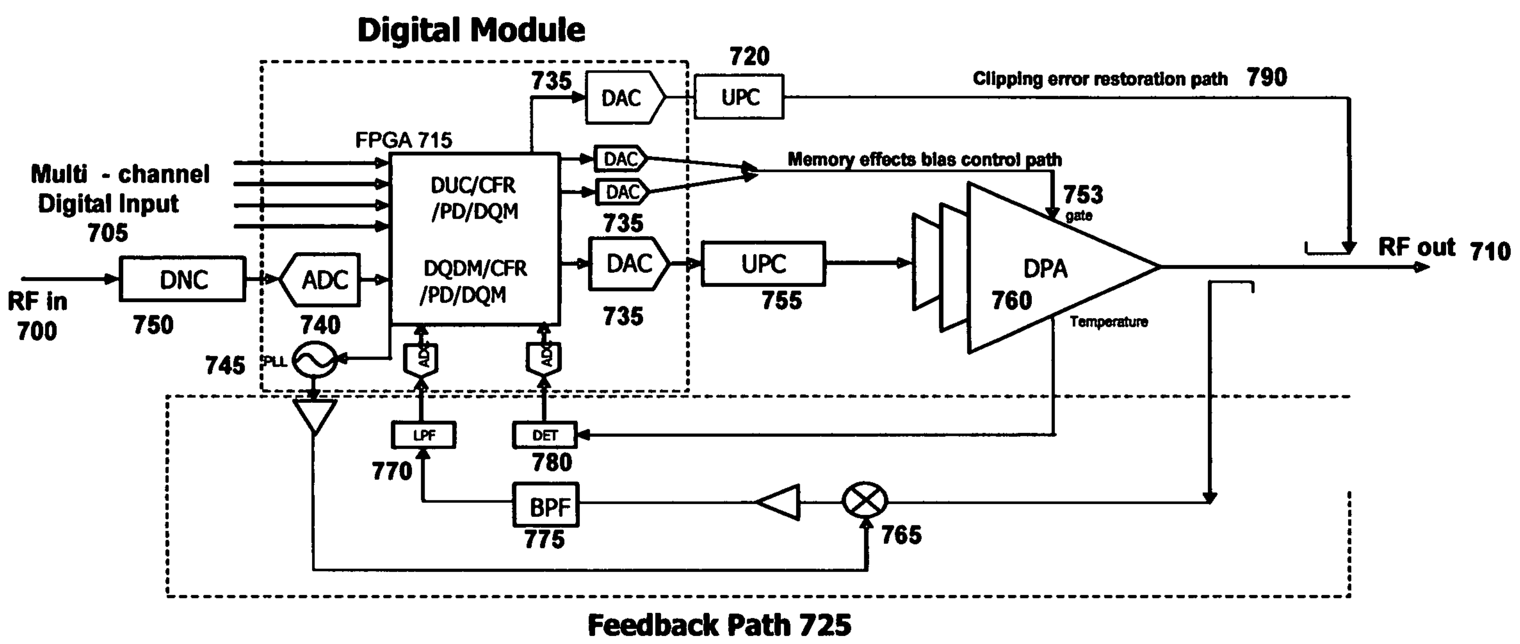


FIG. 7. An embodiment of Digital Hybrid Mode Predistortion PA System: DQM with UPC-based Clipping Error Restoration Path, and Optional or Alternative Multi-Channel Digital Input

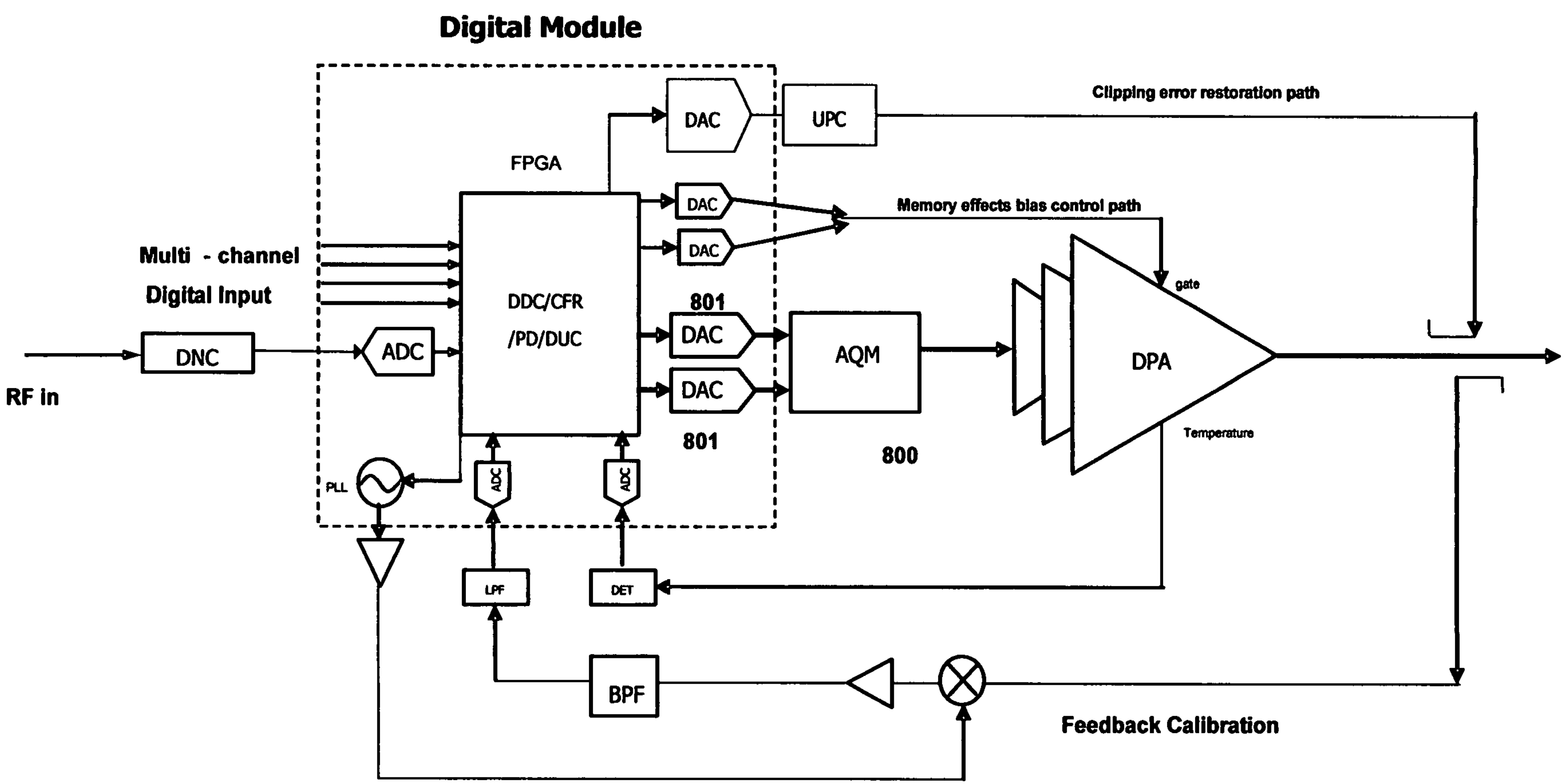


FIG. 8. An embodiment of Digital Hybrid Mode Predistortion PA System: DQM with UPC-based Clipping Error Restoration Path, and Optional or Alternative Multi-Channel Digital Input, with Feedback Calibration

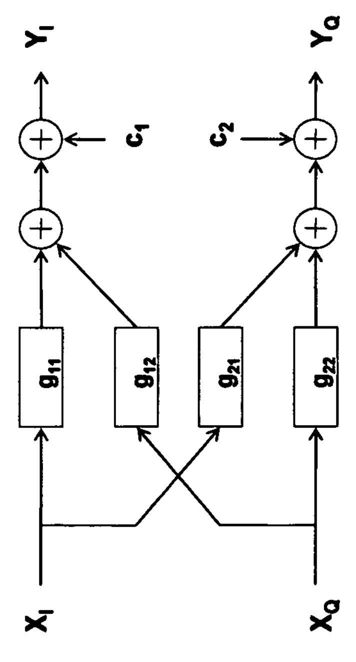


Figure 9 Analog Quadrature Modulator Compensation Block