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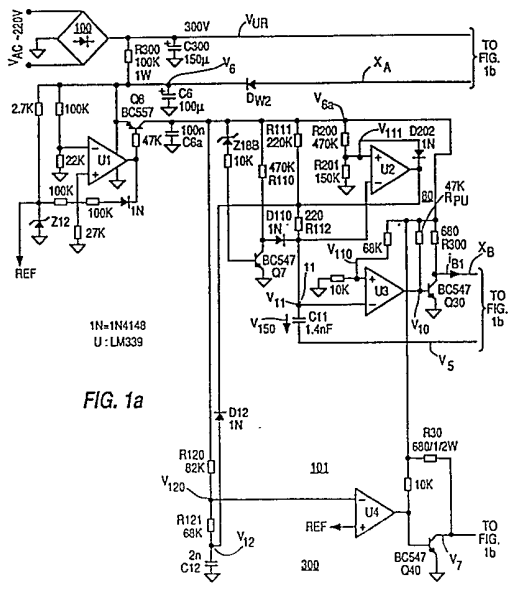
(54) Switch-mode power supply

(57) In a switch mode power supply (300), a first switching transistor Q1 is coupled to a primary winding W1 of an isolation transformer T1. A second winding W4 of the transformer T1 is coupled via a switching diode D3 to a capacitor C3 of a control circuit for developing a DC control voltage V_3 in the capacitor C3 that varies in accordance with an output supply voltage B+. The control voltage V_3 is applied via the transformer T1 by means of a winding W2 and is rectified by a diode DW2 for providing a control voltage V6 to a saw tooth signal generator U2, U3, C12. The saw tooth voltage across a capacitor C12 is applied to a pulse width modulator 101 for producing a pulse-width modulated control signal V_7 which is applied to a second transistor Q2 for generating and regulating the output supply voltage B+ in accordance with the pulse width modulation of the control signal V_7. A further switching transistor Q4 periodically applies a low impedance across a further winding W3 of the transformer T1 that is coupled to an oscillator U2, U3 for synchronizing the oscillator U2, U3 to a horizontal frequency signal V_H.



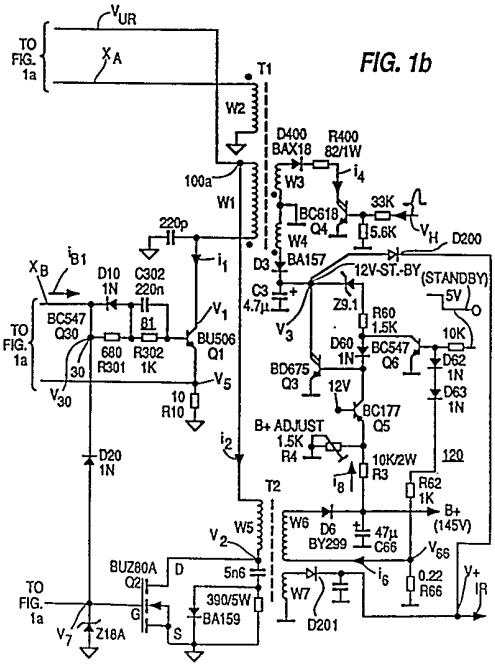


FIG. 1b

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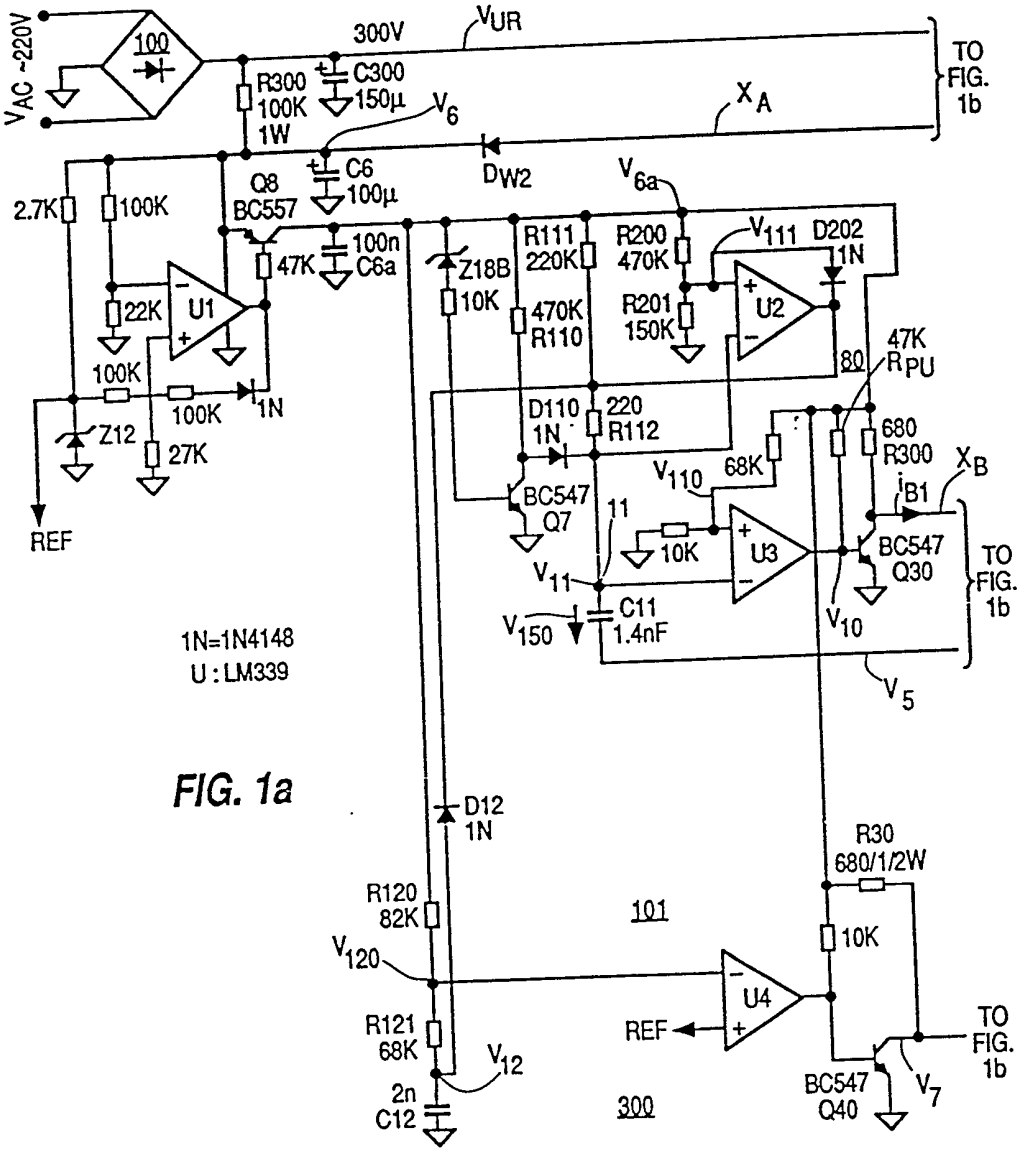
VAC ~220V
100
300V
VUR
TO FIG. 1b
R300 100K 1W
C300 150µ
V6
XA
C6 100µ
DW2
V6a
2.7K
100K
Q8 BC557
47K
100n C6a
Z18B
10K
R111 220K
R200 470K
V111
D202 1N
22K
U1
470K R110
R201 150K
U2
80
47K RPU
100K
100K
1N
D110 1N
220 R112
680 R300
XB
Z12
27K
REF
BC547 Q7
V110
68K
iB1
11
10K
U3
BC547 Q30
TO FIG. 1b
V11
C11 1.4nF
V150
V10
V5
1N=1N4148
U : LM339
FIG. 1a
D12 1N
R30 680/1/2W
R120 82K
101
10K
V120
U4
R121 68K
REF
TO FIG. 1b
V12
2n C12
300
BC547 Q40
V7

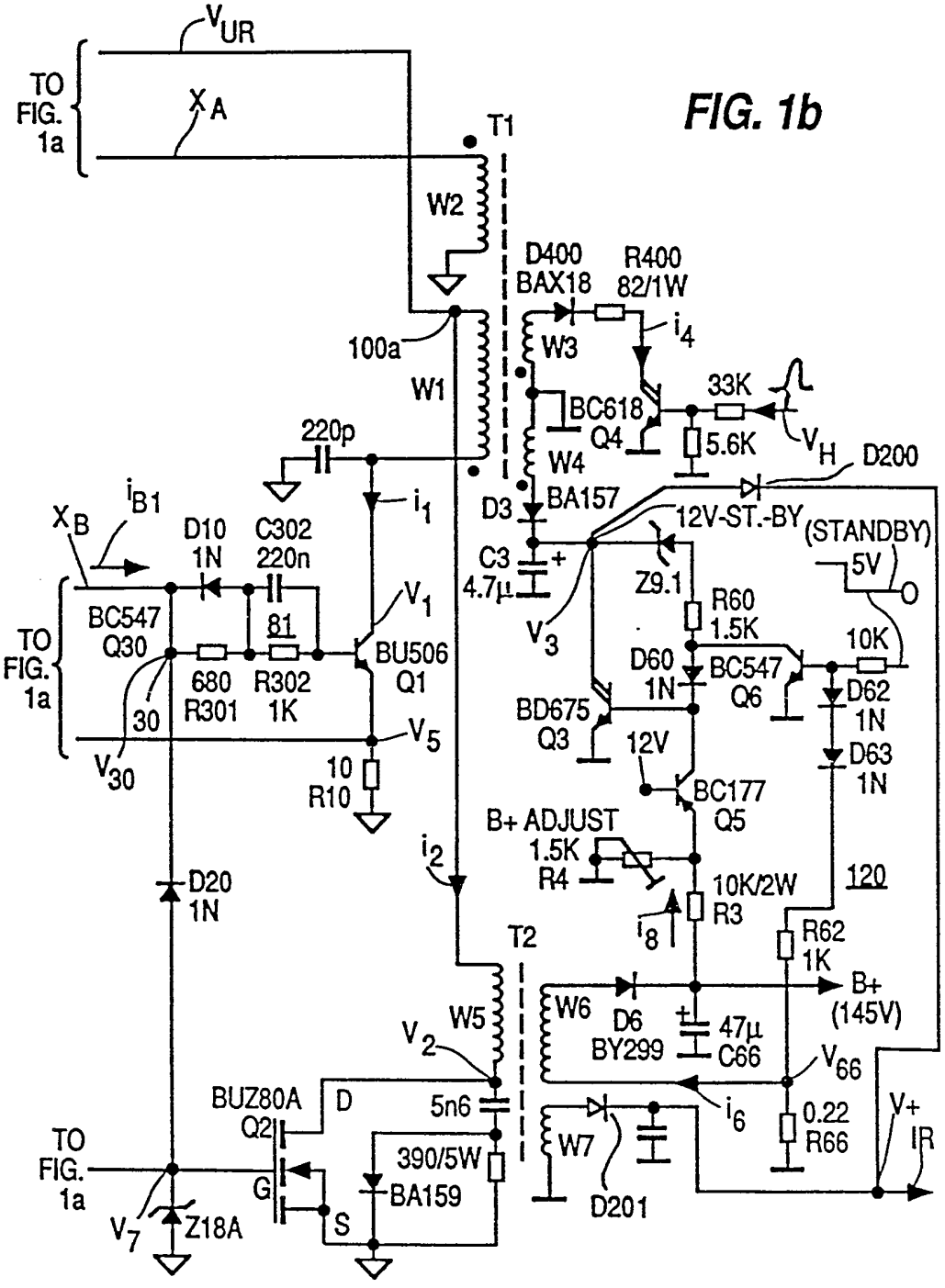
V_UR
TO FIG. 1a
X_A
T1
W2
D400 BAX18
R400 82/1W
i_4
W3
100a
W1
33K
BC618 Q4
5.6K
V_H
D200
220p
W4
i_1
i_B1
X_B
D3 BA157
12V-ST.-BY
(STANDBY)
5V
D10 1N
C302 220n
C3 4.7µ
Z9.1
R60 1.5K
V_1
BC547 Q30
81
BU506 Q1
10K
D60 1N
BC547 Q6
D62 1N
680 R301
R302 1K
30
V_30
V_3
BD675 Q3
12V
D63 1N
V_5
10 R10
BC177 Q5
B+ ADJUST 1.5K R4
10K/2W R3
i_2
i_8
120
D20 1N
T2
R62 1K
B+ (145V)
W6
D6 BY299
47µ C66
W5
V_2
V_66
BUZ80A Q2
D
5n6
i_6
0.22 R66
V+
IR
390/5W
W7
D201
BA159
G
S
V_7
Z18A

FIG. 1b

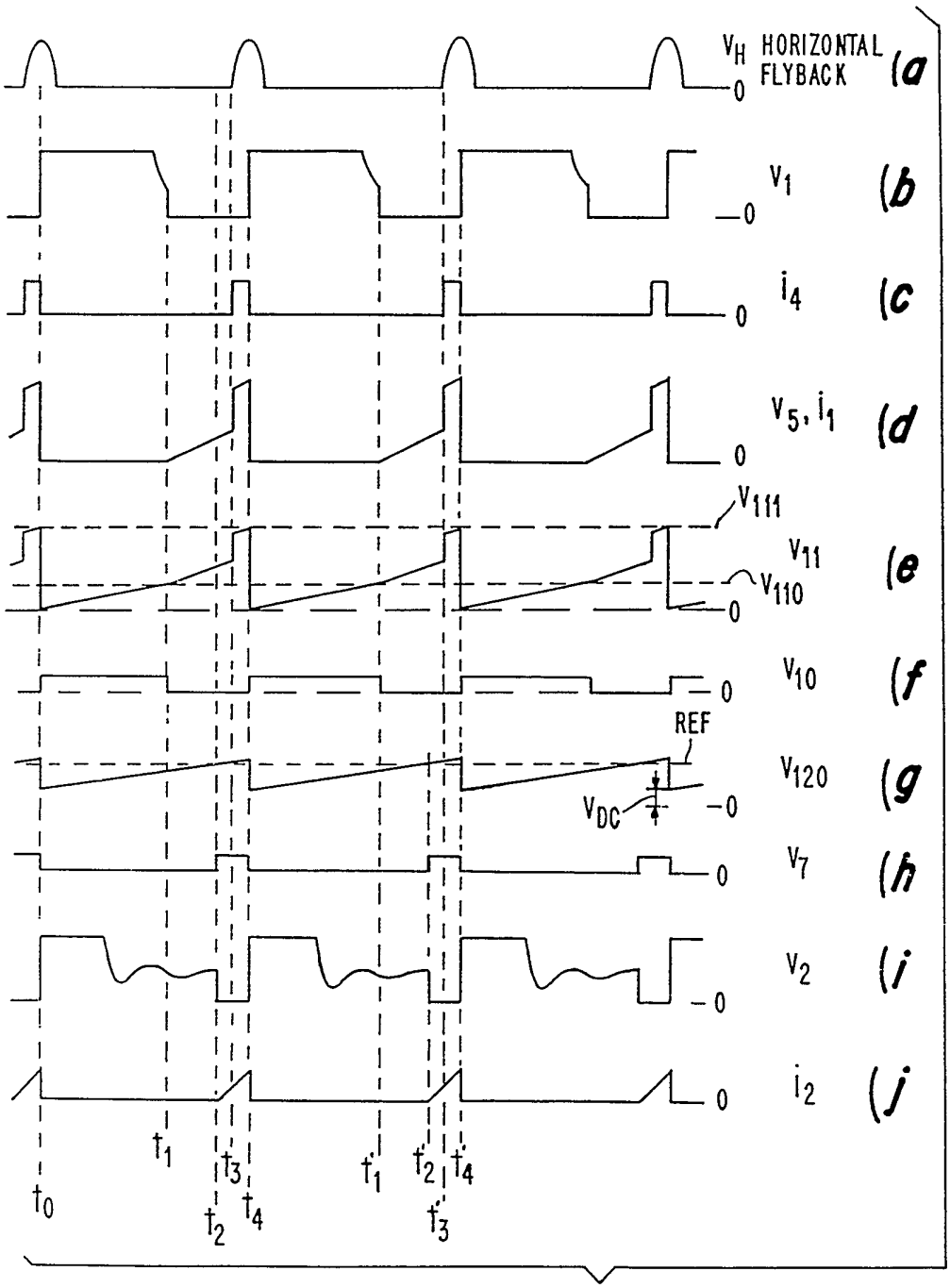
V_H HORIZONTAL FLYBACK
(a
0
V_1
(b
0
i_4
(c
0
V_5, i_1
(d
0
V_{111}
V_{11}
V_{110}
(e
0
V_{10}
(f
0
REF
V_{120}
(g
V_{DC}
0
V_7
(h
0
V_2
(i
0
i_2
(j
0
t_0
t_1
t_2
t_3
t_4
t_1'
t_2'
t_3'
t_4'

FIG. 2

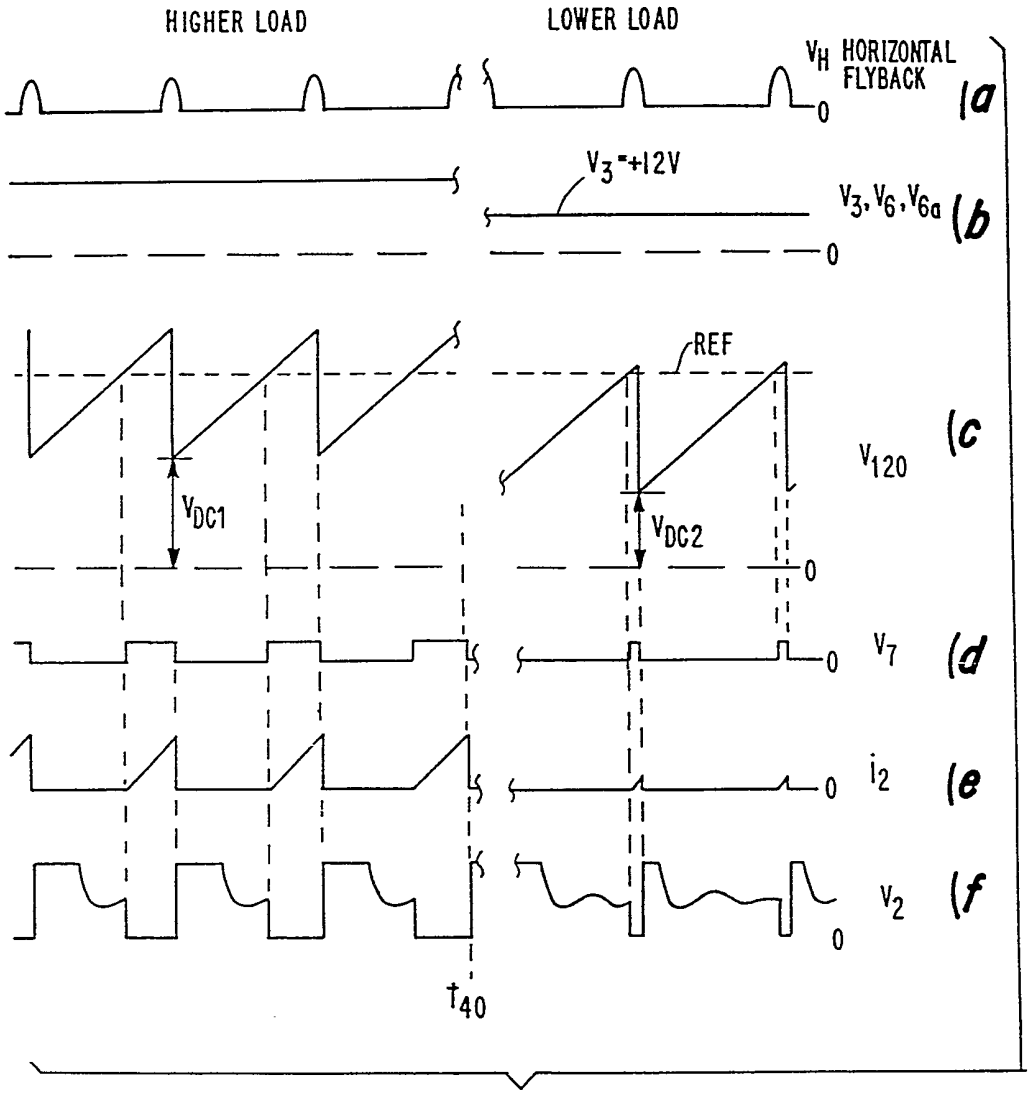
HIGHER LOAD
LOWER LOAD
V_H HORIZONTAL FLYBACK
(a)
0
V_3 = +12V
V_3, V_6, V_{6a}
(b)
0
REF
V_{120}
(c)
V_{DC1}
V_{DC2}
0
V_7
(d)
0
i_2
(e)
0
V_2
(f)
0
t_{40}

FIG. 3

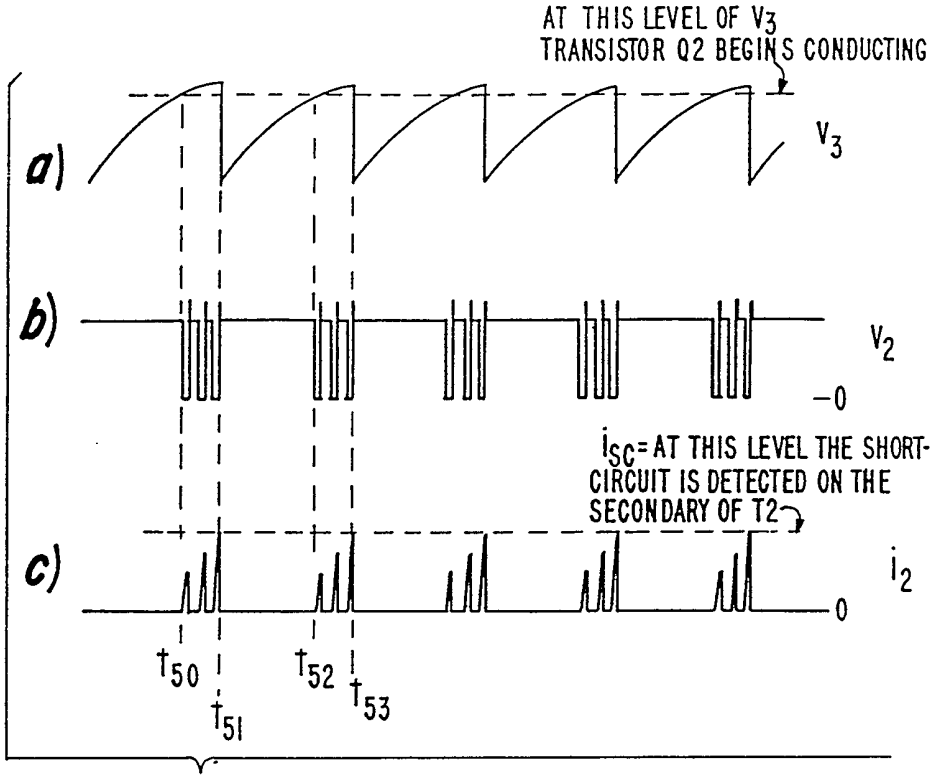
AT THIS LEVEL OF V3
TRANSISTOR Q2 BEGINS CONDUCTING
a)
V3
b)
V2
0
isc = AT THIS LEVEL THE SHORT-CIRCUIT IS DETECTED ON THE SECONDARY OF T2
c)
i2
0
t50
t51
t52
t53

FIG. 4

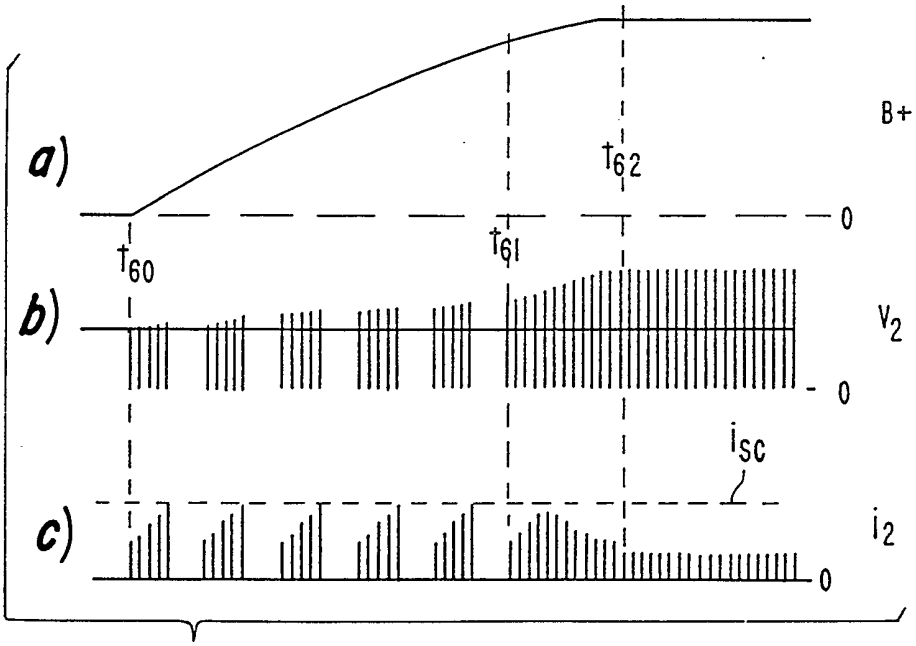
B+
a)
t62
0
t60
t61
b)
V2
0
isc
c)
i2
0

FIG. 5

A SYNCHRONIZED SWITCH-MODE POWER SUPPLY

This invention relates to switch-mode power supplies.

Some television receivers have input signal terminals for receiving, for example, external video input signals such as R, G and B color video input signals, that are developed relative to the common ground conductor of the receiver. Such input signal terminals and the receiver common conductor may be coupled to corresponding signal terminals and common conductors of external devices, such as, for example, a VCR or a teletext decoder.

To simplify the coupling of signals between the external devices and the television receiver, the common ground conductors of the receiver and of the external devices are connected together so that all are at the same potential. The signal lines of each external device are coupled to the corresponding input signal terminals of the receiver. In such an arrangement, the common conductor of each device, such as of the television receiver, may be held "floating", or conductively isolated, relative to the corresponding AC mains supply source that energizes the device. When the common conductor is held floating, a user touching a terminal that is at the potential of the common conductor will not suffer an electrical shock.

A floating common ground conductor is isolated from the potentials of the terminals of the AC mains supply source that provide power to the television typically by a transformer. The floating or isolated common conductor is sometimes referred to as a "cold" ground conductor.

In a typical switch mode power supply (SMPS) of a television receiver, the AC mains supply voltage is coupled, directly, without using transformer coupling, to a bridge rectifier. An unregulated direct current (DC) input supply voltage is produced that is, for example, referenced to a common conductor, referred to as "hot" ground, that is conductively isolated from a cold ground conductor. A pulse width modulator controls the duty cycle of a chopper transistor switch that applies the unregulated supply

voltage across a primary winding of an isolating flyback transformer. A flyback voltage at a frequency that is determined by the modulator is developed at a secondary winding of the transformer and is rectified to produce a DC output supply voltage, such as a B+ voltage that energizes a horizontal deflection circuit of the television receiver. The primary winding of the flyback transformer is, for example, conductively coupled to the hot ground conductor. The secondary winding of the flyback transformer and B+ voltage may be conductively isolated from the hot ground conductor by the hot-cold barrier formed by the transformer.

It may be desirable to synchronize the operation of the chopper transistor to horizontal scanning frequency for preventing the occurrence of an objectionable visual pattern or artifact in an image displayed on the television receiver.

It may be further desirable to couple a horizontal synchronizing signal that is referenced to the cold ground to the pulse-width modulator that is referenced to the hot ground, such that isolation is maintained.

According to the invention, there is provided a switch mode power supply, comprising: a source of an input supply voltage; means energized by said input supply voltage and responsive to a modulated control signal for generating from said input supply voltage an output supply voltage that is regulated in accordance with a timing modulation of said modulated control signal; a transformer including first and second windings; first switching means coupled to said first winding and operating in a given frequency for generating a first switching current in said first winding to energize said second winding; a capacitor; second switching means coupled to said second winding and to said capacitor for rectifying a current that flows in said second winding to generate therefrom a rectified current that flows in said capacitor to develop a first control voltage in said capacitor during a flyback

interval, said capacitor being coupled via said second switching means to said second winding for applying said first control voltage to said second winding to produce in said second winding a second control voltage when said rectified current is generated; means responsive to said output supply voltage and coupled to said capacitor for controlling said first control voltage such that a change in a magnitude of said output supply voltage from a nominal value thereof produces an amplified change in a magnitude of said second control voltage that is developed in said second winding; means coupled to said transformer and having said second control voltage coupled thereto via said transformer during said flyback interval when said rectified current is generated, for rectifying said transformer coupled second control voltage to generate a third control voltage at a level that is determined by said second control voltage; a sawtooth signal generator responsive to said third control voltage for producing a sawtooth signal outside said flyback interval in accordance with said second control voltage; and means responsive to said sawtooth signal for generating said modulated control signal with a timing modulation that varies in accordance with said first control voltage to regulate said output supply voltage.

In the Drawing:

FIGURE 1, formed by FIGURES 1a and 1b, illustrates a power supply embodying an aspect of the invention;

FIGURES 2a-2j illustrate waveforms useful for explaining the run mode operation of the circuit of FIGURE 1 when loading is constant;

FIGURES 3a-3f illustrate waveforms useful for explaining the run mode operation of the circuit of FIGURE 1 under a varying loading condition;

FIGURES 4a-4c illustrate waveforms of the circuit of FIGURE 1 during an overload condition; and

FIGURES 5a-5c illustrate a transient waveform useful for explaining the operation of the circuit of FIGURE 1 during start-up.

FIGURE 1 illustrates a switch-mode power supply (SMPS) 300, embodying an aspect of the invention. SMPS 300 produces a regulated B+ output supply voltage of +145 volts that is used for energizing, for example, a deflection circuit of a television receiver, not shown, and a regulated output supply voltage V+ for energizing a remote control receiver of the television receiver.

A mains supply voltage V_{AC} is rectified in a bridge rectifier 100 to produce an unregulated voltage V_{UR}. A primary winding W5 of a chopper flyback transformer T2 is coupled between a terminal 100a and a drain electrode of a power MOS field effect transistor (FET) Q2 having a source electrode that is coupled to a common conductor, referred to herein as "hot" ground. Transistor Q2 is switched by a pulse-width modulated control signal or voltage V_7 that is produced by a pulse-width modulator 101.

A primary winding W1 of a flyback transformer T1 is coupled between terminal 100a, where voltage V_{UR} is developed, and a collector electrode of a switching transistor Q1, that is included in pulse-width modulator 101. The emitter of transistor Q1 is coupled to the hot ground via an emitter current sampling resistor R10 for developing a voltage V_5, across resistor R10, that is proportional to a collector current i_1 of transistor Q1.

FIGURES 2a-2j illustrate waveforms useful for explaining the normal steady state operation of the SMPS of FIGURE 1. Similar symbols and numerals in FIGURES 1 and 2a-2j indicate similar items or functions.

During an interval t_1-t_4 of FIGURE 2f of a given cycle or period of the switching operation, a base voltage V_{10} of a transistor Q30 of FIGURE 1a is at zero volts, causing a positive pulse voltage V_{30} to be developed at the collector of transistor Q30. Voltage V_{30} is coupled via a network 81 to the base of transistor Q1, causing transistor Q1 to be turned on during interval t_1-t_4 of FIGURE 2d. A diode D20 of FIGURE 1b is coupled between the collector of transistor Q30 and the gate electrode of transistor Q2. Positive pulse voltage V_{30} back biases diode D20.

During an interval t_2-t_4 of FIGURE 2h, a transistor Q40 of FIGURE 1a is nonconductive and, in conjunction with diode D20, permits a voltage V_{6a}, that is coupled via a resistor R30 to the gate electrode of transistor Q2, to produce a positive voltage V_7. Positive voltage V_7 causes transistor Q2 to be turned on during interval t_2-t_4 of FIGURE 2j. Consequently, upramping switching currents i_1 and i_2 of corresponding FIGURES 2d and 2j flow in windings W1 and W5, respectively, of FIGURE 1b and store inductive energy in transformers T1 and T2.

In accordance with an aspect of the invention, a switching transistor Q4 is coupled via diode D400 and a current limiting resistor R400, having a low resistance, across a secondary winding W3 of transformer T1. While transistors Q1 and Q2 are conductive, transistor Q4 is turned on. Transistor Q4 is turned on by a flyback pulse V_H at a horizontal rate f_H that is derived from the horizontal deflection circuit. Pulse V_H is coupled to the base of transistor Q4. Consequently, at time t_3 of FIGURE 2d, that occurs during the horizontal retrace interval of signal V_H of FIGURE 2a, transistor Q4 of FIGURE 1 applies a low impedance across winding W3 that loads transformer T1

causing, by a transformer action, a step increase in collector current i_1 of transistor Q1, as a result of the transformer coupled low impedance.

Collector current i_1 in transistor Q1 develops a sense voltage V_5 of FIGURE 2d across sampling resistor R10 of FIGURE 1b that is coupled via capacitor C11 to form voltage V_{11} at terminal 11. The step increase in current i_1 of FIGURE 2c at time t_3 causes a step increase in a voltage V_{11} of FIGURE 2e at terminal 11 of FIGURE 1a. After the step increase at time t_3, each current i_1 of FIGURE 2c and voltage V_{11} of FIGURE 2e continues to increase in an upramping manner at a rate that is determined by the inductance of winding W1. Voltage V_{11} is developed at an inverting input terminal of a comparator or amplifier U3. Amplifier U3 has an output terminal that is coupled to the base of transistor Q30 for developing switching signal or voltage V_{10}.

Amplifier U3, transistor Q30, and transistor Q1 form an oscillator as a result of a positive feedback path via a capacitor C11 that is coupled between emitter current sampling resistor R10 of transistor Q1 and terminal 11. Terminal 11 is coupled to the inverting input terminal of comparator U3, and also to an inverting input terminal of an amplifier or comparator U2.

In accordance with a feature of the invention, signal V_H, that is coupled to such oscillator via the low impedance formed by transistor Q4, synchronizes the switching timings in SMPS 300 to the horizontal scanning frequency. Such synchronization is desirable for preventing an undesirable disturbance in the displayed image.

A voltage V_{111} is coupled from voltage V_{6a} via a voltage divider formed by resistors R200 and R201. A diode D202 is coupled in the forward direction from a noninverting input terminal of amplifier U2, where voltage V_{111} is developed, to an output terminal of amplifier U2. The output terminal of amplifier U2 is coupled via a relatively small resistor R112 to terminal 11 and also via

a diode D12 to one plate of a capacitor C12. The other plate of capacitor C12 is coupled to the hot ground.

Time t_4 of FIGURE 2d follows the gradual upramping increase in current i_1 between times t_3 and t_4 that, in turn, follows the aforementioned step increase rise at time t_3. At the time t_4, voltage V_{11} of FIGURE 2e becomes larger than voltage V_{111}. The result is that the voltage at the output terminal of amplifier U2 becomes zero relative to the hot ground. Therefore, voltage V_{11} is clamped to zero volts by the output terminal of amplifier U2 via resistor R112, thereby quickly discharging capacitor C11. Simultaneously, a sawtooth voltage V_{12} across capacitor C12, that has been previously charged from voltage V_{6a} via resistors R120 and R121, is clamped to zero volts via a diode D12. Diode D202, that becomes conductive, causes voltage V_{111} to be clamped to a substantially smaller value that provides a Schmitt trigger operation in amplifier U2.

A DC voltage V_{110} is developed at a noninverting input terminal of comparator U3. Voltage V_{110} is produced from voltage V_{6a} via a resistive voltage divider. At time t_0 or t_4 of FIGURE 2e, voltage V_{11} becomes smaller than voltage V_{110} as a result of the clamping operation via resistor 220 of FIGURE 1. Therefore, output signal V_{10} of FIGURE 2f at the output terminal of comparator U3 of FIGURE 1 increases as a result of coupling voltage V_{6a} via a pull-up resistor R_{PU}. At time t_4 of FIGURE 2f, signal V_{10} that is coupled to the base of a driver switching transistor Q30 of FIGURE 1 causes transistor Q30 to turn-on.

When transistor Q30 is turned on, it causes both transistors Q1 and Q2 to turn off. Consequently, the stored inductive energy in transformer T2 is transferred via a secondary winding W6 and via a diode D6 to a filter capacitor C66 in a flyback operation for producing output supply voltage B+. Similarly, voltage V+ is produced via a winding W7.

In the same manner, the energy stored in transformer T1 generates a flyback switching current in a

secondary winding W4 of transformer T1 that turns on a diode D3 and that continues flowing in a capacitor C3. Thus, capacitor C3 is coupled across winding W4 via switching diode D3 after time t_0 of FIGURE 2b. The result is that a DC control voltage V_3 of FIGURE 1 is developed in capacitor C3. The magnitude of voltage V_3 is controllable, as described later on. Control voltage V_3 in capacitor C3 is coupled by the transformer action to a secondary winding W2 of transformer T2 and is rectified by a diode D_{W2} for producing a control voltage V_6 in a filter capacitor C6.

During normal operation, a transistor Q8 of Fig. 1a operates as a conductive switch and couples voltage V_6 to a filter capacitor C6a to form control voltage V_{6a} that is substantially equal to voltage V_6. The ratio of voltage V_{6a} to voltage V_3 is determined by the turns ratio of windings W4 and W2.

After time t_0 or t_4 of FIGURE 2e, when capacitor C11 of FIGURE 1a has discharged, the output terminal of amplifier U2 of FIGURE 1 forms a high impedance. Therefore, during, for example, interval t_0-t_4 of FIGURE 2e, a current flowing in resistors R111 and R112 of FIGURE 1a charges capacitor C11, and a current flowing in resistors R120 and R121 charges capacitor C12.

At time t_0, a voltage V_{120} at a junction between resistors R120 and R121 is at a level V_{DC}, of FIGURE 2g, that is controlled by voltage V_{6a} of FIGURE 1a. After time t_0, each of voltages V_{11} and V_{120} of FIGURES 2e and 2g, respectively, increase in an upramping manner at a rate of change that is determined by voltage V_3 in capacitor C3.

At time t_1 of FIGURE 2e, voltage V_{11} exceeds voltage V_{110} that is developed at a noninverting input terminal of amplifier U3 of FIGURE 1. Consequently, at time t_1 of FIGURE 2e, transistor Q30 of FIGURE 1 is turned off, causing transistor Q1 to be turned on, as explained before.

At a later time in the cycle, time t_2 of FIGURE 2g, upramping voltage V_{120}, at an inverting input terminal of an amplifier U4, exceeds a reference voltage REF at its

noninverting input terminal. Consequently, a transistor Q40 becomes nonconductive, that enables positive voltage V_7 to be developed at the base of transistor Q2. Therefore, transistor Q2 begins conducting, as explained before and as shown in FIGURES 2h-2j. As explained later on, the length of the interval, t_0-t_2, of FIGURE 2j when transistor Q2 of FIGURE 1 is nonconductive increases when voltage V_3 decreases, and vice versa.

Diode D20 prevents the duty cycle of transistor Q2 from becoming higher than the duty cycle of transistor Q1, thus, advantageously, protecting transistor Q2. Without such protection, if, for example, level V_{DC} of voltage V_{120} of FIGURE 2g were higher than voltage REF, transistor Q2 of FIGURE 1 might have been destroyed.

Resistor R301 of network 81 permits gate voltage V_7 to become higher than the gate threshold voltage. When transistor Q30 becomes conducting, diode D10 by-passes resistor R301, causing a faster switch-off time of transistor Q1.

At time t_3 of FIGURE 2c, when horizontal flyback pulse V_H occurs, transistor Q4 goes into saturation, short-circuiting winding W3 of transformer T1, as explained before. Thus, current i1 of transformer T1 increases rapidly at time t_3 of FIGURE 2d. The manner in which the increase in a current such as currenti1 occurs is explained in European Published Application 0332095, published 13 September 1989, in the name of RCA Licensing Corporation, entitled A SWITCH MODE POWER SUPPLY.

At time t_4 of FIGURE 2e, voltage V_{11} becomes higher than V_{111}, triggering the oscillator that is formed by amplifiers U2 and U3, as explained before. Therefore, both transistor Q1 and Q2 are switched off and a new cycle begins.

Control circuit 120 of FIGURE 1b, that is referenced to the cold ground conductor, controls the duty cycle of voltage V_7 at the base of transistor Q2 by varying control voltage V_3 across capacitor C3. A transistor Q5 of

circuit 120 is coupled in a common base amplifier configuration. The base voltage of transistor Q5 may be obtained via a temperature compensated voltage +12V. A resistor R3 is coupled between the emitter of transistor Q5 and voltage B+. As a result of the common base operation, a current i_8 in resistor R3 is proportional to voltage B+. An adjustable resistor R4 that is used for adjusting the level of emitter voltage is coupled between the cold ground conductor and the emitter of transistor Q5. Resistor R4 is used for adjusting the level of the current in transistor Q5. Thus, an adjustable, preset portion of current i_8 flows to the cold ground conductor through resistor R4, and an error component of current i_8 flows through the emitter of transistor Q5.

The collector current of transistor Q5 is coupled to the base of a transistor Q3 for controlling a collector current of transistor Q3. The collector of transistor Q3, forming a high output impedance, is coupled to the junction of capacitor C3 and diode D3.

When transistor Q1 becomes nonconductive, the stored energy in transformer T1 causes a switching current to flow via diode D3 that charges capacitor C3, as indicated before. Regulation of the power supply is obtained by controlling control voltage V_3 in capacitor C3. Voltage V_3 is controlled by controlling the loading across winding W_4 of transformer T1 by means of transistor Q3. When, for example, supply current loading across capacitor C66 decreases, voltage B+ tends to increase.

FIGURES 3a-3f illustrate waveforms useful for explaining the operation of the circuit in FIGURE 1 when voltage B+ of FIGURE 1 increases, such as after time t_{40} of FIGURES 3a-3f. Similar symbols and numerals in FIGURES 1, 2a-2j and 3a-3f indicate similar items or functions.

As a result of such transient excessive level of voltage B+ of FIGURE 1b, a larger base current flows in transistor Q3 via resistor R3 and transistor Q5, causing voltage V_3 in capacitor C3 to become smaller. Hence, voltages V_6 and V_{6a}, that are produced as a result of

voltage rectification during flyback operation in winding W2 of transformer T1, also become smaller. The result is that level V_{DC} of voltage V_{120} of FIGURE 3c at a beginning time of a given upramping portion of voltage V_{120} becomes smaller. Such decrease in level V_{DC} of voltage V_{120} is shown by the variation from level V_{DC1} to level V_{DC2} of FIGURE 3c. Therefore, voltage V_{120} of FIGURE 1a exceeds voltage REF at a later instant in a given cycle, causing a reduction in the duty cycle of transistor Q2 of FIGURE 1, as shown in FIGURES 3d-3f. The reduction in the duty cycle causes less energy to be stored in and transferred via transformer T2 of FIGURE 1 to the load at a terminal where voltage B+ is developed. In this way, regulation of voltage B+ is obtained.

In steady state, voltage V_3 is stabilized at a level that causes an equilibrium between the charging and discharging currents of capacitor C3. An increase in voltage B+ from a nominal value is capable of causing, advantageously, a proportionally greater or amplified change in voltage V_3, as a result of amplification and current integration of the collector current in transistor Q3.

Processing voltage B+ for producing control voltage V_3 is accomplished, advantageously, in a DC coupled signal path for improving error sensing. A given proportional change in voltage B+ is capable of causing a greater proportional change in voltage V_3. Thus, error sensitivity is improved. Only after the error in voltage B+ is amplified, the amplified error contained in DC coupled voltage V_3 is transformer or AC coupled to winding W2. The combination of such features improves the regulation of voltage B+.

Another way by which an arrangement similar to control circuit 120 is used for regulation purposes is shown and explained in U.S. Patent Application 424,354, filed 19 October 1989, in the name of Leonardi, entitled A SWITCH-MODE POWER SUPPLY. (RCA 85438 filed herewith).

In accordance with another feature of the invention, transformer T1 couples both synchronizing signal V_H and control voltage V_3, that is derived from voltage B+, across an isolation barrier. The coupling is done such that both signal V_H and voltage B+ are isolated, with respect to an electrical shock hazard, from mains voltage V_{AC}.

Switching the television receiver into standby mode of operation is accomplished by turning off a transistor switch Q6. The collector of transistor switch Q6 is coupled in a current path that is formed by a series arrangement of a zener diode Z9.1, a resistor R60 and a diode D60. Such series arrangement is coupled between the collector and the base of transistor Q3.

When transistor Q6 is turned off, the negative feedback current flowing in zener diode Z9.1, resistor R60 and diode D60 to the base of transistor Q3 establishes voltage V_3 at approximately +12 volts, that is lower than during normal operation. The result is that voltage V_6 is maintained at +15 volts, and level V_{DC} of voltage V_{120} at the inverting input terminal of amplifier U4 is maintained at about +7 volts. Consequently, the peak voltage of sawtooth voltage V_{120} cannot exceed voltage V_{REF}. Therefore, advantageously, transistor Q2 remains nonconductive throughout standby operation.

Throughout normal operation, voltage V_{6a} produces a base current in a transistor Q7 via a zener diode Z18B. When conductive, transistor Q7 couples the anode of a diode D110 to the hot ground potential. Therefore, voltage V_{11} at the cathode of diode D110 maintains diode D110 nonconductive.

The free running frequency of the oscillator that is formed by amplifiers U2 and U3 is designed to be lower than the horizontal frequency to allow for synchronization. Because voltage V_6 becomes lower during standby operation, transistor Q7 is turned off. Therefore, capacitor C11 is charged by an additional current that flows via a collector pull-up resistor R110 and diode D110. Consequently, the

free running frequency of the oscillator, advantageously, increases beyond the audible range to prevent an audible nuisance.

During stand-by, voltage V+, that is used for energizing an infra red remote control receiver, not shown, is supplied by voltage V_3 via a switch diode D200. On the other hand, during normal operation, diode D200 is back biased and voltage V+ is generated, instead, from a rectified voltage that is produced by transformer T2 and that is coupled via a switch diode D201. Because of the switching mode operation of transistor Q1, advantageously, low power losses occur during stand-by.

Switching the receiver into normal operation is accomplished by turning on transistor Q6. Thereby, voltages V_3, V_6 and the DC level V_{DC} of voltage V_{120} increase, thus enabling transistor Q2 to become conductive.

If a fault condition occurs, for example, if capacitor C66 becomes short circuited, SMPS 300 begins operation in an intermittent mode, for example, between times t_{50} and t_{51} of FIGURES 4a-4c followed by a relatively long dead time interval, t_{51}-t_{52}. Similar symbols and numerals in FIGURES 1 and in FIGURES 4a-4c that depict such fault condition indicate similar items or functions.

In case of such short circuit, a higher current i_6 flows through winding W6 of transformer T2 of FIGURE 1, causing a higher negative voltage V_{66} to be developed across a resistor R66 that is coupled between the low end of winding W6 and the cold ground. Thereby, for example, at time t_{51} of FIGURES 4a-4c, diodes D62 and D63 of FIGURE 1 that are coupled between the base of transistor Q6 and resistor R66 become conductive, transistor Q6 goes into cut-off, and transistor Q3 clamps voltage V_3 to about +12V. Consequently, as explained before with respect to the stand-by operation, transistor Q2 is switched off.

After time t_{51} of FIGURES 4a-4c, transistor Q6 becomes conducting again and decouples zener diode Z9.1 and resistor R60 from the base of transistor Q3. Thereby, as shown in FIGURE 4a, voltage V_3 increases slowly.

Consequently, at time t_{52}, transistor Q2 of FIGURE 1 conducts. However, due to the short-circuit on the secondary side of transformer T2, at time t_{53} of FIGURE 4c, transistor Q2 of FIGURE 1 is switched off again, as explained before.

Immediately after the power or voltage V_{AC} is applied, a capacitor C300 is charged during a portion of a period of voltage V_{AC} Consequently, voltage V_{UR} is developed in capacitor C300. Voltage V_{UR} is coupled to capacitor C6 via a resistor R300 to charge capacitor C6, prior to normal operation.

An amplifier U1 has an inverting input terminal that is coupled to voltage V_6 and a noninverting input terminal that is coupled to voltage REF. After voltage V_{AC} is initially applied, and after voltage V_6 in capacitor C6 becomes sufficiently large to exceed a predetermined minimum level that is determined by voltage REF, the output voltage of amplifier U1 is pulled down to the hot ground potential. The result is that a transistor switch Q8 is turned on into saturation and couples voltage V_6 to capacitor C6a. In this way, operation of SMPS 300 with a proper level of voltage V_6 properly begins.

FIGURES 5a-5c illustrate waveforms useful for explaining the aforementioned start-up operation in the circuit of FIGURE 1 after voltage V_{AC} of FIGURE 1 is first applied. Similar symbols and numerals in FIGURES 1 and 5a-5c indicate similar items or functions.

At time t_{60} of FIGURE 5c, when voltage V_6 of FIGURE 1 becomes sufficiently high, transistor Q2 begins to conduct. Capacitor C66 is in a discharged state, during the first interval t_{60}-t_{61} of FIGURES 5a-5c. Therefore, SMPS 300 of FIGURE 1 operates in an intermittent mode, as in the case of a secondary short-circuit that was explained before. However, the supplied energy slowly charges capacitor C66 of FIGURE 1 on the secondary of transformer T2, thereby increasing voltage B+. At time t_{61} of FIGURE 5a, voltage B+ is high enough so that transistor Q2 of FIGURE 1b receives a proper base drive. The turn-on

process is terminated when voltage B+ has reached its normal value, as shown in FIGURE 5a at time t_{62}.

Attention is invited to copending application 90 050 15.4 from which this application is derived.

CLAIMS:

1. A switch mode power supply, comprising:

a source of an input supply voltage;

means energized by said input supply voltage and responsive to a modulated control signal for generating from said input supply voltage an output supply voltage that is regulated in accordance with a timing modulation of said modulated control signal;

a transformer including first and second windings;

first switching means coupled to said first winding and operating at a given frequency for generating a first switching current in said first winding to energize said second winding;

a capacitor;

second switching means coupled to said second winding and to said capacitor for rectifying a current that flows in said second winding to generate therefrom a rectified current that flows in said capacitor to develop a first control voltage in said capacitor during a flyback interval, said capacitor being coupled via said second switching means to said second winding for applying said first control voltage to said second winding to produce in said second winding a second control voltage when said rectified current is generated;

means responsive to said output supply voltage and coupled to said capacitor for controlling said first control voltage such that a change in a magnitude of said output supply voltage from a nominal value thereof produces an amplified change in a magnitude of said second control voltage that is developed in said second winding;

means coupled to said transformer and having said second control voltage coupled thereto via said transformer during said flyback interval when said rectified current is generated, for rectifying said transformer coupled second control voltage to generate a third control voltage at a level that is determined by said second control voltage;

a sawtooth signal generator responsive to said third control voltage for producing a sawtooth signal outside said flyback interval in accordance with said second control voltage; and

means responsive to said sawtooth signal for generating said modulated control signal with a timing modulation that varies in accordance with said first control voltage to regulate said output supply voltage.

2. A power supply according to claim 1 wherein said second switching means comprises a rectifier and wherein said first control voltage is coupled to said second winding via said rectifier during a portion of a given period when said rectifier is conductive.

3. A power supply according to claim 1 wherein said change in said output supply voltage is DC coupled from said output supply voltage to said second winding.

4. A power supply according to claim 1 wherein said second switching means comprises a diode that is forward biased by the current in said second winding during a first portion of a given period to generate said rectified current that flows in said diode in the forward direction and in said capacitor.

5. A power supply according to claim 1 wherein said first control voltage controlling means comprises means for generating a second current in said capacitor such that both said rectified and second currents that are coupled to said capacitor are DC currents that flow in opposite directions in said capacitor.

6. A power supply according to claim 1 wherein said first control voltage controlling means comprises a transistor for generating a second current that varies in accordance with said output supply voltage and that flows in a main current conducting electrode thereof, said second current being coupled to said capacitor to flow therein in the opposite direction to said rectified current.

7. A power supply according to claim 6 wherein said transistor is responsive to a load current for providing an overcurrent protection.

8. A power supply according to claim 1 wherein said second switching means comprises a diode and wherein said current that flows in said second winding of said transformer forward biases said diode during said flyback interval of said first switching current to render said diode conductive.

9. A power supply according to claim 1 wherein said first control voltage controlling means comprises a transistor having an electrode forming a current source with a high output impedance that is coupled to said capacitor for discharging said capacitor at a rate that is determined in accordance with said output supply voltage to maintain said first control voltage in said capacitor at a level that is determined in accordance with said output supply voltage.

10. A power supply according to claim 1 wherein said transformer isolates said output supply voltage from said modulated control signal with respect to an electrical shock hazard.

11. A power supply according to claim 1 wherein comprising a source of a synchronizing input signal at a frequency that is related to a deflection frequency, third switching means responsive to said input signal and coupled to said second winding for periodically applying a low impedance across said energized second winding, said applied low impedance causing, by a transformer action, a substantial increase in said first switching current, and means responsive to said first switching current and coupled to said modulated control signal generating means for sensing said increase in said first switching current to synchronize said modulated control signal to said input

signal when said increase in said first switching current occurs, in accordance with said input signal.

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Examiner's report to the Comptroller under Section 17 (The Search Report)

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Relevant Technical fields

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(ii) Int Cl (Edition 5) H02M 3/315, 3/335, 3/337, 3/338

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Databases (see over)

(i) UK Patent Office

(ii)

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Documents considered relevant following a search in respect of claims 1-11

Category (see over)	Identity of document and relevant passages	Relevant to claim(s)
A	GB 1535100 (PHILIPS) - see especially Figure 9	1

Category	Identity of document and relevant passages	Relevant to claim(s)

Categories of documents

X: Document indicating lack of novelty or of inventive step.

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