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(54) **SYSTEM AND METHOD FOR PREVENTING UNDESIRABLE SUBSTANTIALLY CONCURRENT SWITCHING IN MULTIPLE POWER CIRCUITS**

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(57) **ABSTRACT**

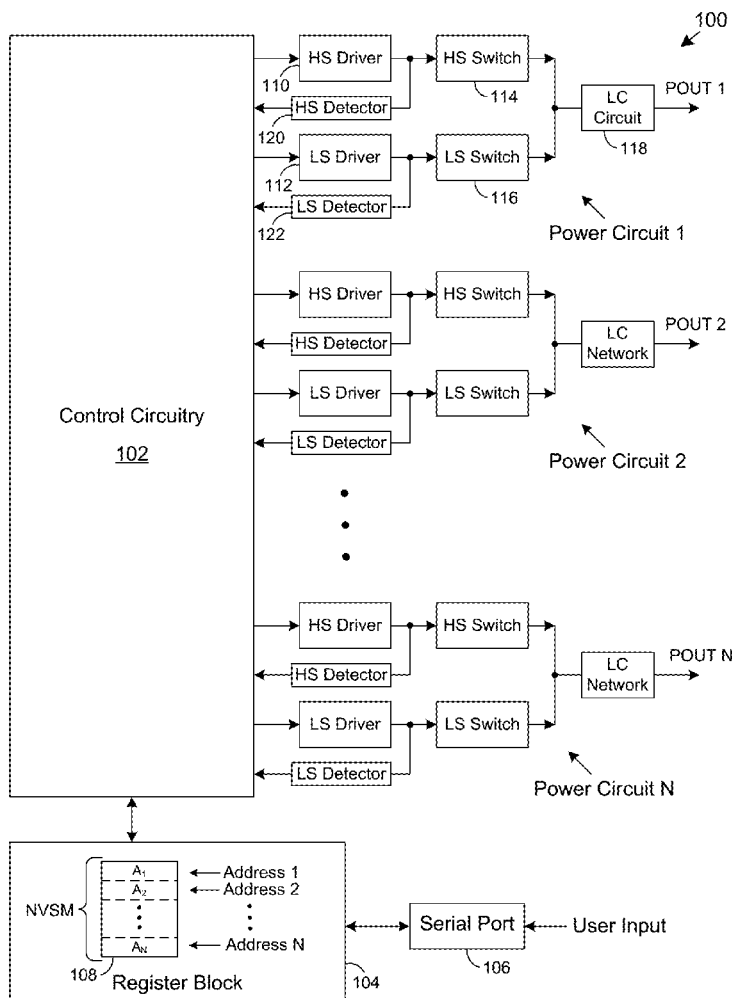
A power system includes a first charge pump configured to supply power, and control circuitry coupled to the first charge pump. The control circuitry is operable to receive a signal indicating whether a second charge pump is turning on. If the first charge pump is about to be turned on and the signal indicates that the second charge pump is turning on, the control circuitry is operable to prevent an output, of first charge pump from substantially aligning with an output of the second charge pump.

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(62) Division of application No. 13/538,844, filed on Jun. 29, 2012, now Pat. No. 9,443,431.



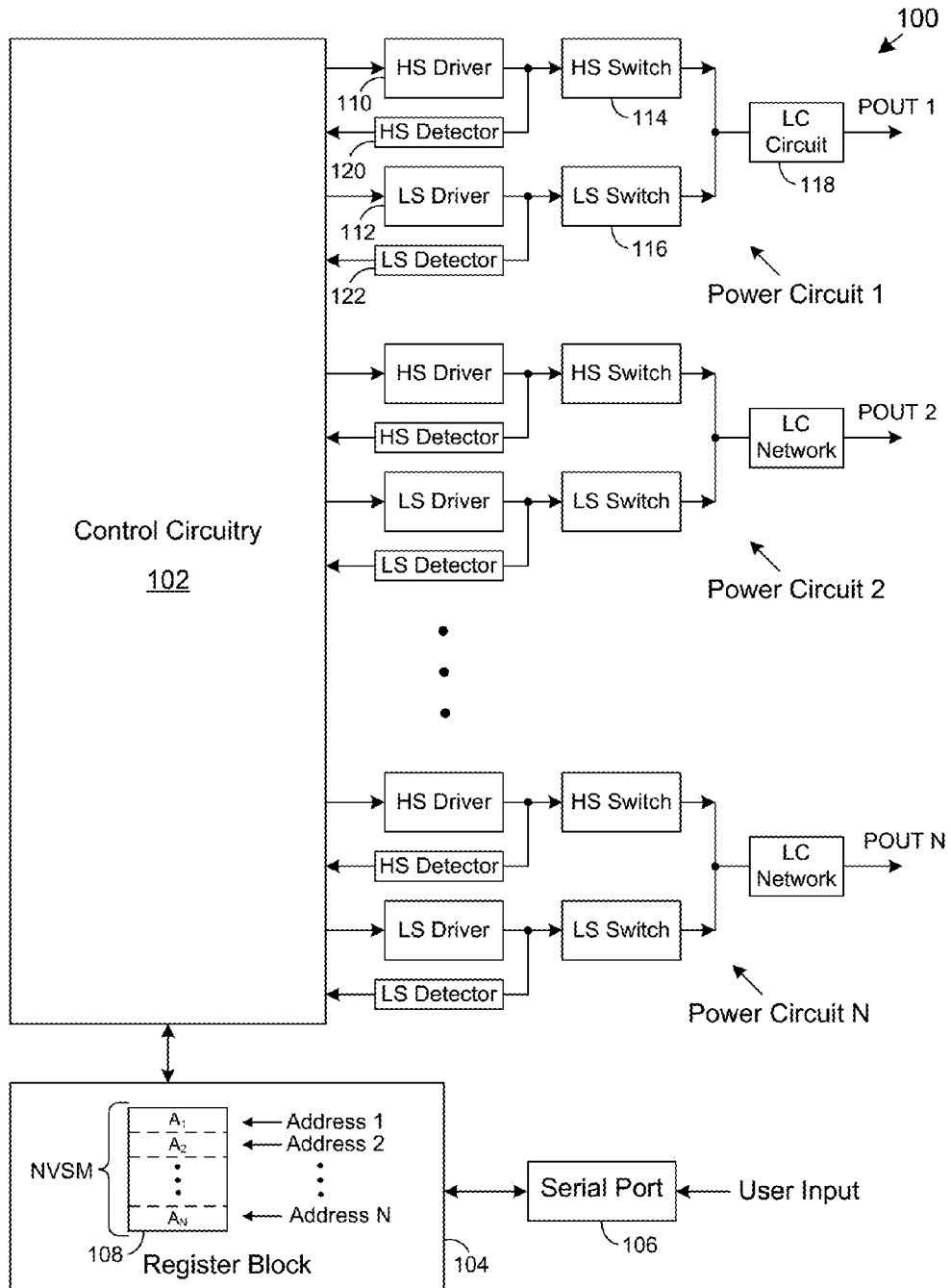


FIG. 1

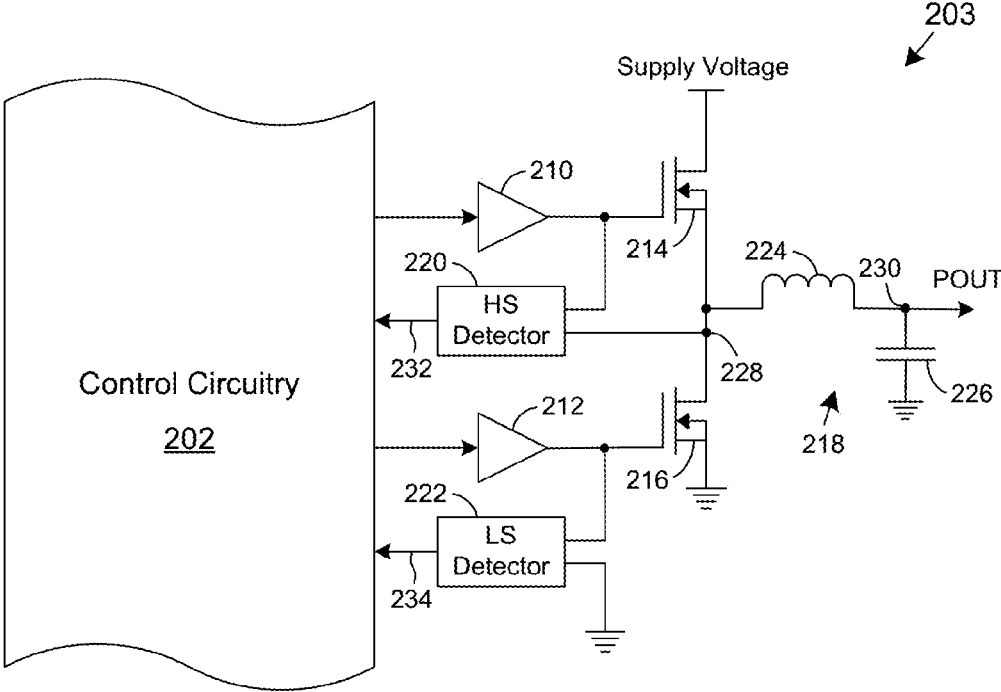


FIG. 2

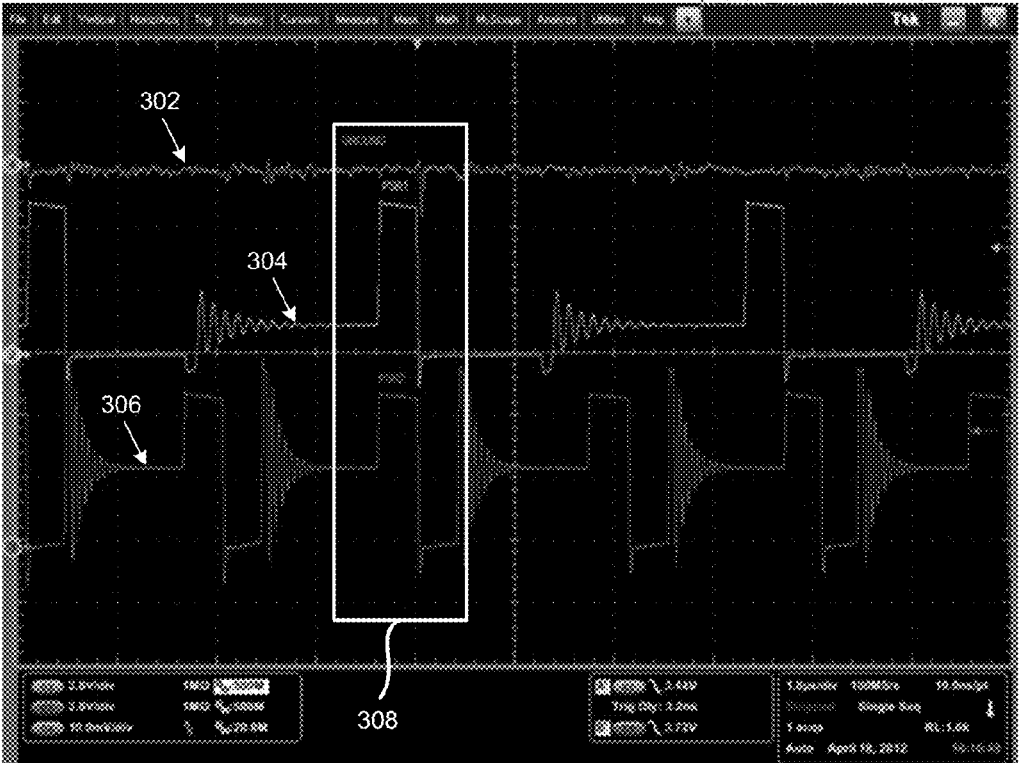


FIG. 3A

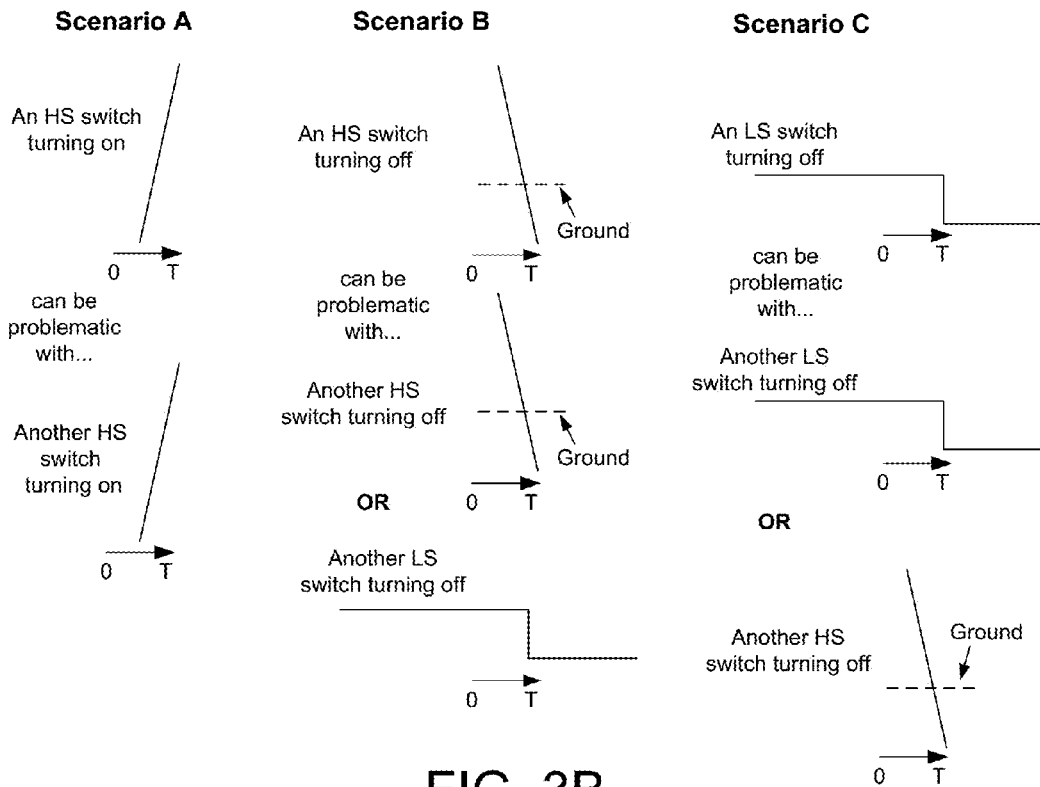
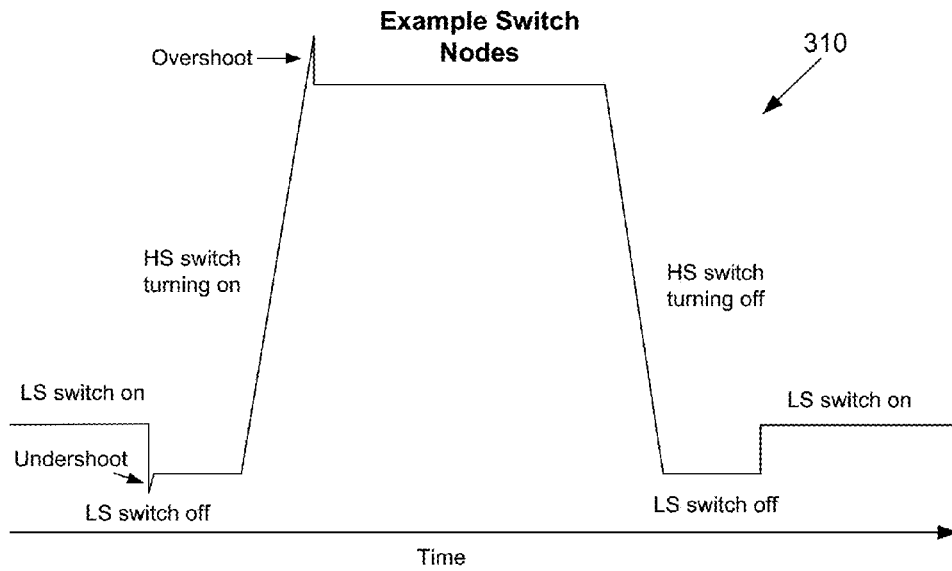


FIG. 3B

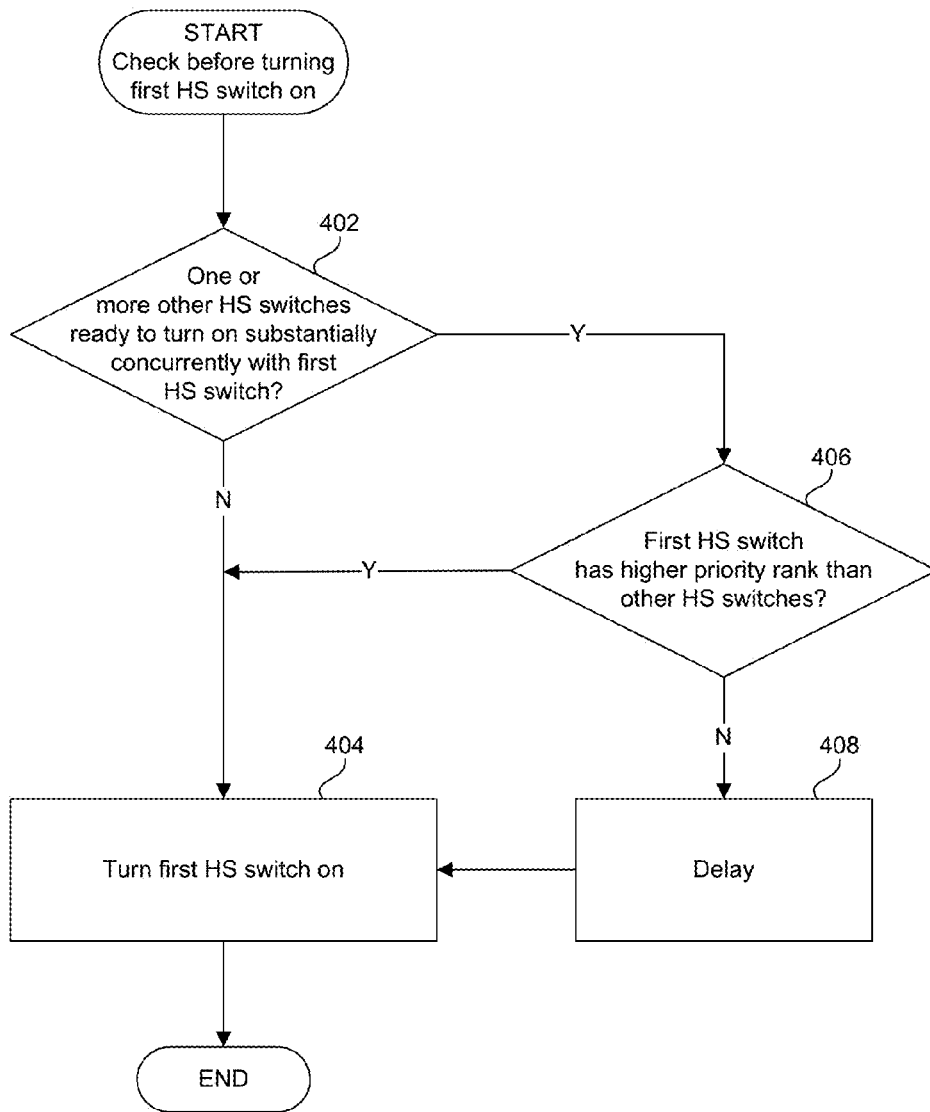


FIG. 4A

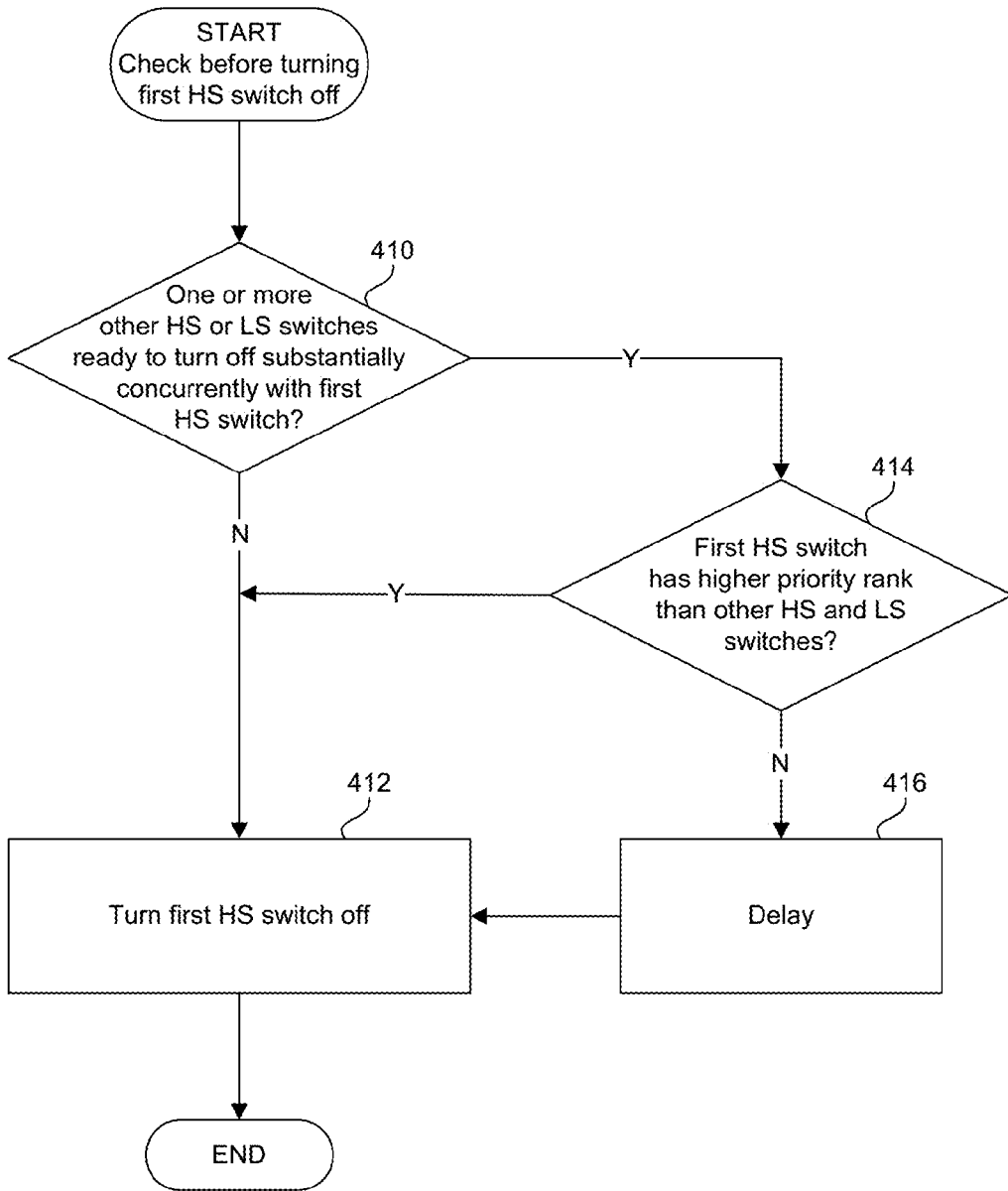


FIG. 4B

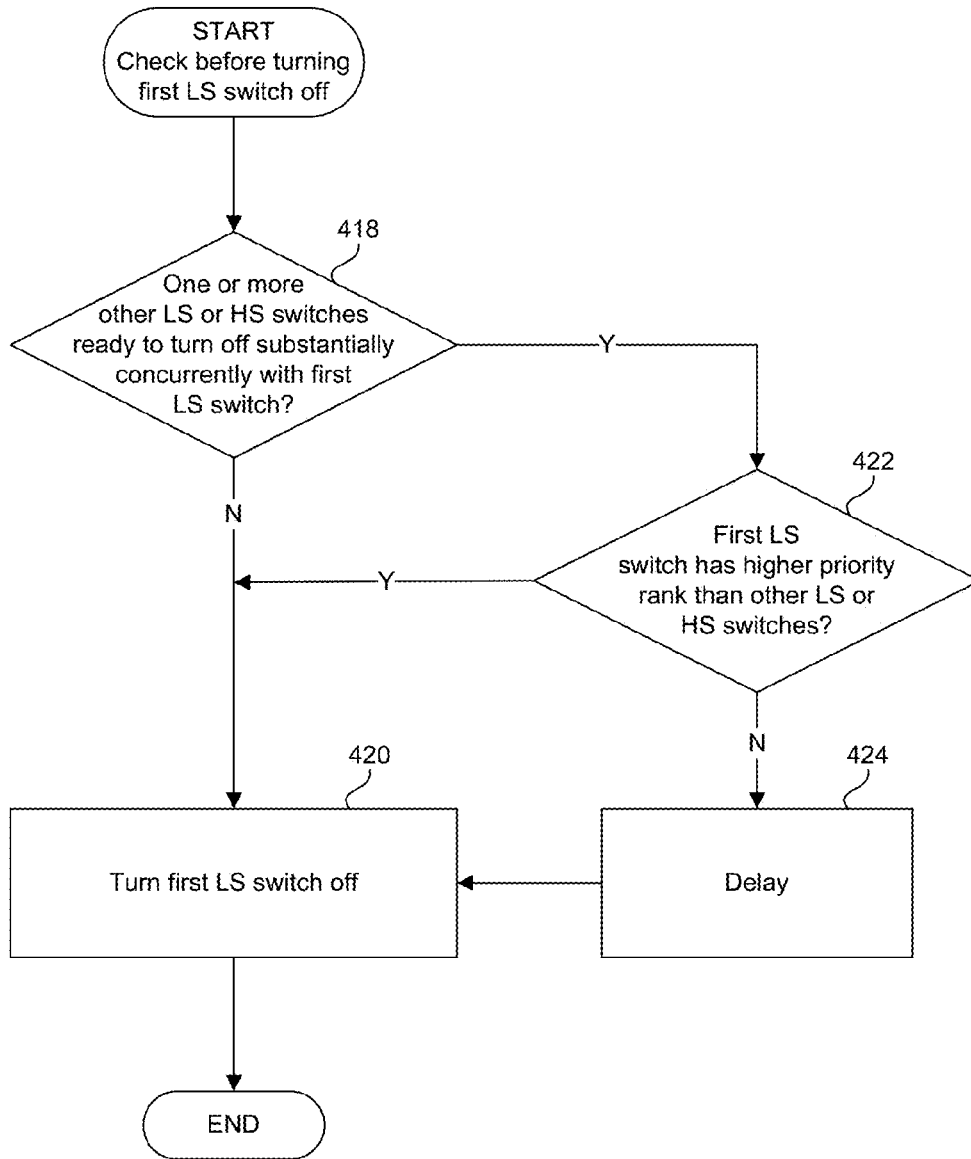


FIG. 4C

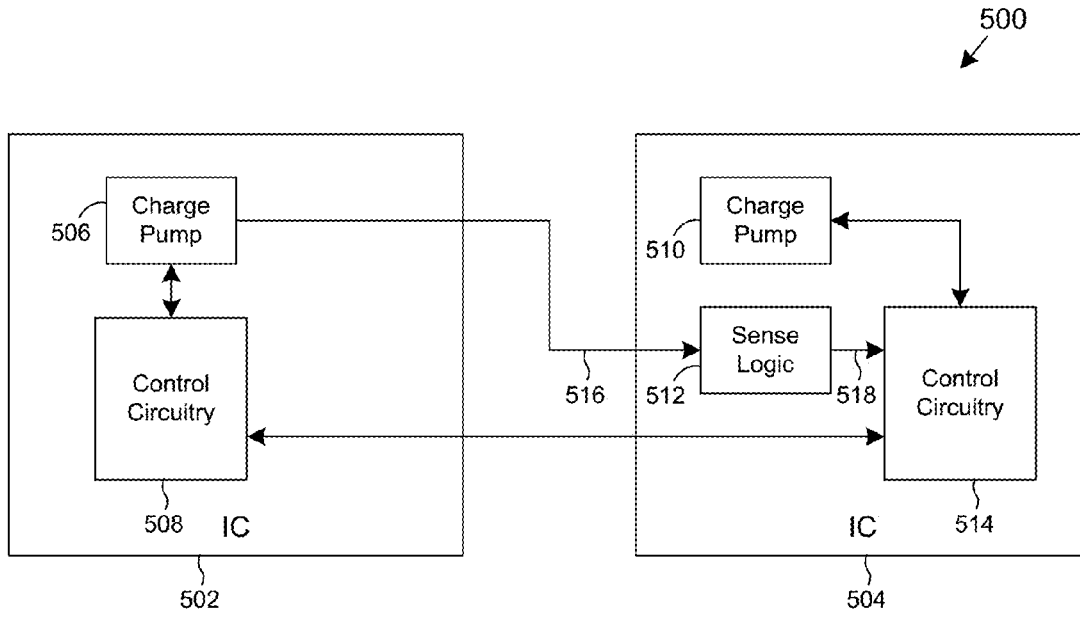


FIG. 5A

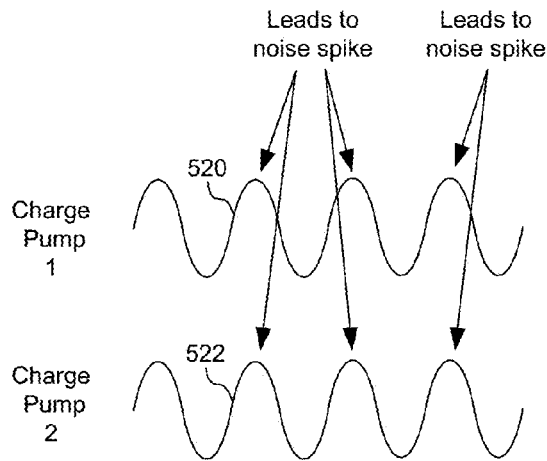


FIG. 5B

**SYSTEM AND METHOD FOR PREVENTING
UNDESIRABLE SUBSTANTIALLY
CONCURRENT SWITCHING IN MULTIPLE
POWER CIRCUITS**

CROSS REFERENCE TO RELATED
APPLICATION

[0001] This application is a divisional of U.S. patent application Ser. No. 13/538,844 (Atty. Docket No. 15957), filed on Jun. 29, 2012, which claims the benefit of U.S. Provisional Application No. 61/644,363 (Atty. Docket No. T5957.P), filed on May 8, 2012, the content of all of which are hereby incorporated by reference in their entirety.

BACKGROUND

[0002] In many power systems (e.g., those used in hard disk drive (HDD) and solid state drive (SSD) applications), power circuits (e.g., switching regulators) are commonly used to supply power to different components. Each power circuit typically includes multiple switches (e.g., field-effect transistors (FETs)) that switch on and off at a high frequency. For example, a power circuit (e.g., a switching regulator) may include a high-side FET coupled to a low-side FET, wherein the high-side FET switches off when the low-side FET switches on, and vice versa.

[0003] A power system may include multiple power circuits that may reside on one or more integrated circuits (ICs). These ICs typically reside on a printed circuit board assembly (PCBA) that includes ground and power planes. However, as a result of the high frequency on/off switching in the power circuits, undesirable noise can be generated and coupled into the ground and power planes of the PCBA. In instances where the switching signals from switches in multiple power circuits line up, the noise on the ground or power plane may be magnified, thereby causing electromagnetic interference (EMI) issues.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] FIG. 1 shows a power system according to an embodiment of the present invention comprising control circuitry coupled to multiple power circuits and a register block.

[0005] FIG. 2 shows a power circuit coupled to control circuitry according to an embodiment of the present invention.

[0006] FIG. 3A shows an example noise scenario that control circuitry in the various embodiments of the invention can mitigate. FIG. 3B shows the switch, nodes in a power circuit (e.g., switching regulator) and various potential undesirable noise scenarios.

[0007] FIG. 4A is a flow diagram according to an embodiment of the present invention wherein a first high-side (HS) switch is delayed from turning on when one or more other HS switches are ready to turn on substantially concurrently with the first HS switch when the first HS switch has a lower prior than the other HS switches.

[0008] FIG. 4B is a flow diagram according to an embodiment of the present invention wherein a first high-side (HS) switch is delayed from turning off when one or more other HS or low-side (LS) switches are ready to turn on substantially concurrently with the first HS switch when the first HS switch has a lower prior than the other HS and LS switches.

[0009] FIG. 4C is a flow diagram according to an embodiment of the present invention wherein a first LS switch is delayed from turning off when one or more other LS or HS switches are ready to turn on substantially concurrently with the first LS switch when the first LS switch has a lower prior than the other LS and HS switches.

[0010] FIG. 5A shows power system according to an embodiment of the present invention comprising two integrated circuits (ICs) wherein each IC comprises a charge pump and control circuitry.

[0011] FIG. 5B shows an example noise scenario that control circuitry in the various embodiments of the invention can mitigate.

DETAILED DESCRIPTION

[0012] In many Application Specific Integrated Circuit (ASIC) devices (e.g., those used in HDD and SSD applications), power circuits (e.g., switching regulators) are commonly used to supply power to different components. Each power circuit typically introduces some amount of noise into the ground or power planes of the printed circuit board assembly (PCBA) in which the power circuit is used. There are instances where the switching signals from multiple power circuits line up in time and the noise on the ground or power plane is magnified. This can cause electromagnetic interference (EMI) issues. For example, in an HDD application, if and when the switching signals from multiple power circuits line up in time, the resulting noise may rise to an unacceptable level with respect to the PCBA's overall design specification.

[0013] In particular, as the form factor of HDDs and SSDs becomes smaller, the thickness of the PCBAs that are used continues to decrease. Many of such storage devices have overall thickness in the millimeter range. This leads to the ground layers of the PCBAs getting thinner. Indeed, sometimes ground layers are removed all together to achieve the thickness requirement in small form factor storage devices. In either case, less copper is used for the ground plane, which can increase the overall system's susceptibility to noise. Thus there is a need to mitigate noise stemming from the operation of power circuits such as switching regulators.

[0014] One example of such noise occurs when a high-side (HS) FET turns off, at which point the recirculation current of the body diode causes the voltage to go below zero volts. A similar phenomenon occurs when a low-side (LS) FET turns off. If one or more power circuits happen to switch off substantially concurrently, the amplitude of the noise is magnified. Thus some embodiments of the invention provide control circuitry to control HS and LS switches (e.g., FETs) in multiple power circuits so as to prevent HS switches from turning on or off substantially concurrently, and the LS switches from turning off substantially concurrently. In other embodiments, this concept is application to charge pumps used in, for example, ASICs.

[0015] Certain embodiments of the invention will now be described. These embodiments are presented by way of example only, and are not intended to limit the scope of the invention. Various omissions, substitutions and changes in the form of the universal test connector and disk drive tester described herein may be made without departing from the spirit of the invention. To illustrate some of the embodiments, reference will now be made to the figures.

[0016] FIG. 1 shows a power system 100 according to an embodiment of the present invention comprising control

circuitry **102**, a plurality of power circuits **1-N**, a register block **104**, and a serial port **106**. In the embodiment shown in FIG. 1, each power circuit provides an independent power output (POUT) and comprises a high-side (HS) and a low-side (LS) driver, an HS and an LS switch, an HS and an LS detector, and an inductor-capacitor (LC) circuit. In the embodiment shown in FIG. 1, each power circuit comprises a switching regulator (e.g., a positive buck switching regulator, a negative switching regulator, or a buck-boost switching regulator). In an embodiment, one or more of the power circuits **1-N** comprises part of a charge pump. The power circuits **1-N** may be used, for example, to supply power to various components of a data storage device such as a hard disk drive (HDD) or solid state drive (SSD). For example, one power circuit may be used to supply power to a System on a Chip (SOC) controlling operations of a HDD and other power circuits may be used to supply power to other components such as servo-mechanical components. In one embodiment, the control circuitry **102**, the power circuits **1-N** (excluding the LC circuits), and the register block **104** reside on a common integrated circuit (IC) (e.g., an ASIC).

[0017] For each of the power circuits **1-N** in the embodiment shown in FIG. 1, the control circuitry **102** is coupled to the inputs of the HS driver **110** and the LS driver **112** of the power circuit **1**, the outputs of the HS driver **110** and the LS driver **112** are coupled to respective inputs of the HS switch **114** and the LS switch **116**, and the outputs of the HS switch **114** and the LS switch **116** are coupled to the input of the LC circuit **118**. In one embodiment, each HS and LS switch comprises a FET (e.g., an N-channel FET). In another embodiment, each HS and LS switch may comprise, for example, a P-channel FET or other suitable switching transistor or device.

[0018] In the embodiment in FIG. 1, the input of the HS detector **120** is coupled to the output of the HS driver **110** and the input of the HS switch **114**, and the output of the HS detector **120** is coupled to the control circuitry **102**. In an embodiment, the HS detector **120** is configured to detect the present state of the HS switch **114** (i.e., whether the HS switch **114** is on or off), and provide a signal to the control circuitry **102** indicating that state. In the embodiment in FIG. 1, the input of the LS detector **122** is coupled to the output of the LS driver **112** and the input of the LS switch **116**, and the output of the LS detector **122** is coupled to the control circuitry **102**. In an embodiment, the LS detector **122** is configured to detect the present state of the LS switch **116** and provide a signal to the control circuitry **102** indicating that state. In the embodiment shown in FIG. 1 the outputs of the HS switch **114** and the LS switch **116** are coupled to the input of the LC circuit **118**, and the output of the LC circuit **118** provides the power output (POUT **1**) of the power circuit **1**. In an embodiment, the LC circuit **118** comprises an inductor and a capacitor.

[0019] In the embodiment shown in FIG. 1, the register block **104** is coupled to the circuitry **102** and the serial port **106** and comprises a non-volatile semiconductor memory (NVSM) **108**, wherein the NVSM **108** comprises a plurality of addressable memory locations A_1-A_N . The NVSM **108** may comprise, for example, flash memory or other type of NVSM. In one embodiment, each of the addressable memory locations A_1-A_N comprises one or more settings associated with one of the HS and LS switches in each of the power circuits **1-N**. In an embodiment, the one or more settings in each addressable memory location comprises a

priority ranking that determines a switching order for the HS or LS switch associated with that addressable memory location with respect to the other HS and LS switches. Thus, in that embodiment each HS and LS switch has a unique priority ranking with respect to the other HS and LS switches. In one embodiment, the serial port **106** enables a user to change the priority ranking of each of the HS and LS switches in each power circuit. In one embodiment, a user can disable the priority ranking setting for each of the HS and LS switches.

[0020] In operation, the control circuitry **102** is operable to detect the present state of each HS and LS switch in each of the power circuits **1-N** via a signal received from each respective HS and LS detector. The control circuitry **102** is further operable to prevent two or more of the HS switches from substantially concurrently switching on or off, or two or more HS switches and one or more LS switches from substantially concurrently switching off, or two or more LS switches from substantially concurrently switching off. In one embodiment, the control circuitry **102** is further operable to obtain a priority rank for each of the HS and LS from a priority setting in an associated addressable memory location A_1-A_N in the NVSM **108** in the register block **104**.

[0021] In one embodiment, the control circuitry **102** is operable to use the priority ranking to prevent two or more of the HS switches from substantially concurrently switching to the same state (on or off) by allowing the HS switch with the highest priority to switch on or off while delaying (in order of priority rank) each of the other HS switches from switching, to the same state. In an embodiment, each of the other HS switches is delayed by an increasing de lay time based on their priority rank. For example, if three HS switches are ready to switch on, the control circuitry **102** allows the HS switch with the highest priority to switch on, delays the HS switch with the next highest priority from switching on by a first time delay (first set amount of time), and delays the HS switch with the lowest priority from switching on by a second time delay, wherein the second time delay is longer than the first.

[0022] In one embodiment, the control circuitry **102** is operable to use the priority ranking to prevent two or more of the HS and LS switches from substantially concurrently switching off by allowing the HS switch or LS with the highest priority to switch off while delaying (in order of priority rank) each of the other HS switches from switching off. In one embodiment, the control circuitry **102** is operable to use the priority ranking to prevent two or more LS switches from substantially concurrently switching off by allowing the LS switch with the highest priority to switch off while delaying (in order of priority ranking) each of the other LS switches from switching off.

[0023] FIG. 2 shows control circuitry **202** coupled to a power circuit **203** according to an embodiment of the present invention, wherein the power circuit **203** comprises HS driver **210**, LS driver **212**, HS switch **214**, LS switch **216**, LC circuit **218**, HS detector **220**, and LS detector **222**. In the embodiment in FIG. 2, the LC circuit **218** comprises an inductor **224** and a capacitor **226**. In one embodiment, the LC circuit **218** also comprises a feedback network in addition to an inductor and capacitor. In the embodiment in FIG. 2 the power circuit **203** comprises a switching regulator, wherein the HS switch **214** and the LS switch **216** each comprise a NFET. In another embodiment, the HS and LS

switches may each comprise a PFET or other type of transistor suitable for a fast switching power application.

[0024] In the embodiment shown in FIG. 2, the control circuitry 202 is coupled to the inputs of the HS driver 210 and the LS driver 212, the outputs of the HS and LS drivers are coupled to the respective gate terminals (inputs) of the HS switch 214 (NFET) and the LS switch 216 (NFET), the drain terminal of the HS switch 214 is coupled to a supply voltage, and the source terminal of the LS switch 216 is coupled to ground. In the embodiment shown in FIG. 2, the source terminal (output) of the HS switch 214 is coupled to the drain terminal (output) of the LS switch, a first end of the inductor 224 and an input of the HS detector at node 228, the second end of the inductor 224 is coupled to a first end of the capacitor 226 at node 230, and a second end of the capacitor 226 is coupled to ground. Node 230 also provides the power output (POUT) of the power circuit 203. In the embodiment in FIG. 2, an input of the HS detector 220 is coupled to the output of the HS driver 210 and the gate terminal of the HS switch 214, the output of the HS detector 220 is coupled to the control circuitry 202, an input of the LS detector 222 is coupled to the output of the LS driver 212 and the gate terminal of the LS switch 216, another input of the LS detector is coupled to ground, and the output of the LS detector 222 is coupled to the control circuitry 202.

[0025] In the embodiment in FIG. 2, the control circuitry 202 is operable to detect the present state (on state or off state) of the HS switch 214 via a signal 232 provided by the HS detector 220, and prevent the HS switch 214 from switching on or off substantially concurrently with one or more other HS switches in other power circuits (such as power circuits 1-N shown in FIG. 1) by delaying the HS switch 214 from switching on, or off if it has a lower prior rank than the other HS switches or allowing the HS switch 214 to switch on or off first if it has a higher prior rank. Similarly, the control circuitry 202 is operable to detect the present state of the LS switch 216 via a signal 234 provided by the LS detector 222, and prevent the LS switch 216 from switching off substantially concurrently with another LS or HS switch in another power circuit by delaying the LS switch 216 from switching off if it has a lower prior rank than the other LS or HS switches or allowing the LS switch 216 to switch first if it has a higher prior rank.

[0026] FIG. 3A shows an example noise scenario that can be mitigated by the control circuitry in various embodiments of the present invention. Shown in FIG. 3A is an oscilloscope output showing a ground signal 302, a first positive switching regulator (PSR1) signal 304, and a second PSR2 signal. As shown in FIG. 3A, When the PSR1 and PSR2 signals do not turn off at substantially the same time, the ground signal remains at approximately zero volts (0V). However, in an instance (shown by box 308) where the PSR1 and PSR2 signals both turn off substantially concurrently, a noise spike is generated that causes the ground signal 302 to extend below 0V, representing undesirable EMI noise. Embodiments of the invention would prevent the PSR1 and PSR2 signals from substantially concurrently turning off, thus mitigating this condition.

[0027] FIG. 3B shows example switch nodes in a power circuit (voltage signal graph 310), with scenarios A, B, and C showing problematic issues if these are HS and LS switches in multiple power circuits switching states substantially concurrently. In FIG. 3B, voltage signal graph 310 shows an example of overshoot that may occur when an HS

switch is turning on and an example of undershoot that may occur when an LS switch is turning off. In FIG. 3B, scenarios A, B, and C are each depicted with respect to a timeline extending from 0 to T, where T indicates a time when substantially concurrent switching occurs. As shown in FIG. 3B, an HS switch turning on can be problematic if it is occurring substantially concurrently with another HS switch turning on (scenario A). An HS switch turning off can be problematic if it is occurring substantially concurrently with another HS switch turning off or another LS switch turning off (scenario B). An LS switch turning off can be problematic if it is occurring substantially concurrently with another LS switch turning off or another HS switch turning off (scenario C). Although each of the scenarios only shows the example output of two power circuits (e.g., switching regulators), those skilled in the art would understand that these are just examples and that various embodiments of the invention can address scenarios involving substantially concurrent switching of HS and/or LS switches in two or more power circuits (e.g., three, four, or more).

[0028] FIG. 4A is a flow diagram executed by the control circuitry 102/202 according to an embodiment of the present invention, wherein, before turning a first HS switch on, the control circuitry 102/202 checks whether it is appropriate to turn on the first HS switch by determining if one or more other HS switches are ready to turn on substantially concurrently with the first HS switch (step 402). If one or more other HS switches are not ready to substantially concurrently turn on, the control circuitry 102/202 turns the first HS switch on (step 404). If one or more other HS switches are ready to substantially concurrently turn on, the control circuitry 102/202 determines if the first HS switch has a higher priority rank than the other HS switches (step 406), and if so, turns the first HS switch on without a time delay. In this case, the control circuitry 102/202 determines the switching order of each of the other HS and the time delay that each will incur before turning on based on its priority rank. However, if the first HS switch does not have a higher priority rank than the other HS switches, the control circuitry 102/202 delays the first HS switch from turning on for a set time delay (step 408) and turns the first HS switch on after the time delay expires. The process shown in the flow diagram in FIG. 4A addresses the scenario A in FIG. 3B.

[0029] FIG. 4B is a flow diagram executed by the control circuitry 102/202 according to an embodiment of the present invention, wherein, before turning a first HS switch off, the control circuitry 102/202 checks whether it is appropriate to turn off the first HS switch by determining if one or more other HS or LS switches are ready to turn off substantially concurrently with the first HS switch (step 410). If one or more other HS or LS switches are not ready to substantially concurrently turn-off with the first HS switch, the control circuitry 102/202 turns the first HS switch off without a time delay (step 412). If one or more other HS or LS switches are ready to substantially concurrently turn off with the first HS switch, the control circuitry 102/202 determines if the first HS switch, has a higher, priority rank than the other HS and LS switches (step 414), and if so, turns the first HS switch off without a time delay. In this case, the control circuitry 102/202 determines the switching order of each of the other HS or LS switches and the time delay that each will incur before turning off based on its priority rank. However, if the first HS switch does not have a higher priority rank than the other HS and LS switches, the control circuitry 102/202

delays the first HS switch from turning off for a set time delay (step 416) and turns the first HS switch off after the time delay expires. The process shown in the flow diagram in FIG. 48 addresses the scenario B in FIG. 3B.

[0030] FIG. 4C is a flow diagram executed by the control circuitry 102/202 according to an embodiment of the present invention, wherein, before turning a first LS switch off, the control circuitry 102/202 checks whether it is appropriate to turn off the first LS switch by determining if one or more other LS or HS switches are ready to turn off substantially concurrently with the first LS switch (step 418). If the one or more other LS or HS switches are not ready to substantially concurrently turn off with the first LS switch, the control circuitry 102/202 turns the first LS switch off (step 420). If the one or more other LS or HS switches are ready to substantially concurrently turn off with the first LS switch, the control circuitry 102/202 determines if the first LS switch has a higher priority rank than the other LS and HS switches (step 420), and if so, the control circuitry 102/202 turns the first LS switch off without a time delay. In this case, the control circuitry 102/202 determines the switching order of each of the other LS or HS switches and the time delay that each will incur before turning off based on its priority rank. However, if the first LS switch does not have a higher priority rank than the other LS and HS switches, the control circuitry 102/202 delays the first LS switch from turning off for a set time delay (step 424) and turns the first LS switch off after the time delay expires. The process shown in the flow diagram in FIG. 4C addresses the scenario C in FIG. 3B.

[0031] FIG. 5A shows a power system 500 according to an embodiment of the present invention comprising integrated circuits (ICs) 502 and 504, wherein IC 502 comprises a charge pump 506 and control circuitry 508, and IC 504 comprises a charge pump 510, sense logic 512, and control circuitry 514. In one embodiment, ICs 502 and 504 each comprise an ASIC (Application Specific Integrated Circuit). In the embodiment shown in FIG. 5A, charge pump 510, sense logic 512, and control circuitry 514 reside on a common IC and charge pumps 506 and 510 reside on separate ICs. In one embodiment, charge pumps 506 and 510 reside on a common IC. In the embodiment, shown in FIG. 5A, control circuitry 508 is coupled to charge pump 506 and control circuitry 514, and is operable to control the operation (e.g., the turning on and off) of charge pump 506. Charge pump 506 is configured to supply power and provide an analog signal 516 indicating its present operating state (e.g., whether it is turning on or off) to sense logic 512.

[0032] In the embodiment shown in FIG. 5A, control circuitry 514 is coupled to sense logic 512 and charge pump 510, and is operable to control the operation (e.g., the turning on and off and the output) of charge pump 510 and receive a digital signal 518 from sense logic 512 indicating the present operating state of charge pump 506 (e.g., whether it is turning on or off). Sense logic 512 is configured to detect the present state of charge pump 506 via the analog signal 516 and provide the digital signal 518 to the control circuitry 514 indicating whether charge pump 506 is turning on or off. Similar to charge pump 506, charge pump 510 is also configured to supply power.

[0033] In the embodiment in FIG. 5A, if charge pump 510 is about to be turned on and the digital signal 518 received from sense logic 512 indicates that charge pump 506 is turning on, the control circuitry 514 is further operable to

prevent an output of charge pump 510 from substantially aligning with an output of charge pump 506. By preventing the outputs of charge pumps 506 and 510 from substantially aligning, control circuitry 514 prevents the occurrence of a noise spike that can occur when the charge pump outputs are in substantial alignment. For example, as shown in FIG. 5B, two charge pumps can be turned on and provide outputs 520 and 522, wherein the outputs are in phase and have substantially the same frequency. As shown in the example in FIG. 5B, when the peaks of the two outputs 520 and 522 are in substantial alignment, undesirable noise spikes can occur.

[0034] In one embodiment, the control circuitry 514 is operable to prevent the output of charge pump 510 from substantially aligning with the output of charge pump 506 by delaying the turning on of charge pump 510 by a predetermined amount of time (e.g., several milliseconds). In one embodiment, the control circuitry 514 is operable to prevent the output of charge pump 510 from substantially aligning with the output of charge pump 506 by causing the output of charge pump 510 to be out of phase with the output of charge pump 506. In an embodiment, the control circuitry is operable to cause the output of charge pump 510 to be out of phase with the output of charge pump 506 by phase shifting the output of charge pump 510 by a predetermined amount of phase with respect to the output of charge pump 506. For example the phase shift may be 90 degrees.

[0035] In another embodiment, the charge pumps can be on the same IC (e.g. ASIC), and control circuitry can prevent the output of one charge pump from substantially aligning with the output of the other charge pump, as described above in the embodiment of the invention in FIG. 5A. In yet another embodiment, external control circuitry may be coupled to the charge pumps and control their operation so as to prevent the outputs of the charge pumps from substantially aligning. The external control circuitry may be configurable to assign priority to one of the charge pumps. The same embodiment can be extended to cover multiple (three or more) charge pumps residing in the same or different ICs (e.g., ASICs).

[0036] It is noted that the steps in the flow diagrams in FIGS. 4A, 4B, and 4C are shown in a particular order to illustrate respective embodiments of the invention. In other embodiments, the steps in the flow diagrams in FIGS. 4A, 4B, and 4C may be performed in a different order. Some steps may be combined into fewer steps and some steps may be expanded into more steps.

[0037] Any suitable control circuitry may be employed in the embodiments of the present invention, such as any suitable integrated circuit or circuits. In one embodiment, the control circuitry comprises a microprocessor executing instructions, the instructions being operable to cause the microprocessor to perform the steps of the flow diagrams described herein. The instructions may be stored in any computer-readable medium. In one embodiment, they may be stored on a non-volatile semiconductor memory external to the microprocessor, or integrated with the microprocessor in a SOC. In another embodiment, the control circuitry comprises suitable logic circuitry, such as state machine circuitry.

[0038] The features and attributes of the specific embodiments disclosed above may be combined in different ways to form additional embodiments, all of which fall within the scope of the present disclosure. Although certain embodiments have been disclosed, other embodiments that are

apparent to those of ordinary skill in the art, including embodiments which do not provide all of the features and advantages set forth herein, are also within the scope of this disclosure. Accordingly, the scope of protection is defined only by the claims.

What is claimed is:

1. A power system comprising:
a first charge pump configured to supply power;
control circuitry coupled to the first charge pump, the control circuitry operable to:
receive a signal indicating whether a second charge pump is turning on; and
if the first charge pump is about to be turned on and the signal indicates that the second charge pump is turning on, prevent an output of first charge pump from substantially aligning with an output of the second charge pump.
2. The power system as recited in claim 1, wherein the control circuitry is operable to prevent the output of first charge pump from substantially aligning with the output of the second charge pump by delaying the turning on of the first charge pump by a predetermined amount of time
3. The power system as recited in claim 1, wherein the control circuitry is operable to prevent the output of first

charge pump from substantially aligning with the output of the second charge pump by causing the output of the first charge pump to be out of phase with the output of the second charge pump.

4. The power system as recited in claim 1, wherein the control circuitry is operable to cause the output of the first charge pump to be out of phase with the output of the second charge pump by phase shifting the output of the first charge pump by a predetermined amount of phase with respect to the output of the second charge pump.

5. The power system as recited in claim 1, further comprising sense logic coupled between the second charge pump and the control circuitry, wherein detects a present state of the second charge pump and provides to the control circuitry the signal indicating that the second charge pump is turning on.

6. The power system as recited in claim, wherein the sense logic, the control circuitry and the first charge pump reside on a common integrated circuit.

7. The power system as recited in claim 1, wherein the first charge pump and the second charge pump reside on different integrated circuits.

* * * * *