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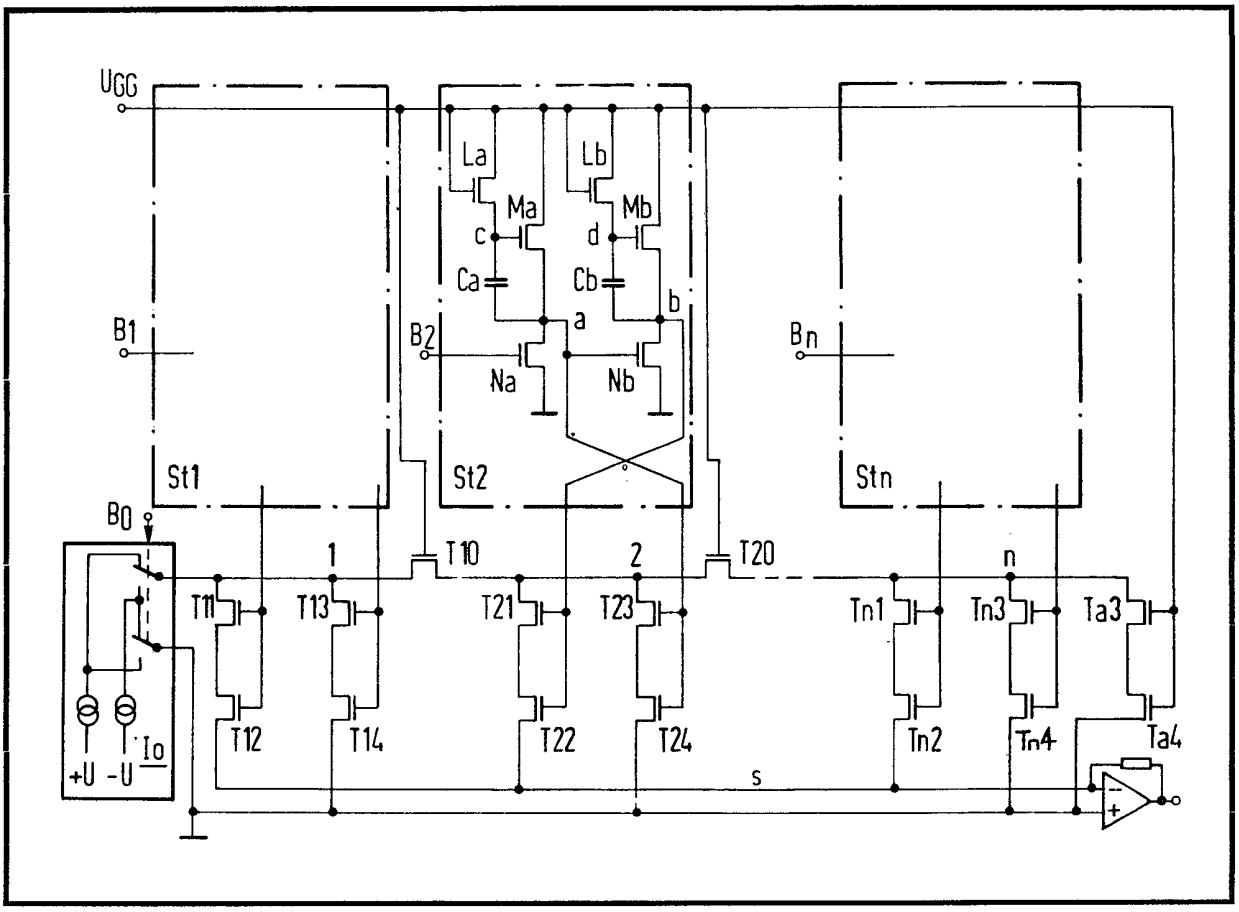
(54) Digital to analogue converter

(57) A digital to analogue converter employs an R–2R network, the resistive elements of which are formed by identical field effect transistors (T10 . . . Tn4), preferably MOS transistors, connected as shown. Current is supplied to one end of the chain from a source (Io). Each shunt element has a control circuit (S*t*1, S*t*2, . . . S*tn*) controlled by a respective bit (B1, B2, . . . B*n*) of the input signal to render conductive one or other of the transistor pairs of that element.

By supplying the gate electrodes of the particular conductive transistor pair and the gate electrodes of the constantly conductive transistors which form the series elements (and also a terminating element (T*a*3, t*a*4) of the network) with one and the same control voltage and by maintaining (virtual) equality of potential on the sum current line and at the base of the constant current source the possibility of inaccuracy due to the resistance values of the individual MOS-transistors deviating from their nominal resistance value R under the influence of different gate-source voltages and gate-drain voltages is reduced. The polarity can be controlled by a sign bit (B_0) fed to the constant current generator.



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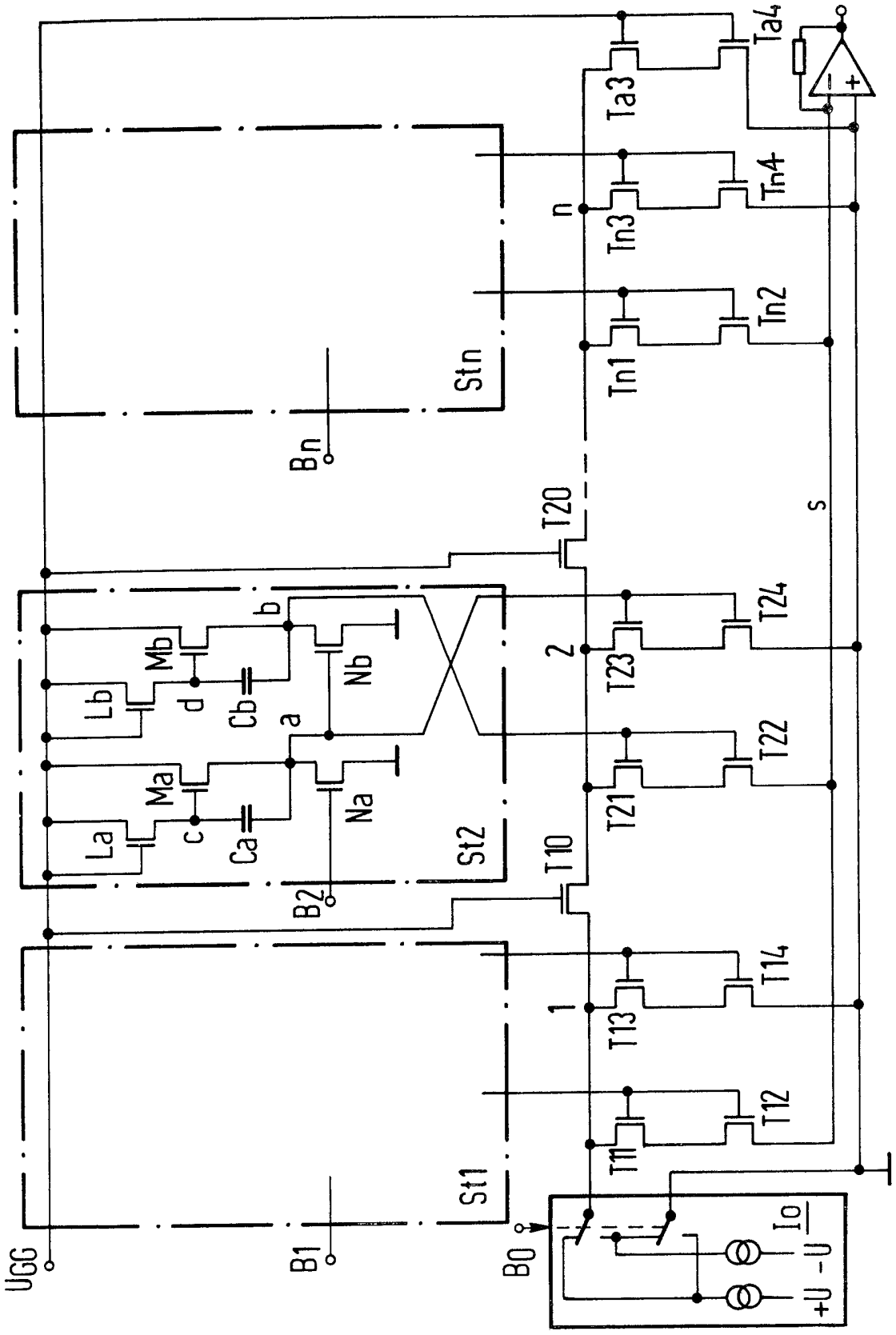
Ta4
Ta3
Tn4
Tn3
Tn2
Tn1
n
Stn
Bn
T20
s
T24
T23
T22
T21
2
Mb
Lb
d
Cb
b
Nb
a
Ma
La
c
Ca
Na
St2
B2
T10
T14
T13
T12
T11
1
St1
B1
B0
UGG
Io
-U
+U

SPECIFICATION

Digital to analogue converter

The invention relates to a digital to analogue converter for converting digital signals, particularly though not exclusively, PCM-signals, which in each case comprise a number of bits, into corresponding analogue signals.

An R–2R network comprises a chain of series-connected resistors resistive elements, all of the same resistance R: the connection points between the elements, and the end connection points of the chain, are connected to shunt resistors or resistive elements. The shunt resistors generally have twice this resistance (2R)—although the resistance at the ends varies with particular designs.

An R–2R network employing resistors is described in German Auslegeschrift 23 15 986 and U.K. patent No. 1 462 246. Here the shunt resistors which are connected to the connection points at the two ends of the chain have a resistance R equal to that of the series resistors all the other shunt resistors being of resistance 2R. The network is part of a digital-analogue converter designed to convert digital signals each comprising $n+m+1$ bits into analogue signals in accordance with a non-linear characteristic curve composed of 2^{m+1} linear sections each containing 2^n amplitude stages. One end of the R–2R chain network forms the analogue signal output. The network has 2^m+n-2 series resistors and hence 2^m+n-1 connection points and 2^m+n-1 shunt resistors. The connection points of a selected group of n adjacent connection points can be selectively supplied with current from a respective one of n constant current sources switched by the n least significant bits of the digital input signal. That connection point of the group of n adjacent connection points which is nearest the output end of the network is spaced from that end by a distance of from 1 to 2^{m-1} connection points. The actual "position" of the group is selected in accordance with the values of the next m bits of the digital signal. The next adjacent connection point, considered in the direction towards the output end of the network, is supplied with a constant current from a further constant current source in the event that at least one of these m bits of the relevant digital signal is formed by a binary "1".

In another arrangement (see for example Elektronik 21 (1972) 2, 39, 40, Fig. 3; 1978 IEEE International Solid-State Circuits Conference, Digest of Technical Papers, 186, 187, top of Fig. 2), all the series resistors possess the resistance value R and all the shunt resistors possess the resistance value 2R: one end of the R-2R-chain network forms the analogue signal output and the other end of the R-2R-chain network is terminated by an additional resistor having the resistance value 2R. In order to convert a digital signal which comprises a number of bits corresponding to the number of shunt resistors, binary voltages corresponding to the bits of the digital signal can be connected to those ends of the shunt resistors which face away from the series resistors. Here the R-2R-chain network can be constructed in that (see for example German Offenlegungsschrift No. 24 23 130 or French patent No. 20 43 946), the series resistive elements are formed by the source-drain-paths of MOS-transistors which are permanently in the conductive state, and the shunt resistive elements are formed by the source-drain-paths of two MOS-transistors or two pairs of MOS-transistors of two groups of MOS-transistors which are connected to voltage sources which are individual to each group and which emit different voltages, which MOS-transistors can be alternatively brought into the conductive state from alternatively activated outputs of a control circuit which can be supplied at its input with one bit of the relevant digital signal, by operation of their control electrodes with the same control potential which is carried by the control electrodes of the MOS-transistors which form the series elements.

One of the two MOS-transistors (or pairs of MOS-transistors) which form those shunt elements of the R–2R network which are arranged at the end of the chain network facing away from the analogue signal output, is connected in parallel with an additional MOS-transistor (or pair of MOS-transistors) which is constantly in the conductive state.

The accuracy of the digital-analogue conversion in a R–2R network of this kind is dependent not only upon the geometrical tolerances of the MOS-transistors but also to a large extent upon the influence of the particular control electrode/source voltage and control electrode/drain voltage upon the resistance of the conductive MOS-transistor; as a result the resistance values of the individual MOS-transistors deviate relatively considerably in both directions from a theoretically standard resistance value R in dependence upon the bit combination of the particular digital signal so that the digital-analogue conversion can involve an error of up to 20%.

Another design of R–2R network is described in "Electronics" 45 (1972) 12, 83, 87, 90, Fig. 5, and in 1978 IEEE International Solid-State Circuits Conference, Digest of Technical Papers, 186, 187, bottom of Fig. 2. Again all the series resistors have the resistance value R and all the shunt resistors possess the resistance value 2R. A constant current is fed in at the point of connection between the shunt resistor connected to one end of the R-2R-chain network and the adjacent series resistor, and the other end of the R-2R-chain network is terminated by an additional resistor having the resistance value 2R;

in order to convert a digital signal which comprises a number of bits corresponding to the number of shunt resistors, those ends of the shunt resistors which face away from the series resistors can be directly connected, in accordance with the bits of the digital signal, to the opposite pole of the constant current source or to a sum current line which carries the same potential and which forms the analogue signal output.

According to the present invention there is provided a digital to analogue converter comprising a chain of series-connected resistive elements each formed by the source-drain path of one of a plurality of field effect transistors the gate electrodes of which are connected to a bias line for the application of a turn on bias potential, the connection points between the elements and the end connection points of the chain each being connected to a respective shunt resistive element comprising a first pair of field effect transistors with their source-drain paths connected in series between the connection point and an earth line and a second pair of field effect transistors with their source-drain paths connected in series between the connection point and a common current summing line which, in use, assumes a potential substantially equal to that of the earth line and from which the analogue output of the converter can be obtained, a constant current source connected to one end of the chain, a further pair of MOS transistors with their source-drain paths connected in series between the other end of the chain and the earth line and their gate electrodes connected to the bias line, all of said field effect transistors being substantially identical, and a plurality of control sections each associated with a respective shunt element and having an input for connection to a respective bit line of a digital input signal, and arranged in operation according to the binary value represented by the state of that bit line to select the first or second pair of transistors of its associated shunt element and to render the selected pair conductive by applying to the gate electrodes thereof a control potential substantially equal to the potential of the bias line.

Preferably said field effect transistors are MOS field effect transistors.

In a preferred arrangement at least the transistors are integrated on a single chip.

If desired, it may be provided that the constant current generator has an input for connection to a further bit line of the digital input signal and is responsive, in use, to the state of this line to reverse the polarity of the current supplied by the generator.

An exemplary embodiment of the invention will now be described with reference to the accompanying drawing, which is a circuit diagram of a digital to analogue converter according to the invention.

The converter is designed for converting digital signals, especially PCM signals which each comprise a number of bits B_0, B_1, B_2, ... B_n, into corresponding analogue signals. The basic component of the converter is an R–2R network which is constructed with MOS-transistors which are identical to one another and which will be assumed to be integrated on a chip. In this embodiment these transistors are all N-channel-MOS-transistors of the enhancement type.

This R-2R-chain network comprises series resistive elements in the form of MOS-transistors T10, T20, ... whose source-drain paths form the series resistances of the R–2R network. The gate electrodes of these MOS-transistors are connected to a bias voltage U_{GG} of for example + 12 V so that they are constantly maintained in a conductive state.

The shunt elements of the R–2R network are formed by MOS-transistors T11–T12, T13–T14; ... T*n*1–T*n*2, t*n*3–T*n*4. Each element comprises four transistors: a first pair of MOS transistors T13, T14; T23, T24; ... T*n*3, T*n*4 with their source-drain paths connected in series, and a second pair T11, T12; T21, T22; ... T*n*1, T*n*2; again with their source-drain paths connected in series. Each shunt element is assigned a respective control circuit S*t*1 ... S*tn*.

Each first pair of MOS-transistors, such as for example the pair T23–T24, is connected between the relevant connection point (2) between series element(s) and a shunt element of the R–2R network and the opposite pole (earth) of a constant current source I*o* which feeds in, at the connection point 1 at one end of the chain, a constant current (of for example 200 μA) the polarity of which is determined by the sign bit B_0 of the particular digital signal which is to be converted. A constant current source of this kind which serves to produce bipolar constant currents can be designed in known manner (for example as disclosed in Elektronik 21 (1972) 5, 165, 167, Fig. 12) for which reason it will not be discussed further here. At its end remote from the constant current source I*o*, the R–2R–chain network is terminated by a pair of series-connected MOS-transistors T*a* 3–T*a*4 which form a 2R resistor and whose gate electrodes are permanently connected to the aforementioned bias voltage U_{GG} so that the pair of MOS-transistors t*a*3–T*a*4 is constantly in the conductive state.

The second pairs of MOS-transistors, for example the pair T21–T22, are each arranged between the relevant connection point, for example the connection point 2, and the analogue signal output formed by a sum current line *s*. In the arrangement shown in the drawing this sum current line *s* is connected to the inverting input (−) of an operational amplifier whose non-inverting input (+) is connected to the earth line. Consequently the

sum current line *s* is constantly maintained at the same potential (virtual earth) as the earth line.

As illustrated in the drawing in respect of the control circuit –S*t*2, the control circuits S*t*1, ... S*tn* each possess two inverters connected in cascade and which comprise MOS-transistors N*a*, N*b*. These MOS-transistors N*a*, N*b* are each connected by their one main electrode to the base of the constant current source (earth), whereas the other main electrode is in each case connected via a bootstrap circuit C*a*, L*a*, M*a*; C*b*, L*b*, M*b* likewise constructed with MOS-transistors M*a*, L*a*; M*b*, L*b* to the bias line which carries the aforementioned bias voltage U_{GG} of for example + 12 V. Here again all the MOS-transistors of the control circuits S*t* will be assumed to be formed by N-channel MOS-transistors of the enhancement type.

The gate electrode of the MOS-transistor N*a* which forms the one inverter is supplied with the bit B_2 of the digital signal to be converted. It is assumed that a "1" bit is represented by a potential of + 10 V and a "0" bit by a potential of 0 V; this voltage appears at the control electrode of the MOS-transistor N*a*. In the former case, i.e. when a "1" bit is supplied, the MOS-transistor N*a* is brought into the conductive state and a potential of approximately 0 V occurs at circuit point *a*; at the same time the MOS-transistor N*a* is conductive and initially so is the MOS-transistor L*a* until a potential of approximately + 10 V occurs at the circuit point *c*. Simultaneously the MOS-transistor N*b* is brought into the blocked state and a potential of + 12 V occurs at the circuit point *b* and a potential of approximately + 20 V occurs at the circuit point *d*, owing to the charge remaining on the capacitor *cb*. Thus the control circuit S*t*2 causes the MOS-transistors T21–T22 (the second pair) of the R–2R network, whose gate electrodes are connected to the circuit point *b*, to be rendered conductive, whereas the MOS-transistors T23–T24 (the first pair), whose control electrodes are connected to the circuit point *a*, are rendered non-conducting.

In the second situation, i.e. when a "0" bit is supplied, the MOS-transistor N*a* is turned off and at the circuit point *c* the potential shifts to approximately + 20 V, whereas a potential of + 12 V occurs at the circuit point *a* and at the same time the MOS-transistor N*b* is rendered conductive and a potential of approximately 0 V occurs at circuit point *b* and a potential of approximately + 10 V occurs at circuit point *d*. The control circuit S*t*2 thus brings the first pair of MOS-transistors T23–T24 into the conductive state whereas the second pair of MOS-transistors T21–T22 is brought into the blocked state.

Although this has not been shown in detail in the drawing, the other control circuits S*t*1, ... S*tn* are also designed similarly and control the pairs of MOS-transistors of the R–2R network to which they are connected in a similar manner.

When the control circuits S*t* are designed as illustrated in the drawing with two MOS-transistor inverters which are each connected to a bootstrap circuits, the function of these bootstrap circuits is to connect the full control voltage U_{GG} to the gate electrodes of that pair of MOS-transistors of the network which is to be brought into the conductive state. Alternatively, the control circuits S*t* could be designed in that the MOS-transistors which form the inverters are each connected to the line carrying the bias voltage U_{GG} via an N-channel MOS-transistor of the depletion type acting as load resistor. Control circuits of this type are basically known (e.g. from the German Offenlegungsschrift 24 23 130, for which reason they will not be discussed in detail here. Furthermore the control circuits can also consist of bistable trigger circuits provided with corresponding load elements so that again the full bias voltage U_{GG} is connected to the gate electrodes of the relevant pair of MOS-transistors of the R–2R network. This need not be discussed in detail either.

The control circuits S*t*1, ... S*tn* which are supplied at their inputs with the individual bits $B_1 \ldots B_n$ of the digital signal which is to be converted, thus feed the gate electrodes of the MOS-transistors T*i*1–T*i*2 or T*i*3–T*i*4 of the relevant one of the two pairs of MOS-transistors with the same control voltage U_{GG} which is connected to the gate electrodes of the permanently conductive MOS-transistors T10, T20 ... and T*a*3–T*a*4; the MOS-transistors T*i*3–T*i*4 or T*i*1–T*i*2 of the other pair of MOS-transistors operated by the relevant control circuit S*ti* are fed, at their gate electrodes, with a control voltage which lies below the threshold voltage of the MOS-transistors. Thus, in accordance with the bit B_i of the digital input signal supplied to the relevant control circuit S*ti*, one of the two pairs of MOS-transistors is conductive: i.e. on the occurrence of a bit "0" it is the first pair of MOS-transistors T*i*3–T*i*4 which leads to the earth line of the constant current source I*o* which is conductive, whereas on the occurrence of a "1" bit it is the second pair of MOS-transistors T*i*1–T*i*2 which leads to the sum current line *s* (which is (virtually) maintained at the same potential and which forms the analogue signal output) which is conductive.

Under the influence of different gate-source voltages and gate-drain voltages, the resistance values of the individual MOS-transistors deviate to a greater or lesser extent from a nominal resistance value R which is standard for all the MOS-transistors, in that under the given condition, when the constant current fed into the R–2R network from the constant current source I*o* has a positive (negative)

sign, the resistance of that MOS-transistor T*i*1, T*i*3 of a pair of MOS-transistors arranged in a shunt element of the network which is nearest the series arm of the network is greater (smaller) than the resistance value of that MOS-transistor T*i*2, T*i*4, of the relevant pair which is remote from the series arm. However, the fact that the gate electrodes of the particular conductive MOS-transistors of the shunt elements, and the gate electrodes of the constantly conductive MOS-transistors which form the series elements and of the terminal element (T*a*3, T*a*4) are supplied with one and the same voltage U_{GG}, in association with the (virtual) equality of potential of the sum current line *s* which forms the analogue signal output and the earth line of the constant current source I*o* ensures that the resistance value of each series MOS-transistor T*i*0 is very closely equal to the resistance value of the MOS-transistor T*i*1 or T*i*3 to which it is directly connected on the current source side and which belongs to the currently conductive pair of MOS-transistors T*i*1–T*i*2 and T*i*3–T*i*4 which forms the shunt resistor. The resistance value of the particular other MOS-transistor of the currently conductive pair of MOS-transistors is, apart from negligible deviations, equal to the resistance value of the remaining part of the R–2R network which faces away from the current source. Consequently, in response to a digital signal $B_0B_1B_2 \ldots B_n$ which is to be converted, a sum current

$$I = \sum_{i=1}^{n} B_i \cdot I_o/2^i,$$

which represents an analogue signal, corresponding with a high degree of accuracy to the digital signal occurs on the sum current line *s*, with the sign being determined by B_0.

Finally it should be noted that the above described exemplary embodiment is based on the use of N-channel MOS-transistors but instead it would also be possible to use P-channel-MOS-transistors of the enhancement type in which case it would be necessary to provide a bias voltage $U_{GG} = -12$ V.

This converter thus provides a circuit arrangement for digital-analogue conversion employing an R–2R network of the type described earlier in which the resistive elements of the R–2R network are formed by MOS-transistors; the elements which possess the resistance value 2R are formed by a pair of two identical, series-connected MOS-transistors having the resistance value R. An R–2R network of this kind facilitates precise digital-analogue conversion if one has a correspondingly precise resistance value R in all the MOS-transistors so that the accuracy with which the digital-analogue conversion takes place is again dependent upon the geometrical tolerances of the transistors and upon the influence of the gate-source voltages and the gate-drain voltages upon the resistors of the conductive transistors. The arrangement decribed reduces the impairment of the accuracy of the digital-analogue conversion due to the influence of control electrode source voltages and control electrode drain voltages upon the resistances of conductive MOS-transistors.

Thus we have a circuit arrangement for converting digital signals, especially PCM-signals, which each comprises a number of bits into corresponding analogue signals, employing an R–2R–chain network which consists of series resistors having the resistance value R and shunt resistors having the resistance value 2R,

(a) into which (network) a constant current is fed in at the point of connection between the shunt resistor arranged at one end of the R–2R–chain network and the adjacent series resistor,

(b) whose other end is terminated by an additional resistor having the resistance value 2R and

(c) in which, in order to convert a digital signal comprising a number of bits corresponding to the number of shunt resistors, those ends of the shunt resistors which face away from the series resistors can be connected, in accordance with the bits of the digital signal, either directly to the opposite pole of the constant current source or to a sum current line which is (virtually) maintained at the same potential and which forms the analogue signal output,

(d) wherein all the resistors of the R–2R–chain network are formed by the source-drain paths of MOS-transistors which are integrated on a chip, are connected individually or in series, and which are identical to one another; and in which:

(e) the MOS-transistors which, with the source-drain paths of two pairs of series-connected MOS-transistors, form the shunt resistors of the R–2R–chain network, belong to two groups of pairs of MOS-transistors, of which

(f) the individual pairs of MOS-transistors which belong to the one group of pairs of MOS-transistors are each arranged between the relevant connection point of series resistor and shunt resistor of the R–2R–chain network and the opposite pole of the constant current source which supplies the constant current with a sign determined by the digital signal and

(g) those individual pairs of MOS-transistors which belong to the other group of pairs of MOS-transistors are in each case arranged between the relevant connection point of series resistor and shunt resistor on the R–2R–chain network and the sum current line, wherein

(h) the two pairs of MOS-transistors can each be alternatively brought into the conductive state by a control circuit which can be supplied at its input with one bit of the relevant digital signal, in that their control electrodes are operated with the same control potential as is carried by the control electrodes of the MOS-transistors whose source-drain paths form series resistors of the R–2R–chain network and which constantly remain in the conductive state.

CLAIMS

1. A digital to analogue converter comprising: a chain of series connected resistive elements each formed by the source-drain path of one of a plurality of field effect transistors the gate electrodes of which are connected to a bias line for the application of a turn on bias potential, the connection points between the elements, and the end connection points of the chain, each being connected to a respective shunt resistive element comprising a first pair of field effect transistors with their source-drain paths connected in series between the connection point and an earth line and a second pair of field effect transistors with their source-drain paths connected in series between the connection point and a common current summing line which, in use, assumes a potential substantially equal to that of the earth line and from which the analogue output of the converter can be obtained; a constant current source connected to one end of the chain; a further pair of field effect transistors with their source-drain paths connected in series between the outer end of the chain and the earth line and their gate electrodes connected to the bias line, all of said field effect transistors being substantially identical; and a plurality of control sections each associated with a respective shunt element and having an input for connection to a respective bit line of a digital input signal, and arranged in operation according to the binary value represented by the state of that bit line to select the first or second pair of transistors of its associated shunt element and to render the selected pair conductive by applying to the gate electrodes thereof a control potential substantially equal to the potential of the bias line.

2. A digital to analogue converter according to claim 1, in which said field effect transistors are MOS field effect transistors.

3. A digital to analogue converter according to claim 1 or 2, in which at least the transistors are integrated on a single chip.

4. A digital to analogue converter according to claim 1, 2 or 3, in which the constant current generator has an input for connection to a further bit line of the digital input signal and is responsive, in use, to the state of this line to reverse the polarity of the current supplied by the generator.

5. A digital to analogue converter substantially as herein described with reference to the accompanying drawing.

6. A digital to analogue converter comprising: a chain of series connected resistive elements each formed by the source-drain path of one of a plurality of field effect transistors the gate electrodes of which are connected to a bias line for the application of a turn on bias potential, the connection points between the elements, and the end connection points of the chain, each being connected to a respective shunt resistive element comprising a first pair of field effect transistors with their source-drain paths connected in series between the connection point and an earth line and a second pair of field effect transistors with their source-drain paths connected between the connection point and a common current summing line which, in use, assumes a potential substantially equal to that of the earth line and from which the analogue output of the converter can be obtained; a constant current source connected to one end of the chain; a further resistive element connected between the other end of the chain and the earth line and their gate electrodes connected to the bias line, all of said field effect transistors being substantially identical; and a plurality of control sections each associated with a respective shunt element and having an input for connection to a respective bit line of a digital input signal, and arranged in operation according to the binary value represented by the state of that bit line to select the first or second pair of transistors of its associated shunt element and to render the selected pair conductive by applying to the gate electrode of at least one of them a control potential substantially equal to the potential of the bias line, the remaining transistor, if any, of the pair having its gate electrode connected to the bias line.

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