(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
24 April 2008 (24.04.2008)

PCT

(10) International Publication Number
WO 2008/048130 A1

(51) International Patent Classification:
G06F 17/50 (2006.01) *H04L 12/00* (2006.01)

(21) International Application Number:
PCT/RU2006/000532

(22) International Filing Date: 16 October 2006 (16.10.2006)

(25) Filing Language: English

(26) Publication Language: English

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LV, LY, MA, MD, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

WO 2008/048130 A1

(54) Title: SYSTEM AND METHOD FOR ELECTROMIGRATION TOLERANT CELL SYNTHESIS

(57) Abstract: A method, data processing system, and computer program product are provided for routing a circuit placement a number of times, resulting in a number of routings. An electromigration quality value is computed for each of the routings, and the routing with the best electromigration quality value is selected. In one embodiment, each routing is analyzed with attention to the the current that passes through each of the routing's segments in order to compute a current distribution that is used to compute a routing quality vector. In another embodiment, multiple placements are generated and the electromigration placement quality vectors are computed for the various placements with the placement with the best electromigration quality vector being selected. In one embodiment, the placement with the best electromigration quality vector is routed the number of times to determine the routing with the lowest (best) electromigration quality value.

System and Method for Electromigration Tolerant Cell Synthesis

Field of the Invention

[0001] The present invention relates generally to a system and method for designing circuits with improved electromigration characteristics. More particularly, the present invention relates to a system and method for generating electromigration quality vectors to select circuit placements and routings.

Related Art

[0002] Electromigration is the transport of material caused by the gradual movement of the ions in a conductor due to the momentum transfer between conducting electrons and diffusing metal atoms. The effect is seen in applications where high direct current densities are used, such as in microelectronics and related structures. As the structure size in electronics such as integrated circuits (ICs) decreases, the practical significance of this effect increases. Research the field of electromigration was pioneered by James R. Black, who set the basis for all research in this area and for whom the Black equation is named.

[0003] Electromigration decreases the reliability of ICs. In the worst case it leads to the eventual loss of one or more connections and intermittent failure of the entire circuit. Since the reliability of interconnects is not only of great interest in the field of space travel and for military purposes but also with civilian applications like for example the anti-lock braking system of cars, high technological and economic values are attached to this effect.

[0004] Due to the relatively high life span of interconnects and the short product lifecycle of most consumer ICs, it is not practical to characterize a product's electromigation under real operating conditions. A mathematical equation, the Black equation, is commonly used to predict the life span of interconnects in

integrated circuits tested under "stress", that is external heating and increased current density, and the model's results can be extrapolated to the device's expected life span under real conditions.

[0005] Although electromigration damage ultimately results in failure of the affected IC, the first symptoms are intermittent glitches, and are quite challenging to diagnose. As some interconnects fail before others, the circuit exhibits seemingly random errors, which may be indistinguishable from other failure mechanisms (such as electro-static discharge (ESD) damage.) In a laboratory setting, electromigration failure is readily imaged with an electron microscope, as interconnect erosion leaves telltale visual markers on the metal layers of the IC.

[0006] With increasing miniaturization the probability of failure due to electromigration increases in Very Large Scale Integrated (VLSI) circuits because both the power density and the current density increase. In advanced semiconductor manufacturing processes, copper has replaced aluminum as the interconnect material of choice. Despite its greater fragility in the fabrication process, copper is preferred for its superior conductivity. It is also intrinsically less susceptible to electromigration. However, electromigration continues to be an everpresent challenge to device fabrication, and therefore the EM research for copper interconnects is ongoing.

[0007] During the circuit development process, many metrics are used to ascertain a circuit's expected performance and other characteristics. These metrics are also used to compare the expected characteristics of one circuit design to the expected characteristics of another circuit design. Yet traditional metrics fail to adequately ensure electromigration tolerant standard cell layouts. One approach to avoiding electromigration issues is to widen wire widths. However, this approach results in extra wiring space and larger circuit areas.

Brief Description of the Drawings

[0008] The present invention may be better understood, and its numerous objects, features, and advantages made apparent to those skilled in the art by referencing the accompanying drawings, wherein:

Figure 1 is a high-level flowchart showing overall processing steps;
Figure 2 is a flowchart showing the steps to select a placement with desired electromigration qualities;
Figure 3 is a flowchart showing the steps taken to compute a placement quality vector for a given placement;
Figure 4 is a flowchart showing the steps taken to select a routing of a selected placement with desired electromigration qualities;
Figure 5 is a flowchart showing the steps taken to compute a routing quality vector for a given routing of the selected placement; and
Figure 6 is a block diagram of a data processing system in which the methods described herein can be implemented.Detailed Description

[0009] The following is intended to provide a detailed description of an example of the invention and should not be taken to be limiting of the invention itself. Rather, any number of variations may fall within the scope of the invention, which is defined in the claims following the description.

[0010] **Figure 1** is a high-level flowchart showing overall processing steps for designing a circuit with desired electromigration qualities. The result of the processing shown in **Figure 1** is a circuit design with desirable electromigration characteristics, both in terms of cell placement as well as routing of the placement.

[0011] Processing commences at **100**, whereupon, at step **110**, unfolded netlist **115** is received as input. Unfolded netlist is a circuit design representation of a desired circuit. The circuit design is created using standard circuit design software tools. At step **120**, the unfolded netlist is folded, creating folded netlist **125**. The folded

netlist is used to generate a placement. Placement processing takes into account electromigration (EM) quality criteria in order to select a placement with a preferred electromigration tolerance (predefined process **130**, see **Figure 2** and corresponding text for processing details). Placement processing results in best electromigration placement **140**. This "best" electromigration placement is routed using predefined process **150** (see **Figure 4** and corresponding text for processing details). Again, during routing, the "best" electromigration routing is identified and stored as best routing of the best placement (**160**).

[0012] At step **170**, the best electromigration routing of the best electromigration placement (**160**) is compacted. At this point, a process or the circuit designer determines whether the compacted design will work given the design constraints (decision **175**). One example of a design constraint is a physical size constraint. Other examples of design constraints are known by those skilled in the art. If the routed design will not work given the design constraints, then decision **175** branches to "no" branch **180** whereupon, at step **185**, the selected design is removed from the list of possible design selections and processing loops back to re-place the design and re-route the re-placed design (with the re-placing and re-routing each using electromigration quality criteria). The action that is performed depends on the step in the process that is being addressed. As shown, step **185** loop back to any of steps **110**, **120**, **130**, or **150** depending on the action that is being taken. This looping continues until a compacted design is created that works given the design constraints, at which point decision **175** branches to "yes" branch **190** and processing ends at **195**.

[0013] **Figure 2** is a flowchart showing the steps to select a placement with desired electromigration qualities. Processing commences at **200** whereupon, at step **210**, an electromigration placement "best quality" vector (Q_{p_best}) is initialized to a high (bad) value. An example of an initial, bad, value to use for the placement best quality vector would be (99, 99) with the first 99 vector value representing a high current value and the second 99 vector value representing 99 occurrences of the high current value. At step **220**, the best placement identifier is initialized to zero (indicating that no "best placement" has yet been identified). At step **225**,

the first placement is generated (p=1), using folded netlist **125** as the input design. The electromigration placement quality vector (Q_p) is computed for the first generated placement (predefined process **235**, see **Figure 3** and corresponding text for details regarding how the electromigration placement quality vector is computed). The electromigration placement quality vector is one embodiment of an electromigration placement quality value. At step **240**, other metrics that may be used to evaluate the placement are computed. The other metrics that are computed may vary based upon the design goals and are generally known to those skilled in the art. In one embodiment, the other metrics are used as a tiebreaker in selecting between placements that have the same electromigration placement quality vectors. In an alternative embodiment, the electromigration placement quality vector and the other quality metrics are given weighted values. In this alternative embodiment, these weighed values are used to determine an overall score and, ultimately, which placement has the best placement quality vector.

[0014] At decision **250**, a determination is made as to whether the latest placement's electromigration quality vector (Q_p) is lower than (i.e., better than) the "best" electromigration placement quality vector (Q_{p_best}). Because the best electromigration placement quality vector was initialized to a high (bad) value, the first placement will have a lower (better) electromigration placement quality vector than the initialized "best" electromigration placement quality vector so that decision **250** branches to "yes" branch **255** whereupon, at step **260**, the best placement (**140**) is set to equal the first placement (p=1) value, and, step **270**, the latest best electromigration placement quality vector (Q_{p_best}) is replaced with the electromigration placement quality vector (Q_p) computed for the first placement. During successive iterations, if another placement's electromigration placement quality vector is better than the "best" electromigration placement quality vector, then decision **250** will again branch to ""yes" branch **255** and perform steps **260** and **270**. However, if a electromigration quality placement vector for a subsequent placement (Q_p) is not less (better) than the "best" electromigration placement quality vector, then decision **250** will branch to "no" branch **275** bypassing steps **260** and **270**.

[0015] A determination is made as to whether another placement should be generated and its electromigration placement quality vector compared with the best quality vector (decision **280**). The decision as to how many placements should be generated and evaluated can be based upon several factors such as termination conditions of particular optimization algorithms, certain metric factors, a time/effort factor of wanting to generate a certain number of placements, or a subjective factor where an experienced circuit designer decides when to stop generating additional placements based on the designer's knowledge and experience in designing circuits. If additional placement(s) are desired, decision **280** branches to "yes" branch **285** whereupon, at step **290**, the next placement (p=p+1) is generated from folded netlist **125** to create latest placement **230** and processing loops back to compute the placement quality vector (Q_p) for the newly generated placement and compare this placement's quality vector with the latest best placement's quality vector. This looping continues until additional placements are no longer desired, at which point decision **280** branches to "no" branch **292** and processing returns at **295**.

[0016] **Figure 3** is a flowchart showing the steps taken to compute an electromigration placement quality vector for a given placement. **Figure 3** depicts two example placements – first example placement **301** and second example placement **302**. The example placement are used to illustrate how current distributions and placement quality vectors are computed. The process that computes the placement quality vectors is shown commencing at **300**, whereupon, at step **310**, the relative current that passes through the first transistor group of a placement is computed. In the first example placement, full current (I) passes though each of the transistor groups, while in the second example placement, full current passes through three of the transistor groups and half-current passes through two of the transistor groups.

[0017] At step **320**, the current that passes through the first transistor group is stored in current distribution memory area **330**. A determination is made as to whether there are more transistor groups to process (decision **340**). The first example placement depicts a placement with four transistor groups, thus decision **340** will

be true (yes) three times when processing the first example placement. The second example placement depicts a placement with five transistor groups, thus decision **340** will be true (yes) four times when processing the second example placement. If there are more transistor groups, decision **340** branches to "yes" branch **345** whereupon, at step **350**, the current that passes through the next transistor group is computed and processing loops back to store the current that passes through the transistor group in current distribution memory area **330**. This looping continues until all transistor groups have been processed, at which point decision **340** branches to "no" branch **355**.

[0018] After the current that passes through all of the transistor groups has been computed, at step **360**, the current distribution values are sorted from high to low values. For example, in the second example placement there are five transistor groups – three transistor groups have full current (I) passing through them and two transistor groups have half current (I/2) passing through them. The result of sorting the current distribution in this example is shown as being (I, I, I, I/2, I/2). The results of the sorting are stored an sorted current distribution memory area **370**. At step **380**, the sorted current distribution is used to generate the electromigration placement quality vector (Q_p) for the placement, and processing returns at **395**.

[0019] The electromigration placement quality vector is computed by counting the number of equal current values. So, for the first example placement where full current (I) passes through each of the transistor groups, the electromigration placement quality vector (Q_p) is (1, 4) with "1" representing full current and "4" representing the number of transistor groups found to have full current passing through them. Likewise, for the second example placement where full current (I) passes through three of the transistor groups and half current (I/2) passes through two of the transistor groups, the electromigration placement quality vector (Q_p) is (1,3, 4/8, 2) where "1" again representing full current, "3" representing the number of transistor groups found to have full current passing through them, "4/8" (which can be reduced to ½ or .5) representing half current (I/2), and "2" representing the number of transistor groups where I/2 current

passes through the group. If the quality vectors (Q_p) for the first and second example placements are compared (e.g., using a decision such as that shown in decision **250** in **Figure 2**), the second example placement has a lower electromigration placement quality vector. Each of the electromigration placement quality vectors have a "1" for the first vector value, but the second example placement has a "3" for the second vector value, while the first example placement has a "4" for the second vector value. Since "3" is less than "4", the second example placement would be considered "better" than the first example placement in terms of the respective electromigration placement quality vectors.

[0020] **Figure 4** is a flowchart showing the steps taken to select a routing of a selected placement with desired electromigration qualities. In one embodiment, a "best" electromigration placement is found using the steps shown in **Figures 2** and **3** and then a preferred routing, in terms of electromigration, is found for the best placement. However, the techniques shown in **Figure 4** and **5** for identifying a routing for a given placement can be used for virtually any placement regardless of whether the techniques shown in **Figures 2** and **3** were used to generate and identify the placement.

[0021] Routing processing commences at **400** whereupon, at step **410**, the best electromigration routing quality vector (Q_{i_best}) is initialized to a high (bad) value. An example of an initial, bad, value to use for the best electromigration routing quality vector would be (99, 99) with the first 99 vector value representing a high current value and the second 99 vector value representing 99 occurrences of the high current value. At step **415**, the best route for the placement is initialized to zero (0) indicating that a best routing has not yet been identified. At step **420**, the placement (**140**) is routed a first time (i=1), resulting in latest routing **425**. In one embodiment, the route is computed using a routing engine.

[0022] The electromigration routing quality vector (Q_i) is computed for the latest routing (predefined process **430**, see **Figure 5** and corresponding text for processing details). The electromigration routing quality vector is one embodiment of an

electromigration routing quality value. The latest electromigration routing quality vector (Q_i) is compared to the best electromigration routing quality vector (Q_{i_best}). In decision **440**, a determination is made as to whether the latest electromigration routing quality vector (Q_i) is lower (better) than the best electromigration routing quality vector (Q_{i_best}). The first electromigration routing quality vector will be lower (better) than the initial best electromigration routing quality vector since the initial best electromigration routing quality vector was set to a high value. In this case, decision **440** will branch to "yes" branch **445** whereupon, at step **450**, the best route (**160**) is set to be the first routing, and, at step **460**, the best electromigration routing quality vector (Q_{i_best}) is set to be the latest electromigration routing quality vector (Q_i). During subsequent iterations, if another routing is found with an electromigration routing quality vector (Q_i) that is better than the best routing quality vector (Q_{i_best}), then decision **440** branches to "yes" branch **445** and steps **450** and **460** are performed. On the other hand, if a subsequent routing is found with an electromigration routing quality vector (Q_i) that is not better than the best routing quality vector (Q_{i_best}), then decision **440** branches to "no" branch **465** bypassing steps **450** and **460**.

[0023] A determination is made as to whether another routing should be generated and its electromigration routing quality vector compared with the best electromigration routing quality vector (decision **470**). The decision as to how many routings should be generated and evaluated can be based upon several factors such as termination conditions of particular optimization algorithms, certain metric factors, a time/effort factor of generating a certain number of routings, or a subjective factor where an experienced circuit designer decides when to stop generating additional routings based on the designer's knowledge and experience in designing circuits. If additional placement(s) are desired, decision **470** branches to "yes" branch **475** whereupon, at step **480**, nets in the latest routed placement (**425**) are identified for re-routing (these nets may be identified based on the quality vectors that are computed in **Figure 5**). At step **485**, the identified nets are re-routed, forming a new latest electromigration routing of the placement (**425**), and the routing number is incremented (i=i+1). Processing then loops back to compute the electromigration routing quality vector for the latest routing.

In one embodiment, rather than identifying specific nets in the placement to re-route, the entire placement is re-routed. This routing may perform the re-routing based on previously computed electromigration routing quality vectors. When no more routings (re-routings) are needed, decision **470** branches to "no" branch **490** and processing returns at **495**.

[0024] **Figure 5** is a flowchart showing the steps taken to compute an electromigration routing quality vector for a given routing. **Figure 5** depicts two example routings – first example routing **501** and second example routing **502**. The example routings are used to illustrate how current distributions and electromigration routing quality vectors are computed. The process that computes the electromigration routing quality vectors is shown commencing at **500**, whereupon, at step **510**, the current that passes through the first segment of the routing is computed. In the first example routing, full current (I) passes though two of the segments, and half-current (I/2) passes through the other two segments. In the second example routing, half current passes through all six segments.

[0025] At step **520**, the current that passes through the first segment is stored in current distribution memory area **530**. A determination is made as to whether there are more routing segments to process (decision **540**). The first example routing depicts a routing with four segments, thus decision **540** will be true (yes) three times when processing the first example routing. The second example routing depicts a routing with six segments, thus decision **540** will be true (yes) five times when processing the second example routing. If there are more segments, decision **540** branches to "yes" branch **545** whereupon, at step **550**, the current that passes through the next segment is computed and processing loops back to store the current that passes through the segment in current distribution memory area **530**. This looping continues until all segments have been processed, at which point decision **540** branches to "no" branch **555**.

[0026] After all of the segments have been processed, at step **560**, the current distribution values are sorted from high to low values. For example, in the first

example routing there are four segments – two segments have full current (I) passing through them and two transistor groups have half current (I/2) passing through them. The result of sorting the current distribution in the first example is shown as being (I, I, I/2, I/2). The results of the sorting are stored an sorted current distribution memory area **570**. At step **580**, the sorted current distribution is used to generate the electromigration routing quality vector (Q_i) for the routing, and processing returns at **595**.

[0027] The electromigration routing quality vector is computed by counting the number of equal current values. So, for the first example routing where full current (I) passes through two of the segments and half-current passes through two of the segements, the electromigration routing quality vector (Q_i) is (1, 2, 1/2, 2) with "1" representing full current, the first "2" representing the number of segments found to have full current passing through them, "1/2" representing half current, and the second "2" representing the number of segments found to have half current passing through them. Likewise, for the second example routing where half current (I/2) passes through all six of the segments, the electromigration routing quality vector (Q_i) is (1/2, 6) where "1/2" again representing half current, and "6" representing the six segments found to have half current passing through them. If the electromigration routing quality vectors (Q_i) for the first and second example routings are compared (e.g., using a decision such as that shown in decision **440** in **Figure 4**), the second example routing has a lower electromigration routing quality vector. The first value ("1/2") of the electromigration routing quality vector for the second example routing is lower than the first value ("1") of the routing quality vector for the first example routing. Since "1/2" is less than "1", the second example routing would be considered "better" than the first example routing in terms of the respective electromigration routing quality vectors.

[0028] **Figure 6** illustrates information handling system **601** which is a simplified example of a computer system capable of performing the computing operations described herein. Computer system **601** includes processor **600** which is coupled to host bus **602**. A level two (L2) cache memory **604** is also coupled to host bus **602**. Host-to-PCI bridge **606** is coupled to main memory **608**, includes

cache memory and main memory control functions, and provides bus control to handle transfers among PCI bus **610**, processor **600**, L2 cache **604**, main memory **608**, and host bus **602**. Main memory **608** is coupled to Host-to-PCI bridge **606** as well as host bus **602**. Devices used solely by host processor(s) **600**, such as LAN card **630**, are coupled to PCI bus **610**. Service Processor Interface and ISA Access Pass-through **612** provides an interface between PCI bus **610** and PCI bus **614**. In this manner, PCI bus **614** is insulated from PCI bus **610**. Devices, such as flash memory **618**, are coupled to PCI bus **614**. In one implementation, flash memory **618** includes BIOS code that incorporates the necessary processor executable code for a variety of low-level system functions and system boot functions.

[0029] PCI bus **614** provides an interface for a variety of devices that are shared by host processor(s) **600** and Service Processor **616** including, for example, flash memory **618**. PCI-to-ISA bridge **635** provides bus control to handle transfers between PCI bus **614** and ISA bus **640**, universal serial bus (USB) functionality **645**, power management functionality **655**, and can include other functional elements not shown, such as a real-time clock (RTC), DMA control, interrupt support, and system management bus support. Nonvolatile RAM **620** is attached to ISA Bus **640**. Service Processor **616** includes JTAG and I2C busses **622** for communication with processor(s) **600** during initialization steps. JTAG/I2C busses **622** are also coupled to L2 cache **604**, Host-to-PCI bridge **606**, and main memory **608** providing a communications path between the processor, the Service Processor, the L2 cache, the Host-to-PCI bridge, and the main memory. Service Processor **616** also has access to system power resources for powering down information handling device **601**.

[0030] Peripheral devices and input/output (I/O) devices can be attached to various interfaces (e.g., parallel interface **662**, serial interface **664**, keyboard interface **668**, and mouse interface **670** coupled to ISA bus **640**. Alternatively, many I/O devices can be accommodated by a super I/O controller (not shown) attached to ISA bus **640**.

[0031] In order to attach computer system **601** to another computer system to copy files over a network, LAN card **630** is coupled to PCI bus **610**. Similarly, to connect computer system **601** to an ISP to connect to the Internet using a telephone line connection, modem **675** is connected to serial port **664** and PCI-to-ISA Bridge **635.**

[0032] While the computer system described in **Figure 6** is capable of executing the processes described herein, this computer system is simply one example of a computer system. Those skilled in the art will appreciate that many other computer system designs are capable of performing the processes described herein.

[0033] One of the implementations of the invention is a client application, namely, a set of instructions (program code) or other functional descriptive material in a code module that may, for example, be resident in the random access memory of the computer. Until required by the computer, the set of instructions may be stored in another computer memory, for example, in a hard disk drive, or in a removable memory such as an optical disk (for eventual use in a CD ROM) or floppy disk (for eventual use in a floppy disk drive), or on a nonvolatile storage device accessible through the Internet or other computer network where the set of instructions may be downloaded from the network-accessible nonvolatile storage device. Thus, the present invention may be implemented as a computer program product for use in a computer. In addition, although the various methods described are conveniently implemented in a general purpose computer selectively activated or reconfigured by software, one of ordinary skill in the art would also recognize that such methods may be carried out in hardware, in firmware, or in more specialized apparatus constructed to perform the required method steps. Functional descriptive material is information that imparts functionality to a machine. Functional descriptive material includes, but is not limited to, computer programs, instructions, rules, facts, definitions of computable functions, objects, and data structures.

[0034] While particular embodiments of the present invention have been shown and described, it will be obvious to those skilled in the art that, based upon the teachings herein, changes and modifications may be made without departing from this invention and its broader aspects. Therefore, the appended claims are to encompass within their scope all such changes and modifications as are within the true spirit and scope of this invention. Furthermore, it is to be understood that the invention is solely defined by the appended claims. It will be understood by those with skill in the art that if a specific number of an introduced claim element is intended, such intent will be explicitly recited in the claim, and in the absence of such recitation no such limitation is present. For non-limiting example, as an aid to understanding, the following appended claims contain usage of the introductory phrases "at least one" and "one or more" to introduce claim elements. However, the use of such phrases should not be construed to imply that the introduction of a claim element by the indefinite articles "a" or "an" limits any particular claim containing such introduced claim element to inventions containing only one such element, even when the same claim includes the introductory phrases "one or more" or "at least one" and indefinite articles such as "a" or "an;" the same holds true for the use in the claims of definite articles.

Claims

What is claimed is:

1. A computer-implemented method comprising:

routing a circuit placement a plurality of times, the routing resulting in a plurality of routings;

computing an electromigration routing quality value for each of the plurality of routings; and

selecting one of the plurality of routings based on the selected routing's electromigration routing quality value.

2. The method of claim 1 wherein the computing further comprises:

identifying one or more segments in each of the plurality of routings;

computing a current through each of the identified segments, the computing of the current resulting in a current distribution corresponding to each of the routings; and

generating a plurality of electromigration routing quality vectors, wherein each of the electromigration routing quality vectors corresponds to one of the routings and to one of the current distributions, wherein the electromigration routing quality value is the electromigration routing quality vector.

3. The method of claim 2 further comprising:

sorting the current distributions from a high current value to a low current value, wherein, generating each of the electromigration routing quality vectors includes:

grouping the sorted current distribution corresponding to the electromigration routing quality vector by storing unique current values

and a count of the number of times that each unique current value appears in the sorted current distribution.

4. The method of claim 1 further comprising:

routing the circuit placement the first of the plurality of times;

computing the electromigration routing quality value of the first routing;

analyzing the first routing's electromigration routing quality value;

identifying one or more nets in the first routing based on the analysis;

re-routing the identified nets, the re-routing resulting in a second of the plurality of routings;

computing the electromigration routing quality value of the second routing;

comparing the first routing's electromigration routing quality value to the second routing's electromigration routing quality value;

selecting the first routing in response to the first routing's electromigration routing quality value being better than the second routing's electromigration routing quality value; and

selecting the second routing in response to the second routing's electromigration routing quality value being better than the first routing's electromigration routing quality value.

5. The method of claim 1 further comprising:

generating the circuit placement prior to the routing, the generating including:

creating a plurality of circuit placements corresponding to a circuit design;

computing an electromigration placement quality value for each of the plurality of circuit placements;

calculating one or more quality metrics corresponding to each of the plurality of circuit placements, wherein one of the metrics is the computed electromigration placement quality value; and

selecting the circuit placement from the plurality of circuit placements based on the quality metrics.

6. The method of claim 5 wherein the computing of the electromigration placement quality value further comprises:

identifying one or more transistor groups in each of the plurality of circuit placements;

computing a current through each of the identified transistor groups, the computing of the current resulting in one or more current distributions; and

generating an electromigration placement quality vector corresponding to the one or more current distributions, wherein the electromigration placement quality value is the electromigration placement quality vector.

7. The method of claim 6 further comprising:

sorting the current distributions from a high current value to a low current value, wherein the generation of the electromigration placement quality vector includes grouping the sorted current distributions by unique current values and a count of the number of times that each unique current value appears in the circuit placement.

8. The method of claim 6 further comprising:

prior to generating the circuit placement:

receiving an unfolded netlist corresponding to a circuit design; and

folding the unfolded netlist, the folding resulting in a folded netlist, wherein the generating of the circuit placement is based on the folded netlist.

9. The method of claim 6 further comprising:

analyzing the selected routing;

determining, based on the analysis, whether the selected routing is a workable design;

in response to determining that the selected routing is an unworkable design:

re-generating the circuit placement; and

performing the routing, the computing of the electromigration routing quality value, and the selecting of one of the routings using the re-generated circuit placement.

10. A data processing system comprising:

one or more processors;

a memory accessible by the processors;

a set of instructions stored in the memory, wherein one or more of the processors executes the set of instructions in order to perform actions of:

routing a circuit placement a plurality of times, the routing resulting in a plurality of routings;

computing an electromigration routing quality value for each of the plurality of routings; and

selecting one of the plurality of routings based on the selected routing's electromigration routing quality value.

11. The data processing system of claim 10 wherein the computing further comprises instructions that perform the actions of:

identifying one or more segments in each of the plurality of routings;

computing a current through each of the identified segments, the computing of the current resulting in a current distribution corresponding to each of the routings; and

generating a plurality of electromigration routing quality vectors, wherein each of the electromigration routing quality vectors corresponds to one of the routings and to one of the current distributions, wherein the electromigration routing quality value is the electromigration routing quality vector.

12. The data processing system of claim 10 further comprising instructions that perform the actions of:

routing the circuit placement the first of the plurality of times;

computing the electromigration routing quality value of the first routing;

analyzing the first routing's electromigration routing quality value;

identifying one or more nets in the first routing based on the analysis;

re-routing the identified nets, the re-routing resulting in a second of the plurality of routings;

computing the electromigration routing quality value of the second routing;

comparing the first routing's electromigration routing quality value to the second routing's electromigration routing quality value;

selecting the first routing in response to the first routing's electromigration routing quality value being better than the second routing's electromigration routing quality value; and

selecting the second routing in response to the second routing's electromigration routing quality value being better than the first routing's electromigration routing quality value.

13. The data processing system of claim 10 further comprising instructions that perform the actions of:

generating the circuit placement prior to the routing, the generating including:

creating a plurality of circuit placements corresponding to a circuit design;

computing an electromigration placement quality value for each of the plurality of circuit placements;

calculating one or more quality metrics corresponding to each of the plurality of circuit placements, wherein one of the metrics is the computed electromigration placement quality value; and

selecting the circuit placement from the plurality of circuit placements based on the quality metrics.

14. The data processing system of claim 13 wherein the computing of the electromigration placement quality value further comprises instructions that perform the actions of:

identifying one or more transistor groups in each of the plurality of circuit placements;

computing a current through each of the identified transistor groups, the computing of the current resulting in one or more current distributions; and

generating an electromigration placement quality vector corresponding to the one or more current distributions, wherein the electromigration placement quality value is the electromigration placement quality vector.

15. A computer program product stored in a computer readable medium, comprising functional descriptive material that, when executed by a data processing system, causes the data processing system to perform actions that include:

routing a circuit placement a plurality of times, the routing resulting in a plurality of routings;

computing an electromigration routing quality value for each of the plurality of routings; and

selecting one of the plurality of routings based on the selected routing's electromigration routing quality value.

16. The computer program product of claim 15 wherein the computing further comprises functional descriptive material that, when executed by a data processing system, causes the data processing system to perform actions that include:

identifying one or more segments in each of the plurality of routings;

computing a current through each of the identified segments, the computing of the current resulting in a current distribution corresponding to each of the routings; and

generating a plurality of electromigration routing quality vectors, wherein each of the electromigration routing quality vectors corresponds to one of the routings and to one of the current distributions, wherein the electromigration routing quality value is the electromigration routing quality vector.

17. The computer program product of claim 16 further comprising comprises functional descriptive material that, when executed by a data processing system, causes the data processing system to perform actions that include:

sorting the current distributions from a high current value to a low current value, wherein, generating each of the electromigration routing quality vectors includes:

grouping the sorted current distribution corresponding to the electromigration routing quality vector by storing unique current values and a count of the number of times that each unique current value appears in the sorted current distribution.

18. The computer program product of claim 15 further comprising functional descriptive material that, when executed by a data processing system, causes the data processing system to perform actions that include:

generating the circuit placement prior to the routing, the generating including:

creating a plurality of circuit placements corresponding to a circuit design;

computing an electromigration placement quality value for each of the plurality of circuit placements;

calculating one or more quality metrics corresponding to each of the plurality of circuit placements, wherein one of the metrics is the computed electromigration placement quality value; and

selecting the circuit placement from the plurality of circuit placements based on the quality metrics.

19. The computer program product of of claim 15 wherein the computing of the electromigration placement quality value further comprises functional descriptive material that, when executed by a data processing system, causes the data processing system to perform actions that include::

identifying one or more transistor groups in each of the plurality of circuit placements;

computing a current through each of the identified transistor groups, the computing of the current resulting in one or more current distributions; and

generating an electromigration placement quality vector corresponding to the one or more current distributions, wherein the electromigration placement quality value is the electromigration placement quality vector.

20. The computer program product of claim 19 further comprising functional descriptive material that, when executed by a data processing system, causes the data processing system to perform actions that include:

sorting the current distributions from a high current value to a low current value, wherein the generation of the electromigration placement quality vector includes grouping the sorted current distributions by unique current values and a count of the number of times that each unique current value appears in the circuit placement.

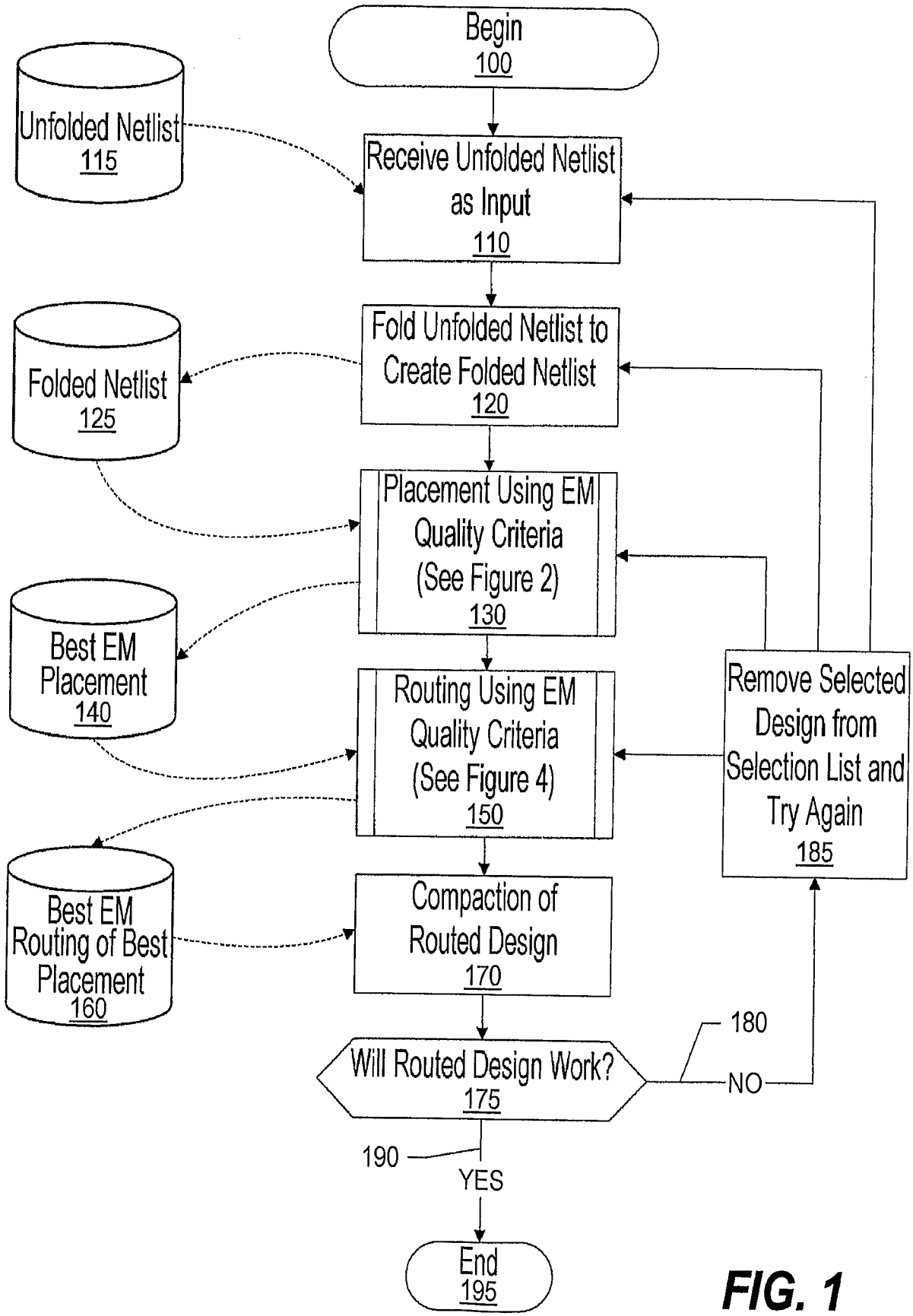
Begin
100
Unfolded Netlist
115
Receive Unfolded Netlist as Input
110
Fold Unfolded Netlist to Create Folded Netlist
120
Folded Netlist
125
Placement Using EM Quality Criteria (See Figure 2)
130
Best EM Placement
140
Routing Using EM Quality Criteria (See Figure 4)
150
Remove Selected Design from Selection List and Try Again
185
Best EM Routing of Best Placement
160
Compaction of Routed Design
170
180
Will Routed Design Work?
175
NO
190
YES
End
195

FIG. 1

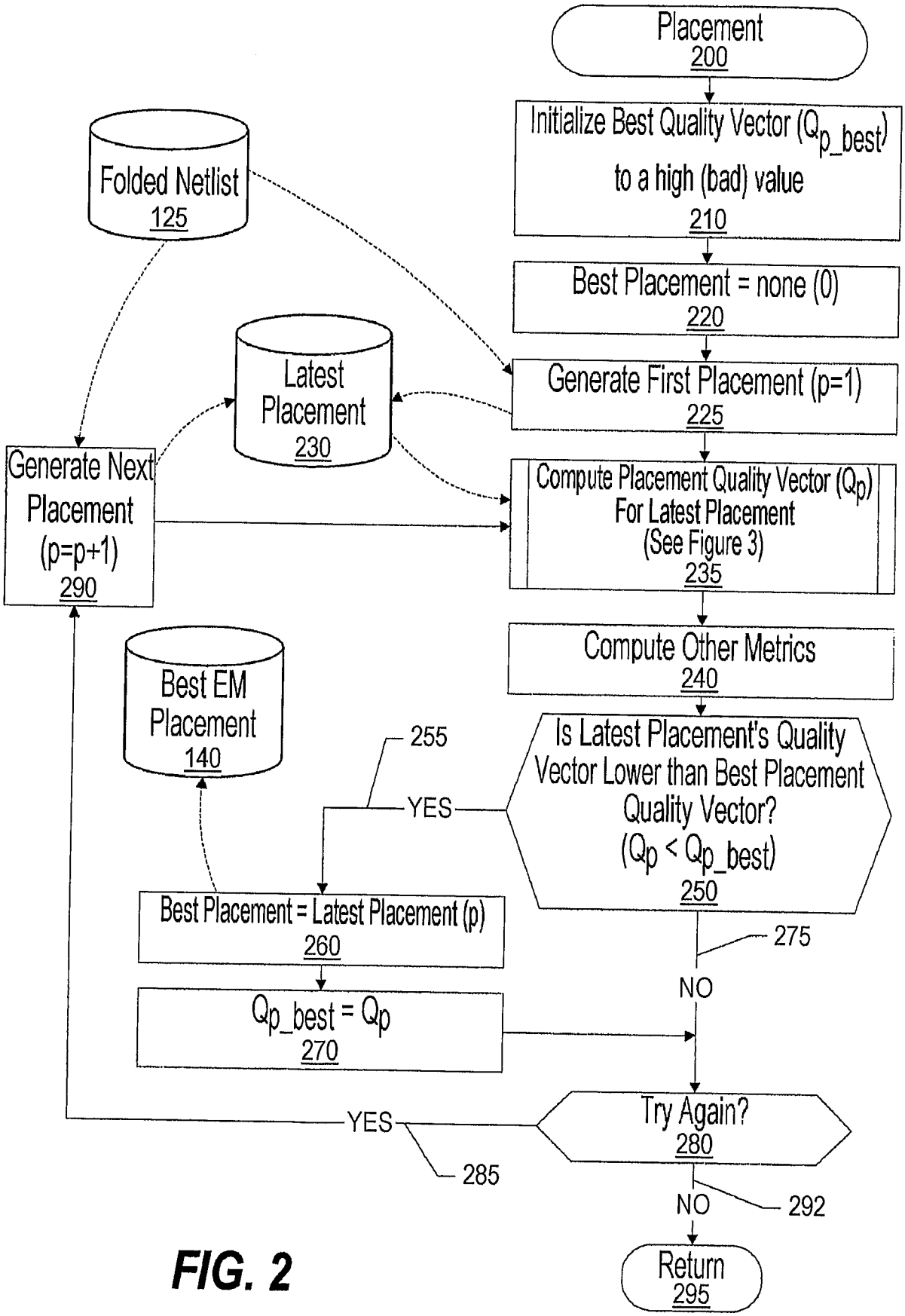
Placement
200
Initialize Best Quality Vector (Q_{p_best}) to a high (bad) value
210
Best Placement = none (0)
220
Generate First Placement (p=1)
225
Compute Placement Quality Vector (Q_p) For Latest Placement (See Figure 3)
235
Compute Other Metrics
240
Is Latest Placement's Quality Vector Lower than Best Placement Quality Vector? ($Q_p < Q_{p_best}$)
250
255
YES
Best Placement = Latest Placement (p)
260
$Q_{p_best} = Q_p$
270
275
NO
Try Again?
280
YES
285
NO
292
Return
295
Folded Netlist
125
Latest Placement
230
Best EM Placement
140
Generate Next Placement (p=p+1)
290

FIG. 2

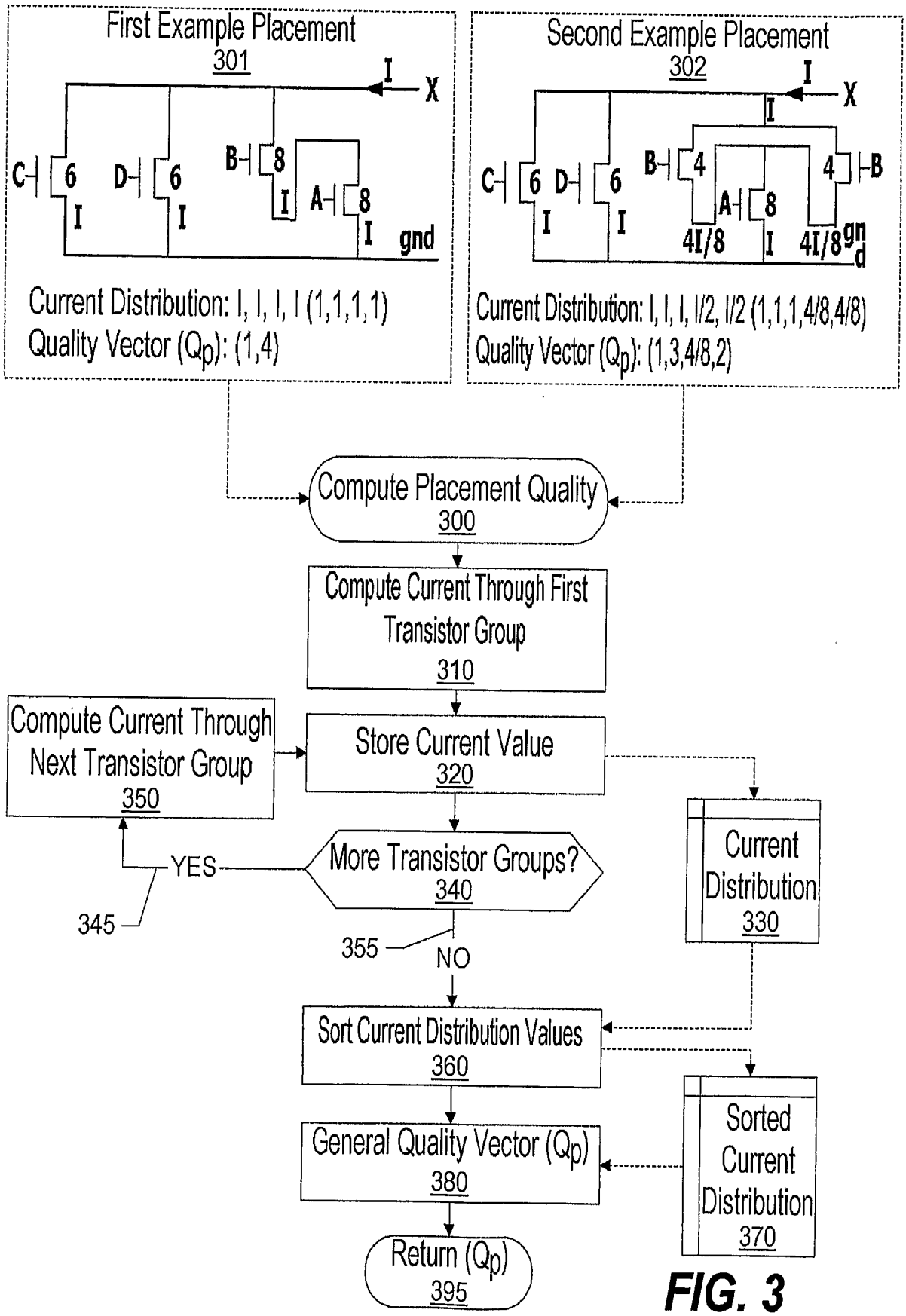
First Example Placement
301
I
X
C
6
I
D
6
I
B
8
I
A
8
I
gnd
Current Distribution: I, I, I, I (1,1,1,1)
Quality Vector (Qp): (1,4)
Second Example Placement
302
I
X
I
C
6
I
D
6
I
B
4
A
8
I
4
B
4I/8
4I/8
gnd
Current Distribution: I, I, I, I/2, I/2 (1,1,1,4/8,4/8)
Quality Vector (Qp): (1,3,4/8,2)
Compute Placement Quality
300
Compute Current Through First Transistor Group
310
Store Current Value
320
Compute Current Through Next Transistor Group
350
More Transistor Groups?
340
YES
345
355
NO
Current Distribution
330
Sort Current Distribution Values
360
Sorted Current Distribution
370
General Quality Vector (Qp)
380
Return (Qp)
395

FIG. 3

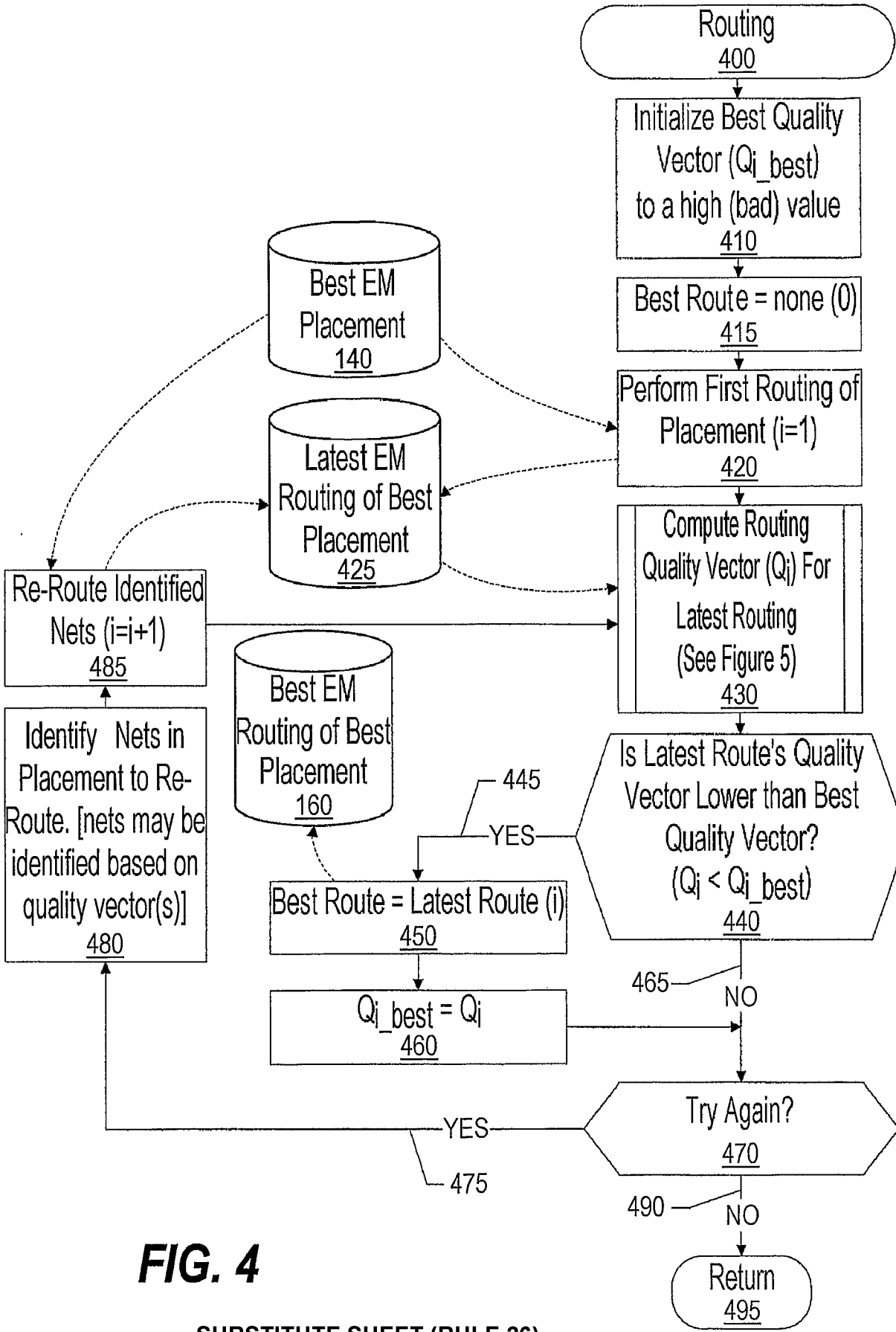
Routing
400
Initialize Best Quality Vector (Qi_best) to a high (bad) value
410
Best Route = none (0)
415
Perform First Routing of Placement (i=1)
420
Compute Routing Quality Vector (Qi) For Latest Routing (See Figure 5)
430
Is Latest Route's Quality Vector Lower than Best Quality Vector? (Qi < Qi_best)
440
445
YES
Best Route = Latest Route (i)
450
Qi_best = Qi
460
465
NO
Try Again?
470
YES
475
490
NO
Return
495
Best EM Placement
140
Latest EM Routing of Best Placement
425
Best EM Routing of Best Placement
160
Re-Route Identified Nets (i=i+1)
485
Identify Nets in Placement to Re-Route. [nets may be identified based on quality vector(s)]
480

FIG. 4

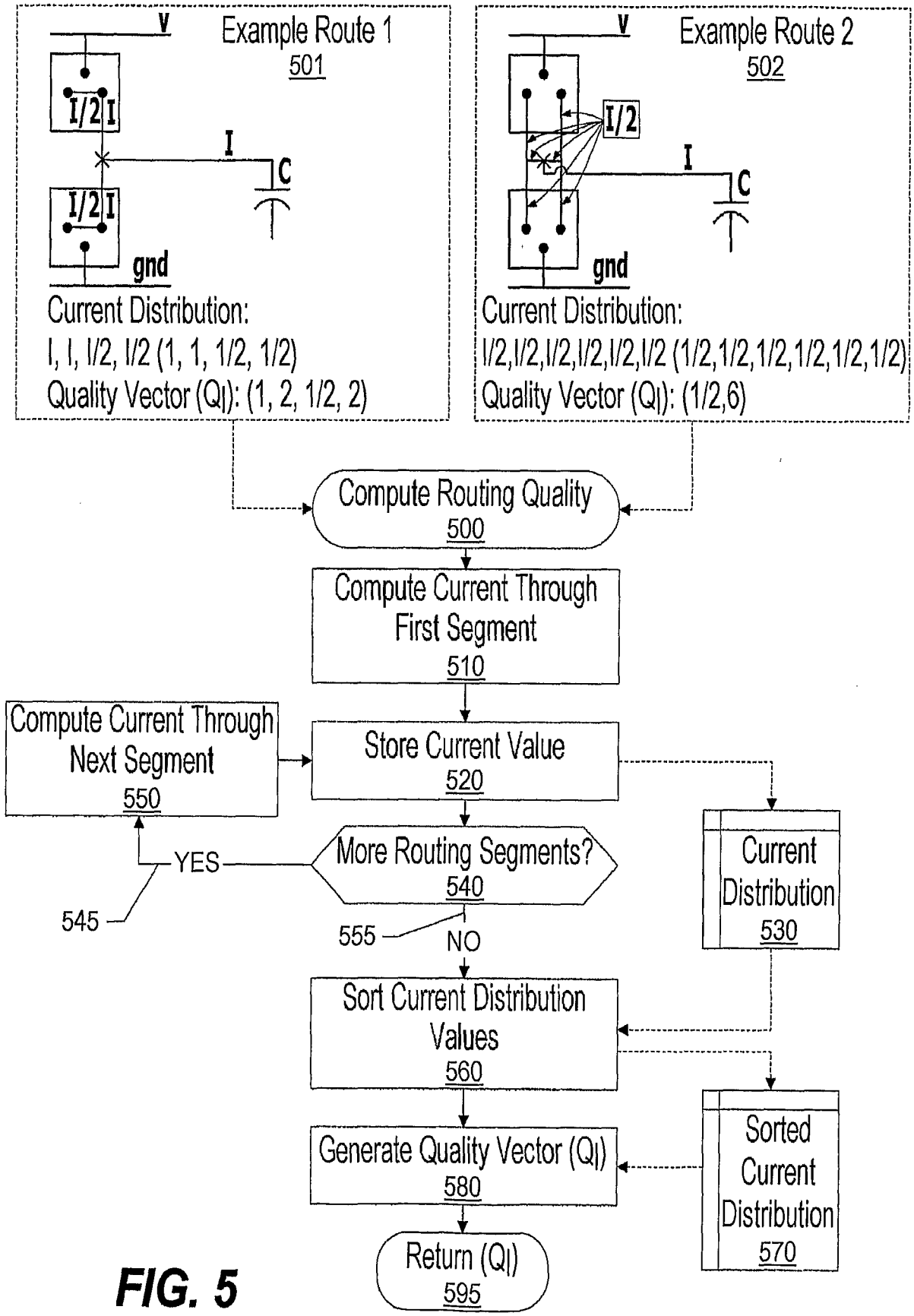
V
Example Route 1
501
I/2 I
I
C
I/2 I
gnd
Current Distribution:
I, I, I/2, I/2 (1, 1, 1/2, 1/2)
Quality Vector (QI): (1, 2, 1/2, 2)
V
Example Route 2
502
I/2
I
C
gnd
Current Distribution:
I/2,I/2,I/2,I/2,I/2,I/2 (1/2,1/2,1/2,1/2,1/2,1/2)
Quality Vector (QI): (1/2,6)
Compute Routing Quality
500
Compute Current Through First Segment
510
Compute Current Through Next Segment
550
Store Current Value
520
Current Distribution
530
YES
More Routing Segments?
540
545
555
NO
Sort Current Distribution Values
560
Sorted Current Distribution
570
Generate Quality Vector (QI)
580
Return (QI)
595

FIG. 5

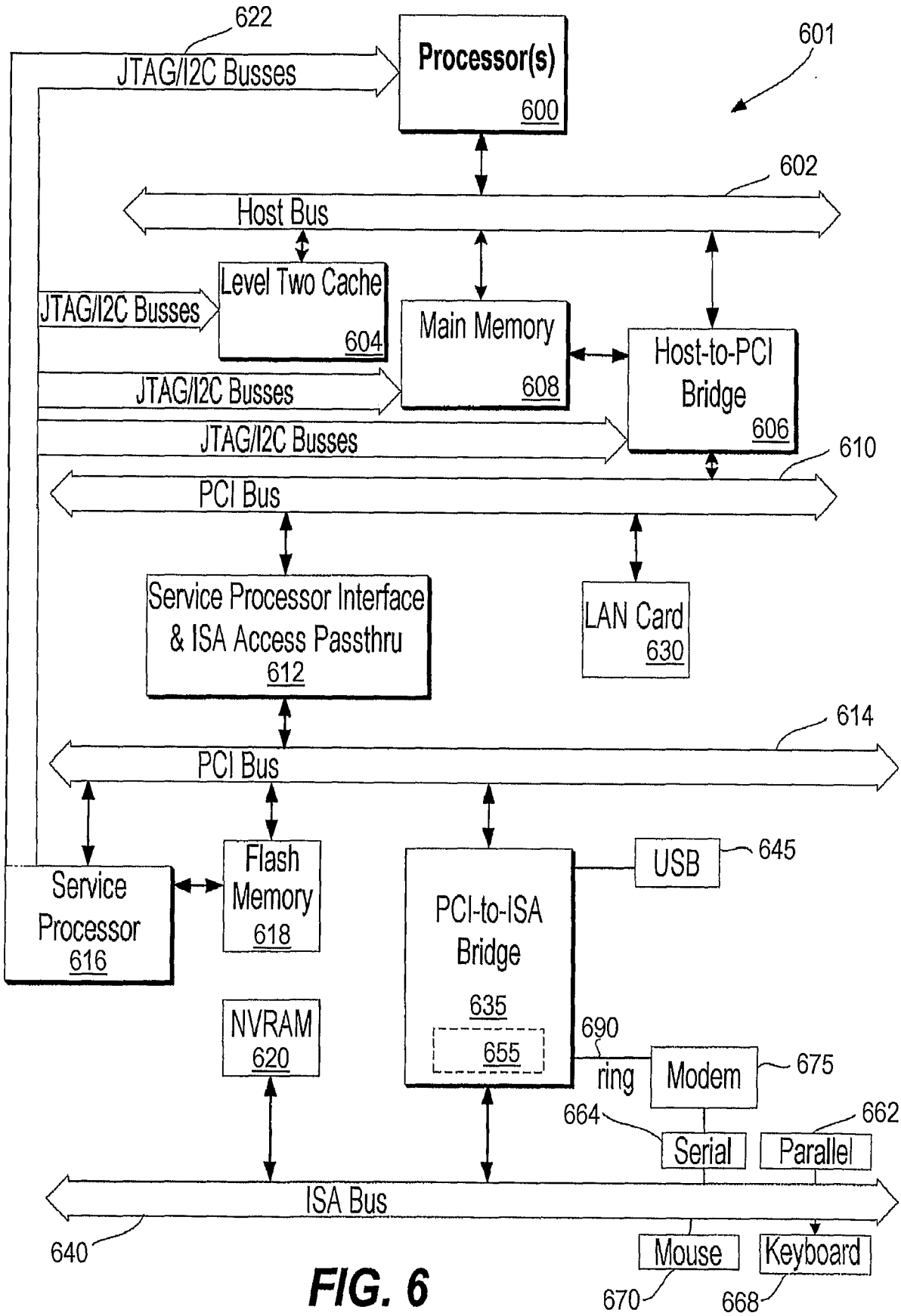
622
JTAG/I2C Busses
Processor(s)
600
601
602
Host Bus
JTAG/I2C Busses
Level Two Cache
604
Main Memory
608
Host-to-PCI
Bridge
606
JTAG/I2C Busses
JTAG/I2C Busses
610
PCI Bus
Service Processor Interface
& ISA Access Passthru
612
LAN Card
630
614
PCI Bus
Service
Processor
616
Flash
Memory
618
PCI-to-ISA
Bridge
635
655
USB
645
NVRAM
620
690
ring
Modem
675
664
662
Serial
Parallel
ISA Bus
640
Mouse
Keyboard
670
668

FIG. 6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/RU 2006/000532

A. CLASSIFICATION OF SUBJECT MATTER ***G06F 17/50*** *(2006.01)*
H04L 12/00 *(2006.01)*
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G06F 17/00, 17/10, 17/16, 17/50, 19/00, H04L 12/00, 12/02, 12/24, 12/26, 12/28, 12/46, 12/50, 12/66, 29/00, 29/02, 29/14, G01N 27/00, 27/26, 27/416, 27/47, H03K 19/00, 19/17 ,19/177

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
PAJ, Esp@cenet, USPTO DB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6493859 B1 (INTERNATIONAL BUSINESS MACHINES CORPORATION) 10.12.2002, abstract, col. 2, line 65 - col. 5, line 39	1-20
X	JP 59061770 A (SHIMADZU CORP) 09.04.1984, abstract	1-20
X	US 2005/0289494 A1 (INTERNATIONAL BUSINESS MACHINES CORPORATION) 29.12.2005, abstract, p. 2, par. 0023 - p. 5, par. 0051, claims 1-9	1-20
X	US 6880139 B2 (SUN MICROSYSTEMS, INC.) 12.04.2005, abstract, col. 4, line 11 - col. 7, line 8, claim 1	1-20
A	EP 0629853 A2 (HEWLETT-PACKARD COMPANY) 21.12.1994	1-20
A	US 2004/0178821 A1 (STMICROELECTRONICS PVT. LTD.) 16.09.2004	1-20
A	RU 2222869 C2 (REDIANT NETWORKS PLC) 27.01.2004	1-20

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
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"E" earlier application or document but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search report	Date of mailing of the international search report
20 June 2007 (20.06.2007)	12 July 2007 (12.07.2007)

Name and mailing address of the ISA/RU FIPS	Authorized officer
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Form PCT/ISA/210 (second sheet) (April 2005)