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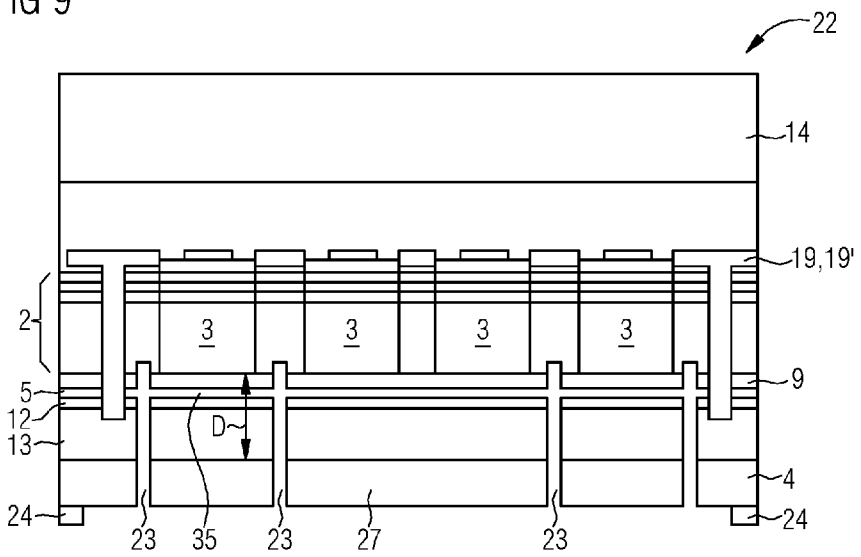
(54) **Title:** METHOD FOR MANUFACTURING A PLURALITY OF SEMICONDUCTOR CHIPS

FIG 9



(57) **Abstract:** A method for manufacturing a plurality of semiconductor chips with the following steps is provided: • - providing a functional semiconductor wafer (1) comprising an epitaxial semiconductor layer sequence (2) with a plurality of chip regions (3), wherein the epitaxial semiconductor layer sequence (2) is connected to a growth substrate (4) with a tether structure (19), and • - removing the growth substrate (4).

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Description

METHOD FOR MANUFACTURING A PLURALITY OF SEMICONDUCTOR CHIPS

A method for manufacturing a plurality of semiconductor chips is provided.

An improved method for manufacturing a plurality of semiconductor chips, wherein a growth substrate is removed from a semiconductor layer sequence on wafer level, is to be provided.

This object is achieved with the method having the steps of claim 1.

Improved embodiments and developments of the method are given in the dependent claims.

According to an embodiment of the method for manufacturing a plurality of semiconductor chips, a functional semiconductor wafer comprising an epitaxial semiconductor layer sequence with a plurality of chip regions is provided. Particularly, the epitaxial semiconductor layer sequence is connected to a growth substrate with a tether structure. For example, the epitaxial semiconductor layer sequence is epitaxially grown on or over the growth substrate. Particularly, the growth substrate is lattice matched to the epitaxial semiconductor layer sequence. For example, the growth substrate comprises or consists of gallium nitride or sapphire.

Particularly, the growth substrate is part of a hanging membrane structure in a central region of the functional semiconductor wafer, wherein the hanging membrane structure

is fixed to the growth substrate at least in a boundary region of the functional semiconductor wafer by the tether structure. For example, the hanging membrane structure comprises or consists of a plurality of membrane elements in the central region.

Particularly, the chip regions of the epitaxial semiconductor layer sequence comprise an active zone generating electromagnetic radiation during operation of the finished semiconductor chips. For example, the active zone is arranged between an n-doped epitaxial semiconductor layer and a p-doped epitaxial semiconductor layer.

According to a further embodiment of the method, the epitaxial semiconductor layer sequence comprises or consists of one or several III/V compound semiconductor materials, particularly nitride semiconductor compound materials. Nitride semiconductor compound materials are semiconductor compound materials containing nitrogen such as the materials from the system $In_xAl_yGa_{1-x-y}N$ mit $0 \leq x \leq 1$, $0 \leq y \leq 1$ and $x+y \leq 1$.

Particularly, the epitaxial semiconductor layer sequence and the growth substrate are provided as part of the functional semiconductor wafer. Therefore, the epitaxial semiconductor layer sequence and the growth substrate each have a main extension plane arranged particularly preferably parallel to each other. The extension of the epitaxial semiconductor layer sequence and the growth substrate along the main extension plane is much larger than perpendicular to the main extension plane.

Particularly, the tether structure is comprised by the functional semiconductor wafer and is part of the epitaxial semiconductor layer sequence as well as of the growth substrate. The tether structure mechanically fixes the epitaxial semiconductor layer sequence to the growth substrate. Preferably, the tether structure is the only element within the functional semiconductor wafer fixing the epitaxial semiconductor layer sequence to the growth substrate. Particularly preferably, the epitaxial semiconductor layer sequence is not in direct contact with the growth substrate.

According to a further embodiment of the method, the growth substrate is removed, preferably completely. Particularly, the growth substrate is removed on wafer level from the functional semiconductor wafer. The functional semiconductor wafer is, for example, singulated into separated semiconductor chips at a later stage. A batch process on wafer level particularly has the advantage of reduced process time.

Particularly, the method for manufacturing a plurality of semiconductor chips comprises the steps:
- providing the functional semiconductor wafer comprising the epitaxial semiconductor layer sequence with the plurality of chip regions, wherein the epitaxial semiconductor layer sequence is connected to the growth substrate with the tether structure, and
- removing the growth substrate.

It is an idea of the method to remove the growth substrate from the functional semiconductor wafer in a controlled manner with the help of the tether structure. Particularly,

removal of the growth substrate takes place in at least two different steps. First, in the central region of the functional semiconductor wafer the sacrificial layer is removed. After removal of the sacrificial layer, the growth substrate is still fixed to the functional semiconductor wafer by the tether structure. Particular, the growth substrate is part of or forms the hanging membrane structure.

Then, the hanging membrane structure comprising the growth substrate is finally removed in a second step. Thus, the tether structure prevents sticking of the growth substrate to the functional semiconductor wafer in an uncontrolled manner. This enhances reliability and prevents damage to the chip regions during manufacturing.

The tether structure can then be removed in a further step, for example, by etching. If the tether structure comprises or consists of silicon dioxide, HF is, for example, used for etching the tether structure. If the tether structure comprises or consists of a polymer, a solvent can be used for removing the tether structure.

According to a further embodiment of the method, a gap is arranged between the epitaxial semiconductor layer sequence and the growth substrate. For example, the gap extends over the central region of the functional semiconductor wafer between the epitaxial semiconductor layer sequence and the growth substrate. The gap is, for example, filled with a gaseous medium, such as ambient air. The gap between the epitaxial semiconductor layer sequence and the growth substrate has a thickness perpendicular to the main extension plane between 100 nanometer and 800 nanometer, limits inclusive.

According to a further embodiment of the method, the gap defines a distance between the epitaxial semiconductor layer sequence and the growth substrate. In particular, the tether structure fixes the distance between the epitaxial semiconductor layer sequence and the growth substrate. In other words, the tether structure acts as a distance holder between the epitaxial semiconductor layer sequence and the growth substrate. Particularly, the tether structure is a mechanically stable element configured to fix the distance between the epitaxial semiconductor layer sequence and the growth substrate mechanically stable. Particularly, the distance between the epitaxial semiconductor layer sequence and the growth substrate is not necessarily the same as a width of the gap, since the hanging membrane structure can comprise further layers, particularly semiconductor layers, between the growth substrate and the epitaxial semiconductor layer sequence.

According to a further embodiment of the method, the gap is generated by electrochemically etching a sacrificial layer arranged at least between the chip regions and the growth substrate. For example, the sacrificial layer is arranged in direct contact on the growth substrate and particularly preferably is also epitaxially grown on the growth substrate. Preferably, the epitaxial semiconductor layer sequence is arranged on or over the sacrificial layer and, for example, epitaxially grown on or over the sacrificial layer. By electrochemically etching the sacrificial layer, the sacrificial layer is dissolved and removed from the functional semiconductor wafer such that the gap is generated at least partially in the central region of the functional semiconductor wafer. Particularly, the tether structure is

not dissolved during electrochemical etching of the sacrificial layer.

For electrochemical etching, the functional semiconductor wafer is arranged within an electrochemical etchant and an ECE voltage is applied between a first ECE contact on the functional semiconductor wafer and a second ECE contact within the electrochemical etchant. When the ECE voltage is applied the sacrificial layer is dissolved.

For example, the sacrificial layer extends completely over the growth substrate. Alternatively, the sacrificial layer is only formed in places over the growth substrate, particularly only between the chip regions and the growth substrate.

According to a further embodiment of the method, the sacrificial layer comprises or consists of a highly n-doped semiconductor material, particularly of a highly n-doped nitride semiconductor compound material. Particularly, a highly n-doped nitride semiconductor compound material has a higher etching rate in the electrochemical etchant than a lower n-doped or undoped nitride semiconductor compound material. Particularly, the active radiation generating zone of the chip regions is low doped, non-doped or only unintentionally doped. Therefore, the sacrificial layer comprising the highly n-doped semiconductor material can be electrochemically etched against the chip regions. Particularly, the highly n-doped semiconductor material has a dopant concentration of at least $10^{18}/cm^3$.

According to a further embodiment of the method, electrochemical etching of the sacrificial layer is carried out through etching channels penetrating partially through

the functional semiconductor wafer. Particularly, the etching channels penetrate through the growth substrate and the sacrificial layer such that the sacrificial layer is accessible through the etching channels. Particularly, the etching channels are arranged between the chip regions and extend perpendicular to the main extension plane. The etching channels can have any geometry. For example, the etching channels have, in plan view on the functional semiconductor wafer, a round, a circular or a cross-formed base area.

It is also possible that the etching channels are embodied as grooves extending along a main extension direction along the functional semiconductor wafer. Particularly, the grooves can extend parallel to each other. For example, the grooves correspond at least partially to separation lines along which the semiconductor chips are separated at a later stage. One or more rows of chip regions can be arranged between two directly adjacent grooves.

For example, the rows of chip regions can be separated from each other by mesas not penetrating the growth substrate. The mesas also correspond to the separation lines and/or the grooves, for example. Particularly, etching channels embodied as grooves extending along separation lines are arranged within the central region of the functional semiconductor wafer. During electrochemical etching of the sacrificial layer, the electrochemical etchant penetrates through the etching channels and reaches the sacrificial layer. When the ECE voltage is applied to the first ECE contact on the functional semiconductor wafer and the second ECE contact arranged within the electrochemical etchant, the sacrificial layer is dissolved such that the gap is created.

According to a further embodiment of the method, the tether structure comprises or consists of a ring-like structure in the boundary region of the functional semiconductor wafer. For example, the tether structure surrounds the central region of the functional semiconductor wafer in plan view. For example, the central region of the functional semiconductor wafer is free of the tether structure.

According to a further embodiment of the method, the ring-like structure of the tether structure acts as an etch stop element during electrochemical etching of the sacrificial layer. In that case, the ring-like structure of the tether structure arranged in the boundary region of the functional semiconductor wafer is freely accessible through the etching channels after etching of the sacrificial layer. Particularly, in that case the ring-like structure penetrates the sacrificial layer and separates the sacrificial layer within the boundary region laterally from the sacrificial layer in the central region. In this way, a hanging membrane structure can be achieved in the central region of the functional semiconductor wafer, which is fixed in the boundary region by the tether structure and the sacrificial layer to the growth substrate.

According to a further embodiment of the method, the tether structure comprises at least one column arranged between two chip regions in the central region of the functional semiconductor wafer. Particularly, the column of the tether structure ensures that the gap between the growth substrate and the semiconductor layer sequence in the central region stays open after electrochemical etching of the sacrificial layer. In other words, the column prevents sticking of the growth substrate and the functional semiconductor layer

sequence after removal of the sacrificial layer. If there is more than one column, particularly at least two columns, comprised by the tether structure arranged within the central region between two chip regions, a lateral distance between the columns is preferably greater than one chip region. In other words, more than one chip region is arranged between two directly adjacent columns or between a column in the central region and the ring-like structure in the boundary region. For example, the column has a diameter not exceeding 10 micrometer or not exceeding 5 micrometer. A lateral distance between two directly adjacent columns or between a column and the ring-like structure in the boundary region is, for example, at least 1 millimeter.

Particularly, the columns extend perpendicular to the main extension plane of the functional semiconductor wafer and penetrate the sacrificial layer. For example, the columns are arranged within the separation lines. Preferably, the columns extend through the sacrificial layer, for example until a surface of the sacrificial layer facing the growth substrate.

After removal of the sacrificial layer, the growth substrate within the central region forms a hanging membrane structure fixed to the functional semiconductor wafer by the columns within the central region. For example, the hanging membrane structure comprises several membrane elements, wherein each membrane element is fixed to the functional semiconductor wafer by to directly adjacent columns or by a column and the directly adjacent ring-like structure.

According to a further embodiment of the method, the tether structure comprises or consists of a dielectric material. For example, an oxide, a nitride, or a polymer can be used as

dielectric material. As an oxide silicon oxide is suitable, while silicon nitride is a suitable as nitride. As a polymer a photoresist can be used.

According to a further embodiment of the method, the etching channels comprise a ring-shaped etching channel separated in at least two parts by at least one connecting element. In other words, the ring-shaped etching channels comprise or consist of at least two parts, wherein the connecting element is arranged therebetween. Particularly, the etching channel is not formed within the connecting element. In this embodiment, the connecting element mechanically connects the growth substrate arranged in a central region of the functional semiconductor wafer with the tether structure. The connecting element is particularly preferably formed at least partially by the growth substrate. Particularly, during electrochemical etching of the sacrificial layer, if the ECE voltage is applied between the first ECE contact on the functional semiconductor wafer and the second ECE contact within the electrochemical etchant, an electrical current runs through the connecting element.

Particularly, the ring-shaped etching channel is arranged between the central region of the functional semiconductor wafer and the ring-like structure of the tether structures in the boundary region of the functional semiconductor wafer.

According to a further embodiment of the method, the etching channels have a round base area or a cross-like base area in plan view on the functional semiconductor wafer. Etching channels having a round base area or a cross-like base area in plan view on the functional semiconductor wafer are particularly arranged within the central region of the

functional semiconductor wafer, while the ring-shaped etching channel is arranged in the boundary region. A lateral distance between two directly adjacent etching channels having a round base area or a cross-like base area is between and including 500 micrometer and 5 millimeter. A diameter of the round or cross-like base area is, for example, between 10 micrometer and 80 micrometer.

According to a further embodiment of the method, the tether structure comprises at least one column arranged at a sidewall of an etching channel. Particularly, the column does not completely fill the etching channel. A part of the etching channel is kept free for excess of the electrochemical etchant to the sacrificial layer. Particularly, application of the column of the tether structure to the sidewall of the etching channel is carried out after bonding the functional semiconductor wafer to a further carrier wafer.

According to a further embodiment of the method, the growth substrate is removed by one of the following methods: tape lift-off, ultrasonic treatment, mechanical picking with a stamp.

During the tape lift-off a tape is adhered to a freely accessible main surface of the growth substrate and peeled off such that the growth substrate adhered to the tape is separated from the functional semiconductor wafer.

During an ultrasonic treatment, the functional semiconductor wafer is inserted into a liquid and ultrasound is applied. For example, afterwards or simultaneously the functional semiconductor wafer is pulled out of the liquid, while the

growth substrate of the functional semiconductor wafer is simultaneously sprayed with a liquid in order to remove remainders of the growth substrate.

As a stamp for mechanical picking a PDMS (short for "polydimethylsiloxane") stamp can be used for example, or a wafer such as a silicon wafer or a sapphire wafer, covered with an adhesive layer.

According to a further embodiment of the method, the growth substrate is thinned prior to the generation of the etching channels. This has the advantage that the material to be penetrated for forming the etching channels is reduced. In such a way the etching channels can, for example, be formed by reactive ion etching (RIE) in a timely manner. For example, after thinning the growth substrate has a thickness not exceeding 15 micrometer or not exceeding 20 micrometer or not exceeding 50 micrometer.

According to a further embodiment of the method, the functional semiconductor wafer is bonded to a carrier wafer prior to the removal of the growth substrate such that a wafer compound is achieved. Particularly, the functional semiconductor wafer is bonded to the carrier wafer before the sacrificial layer is removed. The carrier wafer comprises, for example, a semiconductor material such as silicon, germanium or gallium nitride. Particularly, the etching channels are generated after bonding the functional semiconductor wafer to the carrier wafer. Also, thinning preferably takes place after bonding the carrier wafer and the functional semiconductor wafer. For example, bonding is achieved by connecting a metal layer on or over the carrier wafer with a further metal layer on or over the functional

semiconductor wafer. Particularly, the carrier wafer has the same diameter as the functional semiconductor wafer.

The carrier wafer is particularly configured and intended to be part of the finished semiconductor chip and mechanically stabilizes the epitaxial semiconductor layer sequence within the finished semiconductor chip.

According to a further embodiment of the method, the tether structure is removed from the functional semiconductor wafer in a step separately carried out from the removal of the growth substrate. Particularly, the tether structure is removed after the removal of the growth substrate, for example by breaking and/or wet chemical etching. It is also possible that the tether structure is removed before the removal of the growth substrate to facilitate the peeling of the growth substrate.

With the described method, for example, semiconductor chips embodied as an edge emitting laser device or a VCSEL (short for “vertical cavity surface emitting laser”) can be manufactured. Furthermore, LED chips, particularly, UV-LED chips can be achieved.

The semiconductor chips manufactured with the method can be used, for example, in augmented reality applications as well as in a micro-AFS (short for “microstructured adaptive front lighting system”).

Advantageous embodiments and developments of the method for manufacturing a plurality of semiconductor chips result from the exemplary embodiments described below in connection with the Figures.

Figures 1 to 11 show schematic views of stages of a method for manufacturing a plurality of semiconductor chips according to an exemplary embodiment.

Figure 12 shows a schematic view of a stage of a method for manufacturing a plurality of semiconductor chips according to a further exemplary embodiment.

Figure 13 show exemplarily two etching channels of the exemplary embodiment of Figure 12.

Figure 14 shows a schematic view of a stage of a method for manufacturing a plurality of semiconductor chips according to a further exemplary embodiment.

Figure 15 show exemplarily two etching channels of the exemplary embodiment of Figure 14.

Figure 16 shows a schematic view of a stage of a method for manufacturing a plurality of semiconductor chips according to a further exemplary embodiment.

Figure 17 show exemplarily two etching channels of the exemplary embodiment of Figure 16.

Figures 18 to 25 show schematic views of stages of a method for manufacturing a plurality of semiconductor chips according to a further exemplary embodiment.

Figures 26 to 30 each shows a schematic view of a stage of a method for manufacturing a plurality of semiconductor chips according to a further exemplary embodiment.

Figures 31 to 32 show schematic views of stages of a method for manufacturing a plurality of semiconductor chips according to a further embodiment.

Figures 33 to 35 show schematic views of stages of a method for manufacturing a plurality of semiconductor chips according to further exemplary embodiments.

Equal or similar elements as well as elements of equal function are designated with the same reference signs in the Figures. The Figures and the proportions of the elements shown in the Figures are not regarded as being shown to scale. Rather, single elements, in particular layers, can be shown exaggerated in magnitude for the sake of better presentation and/or better understanding.

According to the method of the exemplary embodiment of Figures 1 to 11, a functional semiconductor wafer 1 is provided. The functional semiconductor wafer 1 comprises an epitaxial semiconductor layer sequence 2 with a plurality of chip regions 3. The epitaxial semiconductor layer sequence 2 is arranged on a growth substrate 4. Between the growth substrate 4 and the epitaxial semiconductor layer sequence 2 a sacrificial layer 5 comprising a highly n-doped semiconductor material is arranged.

The epitaxial semiconductor layer sequence 2 comprises a p-doped semiconductor layer 6 and an n-doped semiconductor layer 7, wherein an active zone 8 with a pn-junction for generation of electromagnetic radiation is arranged therebetween.

An etch stop layer 9 is arranged between the sacrificial layer 5 and the epitaxial semiconductor layer sequence 2. The etch stop layer 9 comprises or consists at present of AlN or AlInN. The etch stop layer 9 is configured to stop electrochemical etching of the sacrificial layer 5. Particularly, the etch stop layer 9 has an etching rate in an electrochemical etchant 10 of the sacrificial layer 5 lower than the etching rate of the sacrificial layer 5 during electrochemical etching.

Between the etch stop layer 9 and the n-doped semiconductor layer 7 an unintentionally doped or low doped gallium nitride layer 11 is comprised by the epitaxial semiconductor layer sequence 2. Further, between the sacrificial layer 5 and the growth substrate 4, a further n-doped semiconductor layer 12 and a further unintentionally doped or low doped gallium nitride layer 13 are arranged (Figure 1).

In a next step, a carrier wafer 14 for example comprising or consisting of gallium nitride, silicon or germanium is provided. Particularly, the carrier wafer 14 has at present the same diameter as the functional semiconductor wafer 1. The diameter of the functional semiconductor wafer 1 and the diameter of the carrier wafer 14 are, for example, 2 inch. At present, the carrier wafer 14 is n-doped and therefore electrically conductive. A metal layer 15 is arranged on the carrier wafer 14. The metal layer 15 covers the carrier wafer 14 completely (Figure 2).

The functional semiconductor wafer 1 is processed starting from the surface facing the p-doped semiconductor layer 6. For example, first mirror layers 16 being part of a resonator of a VCSEL are applied on or over the p-doped semiconductor

layer 6. Further, first mirror layers 16 are arranged on the p-contact layers 17 (Figure 3).

In a boundary region 18 of the functional semiconductor wafer 1 a tether structure 19 is introduced. In the present exemplary embodiment, the tether structure 19 comprises a ring-like structure 19' running through the boundary region 18 and surrounding a central region 20 of the functional semiconductor wafer 1. The chip regions 3 which are intended to be part of the finished semiconductor chips are arranged in the central region 20 of the functional semiconductor wafer 1.

For example, the tether structure 19 is formed by etching cavities within the functional semiconductor wafer 1 and particularly through the epitaxial semiconductor layer sequence 2, for example by dry etching. Then, a dielectric material is inserted within the cavities, for example by sputtering or physical vapour deposition (PVD) of an inorganic material such as silicon oxide or silicon nitride. If a polymer is used to form the tether structure, such as a photoresist or benzocyclobutene (BCB), for example spin coating is used to fill the cavities.

Then, a further metal layer 21 is applied on or over the functional semiconductor wafer 1. The further metal layer 21 covers the functional semiconductor wafer 1 completely. It is possible that the cavities are not completely filled by the dielectric material for forming the tether structure 19. In that case, the remaining space within the cavities is filled by the material of the further metal layer 21.

In a further step, the carrier wafer 14 and the functional semiconductor wafer 1 are bonded together via the metal layer 15 and the further metal layer 21. In this way, a mechanically stable wafer compound 22 comprising the carrier wafer 14 and the functional semiconductor wafer 1 is generated (Figure 4).

Then, as for example shown in Figure 5, the growth substrate 4 is thinned, for example by grinding or polishing, such that a remaining thickness of the growth substrate 4 is for example equal or smaller than 20 micrometer.

In a next step, etching channels 23 are introduced in the functional semiconductor wafer 1(Figure 6). Particularly, the etching channels 23 penetrate the functional semiconductor wafer 1 starting from the growth substrate 4. The etching channels 23 penetrate the growth substrate 4 and the further unintentional or low doped gallium nitride layer 13 and particularly the sacrificial layer 5 such that the sacrificial layer 5 is freely accessible. The etching channels 23 are arranged within the central region 20 of the functional semiconductor wafer 1, while the boundary region 18 of the functional semiconductor wafer 1 is free of etching channels 23. The etching channels 23 are, for example, introduced and generated within the functional semiconductor wafer 1 by reactive ion etching.

Then, a first ECE contact 24 is arranged in a ring-shaped manner on the growth substrate 4 within the boundary region 18 of the functional semiconductor wafer 1 (Figure 7). Seen in plan view, the first ECE contact 24 does not cover the ring-like structure 19’.

A sealing ring 25 is placed on the growth substrate 4. Particularly, the sealing ring 25 is positioned to overlap with the ring-like structure 19' in the boundary region 18 of the functional semiconductor wafer 1 in plan view.

The wafer compound 22 and a second ECE contact 26 are placed within an electrochemical etchant 10 (Figure 8). As an electrochemical etchant 10, for example, a 0.3 molar nitridic acid is used. An ECE voltage V is applied between the first ECE contact 24 and the second ECE contact 26 such that the sacrificial layer 5 within the central region 20 until the ring-like structure 19' of the tether structure 19 is dissolved and removed. The ring-like structure 19' in the boundary region 18 acts as an etch stop element during electrochemical etching of the sacrificial layer 5 stopping the electrochemical etching of the sacrificial layer 5 in a lateral direction D_L parallel to a main extension plane E of the wafer compound 22. Furthermore, the etch stop layer 9 stops electrochemical etching in a vertical direction D_V perpendicular to the lateral direction.

After removal of the sacrificial layer 5 by electrochemical etching the growth substrate 4 and the further unintentionally or low-doped semiconductor gallium nitride layer 13 form a hanging membrane structure 27 between the ring-like structure 19' within the central region 20 of the functional semiconductor wafer 1 (Figure 9).

A gap 35 is generated between the epitaxial semiconductor layer sequence 2 and the hanging membrane structure 27 comprising the growth substrate 4 due to the removal of the sacrificial layer 5. The gap 35 is filled by the surrounding air if the wafer compound 22 is removed from the

electrochemical etchant 10. The gap 35 defines a distance D between the epitaxial semiconductor layer sequence 2 and the growth substrate 4.

The hanging membrane structure 27 is removed, for example by one of the techniques described in connection with Figures 33 to 35 (Figure 10).

Then, second mirror layers 28 are applied to the chip regions 3 in order to form together with the first mirror layers 16 resonators of finished semiconductor chips embodied as VCSELs. n-contacts 29, particularly made from a metal, are inserted in the epitaxial semiconductor layer sequence 2 for electrical contact of the n-doped semiconductor layer 7 of the epitaxial semiconductor layer sequence 2.

In a further step, the chip regions 3 within the central region 20 of the functional semiconductor wafer 1 are singulated along separation lines 30 running between the chip regions 3 (Figure 11). During separation, the layers of the wafer compound 22 are separated in single sections, wherein each section is part of a finished semiconductor chip. For sake of simplicity, the singulated parts in the semiconductor chips are in this description often indicated with the same term as in the continuous form in the wafer compound.

Figure 12 shows a plan view of a functional semiconductor wafer 1 of a wafer compound 22 generated during a method according to an exemplary embodiment. Particularly, a central region 20 of the functional semiconductor wafer 1 comprises etching channels 23 formed as grooves 31 running parallel to each other.

A distance Dg between two directly adjacent grooves 31 is, for example, between and including 500 micrometer to 1 millimeter (Figure 13). For example, two rows of chip regions 3 are arranged between two directly adjacent grooves 31. A width W of a groove 31 is, for example, between and including 10 micrometer and 100 micrometer. Each etching channel 23 is connected to a ring shaped first ECE contact 24 via the growth substrate 4. Particularly, the ring shaped first ECE contact 24 can be completely closed or divided into several subunits.

In a boundary region 18 surrounding the central region 20, a ring-shaped etching channel 23' is arranged. Between a ring-shaped first ECE contact 24 and the ring-shaped etching channel 23', a ring-shaped structure 19' of a tether structure 19 is arranged.

The first ECE contact 24 and the ring-shaped structure 19' form closed rings around the central region 20. In contrast, the ring-shaped etching channel 23' is at present divided into four parts wherein two parts are separated from each other by a connecting element 32. The connection element 32 mechanically connects the growth substrate 4 arranged in the central region 20 of the functional semiconductor wafer 1 with the growth substrate 4 in the boundary region 18 and particularly with the ring-shaped structure 19' of the tether structure 19. In such a way, the connecting elements 32 form hinges connecting the hanging membrane structure 27 formed after the removal of the sacrificial layer 5 with the boundary region 18 and particularly with the tether structure 19. In the present exemplary embodiment, the four connecting elements 32 are only an example for understanding. There might be more or less connecting elements 32. The minimal

number of connecting elements 32 comprised by the wafer compound 22 in this exemplary embodiment is one. The connecting element 32 forms also an ECE current distribution path during electrochemical etching of the sacrificial layer 5.

In contrast to the exemplary embodiment of Figures 12 to 13, the wafer compound 22 according to the exemplary embodiment of Figures 14 to 15 comprises, in a central region 20 of a functional semiconductor wafer 1, etching channels 23 having a round, at present circular, base area 33. The etching channels 23 according to Figure 14 are arranged within the functional semiconductor wafer 1 in a regular cubic grid. As for example schematically shown in Figure 15, two directly adjacent etching channels 23 have a distance Dg to each other between 500 micrometer and several millimeters. A diameter W of the base area 33 of the etching channel 23 is, for example, about 50 micrometer.

The wafer compound 22 according to the exemplary embodiment of Figures 16 and 17 comprises etching channels 23 having a cross-shaped base area 33. Also, these etching channels 23 are arranged in a regular cubic grid in plan view on the functional semiconductor wafer 1. As for example schematically shown in Figure 17, two directly adjacent etching channels 23 have a distance Dg to each other between 500 micrometer and several millimeters. A diameter W of the cross-shaped base area 33 of the etching channel 23 is, for example, about 50 micrometer.

In the method according to the exemplary embodiment of Figures 18 to 25 a functional semiconductor wafer 1 is provided. In contrast to the functional semiconductor wafer 1

according to the exemplary embodiment of Figures 1 to 11, the functional semiconductor wafer 1 according to the exemplary embodiment of Figures 18 to 25 comprises a tether structure 19 having at least one column 34 in a central region 20 of functional semiconductor wafer 1, in addition to the ring-like structure 19' in the boundary region 18 of the functional semiconductor wafer 1.

The column 34 is arranged between two chip regions 3 of the epitaxial semiconductor layer sequence 2 and extends in a direction perpendicular to a main extension plane E of the functional semiconductor wafer 1. Particularly, the column 34 completely penetrates the sacrificial layer 5 and a further n-doped semiconductor layer 12. For example, the column 34 consists of or comprises the same dielectric material as the ring-like structure 19' in the boundary region 18 of the functional semiconductor wafer 1. For example, the tether structure 19 comprises more than one column 34 arranged within the central region 20 of the functional semiconductor wafer 1.

A distance between two directly adjacent columns 34 is not necessarily only one chip region 3. Rather, the distance between two directly adjacent columns 34 within the central region 20 of the functional semiconductor wafer 1 is more than one chip region 3. For example, a distance between two directly adjacent columns 34 is at least 100 micrometer, for example at least 1 millimeter. The column 34 has a diameter, for example not exceeding 10 micrometer or not exceeding 5 micrometer. For example, the column 34 is arranged within a separation line 30 intended for separation of the finished semiconductor chips.

Further, a carrier wafer 14 is provided. A metal layer 15 is arranged over the carrier wafer 14, while a further metal layer 21 is arranged over the functional semiconductor wafer 1 (Figure 18).

The carrier wafer 14 and the functional semiconductor wafer 1 are bonded together in order to form a wafer compound 22. For bonding, the metal layer 15 over the carrier wafer 14 and the further metal layer 21 over the functional semiconductor 1 wafer are directly and mechanically stably connected to each other, for example by impact of temperature and pressure (Figure 19).

After forming the wafer compound 22, the growth substrate 4 of the functional semiconductor wafer 1 is thinned, for example by grinding, polishing or electrochemical polishing (Figure 20).

Then, as for example shown in Figure 21, etching channels 23 are arranged within the functional semiconductor wafer 1. The etching channels 23 particularly completely penetrate the growth substrate 4, the further unintentionally or low doped gallium nitride layer 13, the further n-doped semiconductor layer 12 and the sacrificial layer 5 as well as the etch stop layer 9. The etching channels 23 are arranged between the chip regions 3. Particularly, the etching channels 23 are arranged along separation lines 30 but do not overlap with the columns 34 in plan view on the functional semiconductor wafer 1.

Then, a ring-shaped first ECE contact 24 is applied to the functional semiconductor wafer 1 in the boundary region 18 (Figure 22). Particularly, the first ECE contact 24 is a

metallic layer arranged in a ring-shaped manner running around the central region 20 of the functional semiconductor wafer 1 as described in connection with Figures 12, 14 and 16.

Then, the sacrificial layer 5 within the central region 20 is electrochemically etched, as for example already described in connection with Figures 8 and 9. A hanging membrane structure 27 is created by removal of the sacrificial layer 5, the hanging membrane structure 27 being fixed to the epitaxial semiconductor layer sequence 2 by the column 34 within the central region 20 of the functional semiconductor wafer 1 and by the ring-shaped structure 19' in the boundary region 18 of the functional semiconductor wafer 1.

Again, a gap 35 is generated between the epitaxial semiconductor layer sequence 2 and the growth substrate 4 due to the removal of the sacrificial layer 5. The gap 35 defines a distance D between the epitaxial semiconductor layer sequence 2 and the growth substrate 4. Particularly, the column 34 fixes the distance D within the central region 20 of the functional semiconductor wafer 1.

Then, the hanging membrane structure 27 comprising the growth substrate 4 is removed in the central region 20 of the functional semiconductor wafer 1. The column 34 of the tether structure 19 still remains and exceeds the epitaxial semiconductor layer sequence 2 (Figure 24). The column 34 within the central region 20 of the functional semiconductor wafer 1 and particularly the part of the column 34 exceeding the epitaxial semiconductor layer sequence 2 are, for example, mechanically removed by breaking, or wet chemical etching.

Then, processing takes place as already described in connection with Figure 11 (Figure 25).

Figure 26 shows a plan view on a functional semiconductor wafer 1 of a wafer compound 22 generated during a method according to an exemplary embodiment. Compared to the wafer compound 22 of Figure 12, columns 34 are arranged within the central region 20 of the functional semiconductor wafer 1 along a line between the grooves 31.

Compared to the functional semiconductor wafer 1 of the wafer compound 22 of Figure 14, the functional semiconductor wafer 1 of the wafer compound 22 of the exemplary embodiment of Figure 27 has a tether structure 19 comprising, besides the ring-like structure 19' in the boundary region 18, an additional column 34 within the central region 20 of the functional semiconductor wafer 1.

Compared to the wafer compound 22 of the exemplary embodiment of Figure 16, also the wafer compound 22 according to the exemplary embodiment of Figure 28 comprises a tether structure 19 with an additional column 34 arranged within the central region 20 of the functional semiconductor wafer 1.

With the help of the methods according to the exemplary embodiments of Figures 29 and 30 manufacturing of the etching channels 23 and the tether structure 19 is described in further detail. Particularly, two different photolithographic designs for manufacturing of the etching channels 23 and the tether structure 19 are shown.

The etching channels 23 and the tether structure 19 are both manufactured with the help of a structured photo resist mask. Areas of the surface to be structured are not covered by the structured photo resist mask, while areas of the surface not being structured are covered by the structured photo resist mask or vice versa. In order to generate the structured photo resist mask, stepwise exposure of a photoresist layer is carried out. The photoresist layer is scanned stepwise in exposure steps, wherein in each exposure step an area 36 of the photoresist layer is exposed with the same pattern.

Figure 29 shows a layout of the structured photo resist mask within a central region 20 of the functional semiconductor wafer 1 according to an exemplary embodiment.

Scanning of the photo resist layer on the surface of the functional semiconductor wafer 1 to be patterned takes place such that the exposure steps are carried out exhaustive within in the central region 20. In other words, the areas 36 exposed in directly subsequent exposure steps are directly adjacent to each other.

The pattern of the exposure steps according to Figure 29 comprises etching channels 23 embodied as cross-shaped grooves 31 placed in a center of the area 36 to be exposed. Columns 34 of tether structure 19 with a round base area 33 are placed in a square generated by the cross-shaped etching channels 23. Connecting elements 32 are arranged between two directly adjacent cross-shaped etching channels 31 such that membrane elements 37 of a hanging membrane structure 27 are defined, when the sacrificial layer 5 is removed.

In other words, when the sacrificial layer 5 is removed by electrochemical etching, the hanging membrane structure 27 in the central region 20 of the functional semiconductor wafer 1 is still connected by the connecting elements 32. In order to remove the growth substrate 4 completely from the functional semiconductor wafer 1, the connecting elements 32 are removed in a separate step, for example mechanically and/or chemically.

Figure 30 shows a layout of the structured photo resist mask within a central region 20 of the functional semiconductor wafer 1 according to a further exemplary embodiment.

Compared to the layout of Figure 29, the layout according to Figure 30 comprises etching channels 23 embodied as cross-shaped grooves 31 placed along the rectangular boundaries of the area 36 to be exposed in one exposure step. The grooves 31 are again separated by connecting elements 32. The gross-shaped grooves 31 define rectangular areas forming membrane elements 37 of a hanging membrane structure 27 after removal of the sacrificial layer 5. The membrane elements 37 are connected to each other by the connecting elements 32. In each membrane element 37 at least three columns 34 as part of a tether structure 19 are arranged connecting the membrane elements 37 to the carrier wafer 14 and prevent tilting of the membrane elements 37.

The membrane elements 37 are removed in a subsequent step, for example mechanically (not shown).

In contrast to the exemplary embodiment of Figures 18 to 25, during the method according to the exemplary embodiment of Figures 31 to 32, a column 34 of a tether structure 19 is

arranged at a sidewall 38 of an etching channel 23. Particularly, the column 34 is applied to the sidewall 38 of the etching channel 23 after the functional semiconductor wafer 1 is bonded to a carrier wafer 14 (Figure 31).

The functional semiconductor wafer 1 is covered with a dielectric bonding layer 43 instead of a further metal layer 21. The carrier wafer 22 and the functional semiconductor wafer 1 are connected to each other to form the wafer compound 22 via the metal layer 15 and the dielectric bonding layer 43. For example, the dielectric bonding layer 43 comprises or consists of silicon dioxide.

Then, the sacrificial layer 5 is removed by electrochemical etching. Particularly, the column 34 does not cover the whole sidewall 38 of the etching channel 23 in order to enable access of an electrochemical etchant 10 to the sacrificial layer 5 within the central region 20 (Figure 32).

In connection with the exemplary embodiments of Figures 33 to 35, removal of the hanging membrane structure 27 comprising the growth substrate 4 is explained in further detail.

As for example shown in Figure 33, after removal of the sacrificial layer 5 the wafer compound 22 is introduced parallel to the force of gravity within a liquid 39 such as water. An ultrasound breaking the tether structure 19 is applied to the liquid 39. During treatment with the ultrasound, the wafer compound 22 is pulled parallel to the force of gravity out of the liquid 39 and the part of the wafer compound 22 above the liquid 39 is simultaneous sprayed in order to remove parts of the hanging membrane structure 27

comprising the growth substrate 4 and/or broken parts of the tether structure 19.

Further, the hanging membrane structure 27 with the growth substrate 4 can be removed by a tape lift-off process as, for example, schematically shown in Figure 34. For the tape lift-off a tape 40 is laminated on the hanging membrane structure 27 and pulled off such that the hanging membrane structure 27 with the growth substrate 4 adheres to the tape 40 and is removed from the wafer compound 22.

As for example shown in Figure 35, it is also possible to remove the growth substrate 4 with the help of a stamp 41. The stamp 41 can, for example, be formed by a wafer such as a silicon wafer or a sapphire wafer covered with an adhesive layer 42. As an alternative a PDMS stamp can be used. The stamp is adhered to the growth substrate 4 via the adhesive layer 42 and is then pulled off.

This application claims priority of the German application DE 102023109885.3, the disclosure content of which is incorporated herein by reference.

The invention is not limited to the description of the exemplary embodiments. Rather, the invention comprises each new feature as well as each combination of features, particularly each combination of features of the claims, even if the feature or the combination of features itself is not explicitly given in the claims or the exemplary embodiments.

References

1 functional semiconductor wafer
2 epitaxial semiconductor layer sequence
3 chip region
4 growth substrate
5 sacrificial layer
6 p-doped semiconductor layer
7 n-doped semiconductor layer
8 active zone
9 etch stop layer
10 electrochemical etchant
11 unintentionally doped or low doped gallium nitride layer
12 n-doped semiconductor layer
13 further unintentionally doped or low doped gallium nitride layer
14 carrier wafer
15 metal layer
16 first mirror layer
17 p-contact layer
18 boundary region
19 tether structure
19′ ring-like structure
20 central region
21 further metal layer
22 wafer compound
23 etching channel
23′ ring-shaped etching channel
24 first ECE contact
25 sealing ring
26 second ECE contacta
27 hanging membrane structure
28 second mirror layer

29 n-contact
30 separation line
31 groove
32 connecting element
33 base area
34 column
35 gap
36 area
37 membrane element
38 sidewall
39 liquid
40 tape
41 stamp
42 adhesive layer
43 dielectric bonding layer

V ECE voltage
E main extension plane
D distance
D_L lateral direction
D_V vertical direction
W width/diameter
Dg distance

Claims

1. Method for manufacturing a plurality of semiconductor chips, comprising the steps:
- providing a functional semiconductor wafer (1) comprising an epitaxial semiconductor layer sequence (2) with a plurality of chip regions (3), wherein the epitaxial semiconductor layer sequence (2) is connected to a growth substrate (4) with a tether structure (19), and
- removing the growth substrate (4).

2. Method according to the previous claim, wherein a gap (35) is arranged between the epitaxial semiconductor layer sequence (2) and the growth substrate (4).

3. Method according to the previous claim, wherein
- the gap (35) defines a distance (D) between the epitaxial semiconductor layer sequence (2) and the growth substrate (4), and
- the tether structure (19) fixes the distance (D) between the epitaxial semiconductor layer sequence (2) and the growth substrate (4).

4. Method according to any of the previous claims, wherein the gap (35) is generated by electrochemical etching an sacrificial layer (5) arranged at least between the chip regions (3) and the growth substrate (4).

5. Method according to the previous claim, wherein the electrochemical etching of the sacrificial layer (5) is carried out through etching channels (23) penetrating partially through the functional semiconductor wafer (1).

6. Method according to any of the previous claims, wherein the tether structure (19) comprises a ring-like structure (19') in an boundary region (18) of the functional semiconductor wafer (1).

7. Method according to the previous claim, wherein the ring-like structure (19') acts as an etch stop element during electrochemical etching the sacrificial layer (5).

8. Method according to any of the previous claims, wherein the tether structure (19) comprises at least one column (34) arranged between two chip regions (3) in the central region (20) of the functional semiconductor wafer (1).

9. Method according to any of the previous claims, wherein the tether structure (19) comprises a dielectric material.

10. Method according to any of the previous claims, wherein
- the etching channels (23) comprise a ring-shaped etching channel (23') separated in at least two parts by at least one connecting element (32), and
- the connecting element (32) connects the growth substrate (4) arranged in a central region (20) of the functional semiconductor wafer (1) with the tether structure (19) mechanically.

11. Method according to the previous claim, wherein the ring-shaped etching channel (23') is arranged between the central region (20) of the functional semiconductor wafer (1) and the ring-like structure (19') of the tether structure (19), the ring-like structure (19') being arranged in the boundary region (18) of the functional semiconductor wafer (1).

12. Method according to any of the previous claims, wherein the etching channels (23) have in plan view on the functional semiconductor wafer (1) a round base area (33) or a cross-like base area (33).

13. Method according to any of the previous claims, wherein the tether structure (19) comprises at least one column (34) arranged at a sidewall (38) of an etching channel (23).

14. Method according to any of the previous claims, wherein the growth substrate (4) is removed by one of the following methods: tape lift-off, ultrasonic treatment, mechanical picking with a stamp (41).

15. Method according to any of the previous claims, wherein the growth substrate (4) is thinned prior to the generation of the etching channels (23).

16. Method according to any of the previous claims, wherein the functional semiconductor wafer (1) is bonded to a carrier wafer (14) prior to the removal of the growth substrate (4) such that a wafer compound (22) is achieved.

17. Method according to any of the previous claims, wherein the tether structure (19) is removed from the functional semiconductor wafer (1) in a step separately carried out from the removal of the growth substrate (4).

FIG 1

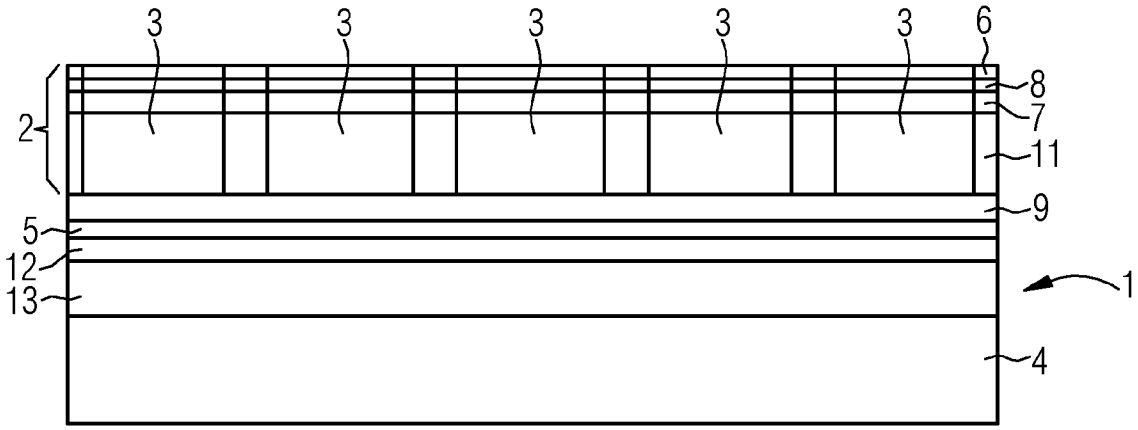

FIG 2

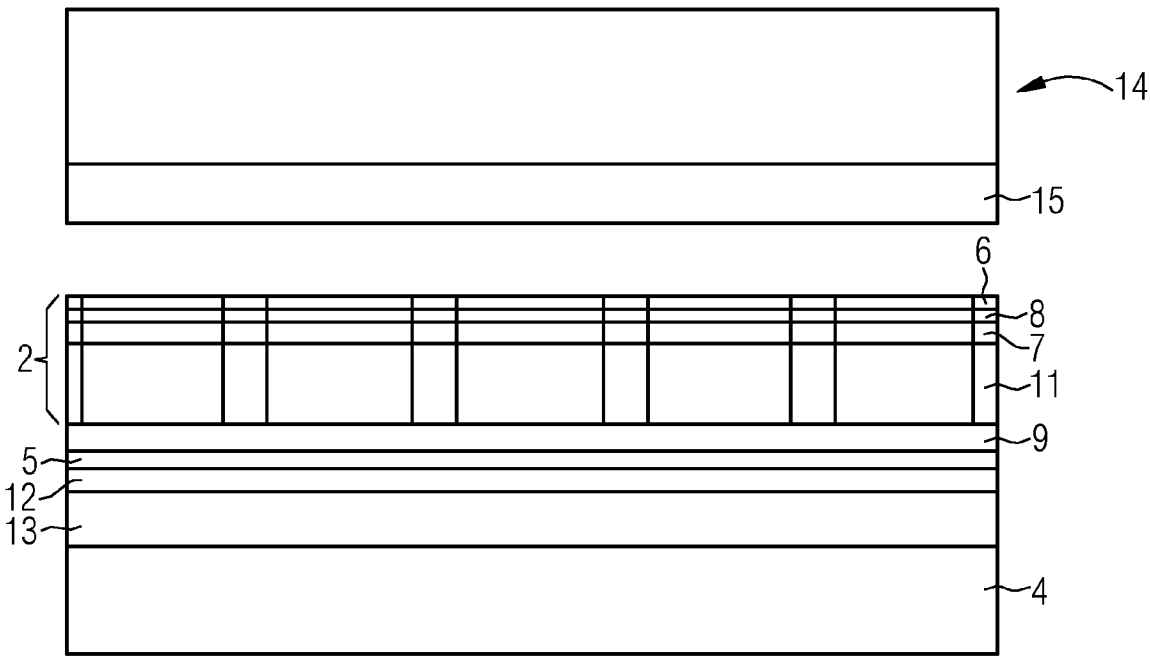

FIG 3

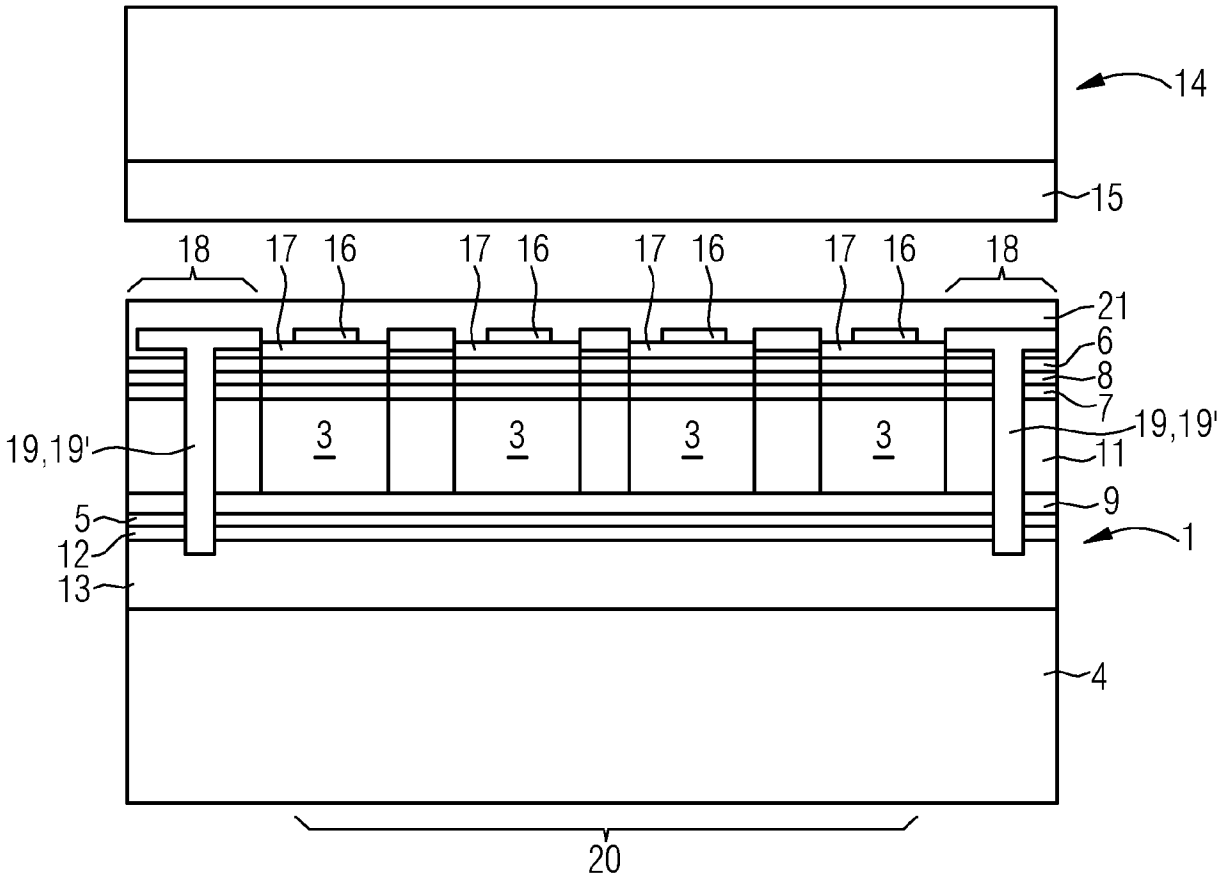
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FIG 4

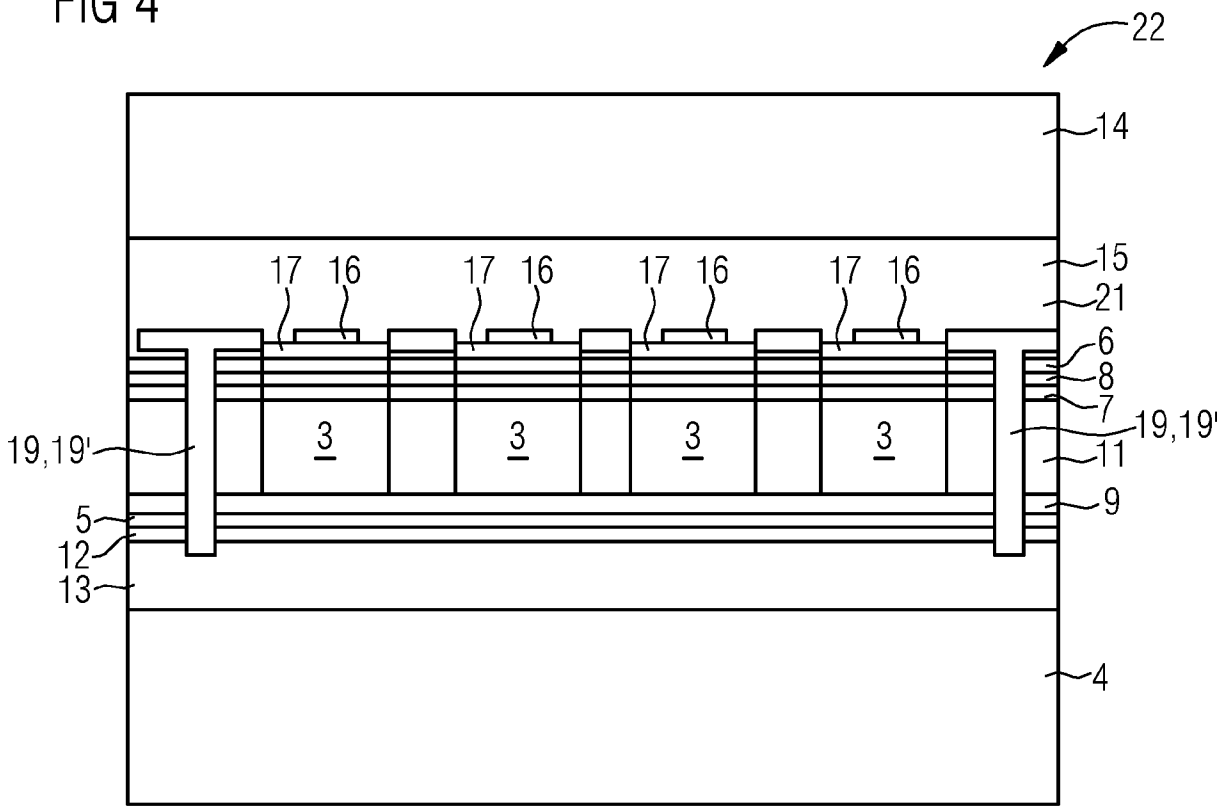
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FIG 5

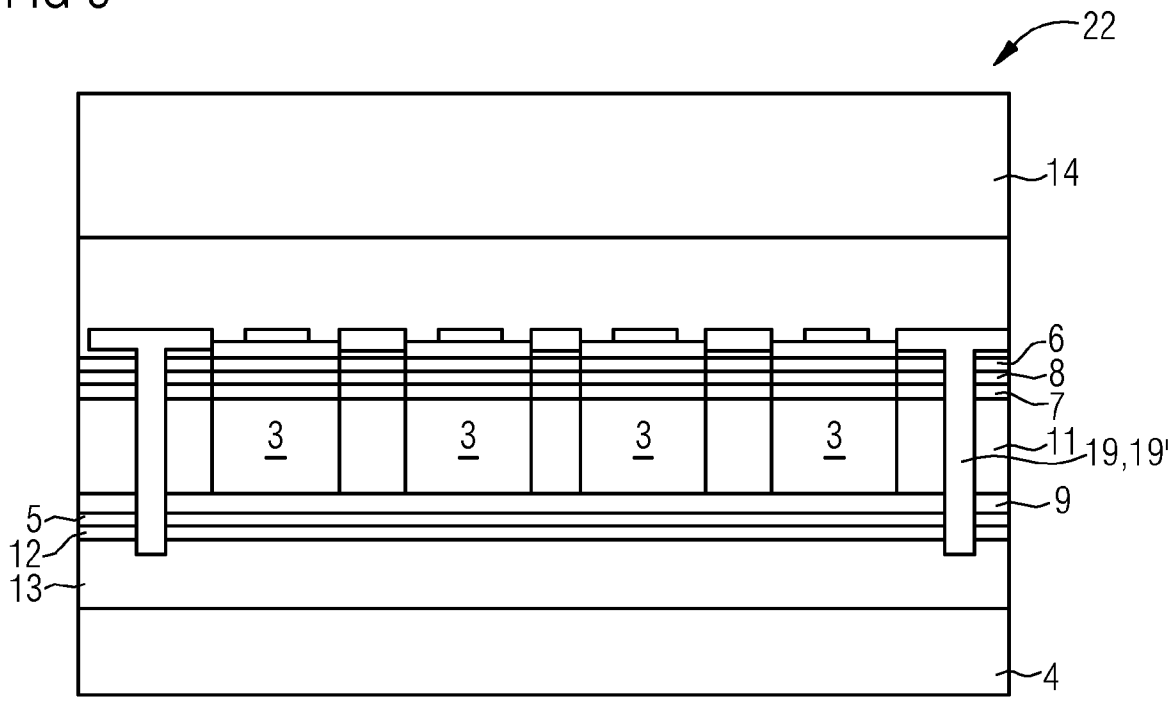
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FIG 6

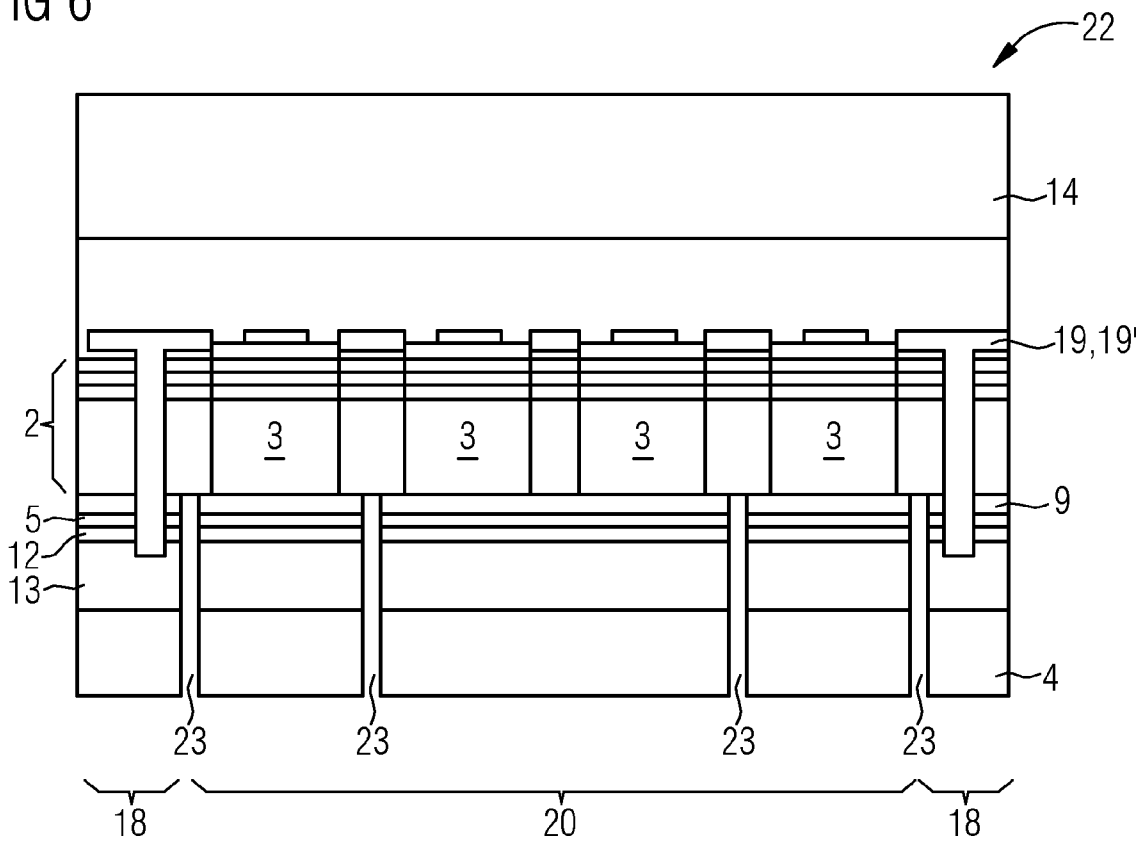
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FIG 7

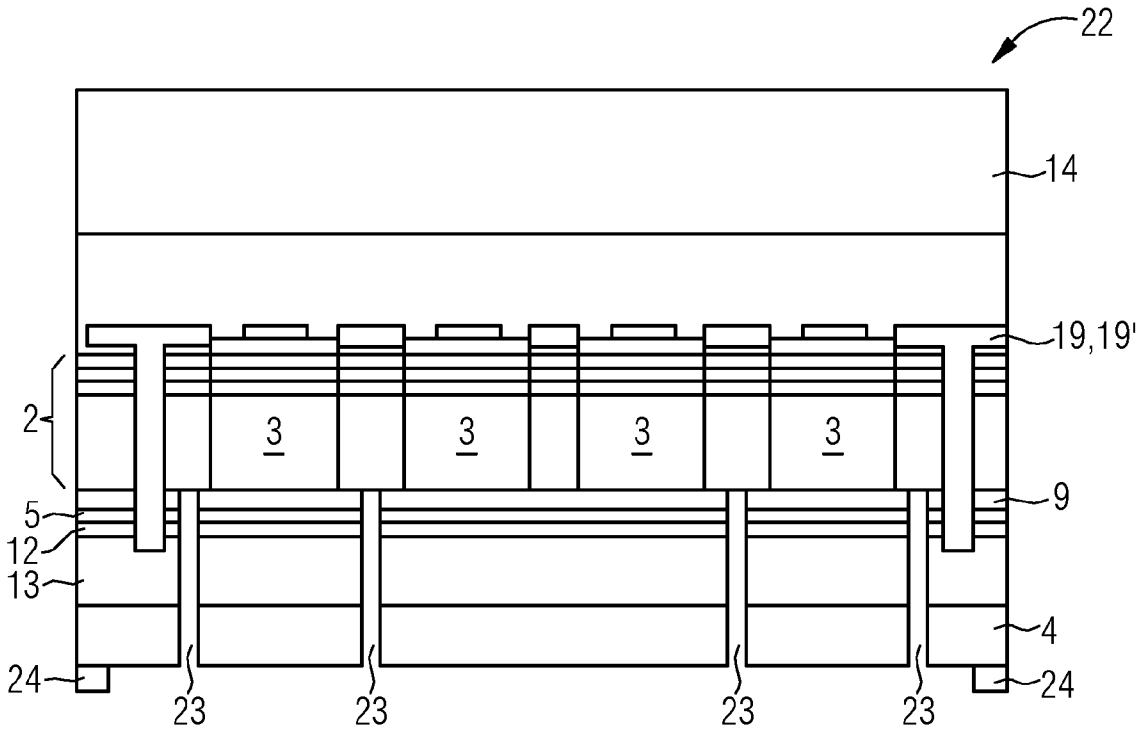
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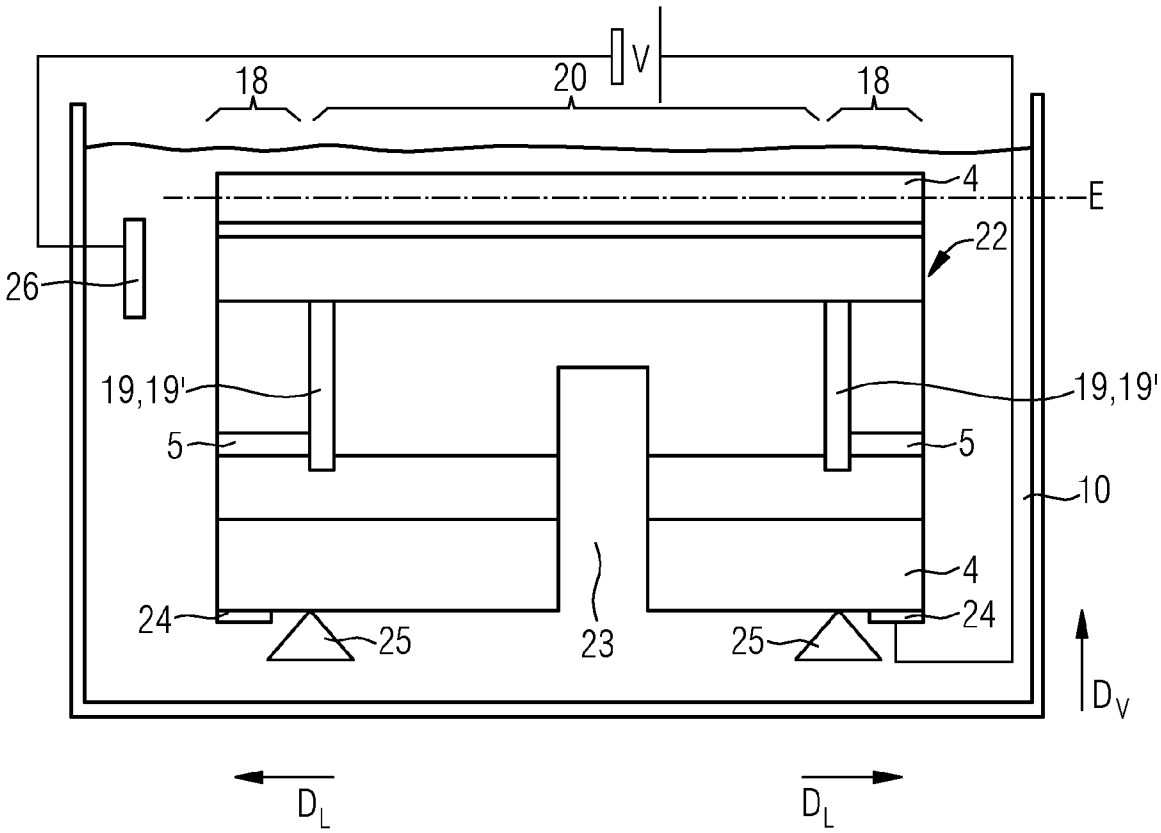
FIG 8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E
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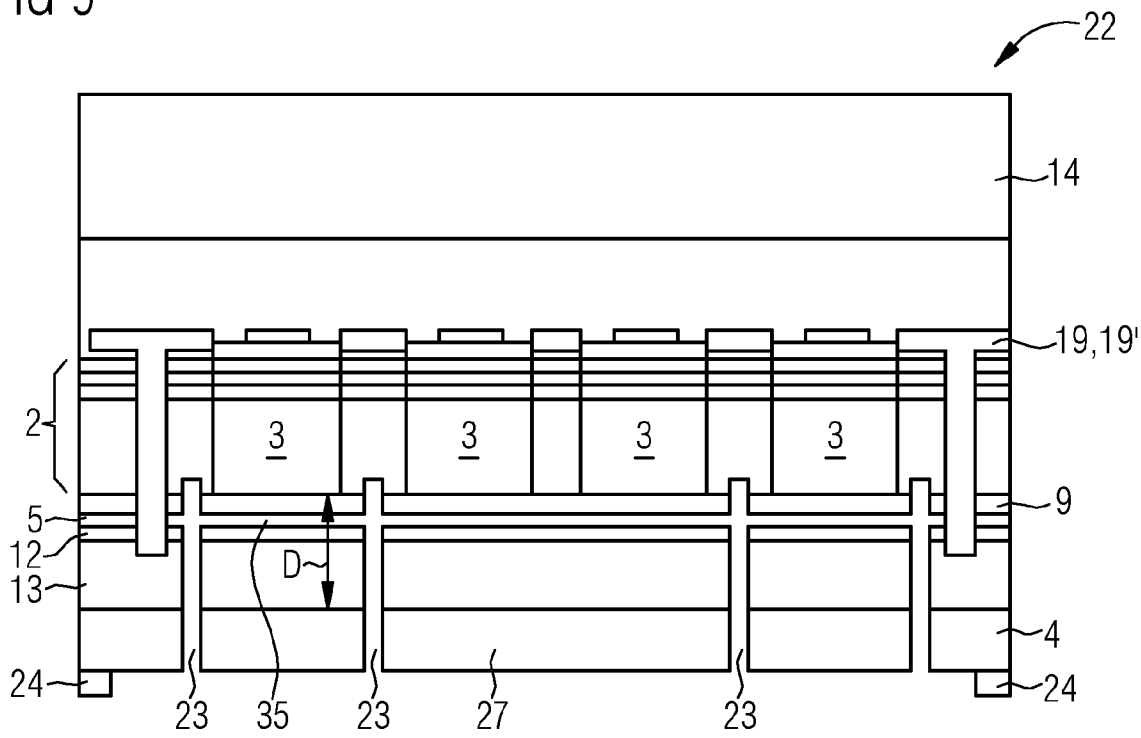
23
25
D_V
D_L
D_L

FIG 9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19,19'
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FIG 10

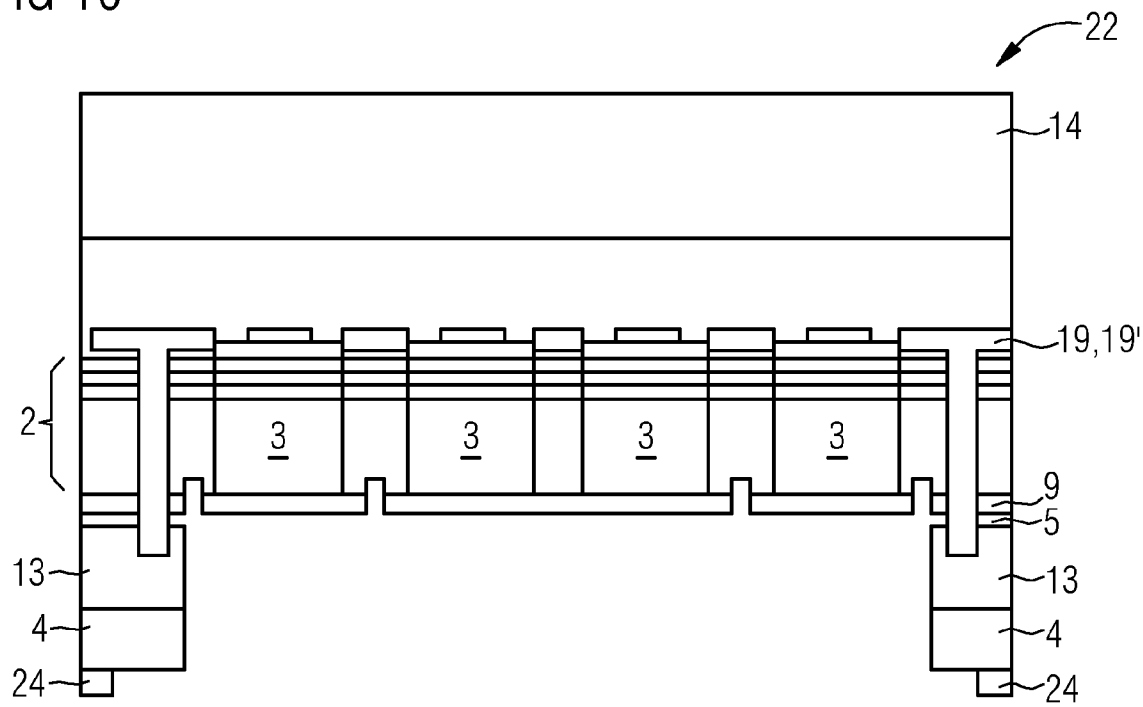
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FIG 11

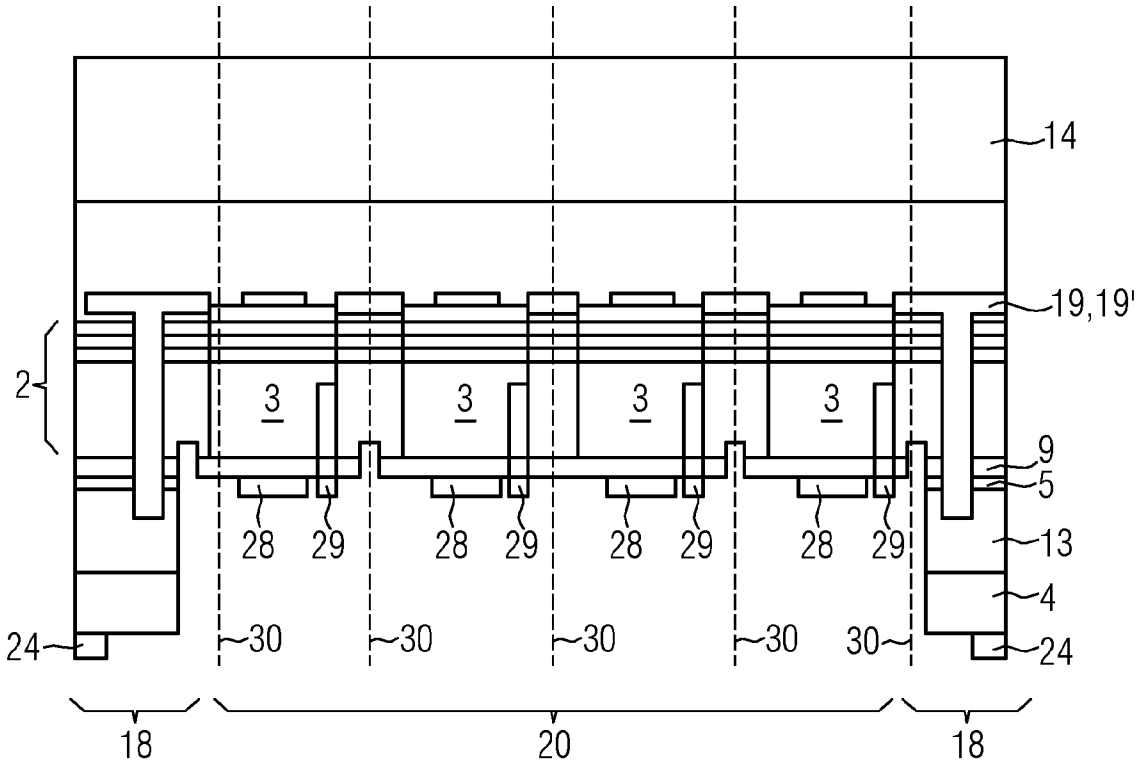
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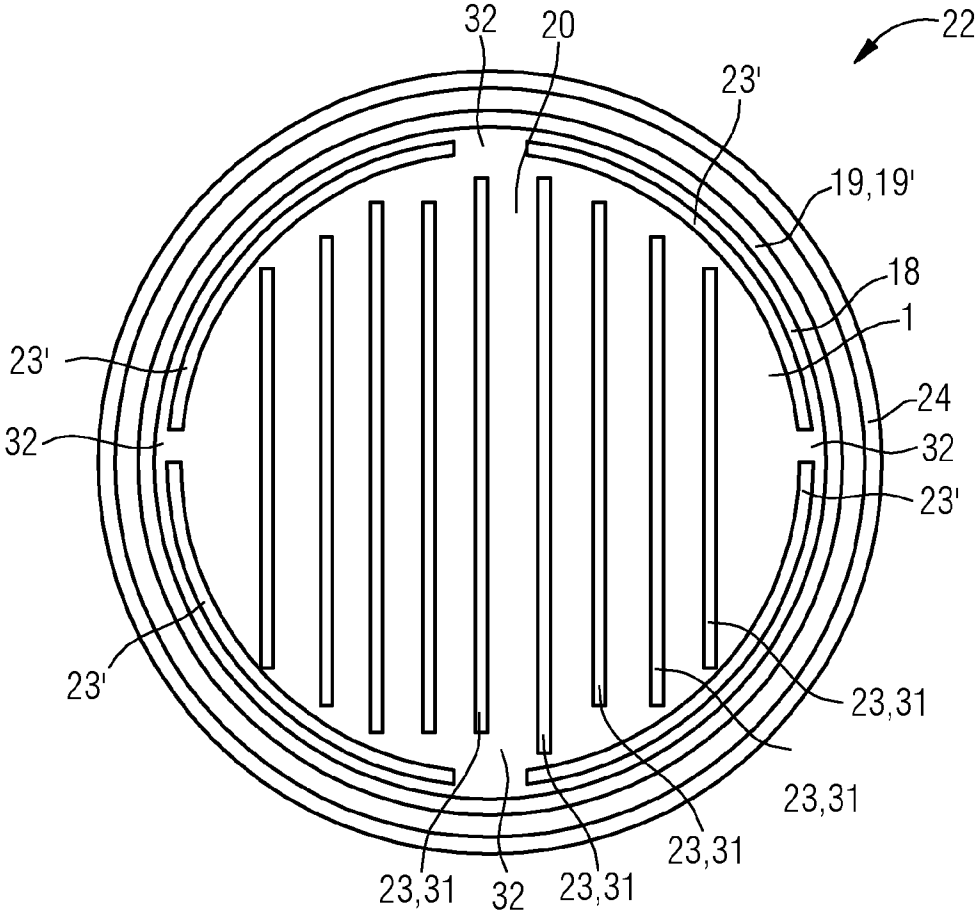
FIG 12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19,19'
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32
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23'
23,31
23,31
23,31
23,31
32
23,31

FIG 13

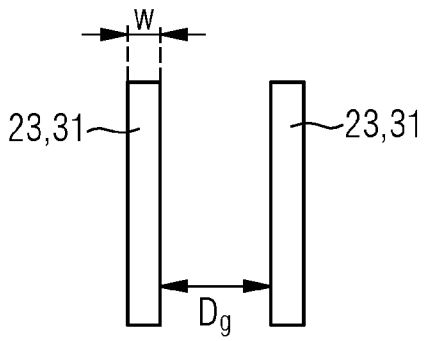
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FIG 14

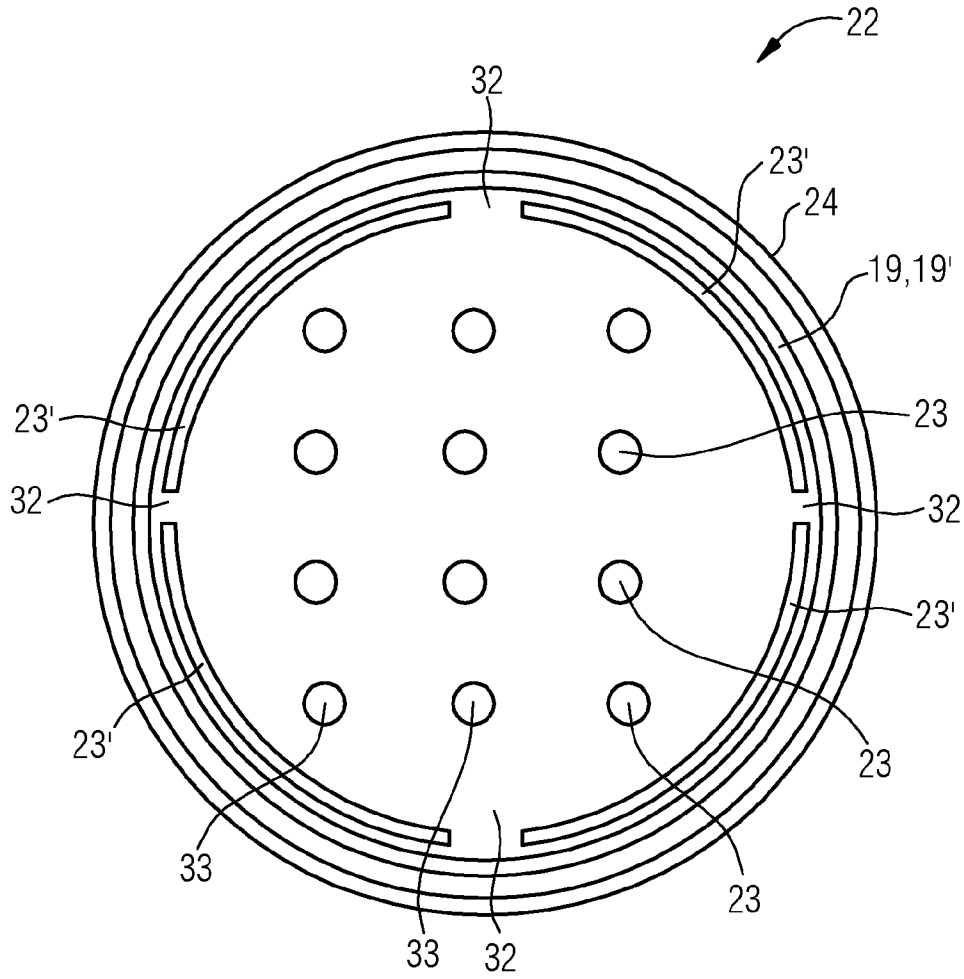

FIG 15

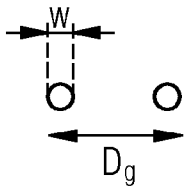

FIG 16

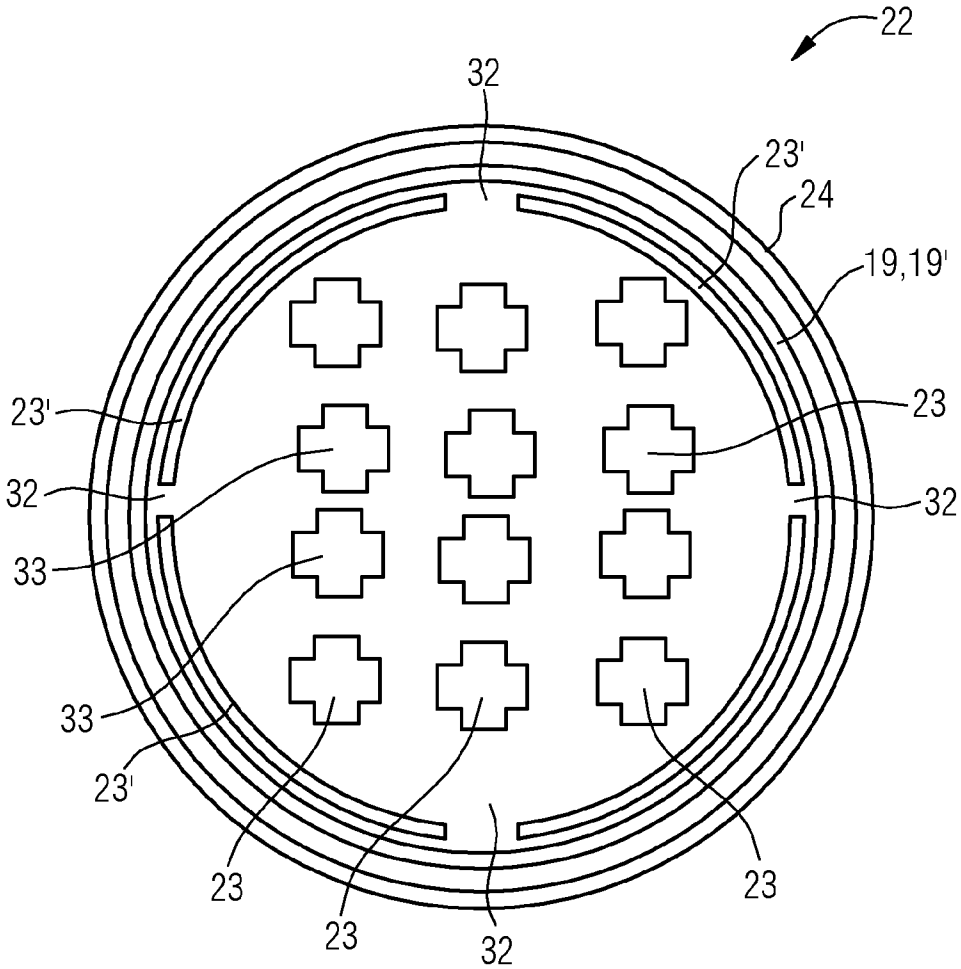

FIG 17

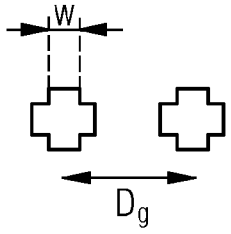

FIG 18

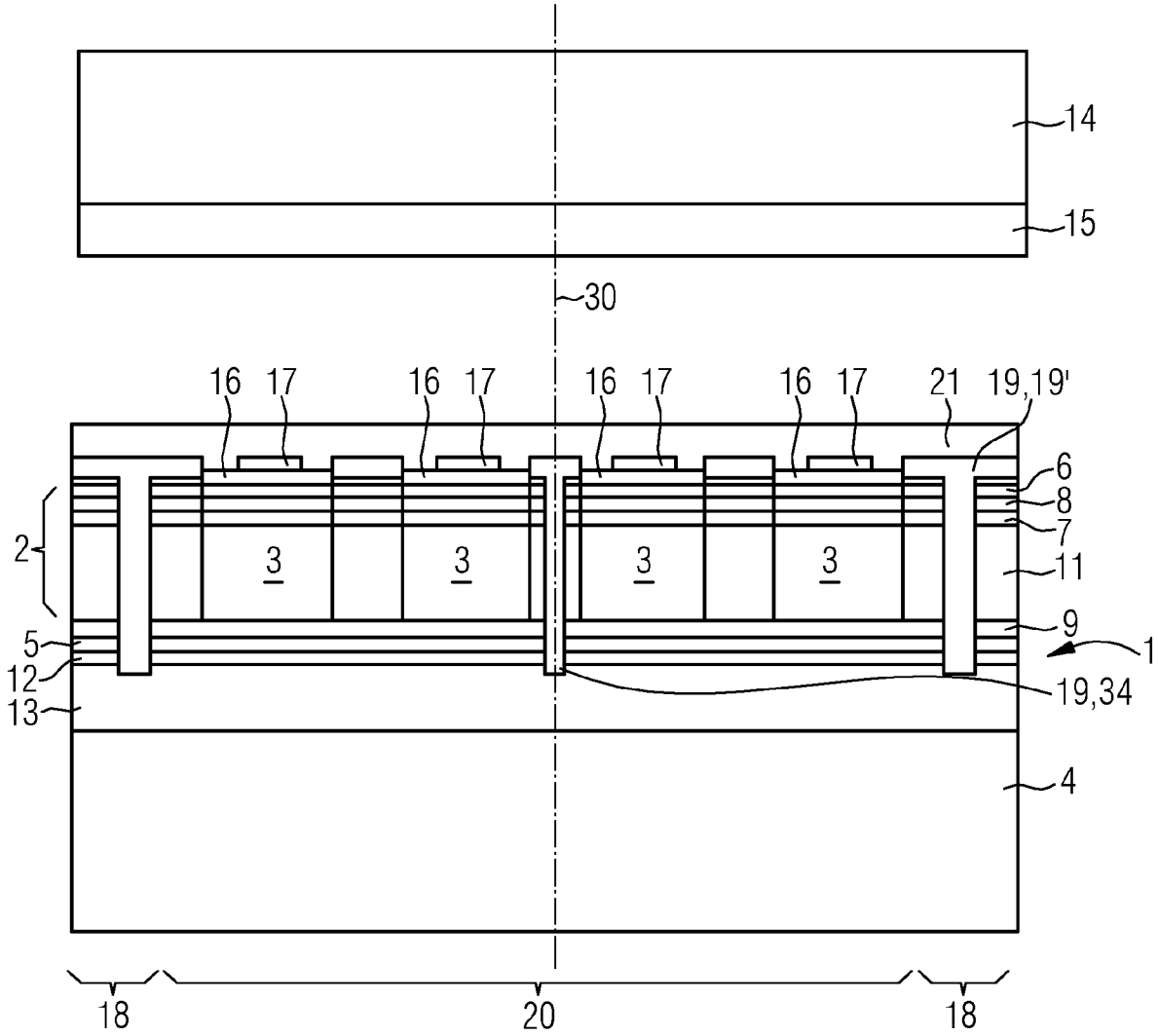
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FIG 19

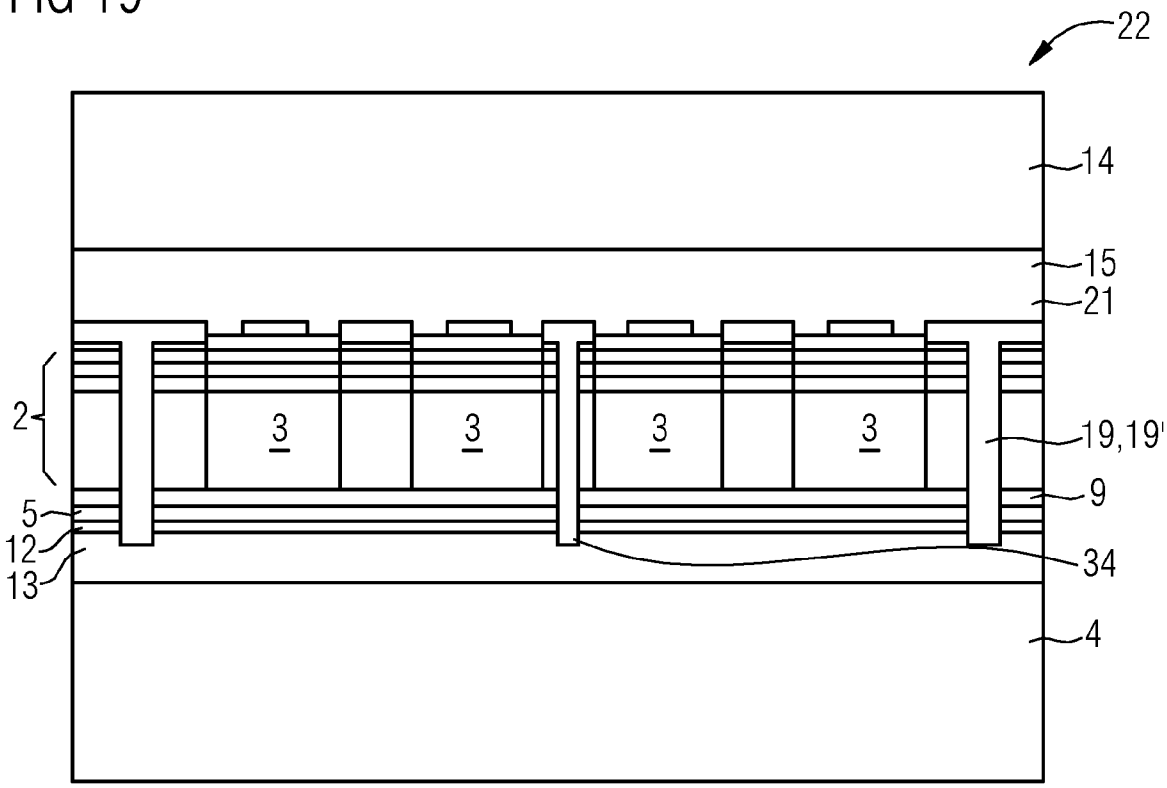
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FIG 20

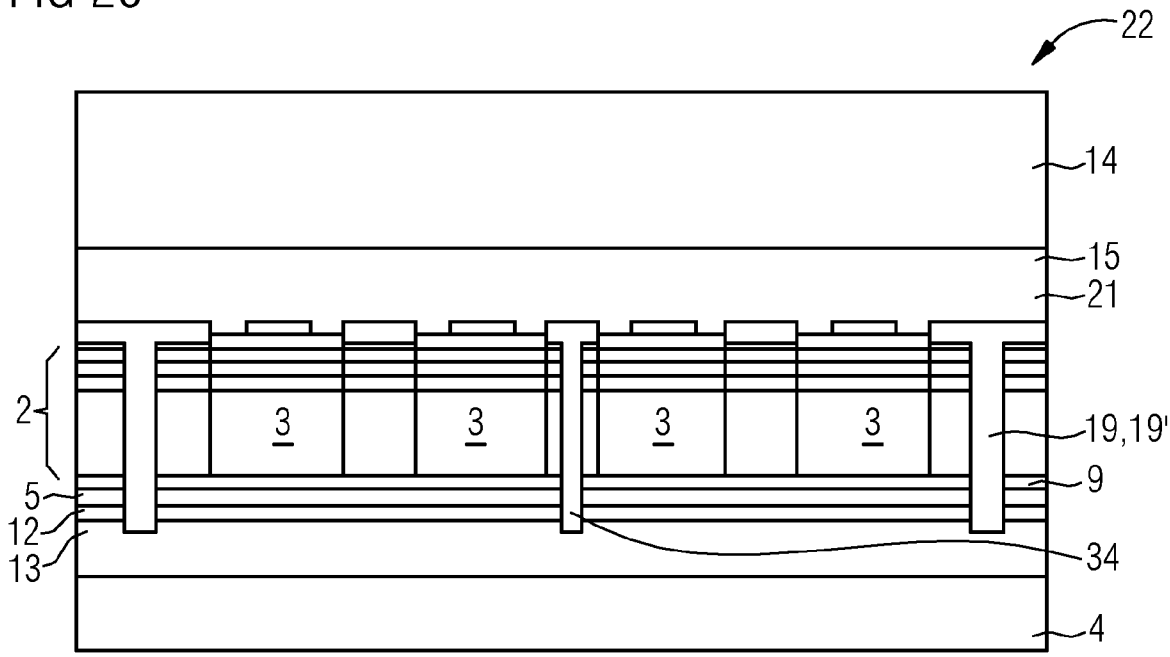
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FIG 21

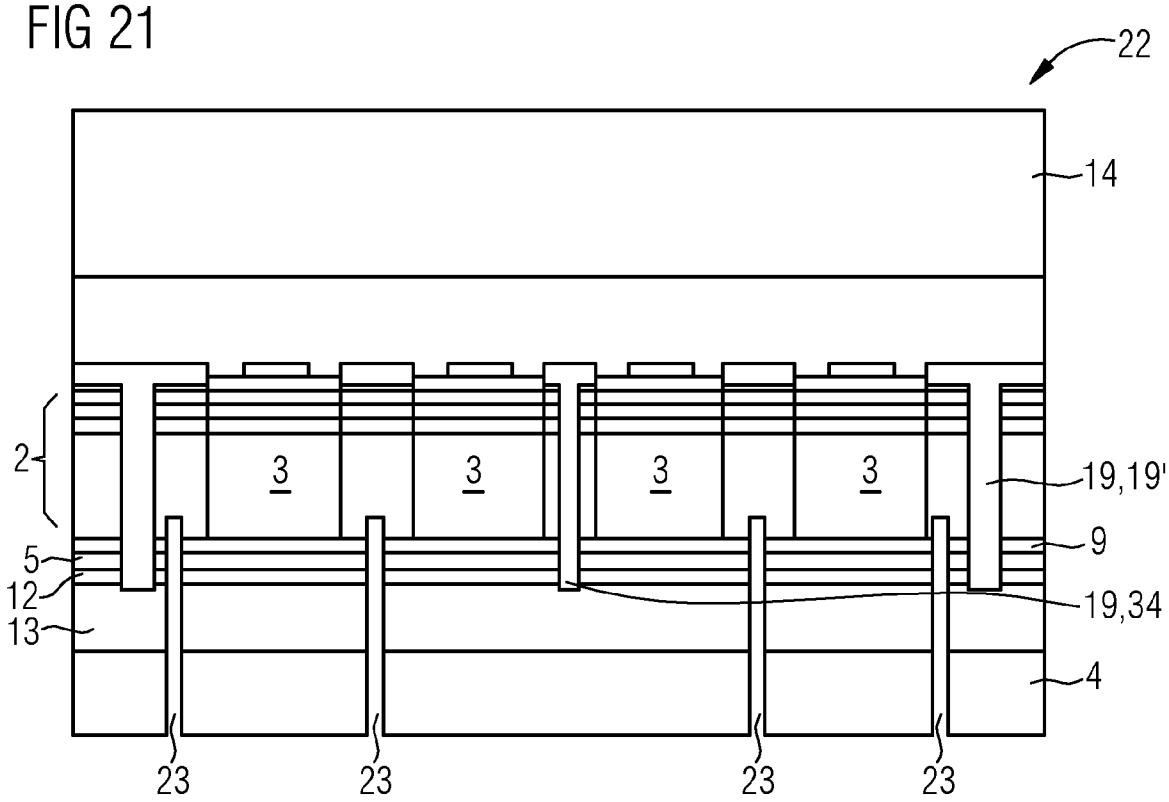
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FIG 22

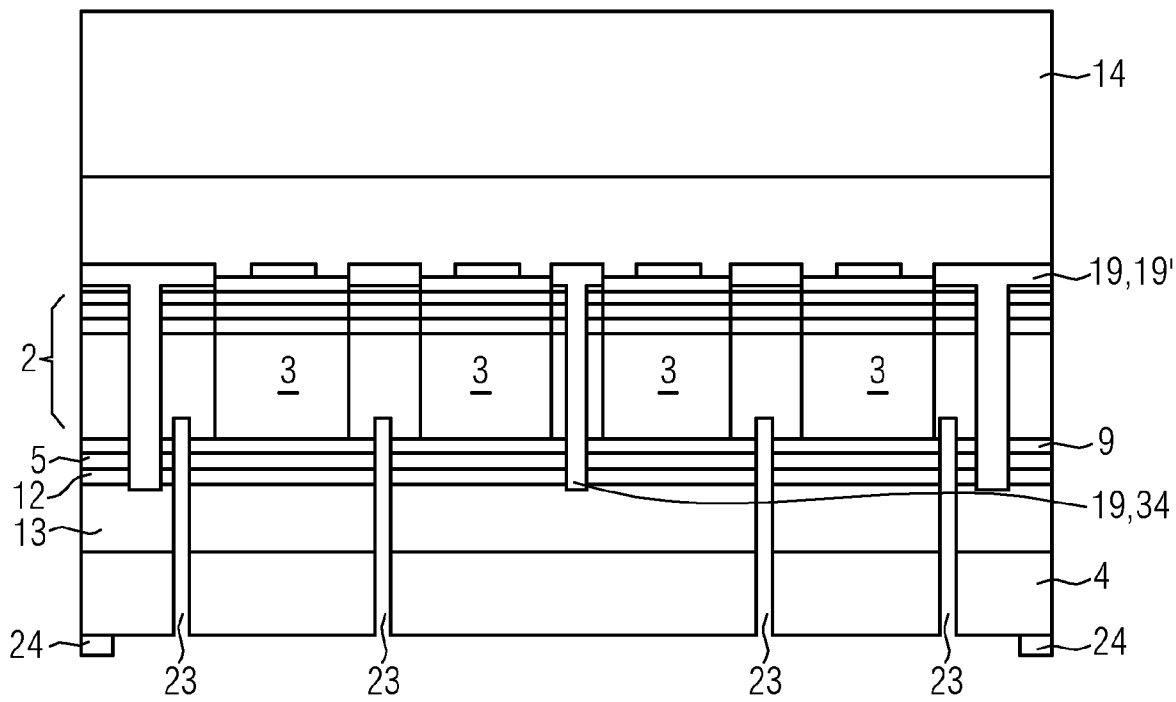
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FIG 23

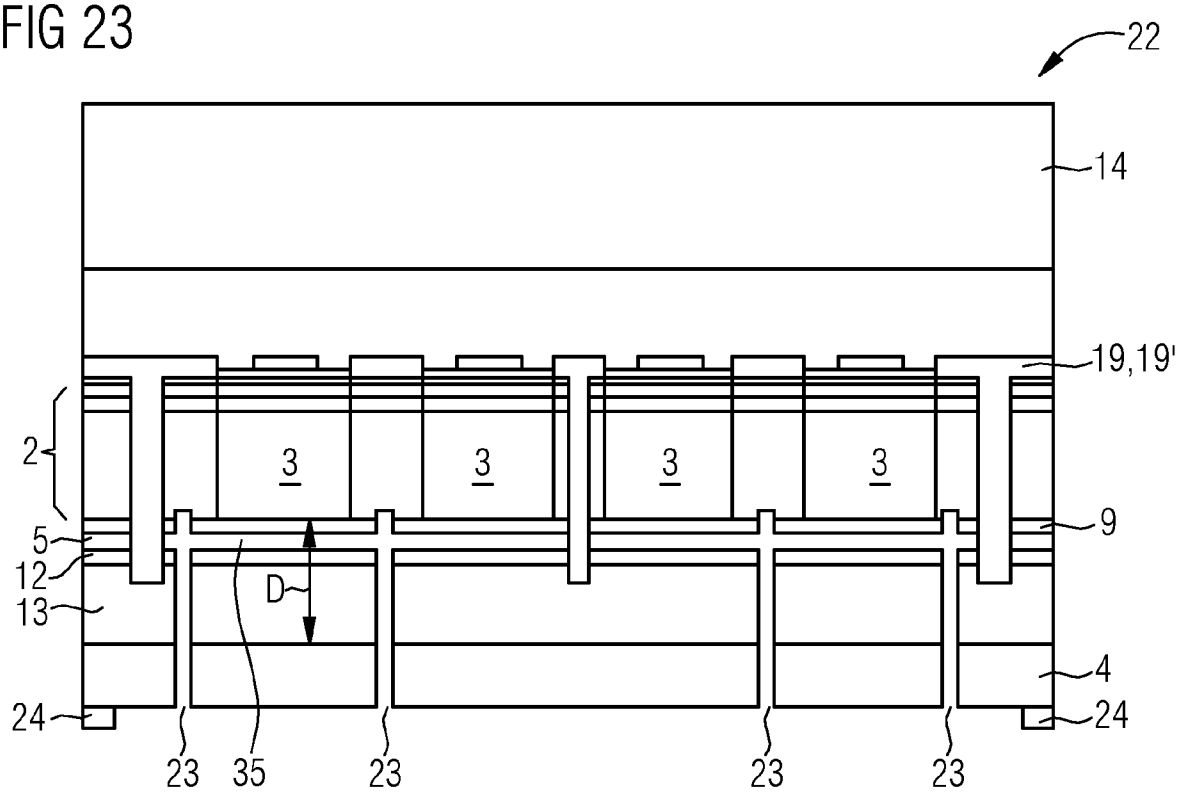
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FIG 24

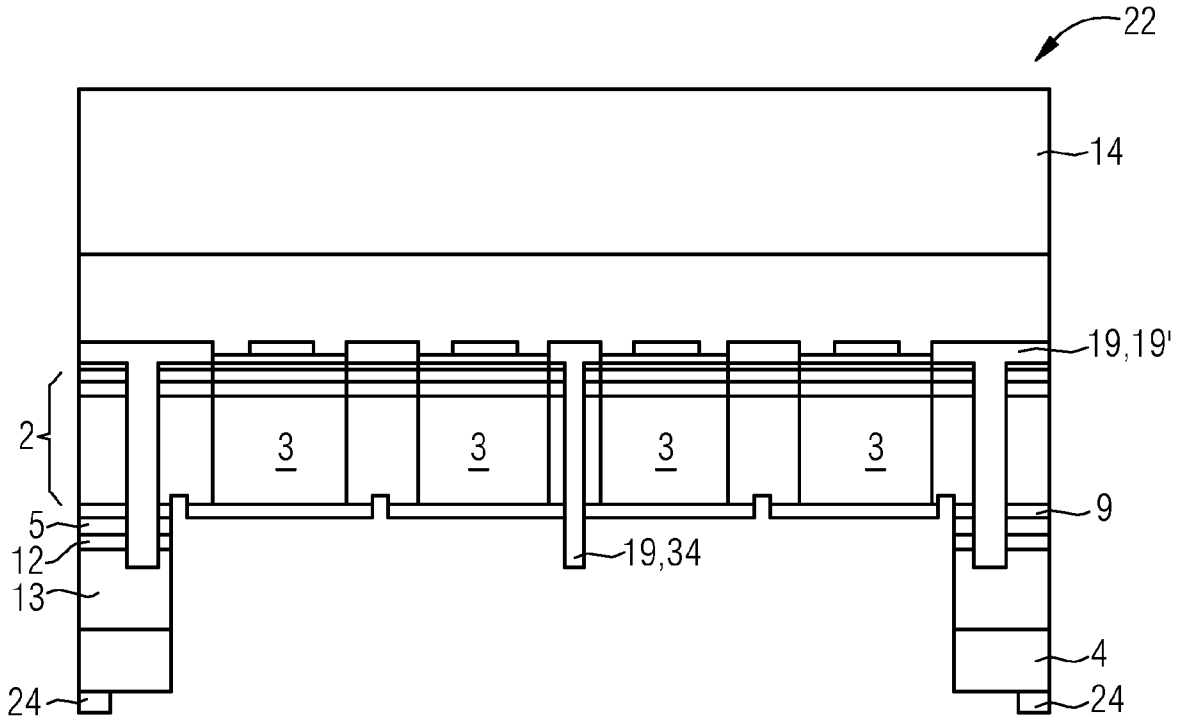
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FIG 25

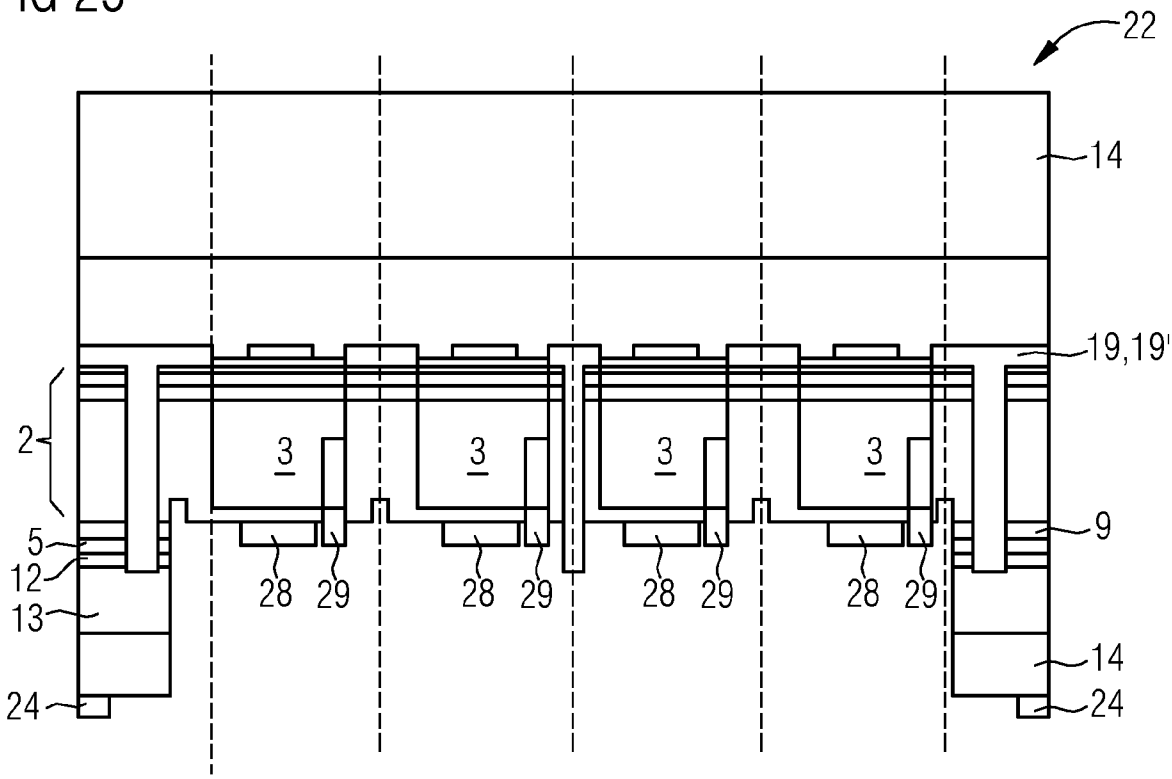
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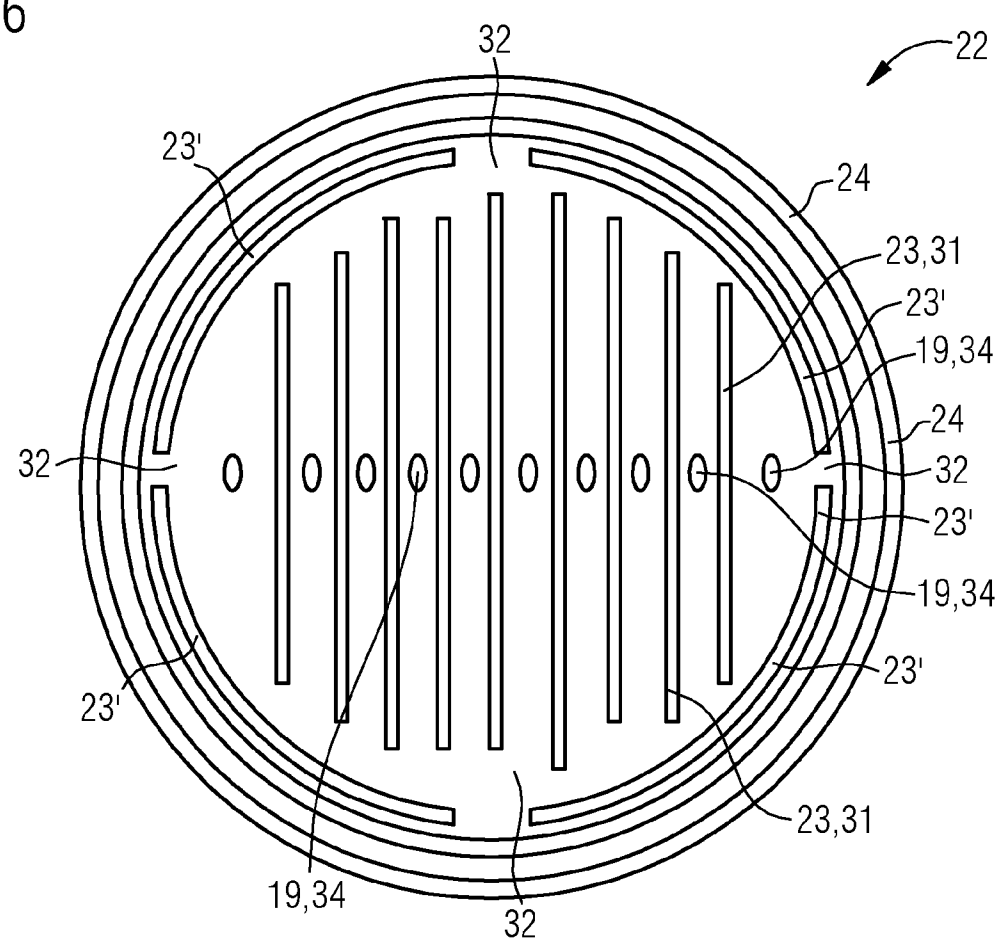
FIG 26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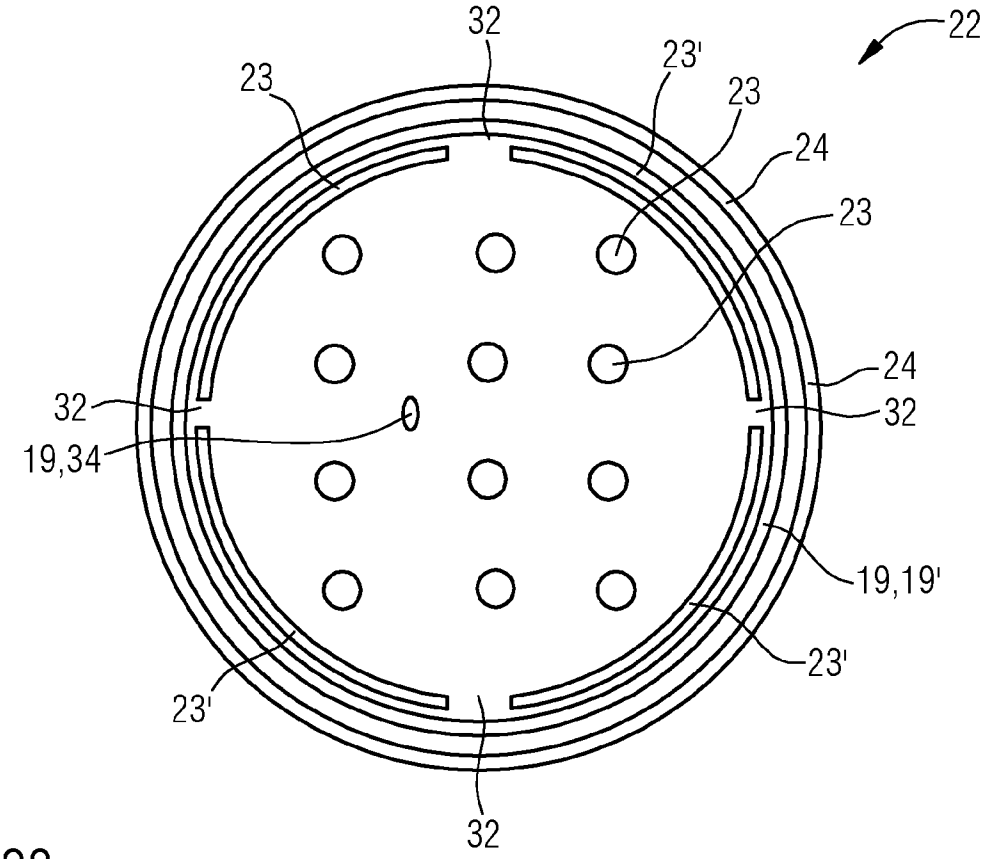
32
23'
19,34
23'
23'
23,31
19,34
32

FIG 27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23'
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23
24
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24
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19,34
19,19'
23'
23'
32

FIG 28

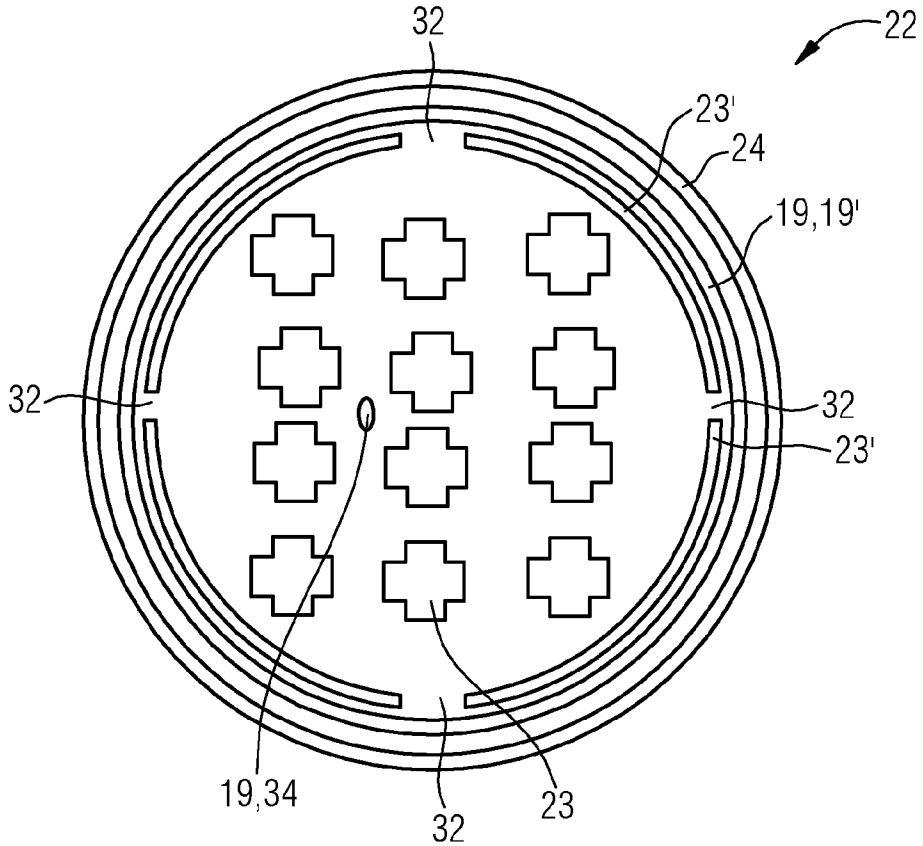
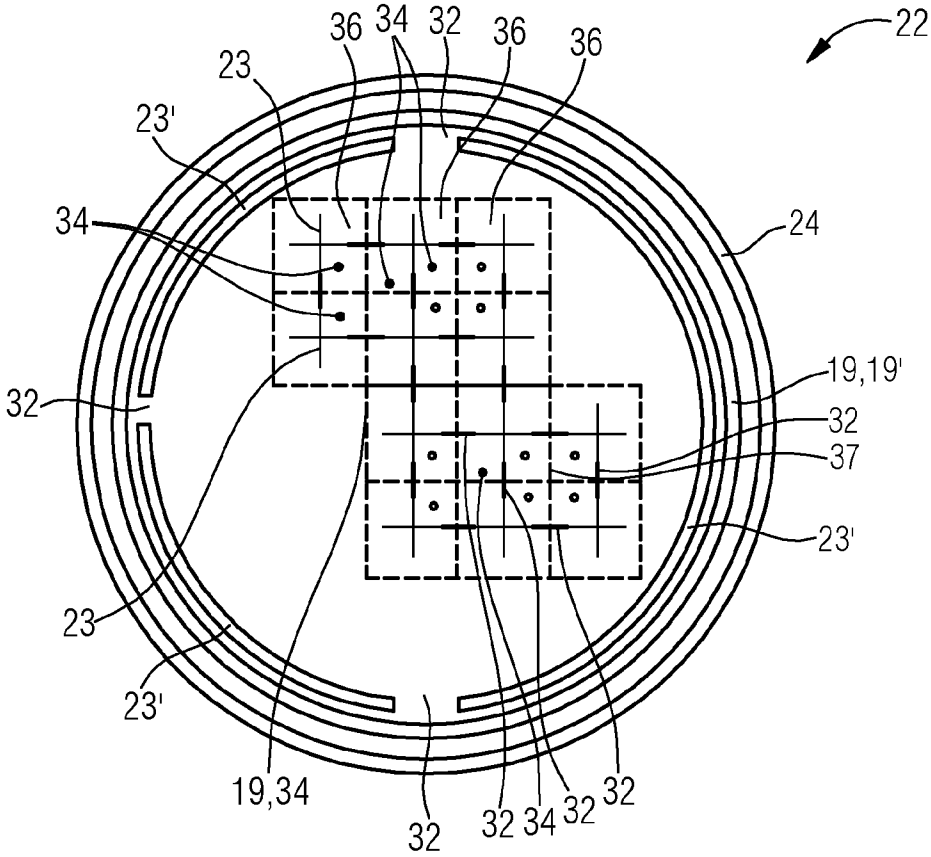

32
22
23'
24
19,19'
32
32
23'
19,34
32
23

FIG 29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36
23
23'
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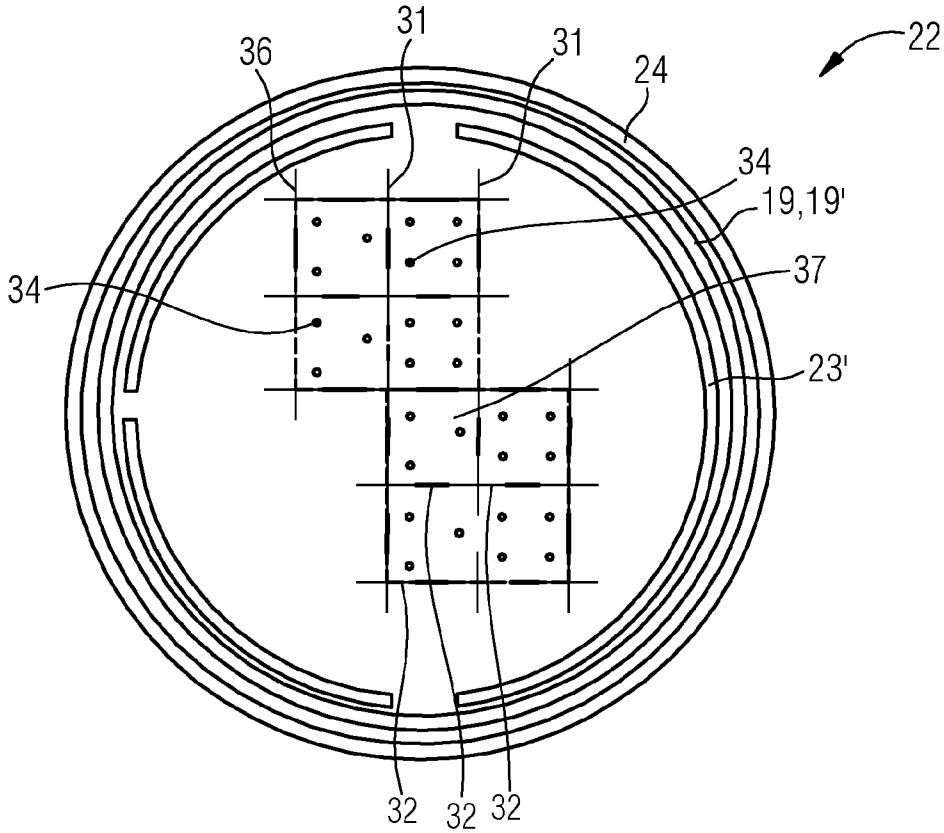
19,19'
32
32
37
23'
23
23'
19,34
32
32
34
32
32

FIG 30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34
19,19'
37
34
23'
32
32
32

FIG 31

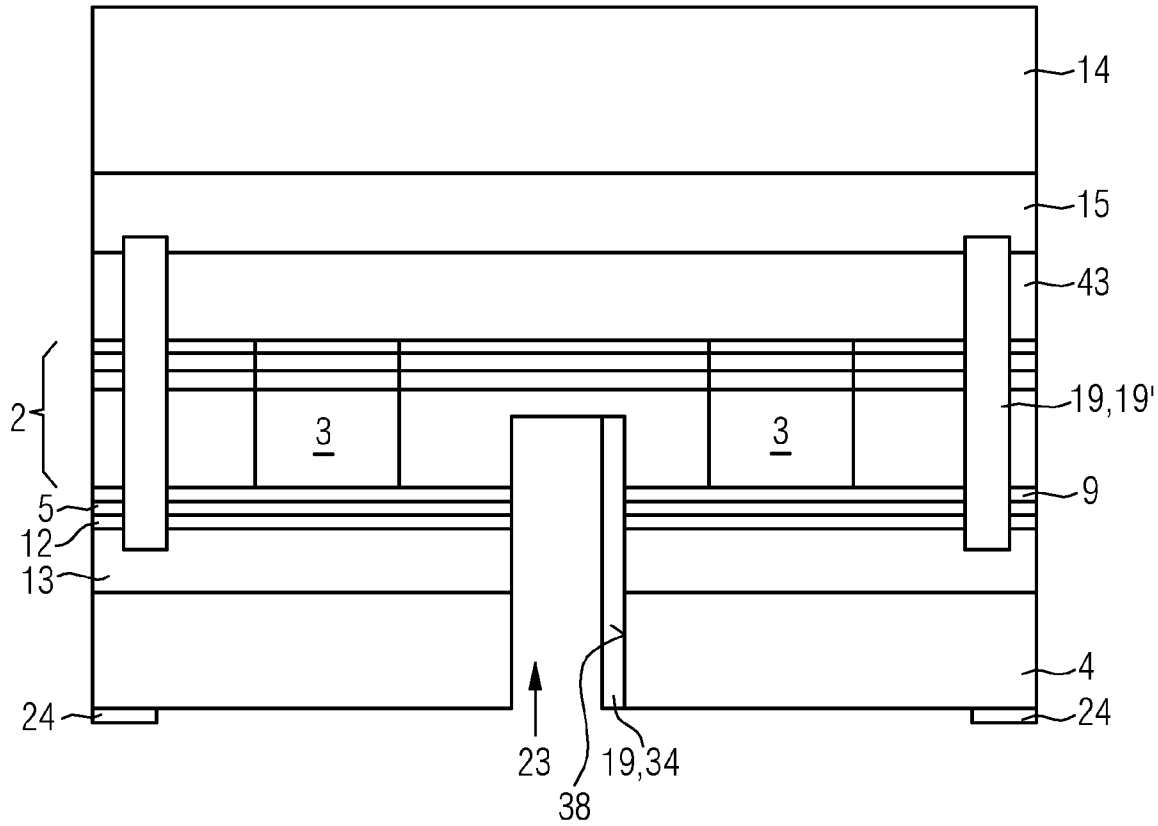
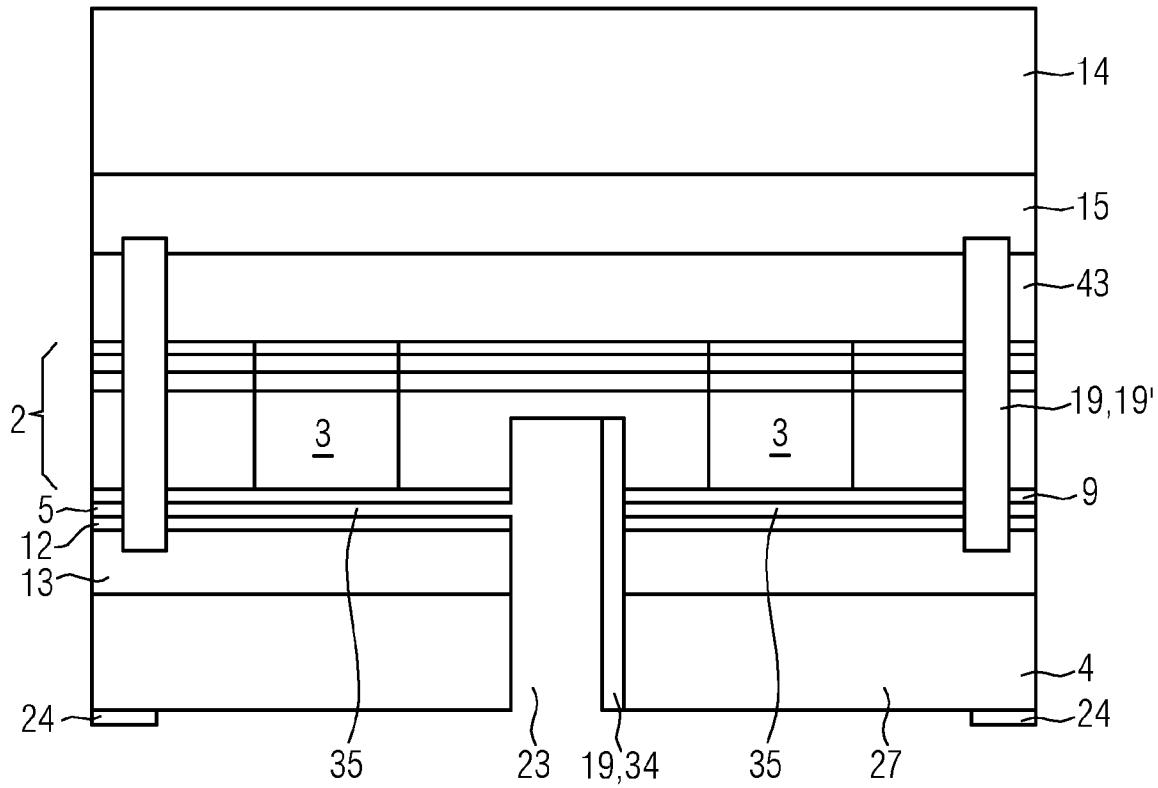

14
15
43
19,19'
9
4
24
2
3
3
5
12
13
24
23
19,34
38

FIG 32


14
15
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19,34
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27

FIG 33

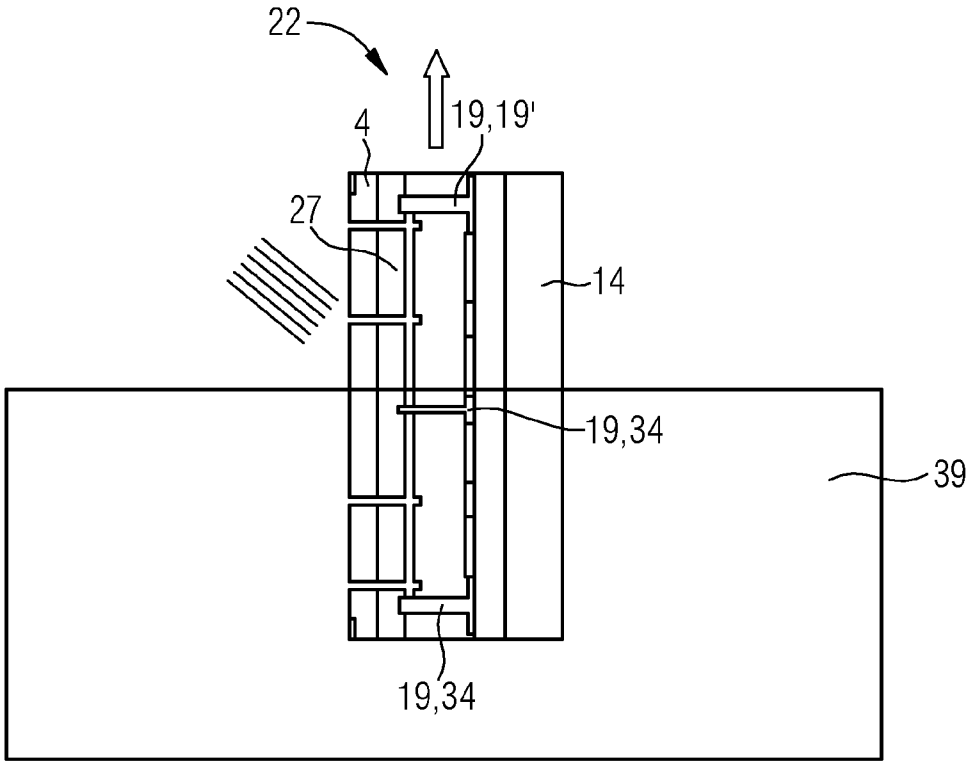


FIG 34

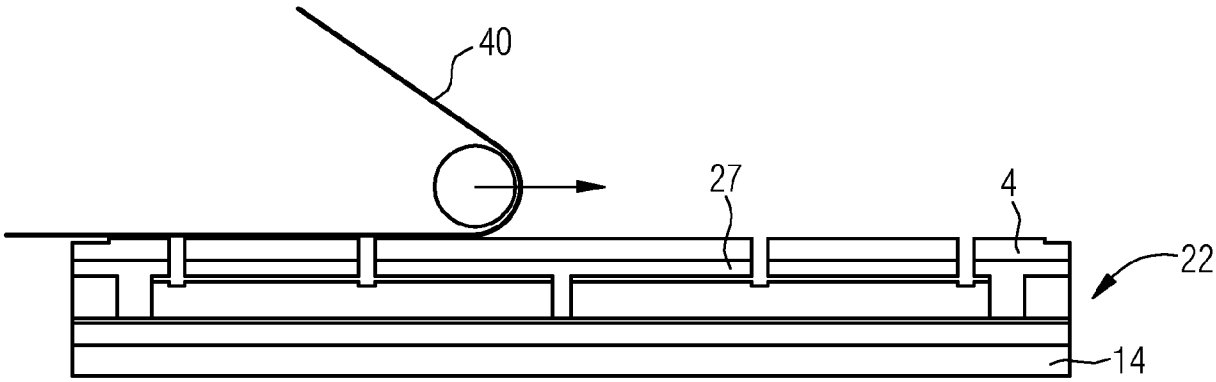
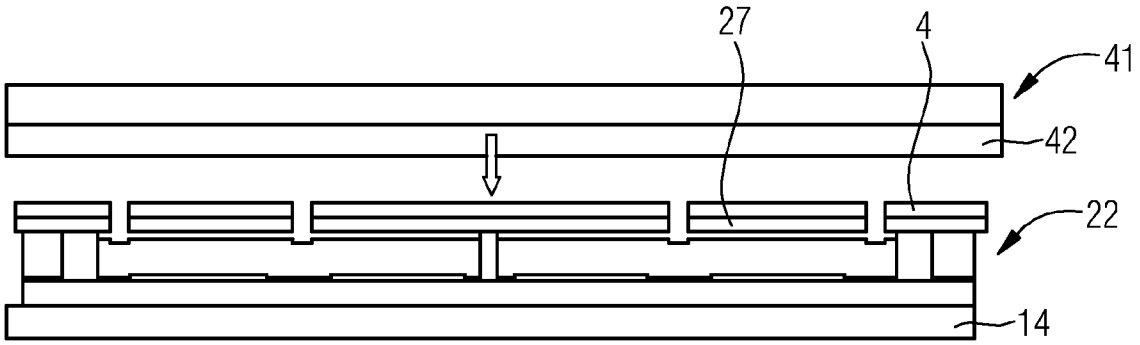


FIG 35



INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2024/057438

A. CLASSIFICATION OF SUBJECT MATTER

INV. H01L21/78
ADD. H01L33/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2022/367750 A1 (YU GUOMIN [US] ET AL) 17 November 2022 (2022-11-17) paragraphs [0008] - [0072]; figure 20	1-17
X	US 2023/036209 A1 (YU GUOMIN [US]) 2 February 2023 (2023-02-02) paragraphs [0008] - [0067]; figures 2-14	1-17
X	US 2017/236807 A1 (HWANG DAVID [US] ET AL) 17 August 2017 (2017-08-17) paragraphs [0016] - [0103]; figures 1-8	1-17
A	US 2020/020840 A1 (SHENG CUICUI [CN] ET AL) 16 January 2020 (2020-01-16) figures 23,24	8

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 June 2024	02/07/2024

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Simeonov, Dobri

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2024/057438

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