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(72) Inventors KLAUS HEUBER
WILFRIED KLEIN
KNUT NAJMANN and
SIEGFRIED K. WIEDMANN

(54) OPERATION OF BIPOLAR TRANSISTOR DATA STORAGE CELLS

(71) We, INTERNATIONAL BUSINESS MACHINES CORPORATION, a Corporation organized and existing under the laws of the State of New York, in the United States of America, of Armonk, New York 10504, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to methods of operating data storage cells comprising a pair of cross-coupled bipolar transistors provided with bipolar load transistors, and to data storage apparatus including such a cell and a circuit arrangement to control its operation.

Methods of and circuit arrangements for powering storage cells whose load elements and cross-coupled transistors consist of bipolar transistors are known. Also known are read/write coupling elements in the form of Schottky diodes. Thus, for example the specification of our co-pending application for United Kingdom Letters Patent No. 6710/76 (Serial No. 1,563,013) describes a method of operating an integrated semiconductor storage of that kind in which the read/write cycles are performed in several phases, characterized in that for selecting a storage cell, a word line is pulsed to a lower level, causing the level of the bit line connected to the conductive transistor of the storage cell to be also pulled down to a lower level, whereas the level of the other bit line is raised slightly, so that the difference between the two bit line levels is sensed in a differential amplifier, that subsequently the storage cell is deselected by raising the potential on the word line as well as by applying a recovery current, so that the inner storage cell nodes are charged until one of the bit lines has reached a predetermined potential, and that finally the bit lines are returned to a common stand-by potential.

The circuit arrangement for controlling the recovery and the restore phase in a read or a write cycle is connected to the bit lines of the storage cells.

According to one aspect of the invention, we provide a method of operating a data storage cell comprising a pair of cross-coupled bipolar transistors provided with bipolar transistor loads, the method including first conducting a read or write operation during which operation the cell current (i.e. the total current entering the cell) is increased from a standby current level and at the end of which operation the cell current is returned to the standby level and subsequently momentarily increasing the cell current to quicken the recovery of the potential of the cell input/output nodes.

Other aspects of the invention are defined in the claims appended hereto.

How the invention can be carried into effect will now be described by way of example, with reference to the accompanying drawings, in which:—

Figure 1 is a circuit diagram of a storage cell comprised of bipolar transistors and having Schottky diodes as coupling elements;

Figure 2A to 2C illustrate the current distribution inside the storage cell of Figure 1;

Figure 3 is a time diagram of the storage cell current with the three voltage levels employed for powering the storage;

Figure 4 is a block diagram of a storage level;

Figure 5 is a typical time diagram relating to the circuit arrangement represented in Figure 4; and

Figure 6 is a detailed time diagram showing the exact times of the phases, the currents on the word lines, on the cell nodes, and on the emitters or collectors of the cell transistors.

A storage cell (Figure 1) includes a pair of cross-coupled NPN transistors T1 and T2, whose emitters are connected to a word line WL. The base of each of transistors T1 and T2 is connected to the collector of the other transistor of the pair. A Schottky diode SD1 and SD2 is arranged between the base and the collector of each of transistors T1 and T2 to prevent them from being driven into saturation. Current sources in the form of PNP load transistors are connected to the collectors of transistors T1 and T2 via input/output nodes A and B, respectively. The emitters of these current sources are connected to a supply line (not shown) which within a storage array is linked to several storage cells of a word line WL. The supply current IC to each of the storage cells is controlled via this line, as will be described in detail below with reference to Figure 4. Schottky diodes SD3 and SD4, are connected between respective ones of a pair of bit lines (B0, B1), and the nodes A and B. Stray capacitances CST occur mainly between nodes A and B, and the substrate which has a potential VS. A fixed reference potential V_{REF} is applied to the bases of the PNP load transistors T3 and T4. The preferred operation of the cell represented in Figure 1 will now be described with reference to Figures 2 and 3. Figure 2A shows the current distribution and the current values in the cross-coupled transistors T1 and T2 in the stand-by state; Figure 2B shows the current distribution and the current values in these transistors during a read or a write operation; and Figure 2C shows the current distribution and the current values in these transistors during the recovery phase. A stand-by current IST (Figure 3) flows, in the stand-by phase (T1) into the cell via the load transistors T3 and T4. It is assumed that the transistor T1 is conductive; in this case both the collector and the base current is IST/2. Thus for each cell the current IST is discharged via word line WL.

The stand-by phase at time T1 is followed by a read cycle comprising times T2 and T3. At time T2 the actual reading operation is carried out by lowering the potential of the word line WL. As shown in Figure 2B, in addition to the stand-by current IST, the read current IR from one or the other of the two bit lines B0, B1 depending on which of the cross-coupled transistors T1 or T2 was conducting, is applied to the cell at time T2. In the present specification the stand-by current level IST is referred to as the first level and the stand-by current level IST plus the read current IR is referred to as the second level. After the information has been read from the storage cell, the bit line current returns to zero, so that the stand-by level IST is again obtained. While the information was read, the voltage on the word line WL was pulled down. Consequently, the cell nodes A and B were charged to a lower potential. At the end of the time T2 the word line WL is again pulsed up and the cell nodes A and B must be recharged. Using only the stand-by current for this purpose would take unduly long.

To reduce this time, the stand-by current IST is raised in the time T3 to a level made up of IST+IPU as depicted in Figure 2C. IPU has a magnitude which is between that of the read current IR and the stand-by current IST. This increased cell current causes the two storage cell nodes A and B to be rapidly charged. During this process, the current is fed to the emitters of the two current sources T3 and T4 serving as load transistors. The circuit controlling this current will be described further on.

As charging of the stray capacitances CST by means of this relatively high current takes only a very short time, the pulse employed can be very short so that it has decayed by the end of time T3. Thus at the end of T3 the storage cell again carries the stand-by current IST, so that the original state is restored.

For the sake of completeness, Figure 3 shows also a write cycle which in principle proceeds in the same manner as the read cycle. For this reason Figure 2B shows the write currents IWR on the bit lines B0 and B1 but no separate circuit diagram. However, it is pointed out that depending upon the storage state of the cell, the current comes either only from bit line B0 or from bit line B1. Changing the contents of a storage cell requires a higher current than that necessary for reading information from it. This is shown clearly in Figure 3 during the time T6. After completion of the write operation, the write current IWR returns to 0 and during the time T7 the current IPU is again superimposed on the stand-by current IST, so that after completion of the write operation, the storage cell nodes A and B can be rapidly charged to a higher potential. At the end of time T7, there is only the stand-by current IST. The subsequent description refers to a control circuit which is used to control the storage cell current in a word organized storage array.

On the right-hand side of Figure 4, the storage cells of a storage array are shown. The emitters of the cross-coupled transistors are connected to respective word lines WL0 to WL63. In addition, each word line is connected to a delay circuit TD and an OR circuit 0 common to all the word lines. The output of OR circuit 0 is linked with a monostable flip-flop MK generating a short pulse TSS. This output pulse TSS is

applied to one input of each of 64 AND circuits &; the other input of each of the AND circuits is connected to the output of a respective one of the delay circuits TD. The output of each AND circuit & is connected to a respective amplifier circuit V, the latter circuit supplying both the stand-by current IST and the current IPU (see Figure 2C). As shown in Figure 4, this current is applied to the emitters of the load transistors T3 and T4 of the storage cells connected to that word line.

The operation of the circuit of Figure 4 will be described in detail below with reference to the timing diagram of Figure 5 which represents a read cycle in the space between the two outer perpendicular lines. For the sake of completeness, it is pointed out that this time diagram could just as well serve to illustrate a write cycle. The first line of the diagram shows the voltage level on the word line WL0 (in the present example it is assumed that the word line WL0 has been selected for reading), line 2 shows the output pulse of the delay circuit TD at (A) in Figure 4, the third line the output pulse TSS of the monostable flip-flop MK in Figure 4, and the fourth line the current waveform on the output of the amplifier circuit V at (C).

After the word line WL0 has been selected, the signal on this word line controls the corresponding delay circuit TD. This delay circuit then generates the signal in accordance with line 2, Figure 5. It is pointed out that the trailing edge of the pulse is delayed by the time TD in relation to the trailing edge of the pulse on the word line WL0.

The delay time TD of the signal (A) is not critical, it must merely be longer than the signal TSS still to be described and must have decayed prior to the completion of the read or the write cycle. The trailing edge of the pulse on line WL0, represented in line 1 of the diagram of Figure 5, controls the monostable flip-flop MK via the OR circuit 0. The monostable flip-flop MK emits a pulse TSS whose duration is accurately defined and which, as described above, is applied to each AND circuit & in the storage array. In the storage array shown in Figure 4 the AND condition exists only for the AND circuit & of the word 0. Thus only this AND circuit supplies an output pulse IPU+IST in the time TPU. In the present case the current IPU+IST applies only to one cell. For n storage cells in a word line WL the circuit actually supplies a current N (IPU+IST) during the time TPU. In this connection it is essential that the time TSS at (B) is shorter than the time TD at (A). This ensures that a pulse of an accurately defined duration is generated in the time TPU at (C). This pulse is applied directly to the load transistors T3 and T4 of the cells on the respective word line WL.

In addition to the voltage on word line WL, Figure 6 shows the voltages on the cell nodes A and B and the currents IPU on the emitter and the collector of the load transistors T3 and T4 of a cell. By means of this diagram the accelerated charging of the cell nodes A and B with the aid of the third storage cell current level is explained in detail for one cell. It is assumed that in the time T1' the cell is either fully or semi-selected; in any case it is assumed that this storage cell is connected to a selected word line WL. Thus during the time T1' (which corresponds to the times T1 and T2 of Figure 3) the voltage of word line WL is at a lower potential. The voltages on the storage cell nodes A and B are also at the lower potential. For a semi-selected storage cell the storage cell current consists of only the stand-by current IST, whereas for a fully selected storage cell the current IST would be supplemented by the current IR or IWR for reading or writing. For simplicity's sake it is assumed that in the present example the storage cell is semi-selected. The period from the beginning of time T2' to the beginning of time T5' in Figure 6 corresponds to the time T3 in Figure 3. During the time T2' the potential on word line WL is pulsed from its lower potential WLD to the stand-by potential WLU. During the time T2' this pulse edge is transferred to the storage cell nodes A and B through the inter-electrode capacitances of transistors T1 and T2, thus causing the potential of both nodes to be raised slightly (as shown at T2' in lines 2 and 3 of the diagram of Figure 6). After this initial rise in potential of the storage cell nodes A and B, they are recharged only by the stand-by current IST during the time T3', since the current IPUC has not yet started to flow from the collectors of the load transistors T3 and T4. However, the current IPU+IST has already started to flow into the emitters of the load transistors T3 and T4, rising to its highest level during the time T4'.

It should be noted that the currents IPUC and IPU+IST are the sum of the currents flowing in the load transistors T3 and T4. During the time T4', the current IPUE flows into the emitters of the load transistors of the storage cell. The pulse in the current IPUE has a shorter duration than the time T4', whereas there flows from the collectors of these load transistors deformed current pulse which reaches its highest level during the time T4', effecting the actual recharging of the cell nodes A and B. The rate of rise of the potentials on storage cell nodes A and B thus is greatest halfway through the time T4'. At the end of time T4' the storage cell nodes A and B have reached their stand-by

potential. The period from the beginning of time T3′ to the middle of time T4′ corresponds to the time T4 in Figure 3. The relatively high current IPU thus caused the potentials on the storage cell nodes A and B to reach their stand-by level very rapidly, so that the write or read cycle obtained is relatively short.

This increased storage cell current is then applied to the selected and also to the semi-selected storage cells in a word line, so that the power dissipation for the whole storage array is very low. For this example it is assumed that the stand-by phase occurs in the time T5′. In this phase only the currents IST flow in the storage cells. It is, of course, also possible to have a new selection phase instead.

WHAT WE CLAIM IS:—

1. A method of operating a data storage cell comprising a pair of cross-coupled bipolar transistors provided with bipolar transistor loads, the method including first conducting a read or write operation during which operation the cell current (i.e. the total current entering the cell) is increased from a stand-by current level and at the end of which operation the cell current is returned to the stand-by level and subsequently momentarily increasing the cell current to quicken the recovery of the potential of the cell input/output nodes.

2. A method as claimed in Claim 1, in which the cell current is momentarily increased to a level less than that to which the cell current is increased during said read or write operation.

3. A method as claimed in Claim 1 or Claim 2, in which the cell current is momentarily increased by increasing the current flow through the load transistors.

4. A method as claimed in any preceding claim, in which the read or write operation comprises first changing the potential of the non-cross-coupled electrodes of the cross-coupled transistors in such a sense that the cell input/output nodes are discharged and then changing the potential of the non-cross-coupled electrodes of the cross-coupled transistors in the opposite sense so that the cell input/output nodes are recharged.

5. A method as claimed in any preceding claims when performed in relation to a storage cell in which the load transistors are of opposite conductivity type to that of the cross-coupled transistors.

6. A method as claimed in Claim 5, in which the cross-coupled transistors are of NPN conductivity type.

7. A method of operating a data storage cell, substantially as described with reference to Figure 1 to 3 of the accompanying drawings.

8. Data storage apparatus comprising a data storage cell comprising a pair of cross-coupled bipolar transistors of one conductivity type and provided with bipolar load transistors of the opposite conductivity type and a circuit arrangement to enable the storage cell to be operated by a method as claimed in Claim 3, the circuit arrangement including a timing circuit to generate a timing pulse in response to a pulse applied to its input, a delay circuit, means to apply an energising pulse to the inputs of both the delay circuit and the timing circuit, an AND circuit having one input connected to the output of the delay circuit and its other input connected to receive such a timing pulse generated by the timing circuit, and an amplifier having its input coupled to the output of the AND circuit and its output coupled to the load transistors of the storage cell.

9. Data storage apparatus as claimed in Claim 8, in which the timing circuit comprises a monostable flip-flop circuit which produces such a timing pulse in response to the trailing edge of each pulse applied to the input of the timing circuit.

10. Data storage apparatus substantially as described with reference to Figure 4 and operable as described with reference to Figures 5 and 6.

F. J. HOBBS,
Chartered Patent Agent,
Agent for the Applicants.

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FIG. 1

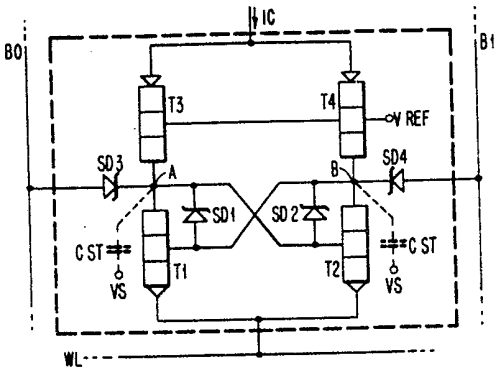

FIG. 2A

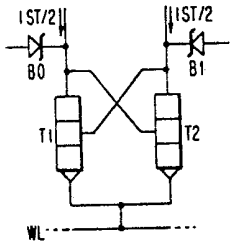

FIG. 2B

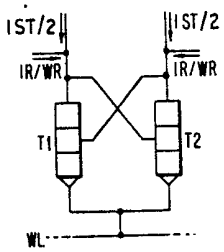

FIG. 2C

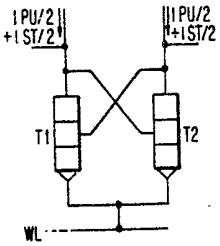

FIG. 3

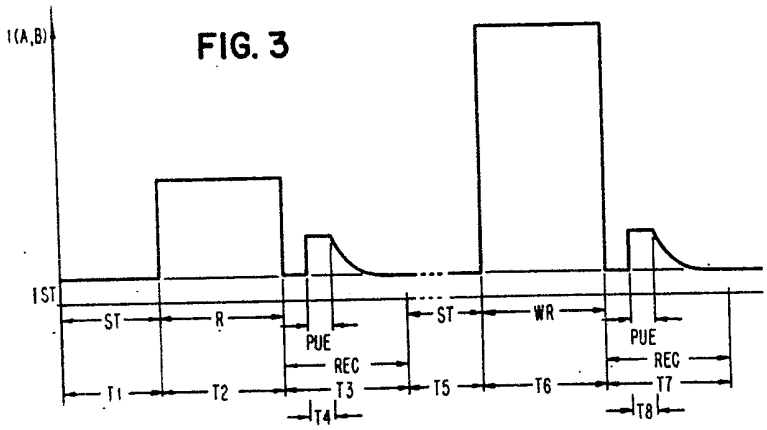

FIG.4

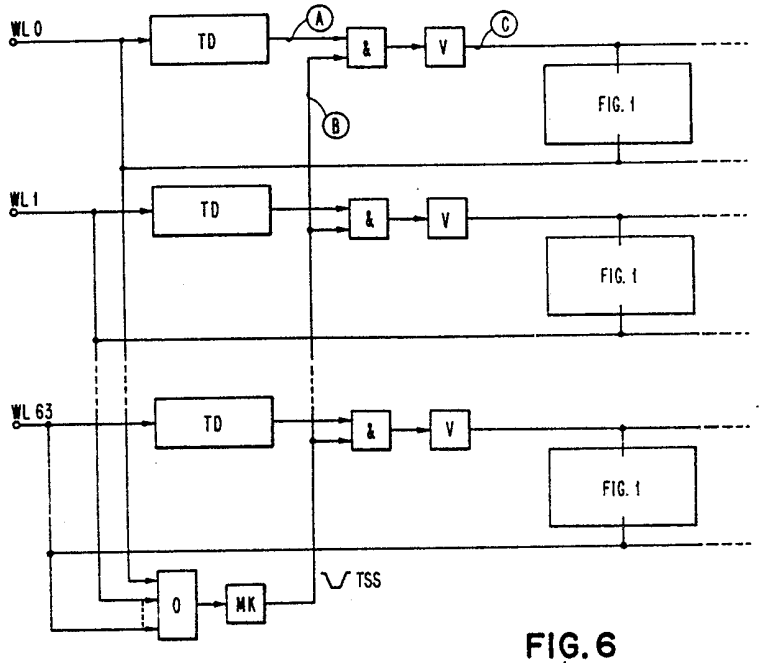

FIG.5

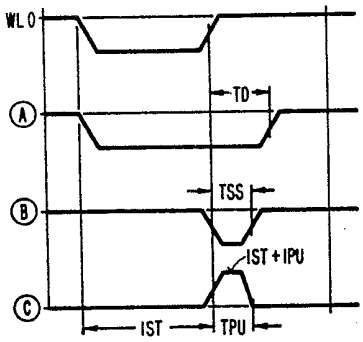

FIG.6