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H3T 2B2 2F1 2T3F 3P 4S 5E HF

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(54) TRUE/COMPLEMENT DRIVER

(71) We, INTERNATIONAL BUSINESS MACHINES CORPORATION, a Corporation organized, and existing under the laws of the State of New York in the United States of America, of Armonk, New York 10504, United States of America do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The invention disclosed relates to FET circuitry and is more particularly concerned with improved true/complement generator circuits. Such circuits generate two output signals corresponding to the true and complementary values of a binary valued input signal applied to an input node of the circuit.

Binary true/complement signal generation circuits are used to drive decoder circuits such as are required to decode the address signals for an array of storage elements. In the state-of-the-art semiconductor memory arrays, the overall storage cycle time is limited by the speed of the signal buffering circuits for address decoders, which must drive the large capacitive loads represented by the large plurality NOR decoder gates.

The invention povides a circuit for generating two output signals at two output nodes corresponding to the true and complementary values of a binary valued input signal applied to an input node, said circuit comprising a first input FET having its gate connected to the input node, its source connected to a first reference potential terminal and its drain connected to a control node; a first output circuit comprising a first isolation FET having its gate connected to a second reference potential terminal and having its source/drain current path connected between the control node and the gate of a first bootstrapped FET, a first bootstrap capacitor connected between the gate and drain of the first bootstrapped FET, a first charging FET having its drain/source current path connected between the second reference potential terminal and the gate of the first bootstrapped FET so that the first isolation FET cuts off when the voltage across the bootstrap capacitor approaches the second reference potential; a second output circuit comprising a second input FET having its source connected to the first reference potential terminal and having its gate. connected to the control node to receive a complementary input signal which places the second input FET in the opposite conducting/non-conducting state to the first input FET, a second isolation FET having its gate connected to the control node and having its source/drain current path connected between the drain of the second input FET and the gate of a second bootstrapped FET, a second bootstrap capacitor connected between the gate and drain of the second bootstrapped FET, a second charging FET having its drain/source current path connected between a terminal at the second reference potential and the gate of the second bootstrapped FET so that the second isolation FET cuts off when the voltage across the second bootstrap capacitor approaches the second reference potential; means for applying during first intervals, gating signals to the first and second charging FETs to charge or tend to charge the bootstrap capacitors to the second potential; and means for applying during second intervals non-overlapping the first intervals, gating signals to the drains of the first and second boot-strapped FETs whereby one or the other of the first and second bootstrapped FETs is rendered conducting depending on the value of the input signal applied at the input node.

The invention will now be more particularly described with reference to the accompanying drawings, in which:—

Figure 1 is a circuit diagram of an example of a true/complement generator embodying the invention.

Figure 2 is a waveform diagram for the circuit of Figure 1.

Figure 3 is another waveform diagram for the circuit of Figure 1.

Figure 4 is a waveform diagram for a prior art true/complement circuit.

Discussion of the Preferred Embodiment

The prior art, low power ratioless true/complement buffer as represented by the publication by Gladstein, et al., "Low-Power Ratioless True-Complement Buffer", IBM Technical Disclosure Bulletin, Vol. 18, #8, January 1976, pp. 2591—92, is improved upon by connecting a first isolation FET (T2) so that its gate is connected to drain potential (V_{DD}) and by connecting to the second isolation FET (T4) so that its gate is connected to the phase-splitting node (1). This enables the number of clock pulse sources necessary to operate the generator circuit to be reduced by one so that the speed of the generator circuit is increased, by virtue of the second isolation FET (T4) having a gate size substantially smaller than the gate size of the inverting FET (T3) so that it will more rapidly switch from its on-state to its off-state than does the inverting FET.

The low power true/complement driver circuit shown in Figure 1, generates a true and complement pulse. The timing diagram for its operation is shown in Figure 2. In the unselected mode T_R (memory select at up-level), node 6 and 7 will be at ground and nodes 2 and 4 are at the up level. In the selected mode (Tsel), memory select is set to ground and CL1 clock is set to a positive up-level. An address pulse applied to the gate of device T1 will set node 1 to ground and disable device T3 and T4. Node 4 will discharge to ground and device T6 and T9 will be off for the remainder of the cycle. However, node 2 will rise to a higher potential than V_{DD} because of the variable bootstrap capacitor C1. Device T8 will conduct and node 3 will rise to the full CL1 clock voltage. Device T12 will conduct and set node 6 at V_{DD}-V_t. Thus, an address at the up-level (logical "1") applied to gate of device T1 generates a true at node 6 and complement and node 7. Converse of this is also true.

The longest delay path in data propagation from the input to the output is through nodes 1, 2, 3 and 6. Connecting gate of device T4 to node 1 minimizes this delay data propagation. The true and complement outputs are capable of driving higher capacitive loads because of the circuits push-pull action. Also, the true and complement outputs are isolated from the input, clock CL1 and memory select. Address transfer is clocked by CL1 signal for a short time interval and noise immunity is provided to the input for the remainder of the cycle.

Figure 3 illustrates that the true/complement generator invention achieves a 46 nanoseconds switching delay under the same conditions that the above cited prior art Gladstein, et al circuit achieves in the longer switching delay of 66 nanoseconds, as shown in Figure 4.

An additional advantage which accrues to the circuit shown in Figure 1 is that the circuit is capable of driving high capacitive loads without capacitively loading the clock CL1 or the address input line A. This is accomplished by the isolation function performed by the transistors T9 and T12 whose drains are connected to the DC potential V_{DD} and whose gates are respectively connected to the source of T6 and T8. By connecting the transistors T9 and T12 in this manner, the full driving potential of the V_{DD} power supply minus the threshold voltages of T9 and T12, is applied to the outputs at nodes 6 and 7.

Transistors T10, T11, T13 and T14 are connected as a bistable latching circuit to latch-up the signals output on nodes 6 and 7. One of the principal advantages of the circuit shown in Figure 1 is that the signal output at the source of transistors T9 and T12 become immediately available at the nodes 6 and 7 for use in subsequent circuits and yet a latching function is accomplished at nodes 6 and 7 by connecting the gate of transistor T10 to node 6 and the gate of transistor T13 to node 7 so that the relative polarity of the signals output on these nodes can be stored for as long as the null transistors T11 and T14 remain off. When the MS signal goes on, transistors T11 and T14 connect the nodes 7 and 6, respectively to ground potential thereby nulling the signal states on these nodes, effectively resetting the output latch for the next cycle.

WHAT WE CLAIM IS:—

1. A circuit for generating two output signals at two output nodes corresponding to the true and complementary values of a binary valued input signal applied to an input node, said circuit comprising a first input FET having its gate connected to the input node, its source connected to a first reference potential terminal and its drain connected to a control node; a first output circuit comprising a first isolation FET having its gate connected to a second reference potential terminal and having its source/drain current path connected between the control node and the gate of a first bootstrapped FET, a first bootstrap

capacitor connected between the gate and drain of the first bootstrapped FET, a first charging FET having its drain/source current path connected between the second reference potential terminal and the gate of the first bootstrapped FET so that the first isolation FET cuts off when the voltage across the bootstrap capacitor approaches the second reference potential; a second output circuit comprising a second input FET having its source connected to the first reference potential terminal and having its gate connected to the control node to receive a complementary input signal which places the second input FET in the opposite conducting/non-conducting state to the first input FET, a second isolation FET having its gate connected to the control node and having its source/drain current path connected between the drain of the second input FET and the gate of a second bootstrapped FET, a second bootstrap capacitor connected between the gate and drain of the second bootstrapped FET, a second charging FET having its drain/source current path connected between a terminal at the second reference potential and the gate of the second bootstrapped FET so that the second isolation FET cuts off when the voltage across the second bootstrap capacitor approaches the second reference potential; means for applying, during first intervals, gating signals to the first and second charging FETs to charge or tend to charge the bootstrap capacitors to the second potential; and means for applying during second intervals non-overlapping the first intervals, gating signals to the drains of the first and second bootstrapped FETs whereby one or the other of the first and second bootstrapped FETs is rendered conducting depending on the value of the input signal applied at the input node.

2. A circuit as claimed in claim 1, in which the first output circuit further comprises a first output FET having its gate connected to the source of the first bootstrapped FET and its source/drain current path connected between a first output reference voltage terminal and one of the output nodes and in which the second output circuit further comprises a second output FET having its gate connected to the source of the second bootstrapped FET and its source/drain current path connected between a terminal at the first output reference voltage and the other of the output node.

3. A circuit as claimed in claim 2, in which the first output circuit further comprises a third output FET having its base connected to the other output node and its source/drain current path connected between a terminal at a second output reference voltage and said one output node and in which the second output circuit further comprises a fourth output FET having its base connected to said one output node and its source/drain current path connected between a terminal at the second output reference voltage and said other output node.

4. A circuit as claimed in claim 3, in which the first output circuit further comprises a fifth output FET having its source/drain current path connected between a terminal at the second output reference voltage and said one output node and in which the second output circuit further comprises a sixth FET having its source/drain current path connected between a terminal at the second output reference voltage and said other output node, said fifth and sixth output FETs having their bases connected to receive the same gating signals as the first and second charging FETs.

5. A circuit as claimed in any one of claims 1 to 4, in which the gate size of the second isolation FET is substantially smaller than the gate size of the complementing FET so that the isolation FET switches from its on-state to its off-state more rapidly than the complementing FET.

6. A true/complement driver substantially as hereinbefore described with reference to and as shown in Figures 1, 2 and 4 of the accompanying drawings.

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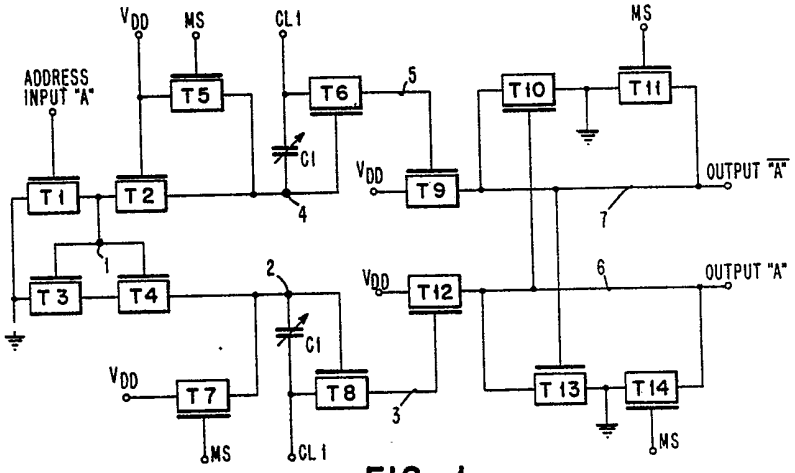
V_{DD}
MS
CL 1
ADDRESS INPUT "A"
T5
T6
5
T10
T11
MS
C1
V_{DD}
T9
OUTPUT "A"
T1
T2
4
7
1
2
V_{DD}
T12
6
OUTPUT "A"
T3
T4
C1
V_{DD}
T7
T8
3
T13
T14
MS
MS
CL 1

FIG. 1

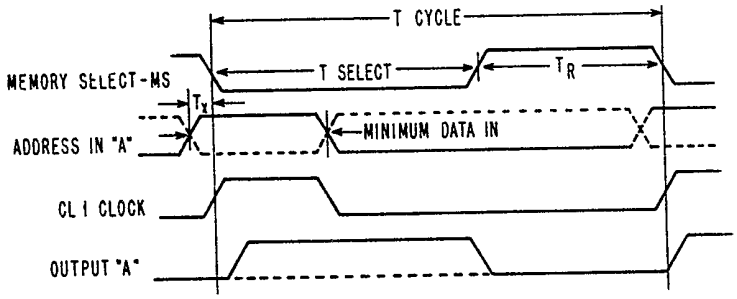
T CYCLE
T SELECT
T_R
MEMORY SELECT-MS
T_A
ADDRESS IN "A"
MINIMUM DATA IN
CL 1 CLOCK
OUTPUT "A"

FIG. 2

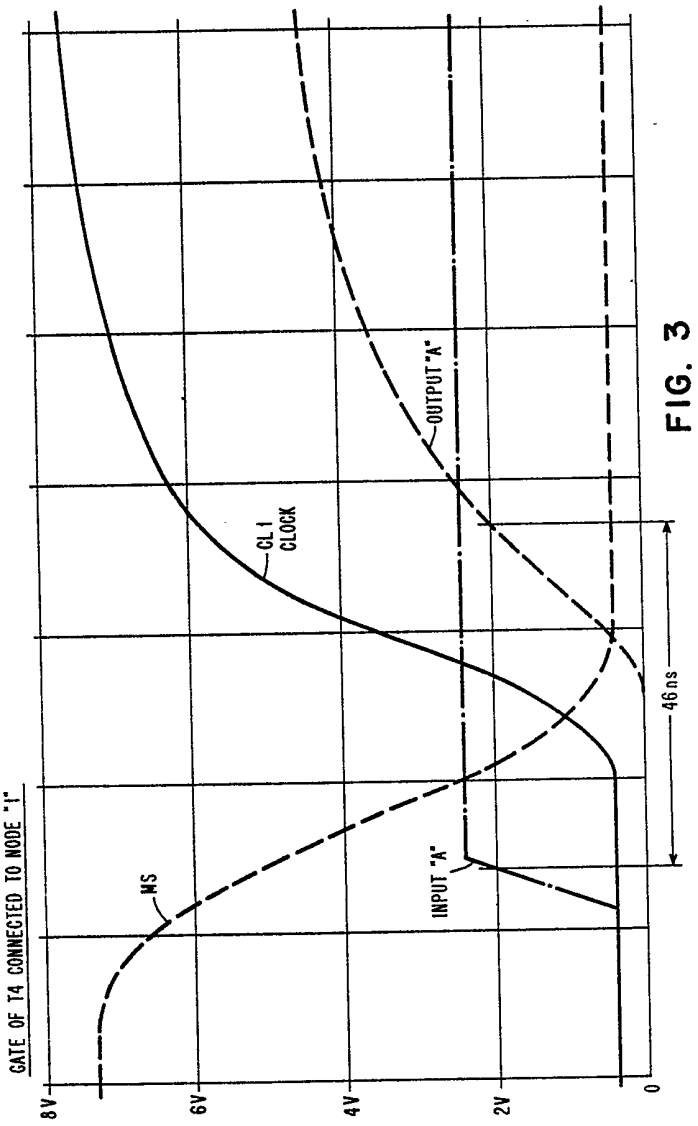
GATE OF T4 CONNECTED TO NODE "1"
8V
6V
4V
2V
0
MS
CL 1 CLOCK
OUTPUT "A"
INPUT "A"
46 ns

FIG. 3

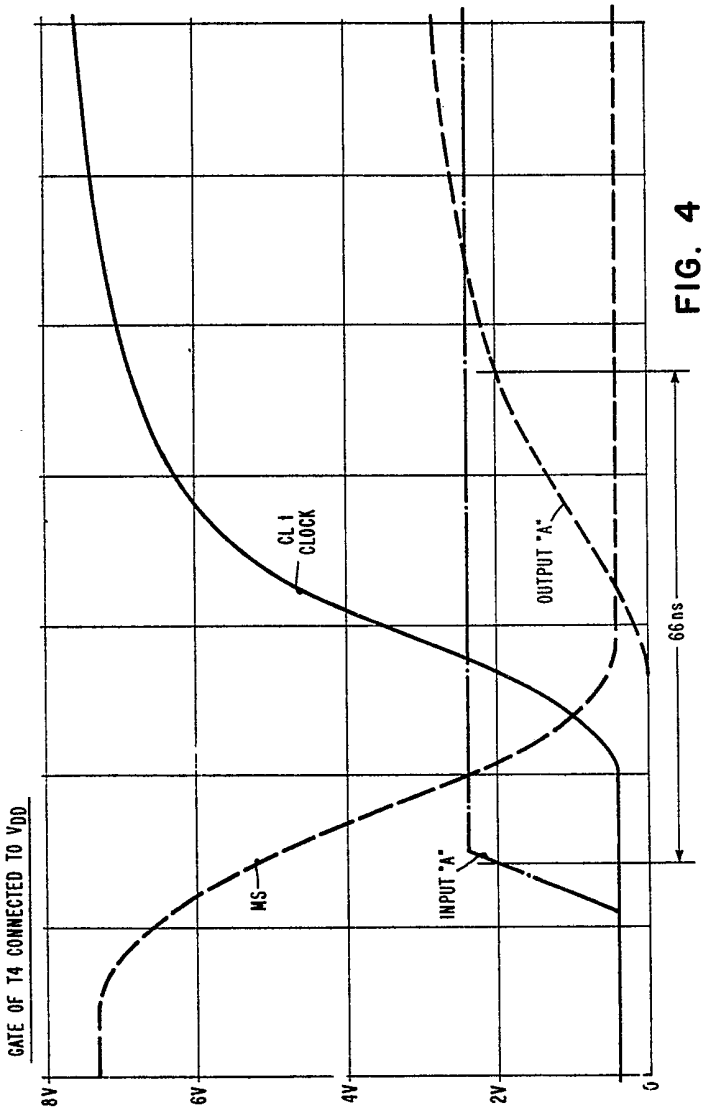
GATE OF T4 CONNECTED TO V_{DD}
8V
6V
4V
2V
0
CL 1 CLOCK
MS
INPUT "A"
OUTPUT "A"
66ns

FIG. 4