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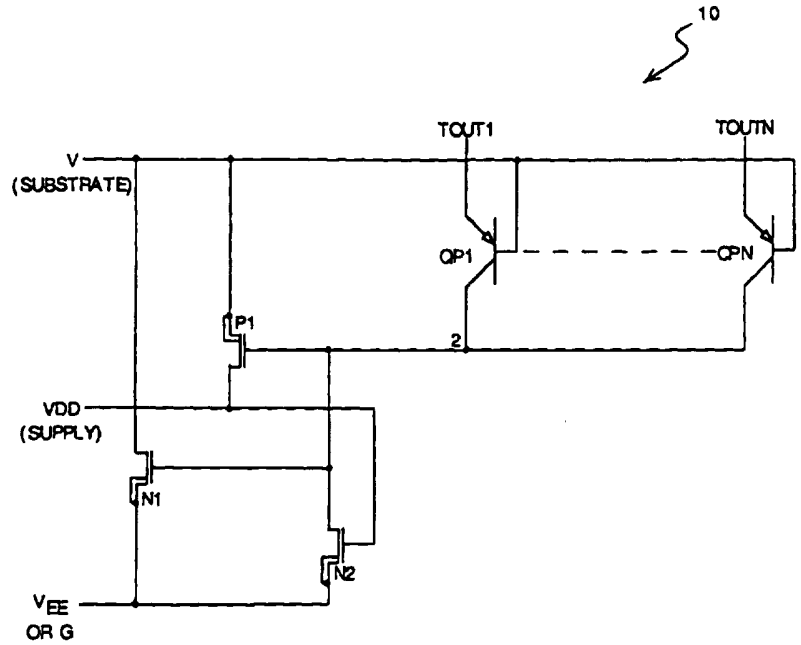

(57) Abstract

A substrate clamp (10) for non-isolated integrated circuits that controls the voltage on a substrate (V) so that the substrate is connected to a specific node (VDD) if the parasitic PN diodes at all the circuit nodes (TOUT1-TOUTN) are not forward biased. If a specific node (TOUT1-TOUTN) is then forced with an applied voltage to forward bias, the substrate is disconnected from its original node (V) and maintains itself at a forward biased diode voltage drop away from the powered node (TOUT1-TOUTN). When the node (TOUT1-TOUTN) returns to no longer being forward biased, the substrate (V) is reconnected to the original power supply node (VDD).

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SUBSTRATE CLAMP FOR NON-ISOLATED INTEGRATED CIRCUITS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to the field of monolithic integrated circuits and more particularly, to an apparatus and method of clamping the voltage of a local or global substrate in non-isolated integrated circuits.

2. Related Art

Each component on monolithic integrated circuits is generally isolated from the substrate through an inherent PN diode. If the applied voltage between the component and the substrate is such that it reverse biases this PN diode, the component is considered to be isolated. On the other hand, if the applied voltage is such that it substantially forward biases this PN diode, isolation does not occur. Without such isolation, one or more of the inherent PN junctions associated with devices that make up a variety of circuits including operational amplifier output stages and line drivers which would become forward biased. At a minimum, this would cause excessive current to flow into the substrate and in an extreme case, it would cause functional failure.

Substrate steering circuits are widely used on commercial monolithic integrated circuits to circumvent this problem. Conventional steering circuits, however, all use comparators that compare the various voltages on circuit nodes and then connect the

substrate to the most appropriate node. The selected node is generally one with a voltage which does not allow forward biasing of the substrate with any of the components on the circuit.

These conventional substrate steering or snatching circuits are often complex, difficult to implement and provide poor transient responses. Use of these conventional substrate circuits are thus generally avoided with the use of more complex semiconductor processes to provide isolated pockets each containing portions of the circuitry. However, these circuits are complicated and involve increased chip area and cost.

Accordingly, there is a need in the technology for a substrate snatching circuit that is simple and which may be implemented without complex semiconductor processing or requiring a significant increase in chip area.

BRIEF SUMMARY OF THE INVENTION

A substrate clamp for non-isolated integrated circuits is disclosed. The substrate clamp comprises a circuit that controls the voltage on a substrate so that the substrate is connected to a specific node if the parasitic PN diodes at all the circuit nodes are not forward biased. If a specific node is then forced with an applied voltage to forward bias, the substrate is disconnected from its original node and maintains itself at a forward biased diode voltage drop away from the powered node. Various embodiments are disclosed.

In one embodiment of the invention, a set of bipolar transistors which utilize the substrate as a common base, is implemented. The emitters of these transistors are connected to a set of nodes which may be driven to voltages outside the range between that provided by the power supply and ground, or any other pair of applied voltages. The collectors of these bipolar transistors are connected together. When any or all of the bipolar transistors are turned on, the substrate is disconnected from the power supply terminal and is forced to a V_{BE} or

diode drop away from the emitter of the turned-on transistor. When the node returns to a voltage within the range of the power supply, the substrate is reconnected to the original power supply node.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic diagram of a substrate snatcher circuit in accordance with one embodiment of the present invention.

Figure 2 is a schematic diagram of a substrate snatcher circuit in accordance with a second embodiment of the present invention.

Figure 3 is a schematic diagram of a substrate snatcher circuit in accordance with a third embodiment of the present invention.

Figure 4 is a schematic diagram of a substrate snatcher circuit in accordance with a fourth embodiment of the present invention.

Figure 5A is an elevational cross sectional view of one embodiment of a double PNP transistor which may be implemented in the substrate snatcher circuit of Figures 3 and 4.

Figure 5B is a schematic representation of the double PNP transistor of Figure 5A.

Figure 5C is a schematic representation of the double PNP transistor of Figure 5B implemented through the use of two transistors.

DETAILED DESCRIPTION OF THE INVENTION

The present invention provides an apparatus and method for clamping the voltage of a local or global substrate, so that, irrespective of the voltages applied to the various components on the substrate, PN junctions formed between regions of devices and the substrate will not become substantially forward biased by the parasitic diodes associated with these components and the substrate.

More particularly, the present invention discloses an apparatus and method for controlling the voltage on a substrate so that the substrate is connected to a specific node, usually a power supply or ground terminal, if the parasitic PN diodes of all the circuit nodes are not forward biased. If a specified node(s) is (are) then forced with an applied voltage(s) to forward bias, the substrate is disconnected from its original specified node and maintains itself at a forward biased diode voltage drop away from the powered node(s). As a result, the substrate will not become substantially forward biased by the parasitic diodes and will be clamped at a specific voltage(s).

Figure 1 depicts one embodiment of a substrate snatching circuit 10 of the present invention utilizing a set of bipolar transistors QP1-QPN with a common terminal, the substrate V, as their common base. The emitters of these transistors are connected to a set of nodes T_{OUT1}-T_{OUTN} which may be driven to voltages beyond the range between that provided by the power supply V_{DD} and ground G or any other pair of applied voltages such as V_{DD} and V_{EE}, where V_{EE} is less than V_{DD}. The collectors of these bipolar transistors QP1-QPN are connected together. If any or all of the bipolar transistors QP1-QPN are turned on, the substrate V is disconnected from the power supply V_{DD} and is forced to a V_{BE} or diode drop away from the most positive of the emitter(s) of the turned on transistor(s) QP1 to QPN. When the node(s) is returned to a voltage(s) within the range of the power supply, the substrate V is reconnected to the original power supply node V_{DD}. This is described in greater detail below.

As depicted in Figure 1, the substrate clamp 10 employs multiple forcing nodes T_{OUT1} through T_{OUTN} that may be forced to a voltage or to voltages more positive than the supply voltage V_{DD}. However, any or all of the nodes from T_{OUT1} through T_{OUTN} can be used to produce the same results. In addition, an n-type substrate is used in the present embodiment for discussion purposes. Accordingly, the bipolar transistors QP1-QPN in the present embodiment are PNP transistors. However, P-type substrate material may also be used, and where

utilized, all transistors QP1-QPN in the substrate clamp 10 will be NPN-type transistors.

The substrate clamp 10 comprises three transistors, P1, N1, N2 and transistor(s) QP1 through QPN. P1 is a P-channel transistor, N1 and N2 are N-channel transistors and QP1 through QPN are PNP transistors. As discussed earlier, the circuit 10 may also be implemented by using complementary transistors, specifically, where P1 is an N-channel transistor, N1 and N2 are P-channel transistors and QP1 through QPN are NPN transistors.

In operation, if a positive voltage that is greater than the turn-on voltage of P1 is applied to V_{DD}, and the applied voltages on nodes T_{OUT1} through T_{OUTN} are greater than the applied voltage on V_{DD} by a value that is less than the turn-on voltage of any one of QP1-QPN, N2 will turn on, and node 2 will be held close to ground. This results in turning P1 on, and turning N1 off, effectively connecting the substrate V to V_{DD}.

Next, if any or all of the nodes T_{OUT1} through T_{OUTN} are forced more positive than V_{DD} by the turn-on voltage of QP1 through QPN respectively, current will be sourced by QP1 through QPN. If the value of that current is greater than the current that N2 can supply, node 2 will rise positively to a value close to that of the forced voltage(s) and will turn off P1 and turn on N1. N1 supplies the necessary base current drive to transistors QP1 through QPN so that their collector current(s) can equal the current that N2 supplies. As a result, the substrate V, will be disconnected from V_{DD} and will assume a potential essentially one PNP turn-on voltage less than the forced voltage(s) on the T_{OUT} line(s). In other words, V will be clamped one V_{BE} below the T_{OUT} line and held at that level by current through N1. As a result, the substrate will not be substantially forward biased.

Figure 2 depicts a schematic diagram of a second embodiment of the substrate snatching circuit 20 of the present invention. In the substrate snatching circuit 20, a Set , Reset (SR) flip flop 12 and a PNP

transistor QPN+1 is added to the circuit 10 of the previous embodiment.

The SR flip-flop 12 consists of 2 cross-coupled inverters - P2, N2 and P3, N3. This SR flip-flop 12 controls the two transistors N1 and P1. If the voltage on T_{OUT1} is less than or approximately equal to the voltage V_{DD}, transistor N1 will be off and transistor P1 will be turned on, connecting the line V and V_{DD}. The flip-flop 12 sets node 1 high and node 2 low. In this state, the circuit consumes no significant power. If a voltage more positive than about 0.7 volt greater than the supply V_{DD} is applied to node T_{OUT1} , the base emitter diode of transistor QP1 is forward biased. The resultant collector current tends to pull node 2 high against the available drain current of N2. If the collector current of QP1 is large enough to exceed the drain current of N2, the flip-flop 12 changes state. Node 2 is set high and node 1 is set low. This turns off P1 and turns on N1. In doing so, N1 draws a small current to ground G from node V through the emitter-base of QP1. This current pulls the substrate down with respect to either node T_{OUT1} or V_{DD} to one V_{BE} below T_{OUT1}. If the drive to T_{OUT1} is removed, the voltage on the substrate node V will be pulled down by transistor N1 until the PNP transistor QPN+1 is turned on. If the collector current of QPN+1 exceeds the drain current of N3, the flip-flop 12 will change state with node 1 acquiring a high state and node 2 a low state. Thus N1 will be turned off and P1 turned on, returning the current to its initial state and resulting in the substrate V being connected to V_{DD}.

Figure 3 illustrates a schematic diagram of a substrate snatcher circuit 30 in accordance with a further embodiment of the present invention. The circuit 30 is a practical implementation of the circuit 20 in which serial collectors are added by means of additional PNP transistors QP1', QP2',...QPN', (QPN+1)'. Due to the proximity of components in an integrated circuit and the ability of minority carriers to diffuse significant distances in the substrate when PN junctions are forward biased, a significant number of minority carriers may not be channeled through the collectors of QP1-QPN. The additional serial

collectors serve to collect most of the minority carriers that are not channeled through the collectors of QP1-QPN.

Transistors QP1', QP2',...QPN', (QPN+1)' are anti-saturation devices that collect minority carriers injected into the substrate, well or pocket, if either QPN+1, or any of QP1 through QPN are forced into saturation whereby their collectors act as emitters. The injection of minority carriers into the substrate should be constrained to the region close to the PNP transistor QPN+1 and the transistors QP1 - QPN connected to the forcing nodes T_{OUT1} through T_{OUTN}. Otherwise, adjacent nodes may collect these minority carriers and have their electrical characteristics corrupted. It should be noted that the collectors of these secondary transistors could alternatively be connected to ground (G) instead of to the substrate (V) as shown in the circuit 40 of Figure 4. This alternative embodiment will be discussed in greater detail in the following sections.

In practice, both Q1 and Q3 are integrated into Q2 and Q3 as additional collectors, as shown in Figure 5A and Figure 5B. Specifically, Figure 5A illustrates an elevational cross sectional view of one embodiment of a double PNP transistor which may be implemented in the substrate snatcher circuit of Figures 3 and 4. Figure 5B illustrates a schematic representation of the double PNP transistor of Figure 5A. When biased to operate in the active mode, the emitter-base voltage V_{EB} causes the P-type emitter to be higher in potential than the N-type base, thus forward-biasing the base-emitter junction. The collector-base junction is reverse-biased by the base-collector voltage V_{BC}, which keeps the N-type base higher in potential than the P-type collector. Current in the PNP device is mainly conducted by holes injected from the emitter into the base by the forward-bias voltage V_{EB}. Since the component of emitter current contributed by electrons injected from base to emitter is kept small by using a lightly doped base, most of the emitter current will be due to holes. The electrons injected from base to emitter give rise to the dominant component of base current. In addition, a number of holes injected into the base will recombine with the majority carriers in the

base (electrons) and will thus be lost. The disappearing base electrons will have to be replaced from the external circuit, giving rise to a second component of base current. The holes that succeed in reaching the boundary of the depletion region of the collector-base junction will be attracted by the negative voltage on the collector. Thus these holes will be swept across the depletion region into the collector and appear as collector current. The addition of a second collector, COLLECTOR 2 ensures that minority carriers injected into the substrate, well or pocket, are attracted to COLLECTOR 2 if either QPN+1, or any of QP1 through QPN are forced into saturation whereby their COLLECTORS 1 act as emitters. Thus, adjacent nodes will be prevented from collecting a number of these minority carriers and their electrical characteristics will not be corrupted. If the double collector transistors were implemented in the circuit 40 of Figure 4, COLLECTOR 2 will be grounded, and minority carriers will be attracted by COLLECTOR 2 and appear as collector current from COLLECTOR 2, which will subsequently be grounded.

Figure 5C depicts a schematic representation of the double PNP transistor of Figure 3 and Figure 4 implemented through the use of two transistors. Separate transistors are shown in Figures 3 and 4 rather than double collector transistors. As shown in Figure 5C, transistor QPN' is an anti-saturation device which collects minority carriers injected into the substrate, well or pocket, if QPN is forced into saturation such that its collector COLLECTOR 1 acts as an emitter. With COLLECTOR 1 acting like an emitter, COLLECTOR 2 is implemented to attract minority carriers so that these minority carriers appear as collector current from COLLECTOR 2, as discussed above.

The present invention offer several advantages. First, unlike conventional circuits, no comparators are utilized, resulting in a simpler circuit arrangement. Secondly, the substrate does not have to be connected directly to any node, resulting in the reduction of errors. Thirdly, the substrate will be forward biased with respect to a forced node, providing an accessible point of control. A particularly important use of the invention is where line drivers are overdriven to

voltages greater than the supply voltages used to power the line drivers. Without the present invention, one or more of the inherent PN junctions associated with the devices that make up the line drivers would become forward biased and at the minimum cause excessive current to flow into the substrate and in the extreme case cause functional failure.

Although the preferred embodiment of the present invention has been described and illustrated above, those skilled in the art will appreciate that various changes and modifications can be made to the present invention without departing from its spirit. Accordingly, the scope of the present invention is defined by the scope of the following appended claims.

CLAIMS:

What is claimed is:

1. A circuit for controlling the voltage applied to a substrate, comprising:

a first transistor of a first conductivity type, having an emitter, a base and a collector;

a second transistor of a second conductivity type having a drain, a source and a gate;

third and fourth transistors of a third conductivity type, each having a drain, a source and a gate;

the collector of said first transistor, the gate of the second transistor and the gate of the third transistor and the drain of the fourth transistor being coupled together;

the base of the first transistor, the source of the second transistor and the drain of the third transistor being coupled to a first node;

the drain of the second transistor and the gate of the fourth transistor being coupled to a first voltage;

the emitter of said first transistor being coupled to a second voltage; and

the sources of the third and fourth transistors being coupled together;

wherein in a first state, the first node is connected to the first voltage if the second voltage is not applied and in a second state, the first node is connected to a third voltage if the second voltage is applied, the third voltage being less than the second voltage.

2. The circuit of Claim 1, further comprising a fifth transistor of the first conductivity type, having an emitter, a base and a collector, the collector of the fifth transistor being coupled to the gate of the second transistor, the base of the fifth transistor being coupled to a second node and the emitter of the fifth transistor being coupled to a fourth voltage, wherein the second node is connected to the first voltage if the second voltage is not applied and the second node is

connected to a fourth voltage if the second voltage is applied, the fourth voltage being less than the second voltage.

3. The circuit of Claim 2, wherein the fourth voltage is greater than the first voltage.

4. The circuit of Claim 1, further comprising a latching circuit for stabilizing said first and second states, said latching circuit having a set state and a reset state, said latching circuit providing a latch onto said second state when in said set state and said latching circuit providing a latch onto said first state when in said reset state.

5. The circuit of Claim 4, wherein said latching circuit comprises:

fifth and sixth transistors of the second conductivity type, each having a drain, a source and a gate;

a seventh transistor of the third conductivity type, each having a drain, a source and a gate;

the sources of the fifth and sixth transistors being coupled to the first node;

the gate of the fifth transistor, the drain of the sixth transistor and the drain of the seventh transistor being coupled together; and

the drains of the fifth transistor, the gate of the sixth transistor and the gate of the fourth transistor being coupled together.

6. The circuit of Claim 1, wherein said first conductivity type is a PNP transistor, said second conductivity type is a P-channel transistor and said third conductivity type is an N-channel transistor.

7. The circuit of Claim 1, wherein said first conductivity type is an NPN transistor, said second conductivity type is an N-channel transistor and said third conductivity type is a P-channel transistor.

8. The circuit of Claim 5, wherein said first conductivity type is a PNP transistor, said second conductivity type is a P-channel transistor and said third conductivity type is an N-channel transistor.

9. The circuit of Claim 5, wherein said first conductivity type is an NPN transistor, said second conductivity type is an N-channel transistor and said third conductivity type is a P-channel transistor.

10. The circuit of Claim 1, further comprising a fifth transistor of the first conductivity type, having an emitter, a base and a collector, the base of the fifth transistor being coupled to the base of the first transistor, the collector of the fifth transistor being coupled to the first node and the emitter of the fifth transistor being coupled to the collector of the first transistor.

11. The circuit of Claim 10, wherein said first conductivity type is a PNP transistor, said second conductivity type is a P-channel transistor and said third conductivity type is an N-channel transistor.

12. The circuit of Claim 10, wherein said first conductivity type is an NPN transistor, said second conductivity type is an N-channel transistor and said third conductivity type is a P-channel transistor.

13. A method of controlling the voltage applied to a substrate, said method comprising the steps of:

providing:

a first transistor of a first conductivity type, having an emitter, a base and a collector;

a second transistor of a second conductivity type having a drain, a source and a gate;

third and fourth transistors of a third conductivity type, each having a drain, a source and a gate;

the collector of said first transistor, the gate of the second transistor and the gate of the third transistor and the drain of the fourth transistor being coupled together;

the base of the first transistor, the source of the second transistor and the drain of the third transistor being coupled to a first node;

the drain of the second transistor and the gate of the fourth transistor being coupled to a first voltage;

the emitter of said first transistor being coupled to a second voltage; and

the sources of the third and fourth transistors being coupled together;

connecting the first node to the first voltage if the second voltage is not applied; and

connecting the first node to a third voltage if the second voltage is applied, the third voltage being less than the second voltage.

14. The method of Claim 13, further comprising the steps of:

providing a fifth transistor of the first conductivity type, having an emitter, a base and a collector, the collector of the fifth transistor being coupled to the gate of the second transistor, the base of the fifth transistor being coupled to a second node and the emitter of the fifth transistor being coupled to a fourth voltage;

in a first state, connecting the second node to the first voltage if the second voltage is not applied; and

in a second state, connecting the second node to a fourth voltage if the second voltage is applied, the fourth voltage being less than the second voltage.

15. The method of Claim 14, wherein the fourth voltage is greater than the first voltage.

16. The method of Claim 14, further comprising the steps of:

providing a latching circuit for stabilizing said first and second states, said latching circuit having a set state and a reset state;

setting said latching circuit to provide a latch onto said second state; and resetting said latching circuit to provide a latch onto said first state.

17. The method of Claim 14, wherein in said providing a latching circuit step, said latching circuit comprises:

fifth and sixth transistors of the second conductivity type, each having a drain, a source and a gate;

a seventh transistor of the third conductivity type, each having a drain, a source and a gate;

the sources of the fifth and sixth transistors being coupled to the first node;

the gate of the fifth transistor, the drain of the sixth transistor and the drain of the seventh transistor being coupled together; and

the drain of the fifth transistor, the gate of the sixth transistor and the drain of the fourth transistor being coupled together.

18. The method of Claim 13, wherein in said providing step, said first conductivity type is a PNP transistor, said second conductivity type is a P-channel transistor and said third conductivity type is an N-channel transistor.

19. The method of Claim 13, wherein in said providing step, said first conductivity type is an NPN transistor, said second conductivity type is an N-channel transistor and said third conductivity type is a P-channel transistor.

20. The method of Claim 17, wherein in said providing step, said first conductivity type is a PNP transistor, said second conductivity type is a P-channel transistor and said third conductivity type is an N-channel transistor.

21. The method of Claim 17, wherein in said providing step, said first conductivity type is an NPN transistor, said second

conductivity type is an N-channel transistor and said third conductivity type is a P-channel transistor.

22. The method of Claim 13, wherein said providing step further includes providing a fifth transistor of the first conductivity type, having an emitter, a base and a collector, the base of the fifth transistor being coupled to the base of the first transistor, the collector of the fifth transistor being coupled to the first node and the emitter of the fifth transistor being coupled to the collector of the first transistor.

23. The method of Claim 22, wherein in said providing step, said first conductivity type is a PNP transistor, said second conductivity type is a P-channel transistor and said third conductivity type is an N-channel transistor.

24. The method of Claim 22, wherein in said providing step, said first conductivity type is an NPN transistor, said second conductivity type is an N-channel transistor and said third conductivity type is a P-channel transistor.

25. A circuit for controlling the voltage applied to a substrate, comprising:

a first voltage source providing a first voltage;

a clamping circuit connected to the first voltage source, said clamping circuit having at least one forcing node; and

a second voltage source providing a second voltage, said second voltage source connected to the forcing node, wherein in a first state, the forcing node is connected to the first voltage source if the second voltage is not applied and in a second state, the forcing node is connected to a third voltage if the second voltage source is applied, the third voltage being less than the second voltage.

26. A method for controlling the voltage applied to a substrate, said method comprising the steps of:

providing:

a first voltage source providing a first voltage;

a clamping circuit connected to the first voltage source, said clamping circuit having at least one forcing node; and

a second voltage source providing a second voltage, said second voltage source connected to the forcing node;

connecting the forcing node to the first voltage source if the second voltage source is not applied; and

connecting the forcing node to a third voltage if the second voltage is applied, the third voltage being less than the second voltage.

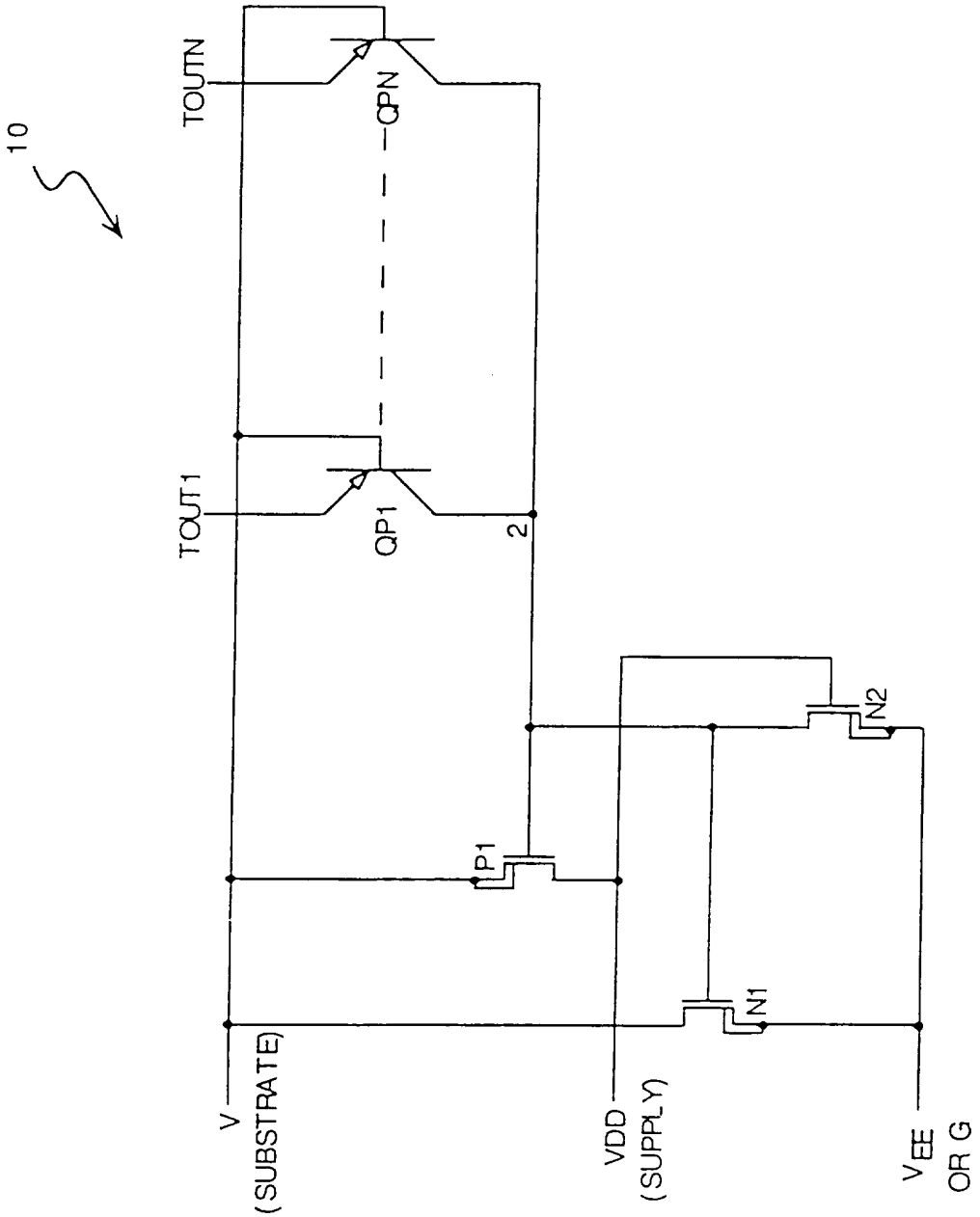
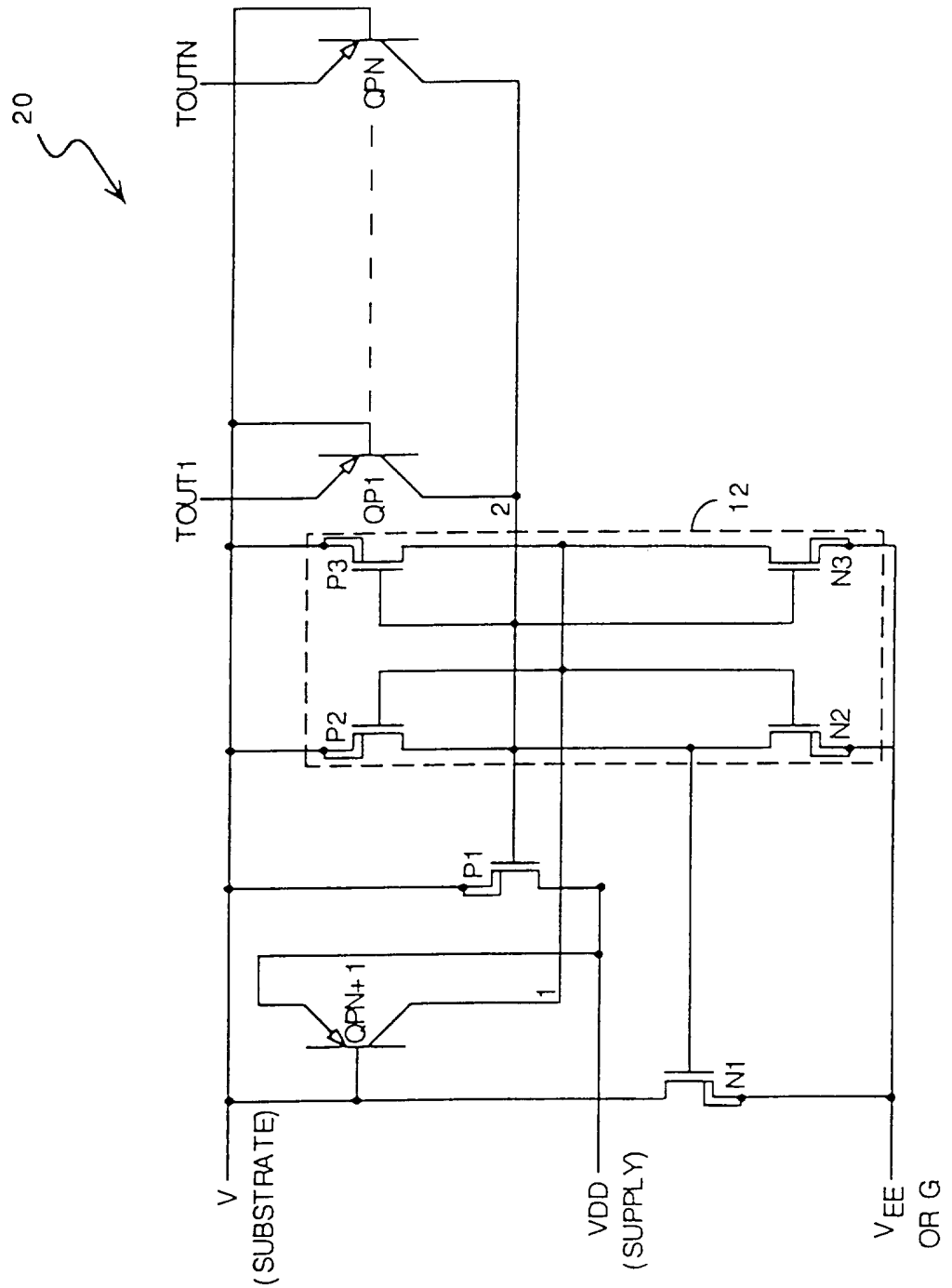

10
TOUTN
QPN
TOUT1
QP1
2
P1
N2
N1
V
(SUBSTRATE)
VDD
(SUPPLY)
VEE
OR G

Figure 1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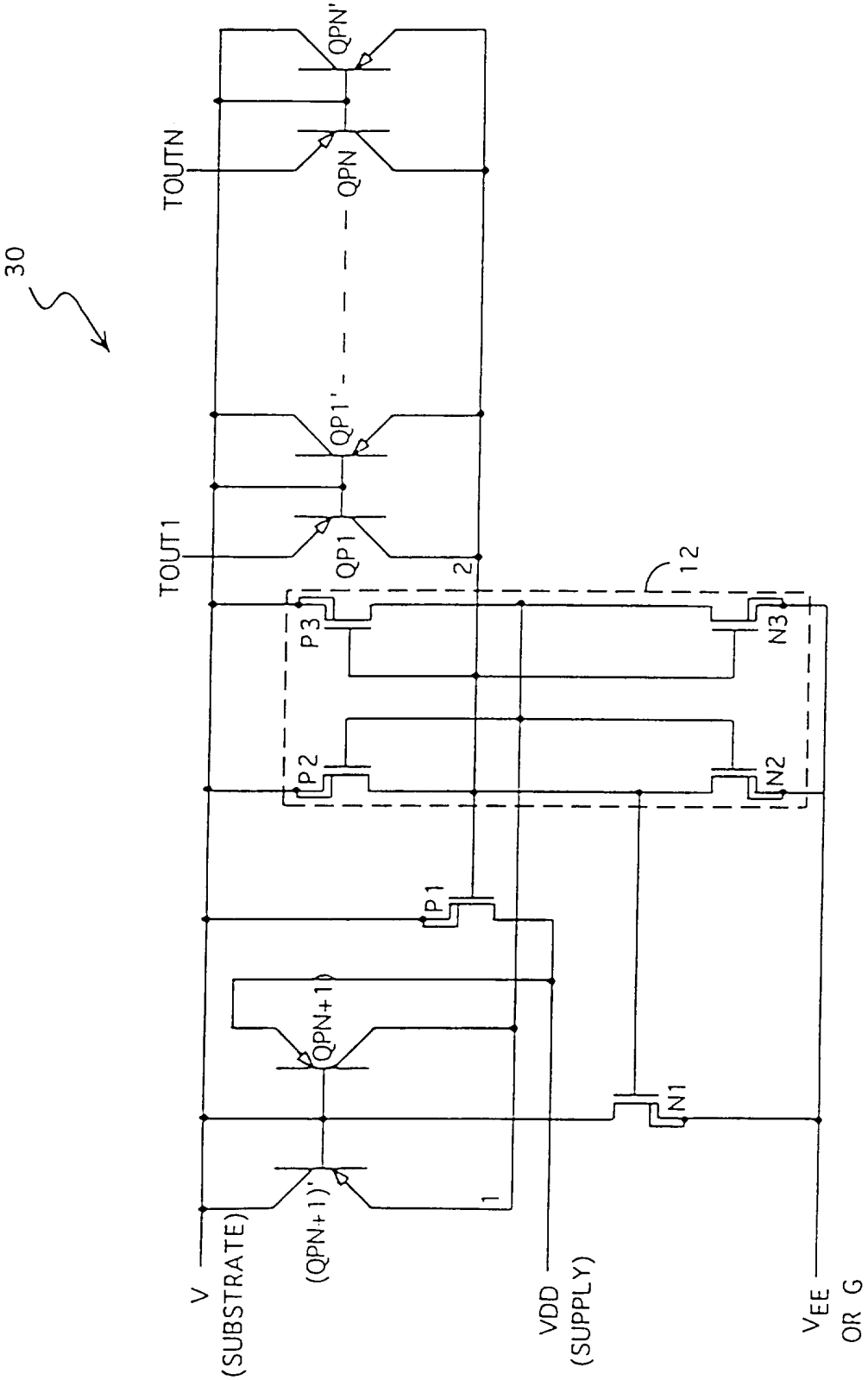
TOUTN
QPN
TOUT1
QP1
2
12
P3
N3
P2
N2
P1
QPN+1
1
N1
V
(SUBSTRATE)
VDD
(SUPPLY)
VEE
OR G

Figure 2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QPN'
QPN
TOUTN
QP1'
QP1
TOUT1
2
12
P3
N3
P2
N2
P1
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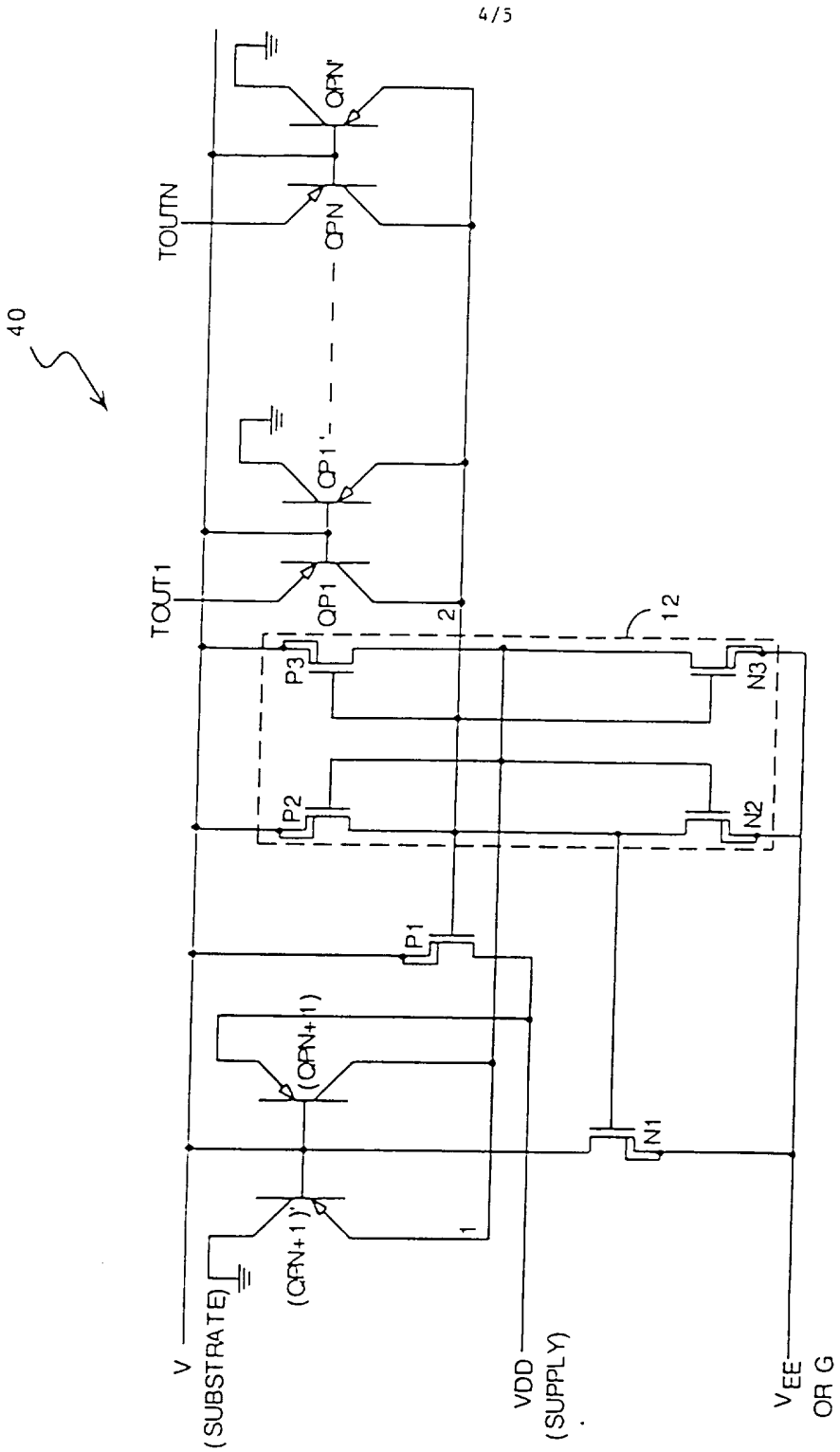
N1
1
(QPN+1)'
V
(SUBSTRATE)
VDD
(SUPPLY)
VEE
OR G

Figure 3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QPN'
QPN
QP1'
TOUT1
QP1
2
12
P3
N3
P2
N2
P1
(QPN+1)
N1
(QPN+1)'
1
V
(SUBSTRATE)
VDD
(SUPPLY)
VEE
OR G

Figure 4

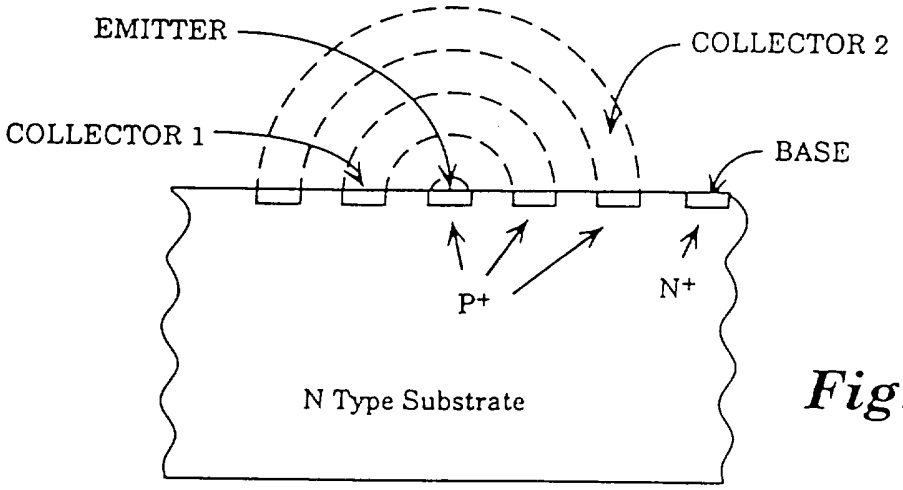

Figure 5A

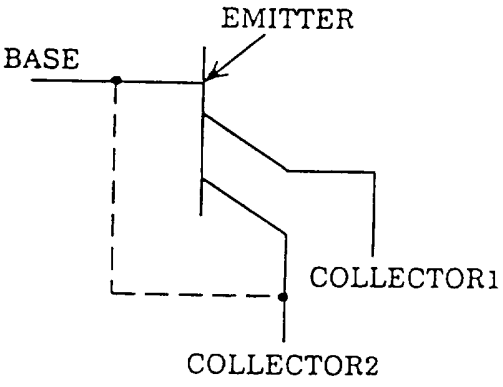

Figure 5B

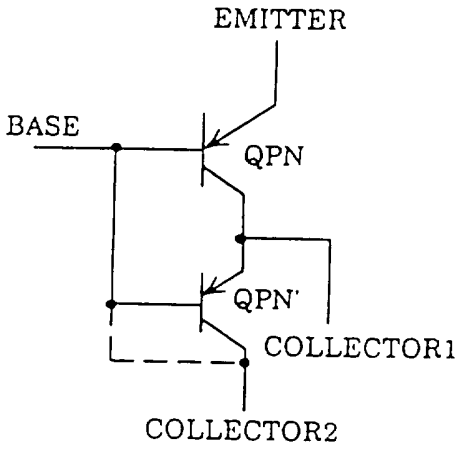

Figure 5C

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US95/16625

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) : H03K 17/16, 17/735
US CL :327/535, 78, 81, 407, 410, 537, 543, 546
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 327/77, 78, 81, 407, 408, 410, 411, 535, 536, 537, 538, 543, 546

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A,P	US, A, 5,442,307 (SHIGEHARA ET AL.) 15 August 1995, see Fig. 4.	25-26
A,P	US, A, 5,382,837 (AIELLO ET AL.) 17 January 1995, see Fig. 1.	25-26
X	US, A, 5,157,280 (SCHRECK ET AL.) 20 October 1992, see Fig. 4a.	25-26
A	US, A, 4,965,466 (PIGOTT) 23 October 1990, see Fig. 2.	25-26
X	US, A, 4,686,388 (HAFNER) 11 August 1987, see the figure.	25-26
X	US, A, 4,617,473 (BINGHAM) 14 October 1986, see Fig. 2.	25-26

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 28 MARCH 1996	Date of mailing of the international search report 04 APR 1996
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 308-7722	Authorized officer TERRY D. CUNNINGHAM Telephone No. (703) 308-4872

Form PCT/ISA/210 (second sheet)(July 1992)*

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US95/16625

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US, A, 4,473,758 (HUNTINGTON) 25 September 1984, see Fig. 2.	25-26