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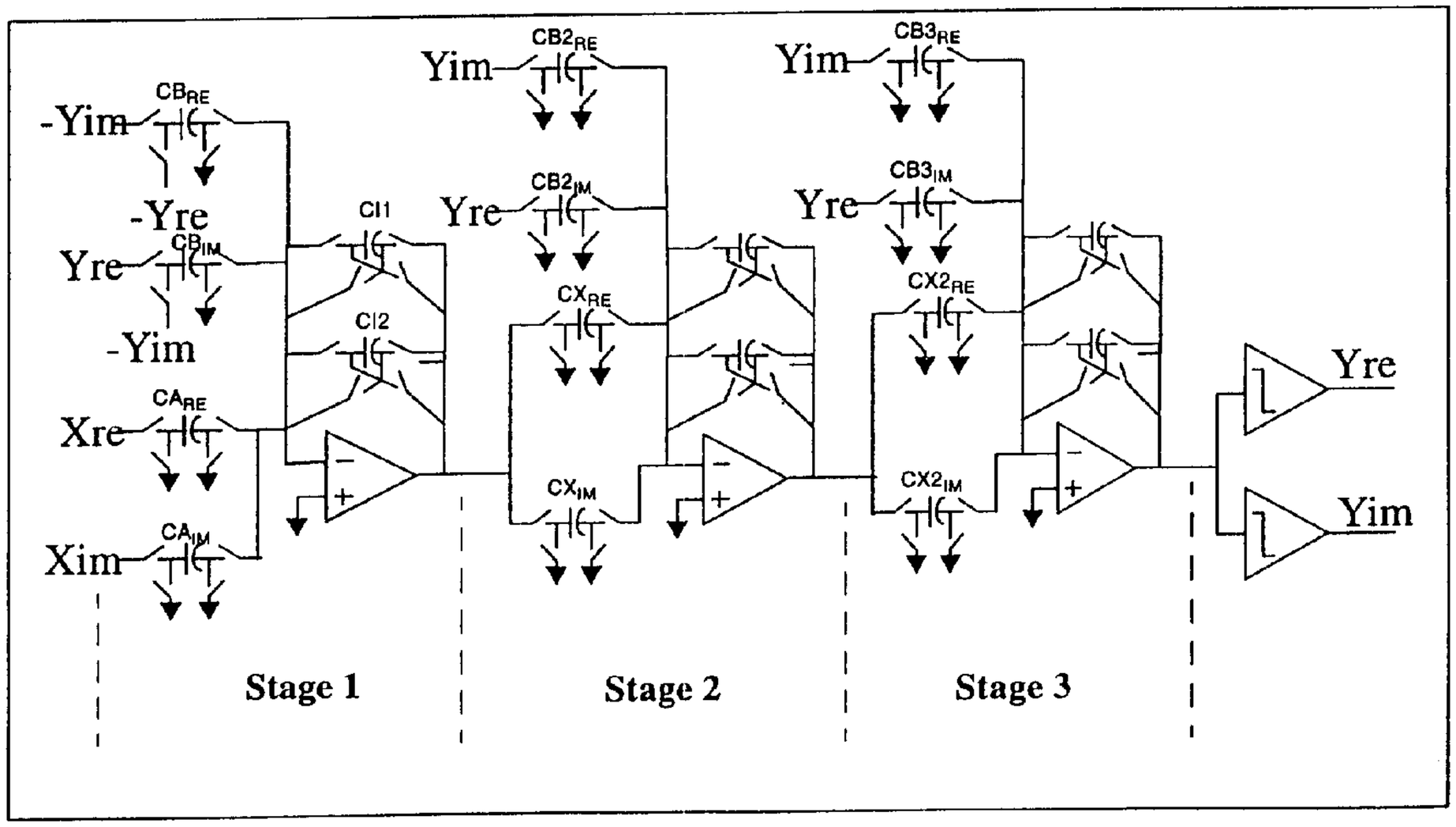
(54) **CONVERTISSEUR ANALOGIQUE/NUMERIQUE POUR APPLICATIONS RADIOELECTRIQUES**

(54) **ANALOG TO DIGITAL CONVERTER FOR RADIO APPLICATIONS**



(57) An analog to digital converter for radio applications includes an alternative complex BP.SIGMA..DELTA.M, having fewer components (making it more power efficient) than prior art devices, as well as a technique to compensate for circuit imperfections that can destroy the performance of this type of converter. One advantage of this converter is that the amount of noise that is close to the signal is greatly reduced.

ABSTRACT

An analog to digital converter for radio applications includes an alternative complex BPΣΔM, having fewer components (making it more power efficient) than prior art devices, as well as a technique to compensate for circuit imperfections that can destroy the performance of this type of converter. One advantage of this converter is that the amount of noise that is close to the signal is greatly reduced.

ANALOG TO DIGITAL CONVERTER FOR RADIO APPLICATIONS

FIELD OF INVENTION

The present invention relates to an analog to digital converter for radio applications.

BACKGROUND OF THE INVENTION

Radio receivers are often built around a direct conversion architecture as seen in Figure 1. This allows for many of the component circuits to be integrated on one chip. But such receivers suffer from problems such as fixed DC offset, even-order harmonic distortion, and the like.

Other receivers, such as super-heterodyne structures, suffer from the fact that most of the required circuitry cannot be integrated onto a single chip, leading to a more expensive receiver. One approach around both of these problems is to use a receiver that does not mix the signal to DC, but rather to a set intermediate frequency (IF) as seen in Figure 2. If the signal is then digitized through an Analog to Digital (A/D) converter, then much of the remaining functions of a receiver (channel select, image rejection, and the like) can be moved to digital components, where it is easy to manufacture circuits with ideal performance.

Since many of the signals to be received have a relatively narrow bandwidth (BW), and the IF is usually much larger than the BW, it is a waste to A/D convert the entire frequency spectrum, up to the IF. This also gives a trade off between resolution and component expense, since a high-resolution A/D would operate at low speeds, making the filter in front of it more expensive, and a high-speed A/D typically will be limited in resolution to 8-10 bits because of circuit imperfections.

Conventional approaches have been to use an A/D convertor with limited resolution and use automatic gain control (AGC) to increase dynamic range. Recently, another solution has been proposed, namely that of using a bandpass sigma/delta modulator (BPΣΔM). This type of A/D converter has the advantage that it can give good resolution in a relatively narrow band (compared to its sampling rate), as seen in Figure 3. For BPΣΔM, there is a trade off between bandwidth and resolution, ie. the lower the bandwidth, the higher the resolution.

BPΣΔM are routinely used in radio receiver design and have been shown to give adequate performance for reasonable bandwidths. One major trade off is: to get the required resolution, it might be necessary to operate the BPΣΔM at high sampling rates, increasing the power consumption, and therefore making it prohibitive for a portable application. Thus, the goal is to get the required resolution with a low sampling rate, and as little power consumption as possible.

Recently, the complex BPΣΔM has been demonstrated to give increased resolution and wider bandwidths as compared to a conventional BPΣΔM (for similar sampling rates).

SUMMARY OF THE INVENTION

The object of the present invention is to provided an improved analog to digital converter for radio applications.

The present invention provides an alternative complex BPΣΔM, having fewer components (making it more power efficient) than prior art devices, as well as a technique to compensate for circuit imperfections that can destroy the performance of this type of convertor. The advantage of this convertor can be seen in Figure 4, where it can be seen that the amount of noise that is close to the signal is greatly reduced.

The complex BPΣΔM can be thought of as two real filters (one for each of the imaginary and real channels) that are coupled together as shown in Figures 5 and 6. The circuit implementing this is shown in Figure 7. By exploiting the fact that the output of each channel depends on the previous value of the other channel, and its input, we can use the same opamp circuit to perform the operation for both the real and imaginary channel.

A complex BPΣΔM is basically an inphase/quadrature (I/Q) system. It is well known that any mismatch in I/Q systems causes 'images' to be created within the desired signal band as is shown in Figure 8. If the complex term is perfectly accurate, then no image appears inside the signal. But for any non-idealities in the circuit that implements this function, the image appears in the signal and can easily be more powerful than the desired signal. In a complex BPΣΔM, the effect is even worse, in that the A/D converter has an input that consists of both a signal, and quantization noise. For any mismatch, this quantization noise can show up within the signal band, which can degrade the quality of the A/D converter. One method around this is to feed both the real and imaginary (I and Q) parts of the signal into both paths (Figure 9). Since the same input goes through both paths, the mismatch error is cancelled to a first-order approximation.

The underlying principal is that it uses the same output from the analog to digital converter and feeds it back through both channels in order to negate the circuit imperfections that can degrade performance. Both channels are implemented as one circuit element instead of two, which uses half the power.

According to the invention, there is provided an analog to digital converter for radio applications, comprising: real and imaginary inputs; real and imaginary outputs; at least one stage having real and imaginary inputs and real and imaginary

outputs; a summing node connecting the real and imaginary inputs of the analog to digital converter to the real and imaginary inputs of the stage; a summing node connecting the real and imaginary outputs of the analog to digital converter to the real and imaginary inputs of the stage; a switching scheme in the stage for minimizing the effect of component imperfections using the real and imaginary outputs of the analog to digital converter; a quantizer connecting the real output of the stage to the real output of the analog to digital converter; a quantizer connecting the imaginary output of the stage to the imaginary output of the analog to digital converter; and a switching scheme within the stage for reducing the number of active components by a factor of two by using a single active component for both the real and imaginary outputs of the stage.

According to the invention, there is further provided an analog to digital converter for radio applications, comprising: real and imaginary inputs; real and imaginary outputs; first, second and third stages, each having real and imaginary inputs and real and imaginary outputs; a summing node connecting the real and imaginary inputs of the analog to digital converter to the real and imaginary inputs of the first stage; a summing node connecting the real and imaginary outputs of the analog to digital converter to the real and imaginary inputs of the first stage; a switching scheme in the first, second and third stages for minimizing the effect of component imperfections

using the real and imaginary outputs of the analog to digital converter; a summing node connecting the real and imaginary outputs of the first stage to the real and imaginary inputs of the second stage; a summing node connecting the real and imaginary outputs of the analog to digital converter to the real and imaginary inputs of the second stage; a summing node connecting the real and imaginary outputs of the second stage to the real and imaginary inputs of the third stage; a summing node connecting the real and imaginary outputs of the analog to digital converter to the real and imaginary inputs of the third stage; a quantizer connecting the real output of the third stage to the real output of the analog to digital converter; a quantizer connecting the imaginary output of the third stage to the imaginary output of the analog to digital converter; and a switching scheme within each of the first, second and third stages for reducing the number of active components by a factor of two by using a single active component for both the real and imaginary outputs of each stage.

Note that there can be any number of stages. The switching scheme can be present in one or more stages.

Other advantages, objects and features of the present invention will be readily apparent to those skilled in the art from a review of the following detailed description of

preferred embodiments in conjunction with the accompanying drawings and claims.

BRIEF DESCRIPTION OF THE DRAWINGS

The embodiments of the invention will now be described with reference to the accompanying drawings, in which:

Figure 1 is a diagram of a direct conversion receiver;

Figure 2 is a diagram of a single intermediate frequency receiver;

Figure 3 is a graph comparing outputs of typical analog to digital converters used in receivers;

Figure 4 is a graph comparing outputs of a bandpass sigma delta modulator analog to digital converter and a complex bandpass sigma delta modulator analog to digital converter;

Figure 5 is a diagram of one component of a complex bandpass sigma delta modulator analog to digital converter;

Figure 6 is a diagram of an implementation of the component of Figure 5;

Figure 7 is a diagram of a circuit implementing the component of Figure 5;

Figure 8 is a graph showing the effect of image aliasing in an IQ system;

Figure 9 is a diagram of a circuit implementing the component of Figure 5 with correction for image aliasing as shown in Figure 8;

Figure 10 is a diagram of a circuit implementing an embodiment of the analog to digital converter of the present invention; and

Figure 11 is a diagram showing the analog to digital converter of the present invention incorporated into a radio receiver.

Similar references are used in different figures to denote similar components.

DETAILED DESCRIPTION OF THE INVENTION

This invention is designed as a discrete time switched-capacitor (SC) circuit in a BiCMOS process. The single-ended circuit is shown in Figure 10. This invention can be incorporated into any mainstream CMOS process, and with some

small modifications, can be built with a continuous time filter for high-speed applications. The circuit, incorporated into a receiver architecture is shown in Figure 11.

The circuit operates on multiple clocks (rather than the traditional phi1 and phi2 clocks that are normally seen in SC circuits). As a brief explanation, the inputs to the A/D (Xre and Xim) are sampled on opposite phases of the clock onto the capacitors CA_{RE} and CA_{IM}. This charge is then dumped onto CI1 on the first complete clock cycle, then CI2 on the next complete clock cycle. During the middle of this charge dumping onto CI1 and CI2, the capacitor is effectively 'flipped' by the cross-coupling switches that are seen in Figure 10. This serves to effectively make the integrator (1/(z-1) transfer function) look like a band-pass integrator (1/(z+1) transfer function). This is needed because if we are to realize a bandpass notch (not at DC) then we need a circuit element inside the ΣΔM that has a very large gain at that non-DC frequency. The next two stages work in a very similar way to the first stage. Now, it is important to discuss the feedback inherent to a ΣΔM, specifically by dumping charge from CB_{RE}, CB_{IM}, $CB2_{RE}$, etc. onto the capacitors CI1, CI2, etc. This operates with exactly the same mechanism as was outlined for the input capacitors above. The one notable difference is that for example, in the case of CB_{RE}, the capacitor is charged with a voltage -Yim. But in the process of its charge being transferred to CI1 and CI2, the voltage -Yre is subtracted from

it. And it can be seen that a very similar thing also happens to the capacitor CBIM. As mentioned above, if there is mismatch between the real (represented in part by $_{RE}$ subscript) and imaginary (represented in part by $_{IM}$ subscript) the performance of this A/D converter is seriously degraded. By having both RE and IM outputs going through the same capacitor, the effect of this mismatch error is reduced. This particular technique is only shown on the first stage of the ΣΔM, but it's application can be used in all stages of this type of complex ΣΔM.

Numerous modifications, variations and adaptations may be made to the particular embodiments of the invention described above without departing from the scope of the invention, which is defined in the claims.

THE EMBODIMENTS OF THE PRESENT INVENTION IN WHICH AN EXCLUSIVE PROPERTY OR PRIVILEGE IS CLAIMED ARE DEFINED AS FOLLOWS:

1. An analog to digital converter for radio applications, comprising:

real and imaginary inputs;

real and imaginary outputs;

at least one stage having real and imaginary inputs and real and imaginary outputs;

a summing node connecting the real and imaginary inputs of the analog to digital converter to the real and imaginary inputs of the stage;

a summing node connecting the real and imaginary outputs of the analog to digital converter to the real and imaginary inputs of the stage;

a switching scheme in the stage for minimizing the effect of component imperfections using the real and imaginary outputs of the analog to digital converter;

a quantizer connecting the real output of the stage to the real output of the analog to digital converter;

a quantizer connecting the imaginary output of the stage to the imaginary output of the analog to digital converter; and

a switching scheme within the stage for reducing the number of active components by a factor of two by using a single active component for both the real and imaginary outputs of the stage.

2. An analog to digital converter for radio applications, comprising:

real and imaginary inputs;

real and imaginary outputs;

first, second and third stages, each having real and imaginary inputs and real and imaginary outputs;

a summing node connecting the real and imaginary inputs of the analog to digital converter to the real and imaginary inputs of the first stage;

a summing node connecting the real and imaginary outputs of the analog to digital converter to the real and imaginary inputs of the first stage;

a switching scheme in the first, second and third stages for minimizing the effect of component imperfections using the real and imaginary outputs of the analog to digital converter;

a summing node connecting the real and imaginary outputs of the first stage to the real and imaginary inputs of the second stage;

a summing node connecting the real and imaginary outputs of the analog to digital converter to the real and imaginary inputs of the second stage;

a summing node connecting the real and imaginary outputs of the second stage to the real and imaginary inputs of the third stage;

a summing node connecting the real and imaginary outputs of the analog to digital converter to the real and imaginary inputs of the third stage;

a quantizer connecting the real output of the third stage to the real output of the analog to digital converter;

a quantizer connecting the imaginary output of the third stage to the imaginary output of the analog to digital converter; and

a switching scheme within each of the first, second and third stages for reducing the number of active components by a factor of two by using a single active component for both the real and imaginary outputs of each stage.

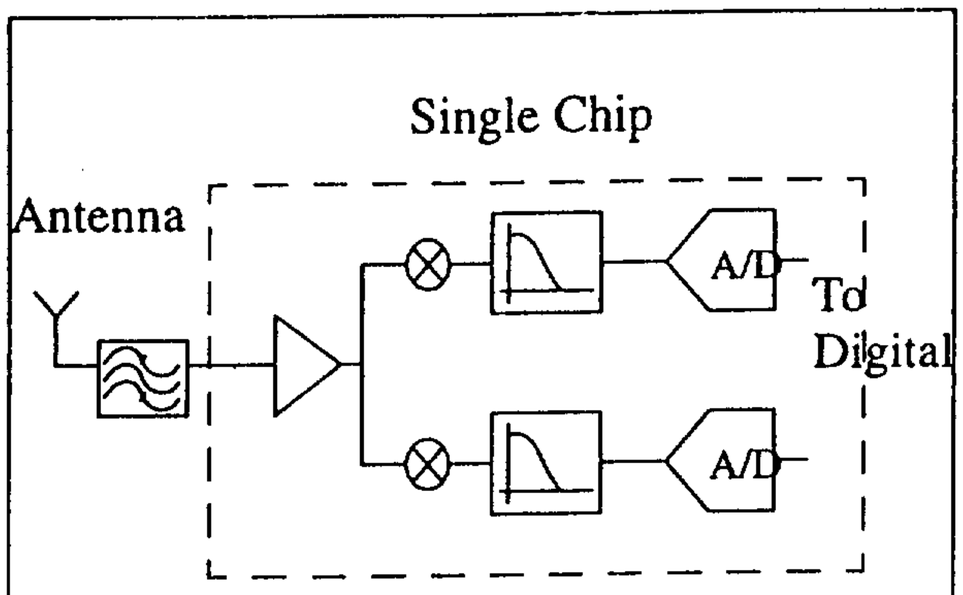


Fig. 1

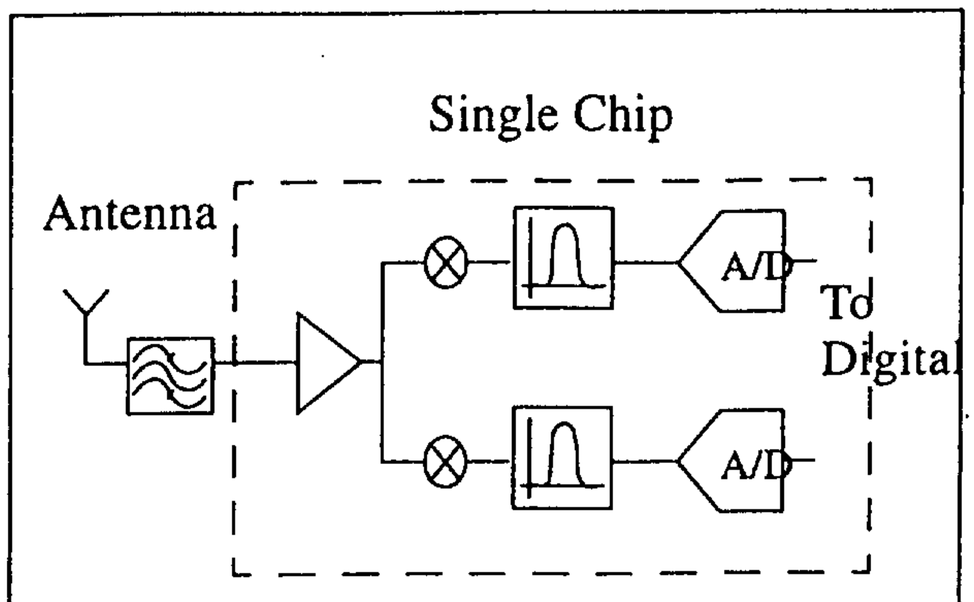


Fig. 2

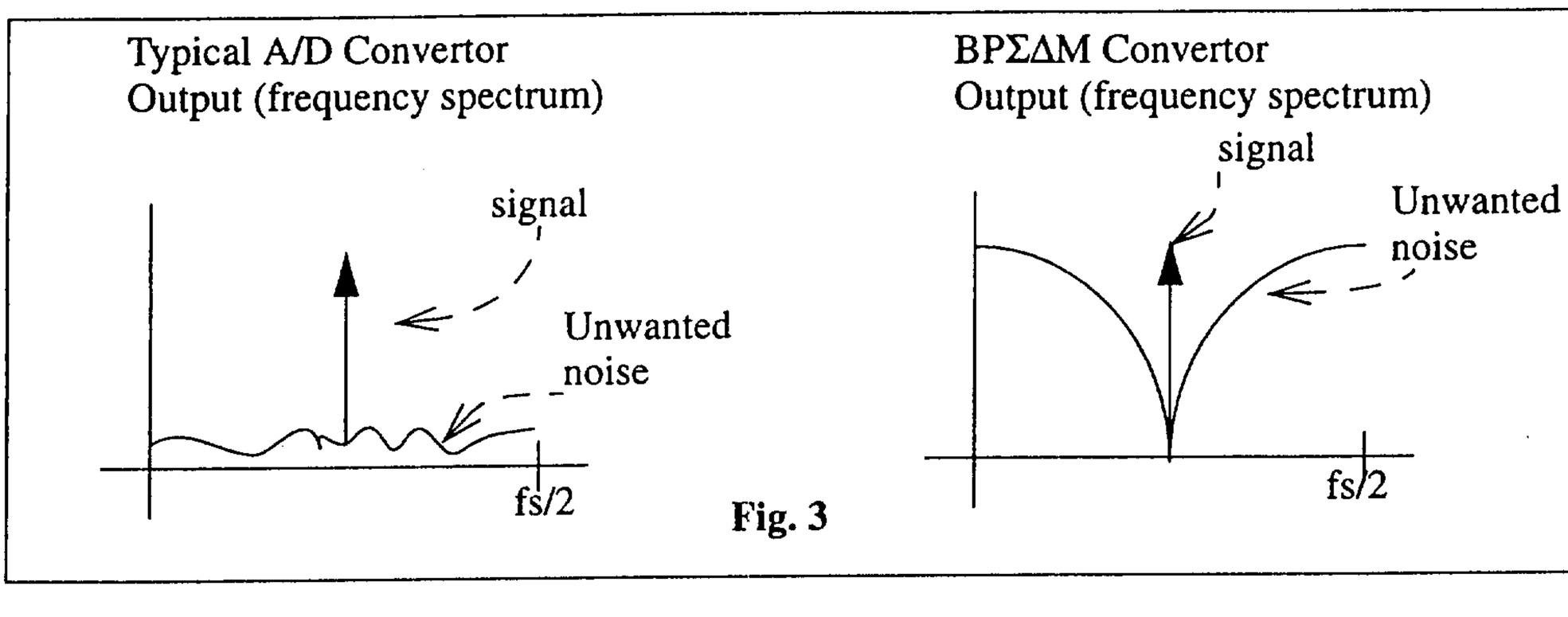


Fig. 3

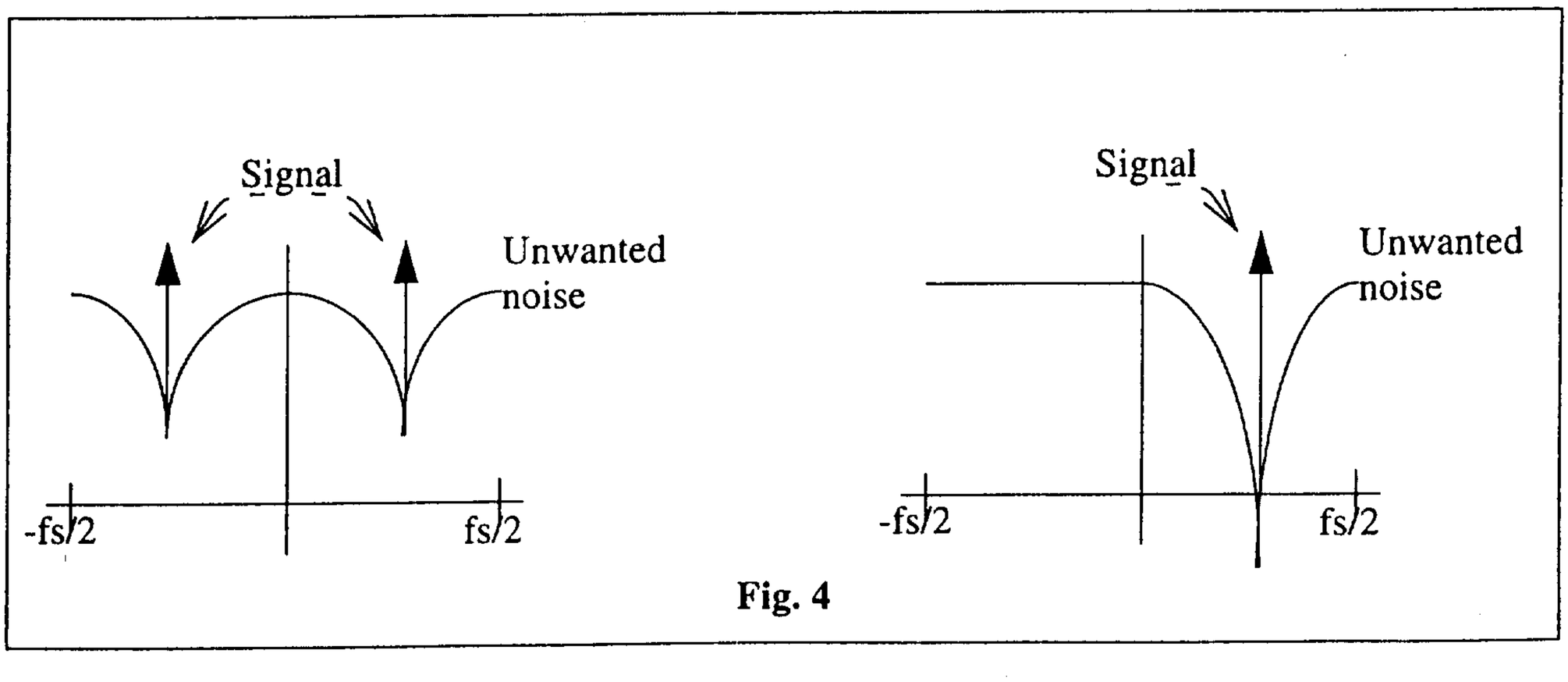


Fig. 4

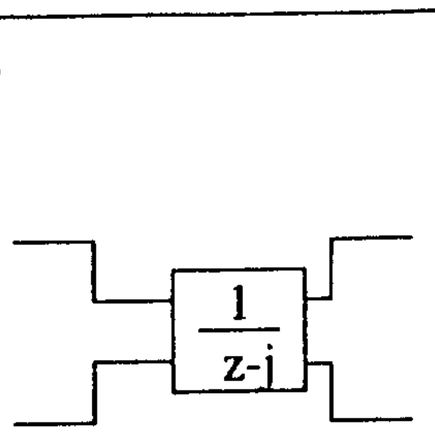


Fig. 5

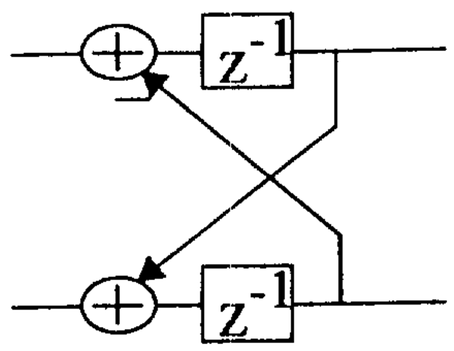


Fig. 6

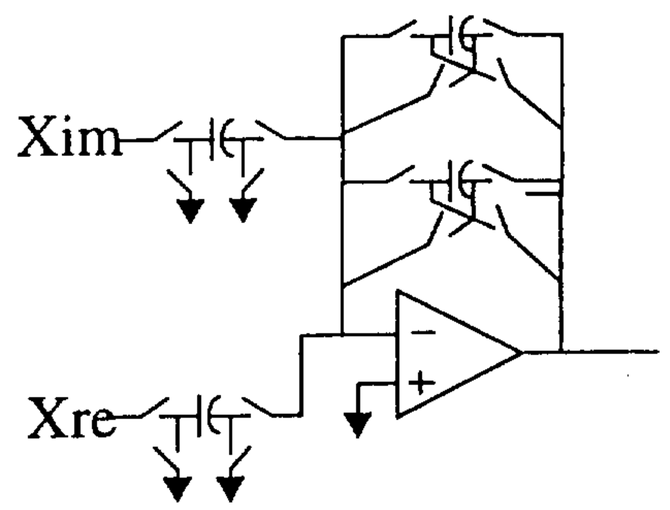


Fig. 7

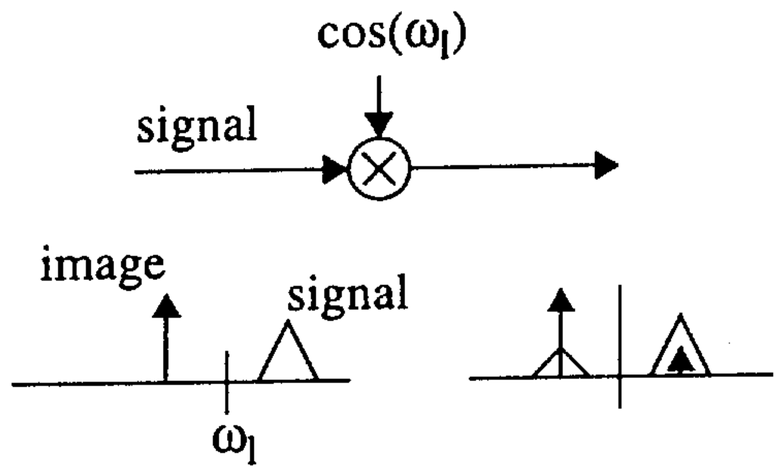


Fig. 8

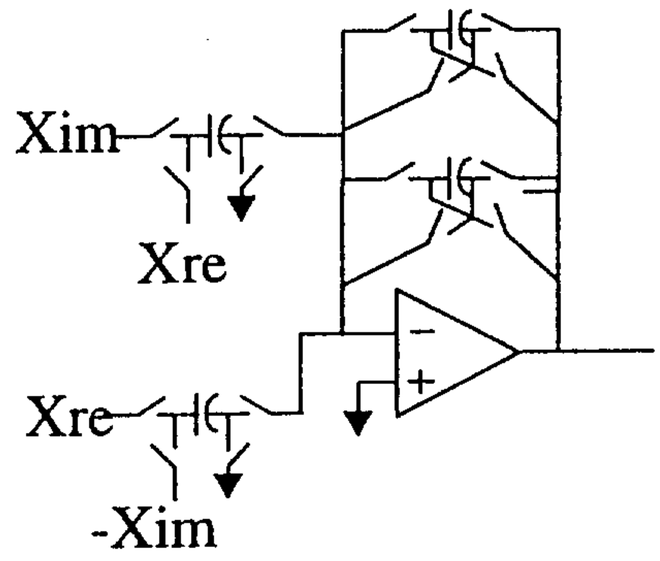


Fig. 9

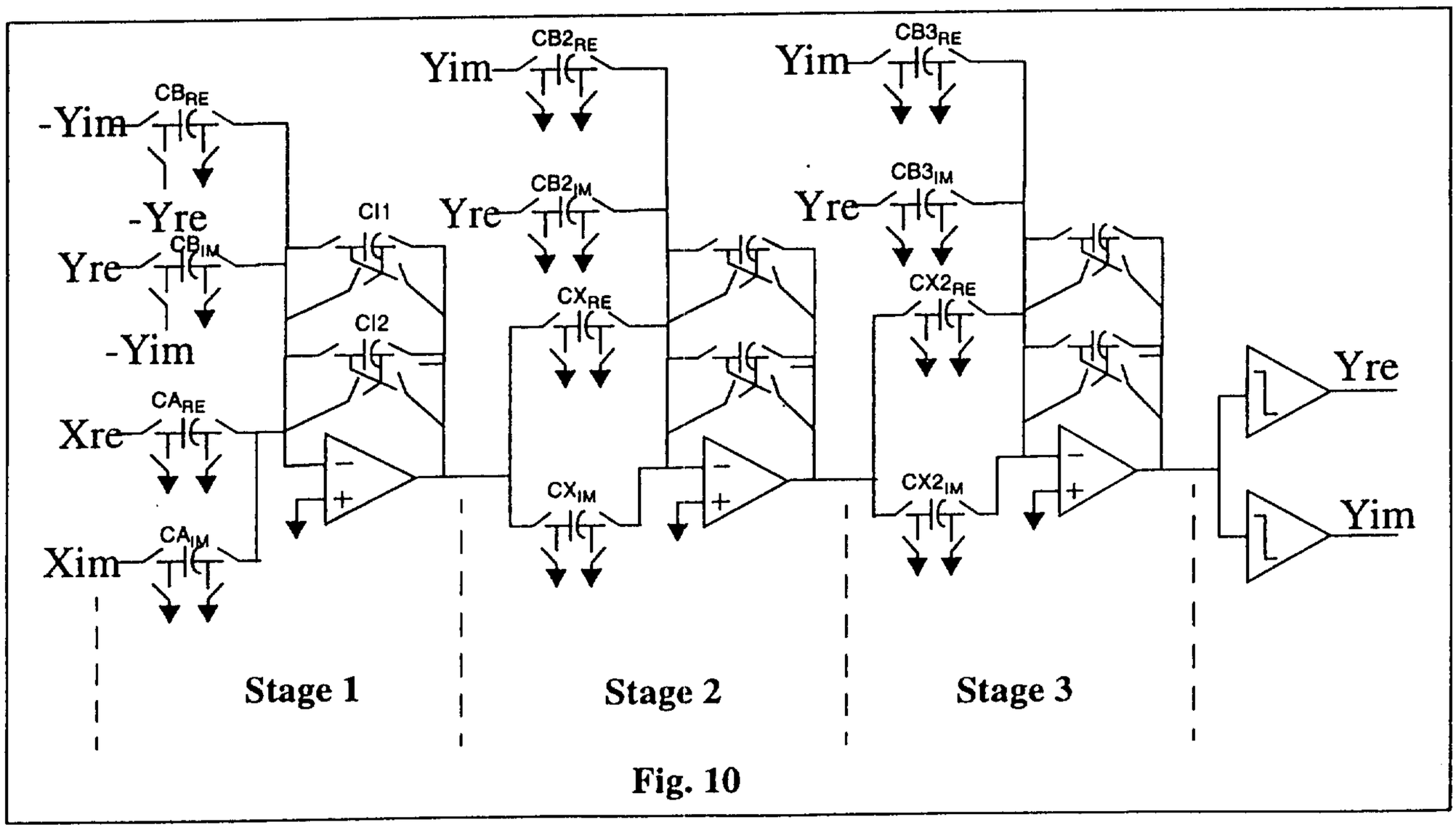


Fig. 10

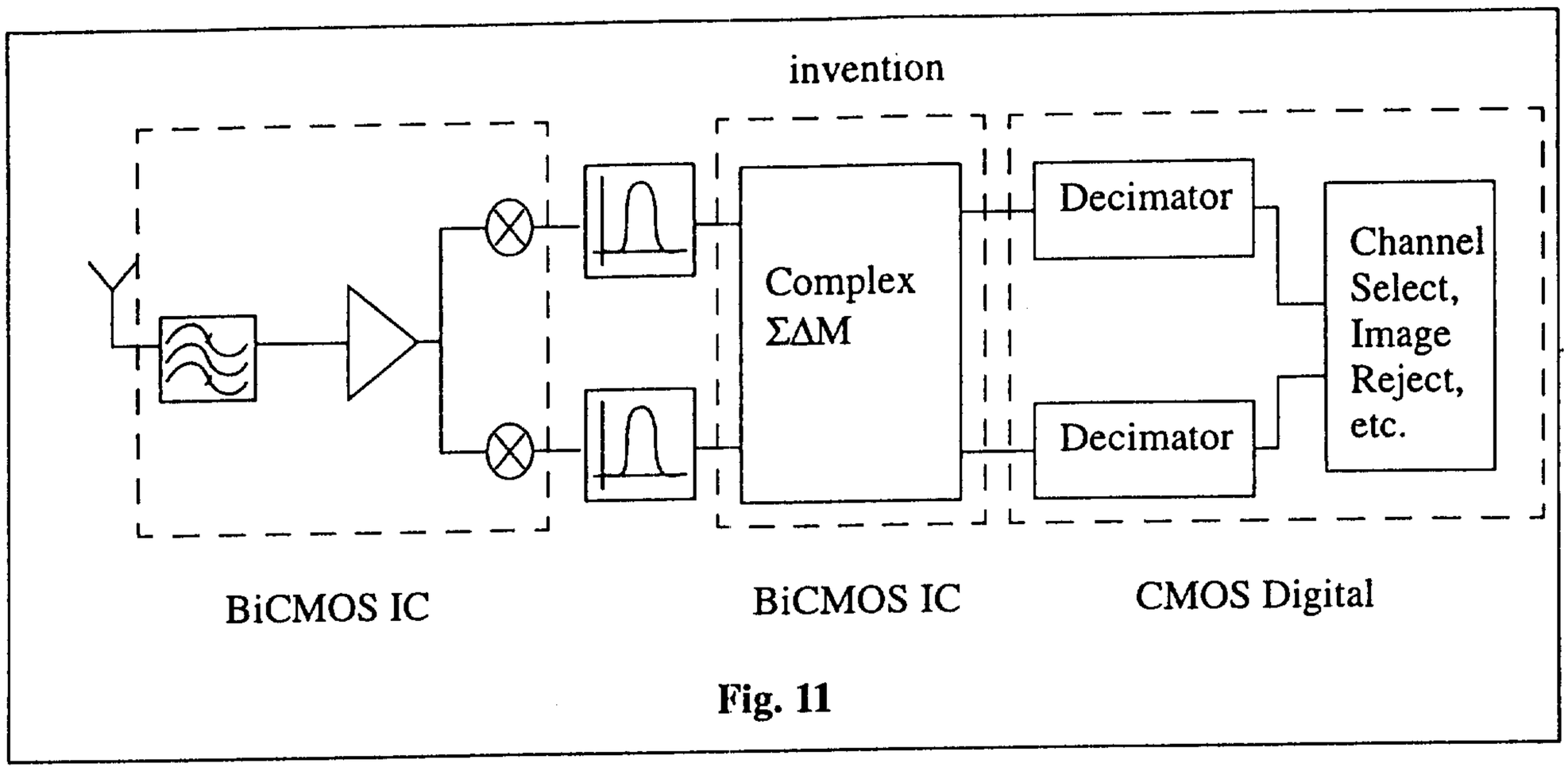

invention
Complex
ΣΔM
Decimator
Channel
Select,
Image
Reject,
etc.
Decimator
BiCMOS IC
BiCMOS IC
CMOS Digital

Fig. 11