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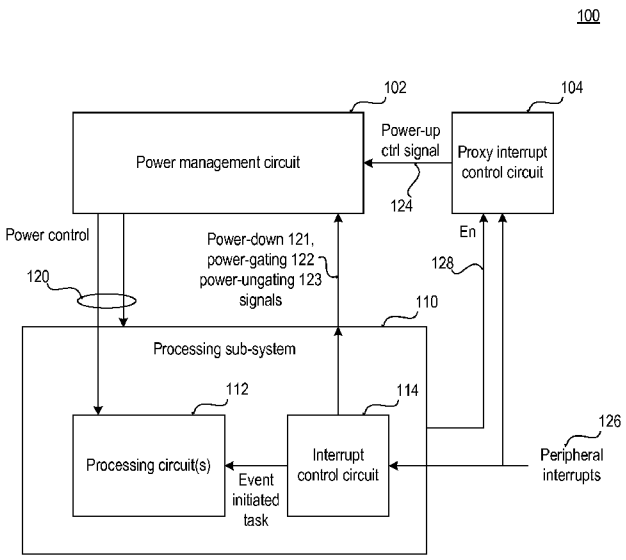

FIG. 1

(57) Abstract: An apparatus is disclosed that includes a processing sub-system (110/240) having a plurality of processor circuits and an interrupt control circuit. The interrupt control circuit (114/242) is configured to, in response to a peripheral interrupt, initiate performance of a task indicated by the peripheral interrupt by at least one of the plurality of processor circuits. The processing sub-system (110/240) is configured to generate a power-down control signal in response to suspension of the plurality of processor circuits. A power management circuit disables power to the processing sub-system (110/240), including the interrupt control circuit, in response to the power-down control signal. The power management circuit enables power to the processing sub-system (1 10/240) in response to a power-up control signal. The apparatus also includes a proxy interrupt control circuit (104/220) configured to generate the power-up control signal in response to receiving a peripheral interrupt and power to the processing sub-system (110/240) being disabled.

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SUB-SYSTEM POWER MANAGEMENT CONTROL

FIELD OF THE INVENTION

The disclosure generally relates to power management control of circuits.

BACKGROUND

Programmable integrated circuits (ICs) are devices that can be programmed to perform specified logic functions. One type of programmable IC, the field programmable gate array (FPGA), typically includes an array of programmable tiles. These programmable tiles comprise various types of logic blocks, which can include, for example, input/output blocks (IOBs), configurable logic blocks (CLBs), dedicated random access memory blocks (BRAM), multipliers, digital signal processing blocks (DSPs), processors, clock managers, delay lock loops (DLLs), bus or network interfaces such as Peripheral Component Interconnect Express (PCIe) and Ethernet and so forth.

Each programmable tile typically includes both programmable interconnect and programmable logic. The programmable interconnect typically includes a large number of interconnect lines of varying lengths interconnected by programmable interconnect points (PIPs). The programmable logic implements the logic of a user design using programmable elements that can include, for example, function generators, registers, arithmetic logic, and so forth.

The programmable interconnect and programmable logic are typically programmed by loading a stream of configuration data into internal configuration memory cells that define how the programmable elements are configured. The configuration data can be read from memory (*e.g.*, from an external PROM) or written into the FPGA by an external device. The collective states of the individual memory cells then determine the function of the FPGA.

Some programmable ICs include an embedded processor that is capable of executing program code. The processor can be fabricated as part of the same die that includes the programmable logic circuitry and the programmable interconnect circuitry, also referred to collectively as the “programmable circuitry” of the IC. It should be appreciated that execution of program code within a processor is distinguishable from “programming” or “configuring” the programmable circuitry that may be available on an IC. The act of programming

or configuring the programmable circuitry of an IC results in the implementation of different physical circuitry as specified by the configuration data within the programmable circuitry.

SUMMARY

An apparatus is disclosed that includes a processing sub-system and a power management sub-circuit. The processing sub-system includes a plurality of processor circuits and an interrupt control circuit. The interrupt control circuit is configured to, in response to a peripheral interrupt, initiate performance of a task indicated by the peripheral interrupt by at least one of the plurality of processor circuits. The processing-sub-system is configured to generate a power-down control signal in response to suspension of the plurality of processor circuits. The power management circuit disables power to the processing sub-system, including the interrupt control circuit, in response to the power-down control signal. The power management circuit enables power to the processing sub-system in response to a power-up control signal. The apparatus also includes a proxy interrupt control circuit configured to generate the power-up control signal in response to receiving a peripheral interrupt and power to the processing sub-system being disabled.

A system is also disclosed. The system includes a first sub-system having a shared circuit, a plurality of processor circuits, and an interrupt control circuit. The processor circuits are configured to perform one or more operations using the shared circuit. In response to a peripheral interrupt, the interrupt control circuit initiates performance of a task indicated by the peripheral interrupt by at least one of the plurality of processor circuits. The first sub-system is configured to generate a power-down control signal in response to suspension of the plurality of processor circuits. The system also includes a second sub-system having circuits configured to perform one or more operations using the shared circuit. The system also includes a third sub-system having a power management circuit and a proxy interrupt control circuit. The power management circuit disables power to the first sub-system, including the interrupt control circuit, in response to the power-down control signal and the shared circuit being unused by the first and second sub-systems. The power management circuit also enables power to the first sub-system in response to

the power-up control signal. The proxy interrupt control circuit generates the power-up control signal in response to receiving a peripheral interrupt and power to the first sub-system being disabled.

A method for operating a power management circuit is also disclosed. Using the power management circuit, power is provided to a first sub-system and a second sub-system. The second sub-system is configured to perform one or more operations using a shared circuit of the first sub-system. In response to a power-down request signal from the first sub-system, power is continued to be provided to the first sub-system while the shared circuit is being unused by the second sub-system. In response to the shared circuit being unused by the second sub-system, power is removed from the first sub-system.

Other features will be recognized from consideration of the Detailed Description and Claims, which follow.

BRIEF DESCRIPTION OF THE DRAWINGS

Various aspects and features of the disclosed methods and circuits will become apparent upon review of the following detailed description and upon reference to the drawings in which:

FIG. 1 shows a first device having an application processing circuit, power management circuit and proxy interrupt control circuit, consistent with one or more implementations;

FIG. 2 shows a second device having an application processing circuit, power management circuit and proxy interrupt control circuit, consistent with one or more implementations;

FIG. 3 shows a system, in accordance with one or more implementations;

FIG. 4 shows a process for controlling power of individual sub-systems, consistent with one or more implementations;

FIG. 5 shows example processes performed by an interrupt controller, proxy interrupt controller, and power management circuit, consistent with one or more implementations; and

FIG. 6 shows a programmable IC that may be configured consistent with one or more implementations.

DETAILED DESCRIPTION OF THE DRAWINGS

Some processing sub-systems include multiple processors that may be suspended or powered down when idle to save power. Processing sub-systems typically include other circuits that continue to consume power while processors are suspended. These circuits are generally not powered down because they are needed for various tasks. For example, a processing sub-system may include circuits, such as a memory controller, that are shared with other sub-systems. As another example, processing sub-systems typically include an interrupt controller configured to wake a suspended processor when a task for the processor is initiated by an interrupt. Because the interrupt controller is needed to wake the suspended processors, it cannot be powered down when processors are suspended.

Circuits and methods are disclosed that enable an entire processing sub-system to be powered down—thereby reducing power consumption. In some implementations, a system includes a processing sub-system having a set of processors and an interrupt control circuit. A power management circuit is configured to disable power to the processing sub-system circuit (including the interrupt controller) when unused. In some implementations, the processing sub-system provides a power-down request signal to the power management circuit when all of the processors have been suspended for a threshold period of time. The system includes a proxy-interrupt controller that is powered independent of the processing sub-system. The proxy-interrupt controller is configured to cause the power management circuit to enable power to the processing sub-system in response to an interrupt.

In some implementations, the processing sub-system includes one or more circuits that are shared with at least one other sub-system. The power management circuit is configured to only disable power to the processing sub-system circuit after the power-down request signal has been received and a power-down authorization signal has been received by each of the other sub-systems that uses the shared circuits of the processing sub-system.

In the following description, numerous specific details are set forth to describe specific examples presented herein. It should be apparent, however, to one skilled in the art, that one or more other examples and/or variations of these examples may be practiced without all the specific details given below. In other

instances, well known features have not been described in detail so as not to obscure the description of the examples herein. For ease of illustration, the same reference numerals may be used in different diagrams to refer to the same items; however, in alternative examples the items may be different.

Turning now to the figures, FIG. 1 shows a first device 100 having a processing sub-system, a power management circuit, and a proxy interrupt control circuit, in accordance with one or more implementations. The processing sub-system 110 includes one or more processing circuit(s) 112 and an interrupt control circuit 114. The interrupt control circuit 114 is configured to monitor peripheral interrupts 126 and initiate tasks on the processing circuit(s) 112 in response thereto. Interrupts may trigger a number of various processes. As one example, a hardware device connected to the system may generate an interrupt to read data values stored in a memory of the system.

The power management circuit 102 provides power control signals 120 to adjust power consumption of the processing sub-system 110 in response to control signals 121, 122, 123, and 124. The control signals may include, for example, a power-down control signal 121, a power-gating control signal 122, a power ungating control signal 123, and power-up control signals 124.

The power management circuit 102 is configured to suspend/resume various ones of the processing circuit(s) 112 in response to power-gating/power-ungating control signals received from the processing sub-system 110. The power management circuit 102 is configured to disable power to the processing sub-system 110 (including the interrupt control circuit 114) in response to the power-down control circuit. The power management circuit 102 is also configured to enable power to the processing sub-system 110 in response to a power-up control signal 124. For instance, an interrupt may be received that requires action by the processing circuits. However, as indicated above, while power to the processing sub-system 110 is disabled, the interrupt control circuit 114 is not available to monitor peripheral interrupts.

Proxy interrupt control circuit 104 is configured to monitor for peripheral interrupts when power to the processing sub-system is disabled. The proxy interrupt control circuit 104 is configured to generate the power-up control signal 124 in response to a peripheral interrupt for one of the processing circuits 112.

In response to the power-up control signal, the power management circuit 102 enables power to the processing sub-system 110.

In some implementations, the proxy interrupt controller is enabled/disabled according to an enable signal 128 provided by the processing sub-system. Alternatively, the enable signal 128 may be provided by the power management circuit. In some embodiments, the proxy control circuit is configured to monitor the control signals 121, 122, and 123 provided to the power management circuit to determine when the processing sub-system is being disabled.

In some implementations, the power management circuit may be adapted to control power for multiple sub-systems. FIG. 2 shows a second device having processing sub-systems, a power management circuit, and a proxy interrupt control circuit, in accordance with one or more implementations. The device 200 includes a first processing sub-system 210, a power management circuit 202, and a proxy interrupt control circuit 204 similar to the processing sub-system 110, power management circuit 102, and proxy interrupt control circuit 104 described with reference to in FIG. 1. In this example, the device 200 also includes a second processing sub-system 230.

Each of the processing sub-systems 210 and 230 includes a respective set of processing circuits 212 and 232 and a respective interrupt control circuit 214 and 234 configured to monitor peripheral interrupts 226 and initiate tasks on the processing circuit(s) 212 and/or 232 in response thereto.

The power management circuit 202 provides power control signals 220 and 238 to adjust power consumption of the processing sub-systems 210 and 230 in response to sets of control signals 222 and 236 received from the processing sub-systems. Each set of control signals 222 and 236 may include, for example, power-down/power-gating and power-up/power-ungating control signals. The power management circuit 202 is configured to suspend/resume various ones of the processing circuit(s) 212 and 232 in response to power-gating/power-ungating signals received from the respective processing sub-system. The power management circuit 202 is configured to disable power to the processing sub-system 210 in response to the power-down control signal from processing sub-system 210 and disable power to the processing sub-system 230 in response to the power-down control signal from processing sub-

system 230. The power management circuit 202 also enables power to one of the processing sub-systems 210 or 230 in response to a power-up control signal 224 indicative of the one of the processing sub-systems 210 or 230.

Proxy interrupt control circuit 204 monitors for peripheral interrupts when power is disabled for either of the processing sub-systems 210 and 230. The proxy interrupt controller may be enabled, for example, by an enable control signal 228 asserted prior to one of the processing sub-systems 210 and 230 powering down. In response to a peripheral interrupt to a powered-down one of the processing sub-systems, the proxy interrupt control circuit 204 generates a power-up control signal to cause the power management circuit 202 to power up the processing sub-system.

FIG. 3 shows a system, in accordance with one or more implementations. The system 300 includes a first sub-system 330, a second sub-system 380, and a third sub-system 310. The first sub-system 330 has a multi-core processor 344 and an interrupt control circuit 342. In this example, the multi-core processor 344 includes four processing cores 346, 348, 350, and 352. In response to a peripheral interrupt, the interrupt control circuit 342 is configured to initiate performance of a task by one of the processing cores via control signals 354. The interrupt control circuit 342 also generates a power-down control signal 371 in response to all of the processing cores being suspended.

The first sub-system 330 includes one or more circuits 360 that are shared by other sub-systems of the system 300 via connections 364. For example, the second sub-system 380 of the system 300 may include circuitry configured to perform one or more operations using the shared circuit 360 of the first sub-system. In some implementations, the second sub-system includes programmable logic circuits that may be configured, in certain applications, to access a memory of the system (not shown) via a shared memory controller (*e.g.*, 360) included in the first sub-system.

The third sub-system 310 includes a power management circuit 320 configured to adjust power consumption of the first sub-system. In this example, the first-sub-system 330 operates in a separate power domain from the second sub-system 380 and third sub-system 310 and may be powered down independently by the third sub-system 310.

In some implementations, the system 300 is configured to operate in a full-power mode and a low-power mode. When operated in the full-power mode, each of the power domains is powered up. When operated in the low-power mode, the power domain of the first sub-system is powered down. The power domain of the second and third sub-systems remains powered up when the system 300 is operated in the low power mode. Because the power domain of the first sub-system is powered down, in the low power mode, less power is consumed. For ease of reference, the power domain used to power the first sub-system may be referred to as the "full power domain" and the power domain used to power the third sub-system may be referred to as the "low-power domain." The full power domain is only powered up when the system 300 is operated in the full-power mode. The low power domain is the only power domain powered up when the system 300 is operated in the low–power mode.

In this example, the third sub-system 310 includes a power management circuit 320 configured to adjust power consumption of the first sub-system 330 via power control signals 370, in response to control signals 371, 372, and 373 from the first sub-system 330. For example, the power management circuit 320 may disable power to the first sub-system, including the interrupt control circuit, in response to the power-down control signal and the shared circuit 360 being unused by the second and third sub-systems 380 and 310. For instance, in some embodiments, the first sub-system 330 includes a memory controller for controlling access to a memory (not shown). Various circuits of the second sub-system 380 and third sub-system 310 may access the memory via the memory controller. In this example, the third sub-system includes a processing unit 324 including processing cores 326 and 327 and a respective interrupt control circuit 325. The processing cores 326 and 327 may access the memory via the shared memory controller of the first-sub-system.

In this example, the power management circuit 320 is configured to only power-down the first sub-system 330 after other sub-systems which use the shared circuit 360 provide authorization signals indicating that the shared circuit is not in use. In this example, the second sub-system provides authorization signal 312 to the power management circuit 320 when the shared circuit 360 is not needed by the second sub-system. Similarly, processing unit 324 provides authorization signal 314 to the power management circuit 320 when the shared

circuit 360 is not needed by the processing unit 324. In some other implementations, the first sub-system is configured to receive the authorization signals and generate the power-down control signal only if the authorization signals indicate that the shared circuit 360 is unused.

The power management circuit 320 enables power to the first sub-system in response to a power-up control signal 374. The power-up control signal 374 is generated by a proxy interrupt control circuit 322, in response to receiving a peripheral interrupt 378 corresponding to the first sub-system while the proxy interrupt control circuit 322 is enabled by an enable control signal 376.

In this example, the power management circuit 320 is also configured to suspend/awaken various cores 346, 348, 350, and 352 of the multi-core processor 344 in response to receiving the power-gating control signal 372 or power-ungating control signals 373 from the first sub-system. The first sub-system generates the gating control signals to suspend one or more of the processing cores that have been idle for a threshold period of time. The first sub-system generates the ungating control signals to wake suspended processing cores when needed for processing in response to an interrupt from a peripheral device or another sub-system. The sub-systems of the system 300 may also include various other circuits, in addition to those discussed above, which may or may not be shared with other sub-systems. For instance, in this example, the first and third sub-systems include communication I/O circuits 362 and 364, respectively. In another implementation, the communication I/O circuit 362 may be shared with the third sub-system 310 and the communication I/O circuit 364 may be omitted. If the first sub-system includes multiple shared circuits, the first-sub-system is not powered down by the power management circuit 320 unless each of the shared circuits is unused.

FIG. 4 shows a process for controlling power of individual sub-systems, in accordance with one or more implementations. At system boot 402, if a full power domain is disabled, decision block 404 directs the process to enable the full power (FP) domain at block 406 using a power management circuit.

As discussed with reference to FIG. 3, the full power domain may be used to power a first sub-system including a processing circuit having a plurality of processing cores. After powering up the full power domain, a default processing core of the first sub-system may be awakened at block 410 (if needed). For

instance, in some implementations, one processing core may be designated to wake at startup in case it is needed for processing. The processing circuit is active at block 408. When a processing core is idle and ready to be suspended, the processing core is suspended using a power management circuit at block 412.

At decision block 414, if one or more of the processing cores of the processing circuit are not suspended, the processing circuit continues to operate in the active state at block 408. Otherwise, if all of the processing cores of the processing circuit are suspended, it is possible that the full power domain may be powered down to save power. If all of the processing cores are suspended at decision block 416, the process is directed to decision block 420. The process repeats decision block 420 while a shared memory controller (MC) of the first sub-system is needed by other sub-systems to access a memory. If a shared memory controller is not needed by other sub-systems, for example, the process may place a memory in self-refresh mode at block 422 to save additional power. At block 418, the full-power domain that powers the first-sub-system is powered down by a the power management circuit.

The full-power domain remains powered down until a peripheral interrupt corresponding to the first sub-system is received at decision block 414. In response to the peripheral interrupt, the full-power domain is powered up with the power management circuit at block 406 and the process is repeated. If a specific processing core is required to process the peripheral interrupt, the process wakes the processing core at block 410.

FIG. 5 shows processes performed by an interrupt controller, proxy interrupt controller, and power management circuit in an example implementation. At system boot 502, the power management circuit is initially in an idle state 530 and the proxy interrupt controller is initially in idle state 520. The interrupt control circuit initiates power-on of the processor(s) in state 506 by directing the power management circuit to power up the full-power domain in state 534. After which, the power management circuit returns to the idle state 530

In response to a peripheral interrupt, the interrupt control circuit transitions to state 504 where it schedules a task indicated by the peripheral interrupt. If required, the interrupt control circuit may also wake a suspended processor in

state 504, for example, by generating a power ungating signal. In response to the power ungating signal, the power management circuit wakes the processor indicated by the power ungating signal at state 536 and then returns to the idle state.

If a processor is idle for a threshold period of time, a power-gating signal is generated at state 510 to cause the idle processor to be powered down. In some implementations, the power-gating signal may be generated by one of the processors. In some other implementations, the power-gating signal may be generated by another control circuit, such as the interrupt control circuit. In response to the power-gating signal, the power management circuit transitions to state 538, where it suspends the processor indicated by the power-gating signal. After suspending the processor, the power management circuit, returns to the idle state 530.

In response to a power-down request signal, the processing sub-system transitions to state 512 where it waits to be powered down. The power management circuit transitions to state 531, where it prompts circuits, which use shared circuits, for authorization to power-down. In response to receiving authorization signals from each sub-system that uses the shared circuits, the power management circuit enables the proxy interrupt controller and powers down the full power domain (FPD) at state 532. After which, the power management circuit returns to the idle state 530 and the processing sub-circuit transitions to the powered down state 508.

When enabled, the proxy interrupt control circuit monitors peripheral interrupts at state 522. In response to a peripheral interrupt for one of the processors powered by the full-power domain, the proxy interrupt control circuit generates a power up control signal at state 524. In response to the power-up control signal, the power management circuit powers up the full power domain in state 534 and then returns to the idle state 530. After the full power domain is powered up, the proxy interrupt control circuit transitions to the idle/disabled state 520 and the interrupt control circuit transitions back to state 506.

FIG. 6 shows a programmable IC 602 that may be configured in accordance with one or more implementations. The programmable IC may also be referred to as a System On Chip (SOC), which includes a processing sub-system 610 and a programmable logic sub-system 630. The processing sub-

system 610 may be programmed to implement a software portion of the user design, via execution of a user program. The program may be specified as part of a configuration data stream or may be retrieved from an on-chip or off-chip data storage device. The processing sub-system 610 may include various circuits 612, 614, 616, and 618 for executing one or more software programs. The circuits 612, 614, 616, and 618 may include, for example, one or more processor cores, floating point units (FPUs), an interrupt processing unit, on chip-memory, memory caches, and/or cache coherent interconnect.

The programmable logic sub-system 630 of the programmable IC 602 may be programmed to implement a hardware portion of a user design. For instance, the programmable logic sub-system may include a number of programmable resources 632, which may be programmed to implement a set of circuits specified in a configuration data stream. The programmable resources 632 include programmable interconnect circuits, programmable logic circuits, and configuration memory cells. The programmable logic implements the logic of a user design using programmable elements that can include, for example, function generators, registers, arithmetic logic, and so forth. Programmable interconnect circuits may include a large number of interconnect lines of varying lengths interconnected by programmable interconnect points (PIPs).

The programmable resources 632 may be programmed by loading a configuration data stream into the configuration memory cells, which define how the programmable interconnect circuits and programmable logic circuits are configured. The collective states of the individual memory cells then determine the function of the programmable resources 632. The configuration data can be read from memory (*e.g.*, from an external PROM) or written into the programmable IC 602 by an external device. In some implementations, configuration data may be loaded into configuration memory cells by a configuration controller 634 included in the programmable logic sub-system 630. In some other implementations, the configuration data may be loaded into the configuration memory cells by a start-up process executed by the processor sub-system 610.

The programmable IC 602 may include various circuits to interconnect the processing sub-system 610 with circuitry implemented within the programmable logic sub-system 630. In this example, the programmable IC 602 includes a

core switch 626 that can route data signals between various data ports of the processing sub-system 610 and the programmable logic sub-system 630. The core switch 626 may also route data signals between either of the programmable logic or processing sub-systems 610 and 630 and various other circuits of the programmable IC, such as an internal data bus. Alternatively or additionally, the processing sub-system 610 may include an interface to directly connect with the programmable logic sub-system—bypassing the core switch 626. Such an interface may be implemented, for example, using the AMBA AXI Protocol Specification (AXI) as published by ARM.

In some implementations, the processing sub-system 610 and the programmable logic sub-system 630 may also read or write to memory locations of an on-chip memory 622 or off-chip memory (not shown) via memory controller 621. The memory controller 621 can be implemented to communicate with one or more different types of memory circuits including, but not limited to, Dual Data Rate (DDR) 2, DDR3, Low Power (LP) DDR2 types of memory, whether 16-bit, 32-bit, 16-bit with ECC, etc. The list of different memory types with which memory controller 621 is able to communicate is provided for purposes of illustration only and is not intended as a limitation or to be exhaustive. As shown in FIG. 6, the programmable IC 602 may include a memory management unit 620 and translation look-aside buffer 624 to translate virtual memory addresses used by the sub-systems 610 and 630 to physical memory addresses used by the memory controller 621 to access specific memory locations.

The programmable IC may include an input/output (I/O) sub-system 650 for communication of data with external circuits. The I/O sub-system 650 may include various types of I/O devices or interfaces including for example, flash memory type I/O devices, higher performance I/O devices, lower performance interfaces, debugging I/O devices, and/or RAM I/O devices.

The I/O sub-system 650 may include one or more flash memory interfaces 660 illustrated as 660A and 660B. For example, one or more of flash memory interfaces 660 can be implemented as a Quad-Serial Peripheral Interface (QSPI) configured for 4-bit communication. One or more of flash memory interfaces 660 can be implemented as a parallel 8-bit NOR/SRAM type of interface. One or more of flash memory interfaces 660 can be implemented as a NAND interface configured for 8-bit and/or 16-bit communication. It should

be appreciated that the particular interfaces described are provided for purposes of illustration and not limitation. Other interfaces having different bit widths can be used.

The I/O sub-system 650 can include one or more of interfaces 662 providing a higher level of performance than memory interfaces 660. Each of interfaces 662A-662C can be coupled to a DMA controller 664A-664C respectively. For example, one or more of interfaces 662 can be implemented as a Universal Serial Bus (USB) type of interface. One or more of interfaces 662 can be implemented as a gigabit Ethernet type of interface. One or more of interfaces 662 can be implemented as a Secure Digital (SD) type of interface.

The I/O sub-system 650 may also include one or more interfaces 666 such as interfaces 666A-666D that provide a lower level of performance than interfaces 662. For example, one or more of interfaces 666 can be implemented as a General Purpose I/O (GPIO) type of interface. One or more of interfaces 666 can be implemented as a Universal Asynchronous Receiver/Transmitter (UART) type of interface. One or more of interfaces 666 can be implemented in the form of a Serial Peripheral Interface (SPI) bus type of interface. One or more of interfaces 666 can be implemented in the form of a Controller-Area-Network (CAN) type of interface and/or an I^2C type of interface. One or more of interfaces 666 also can be implemented in the form of a Triple Timer Counter (TTC) and/or a Watchdog Timer (WDT) type of interface.

The I/O sub-system 650 can include one or more debug interfaces 668 such as processor JTAG (PJTAG) interface 668A and a trace interface 668B. PJTAG interface 668A can provide an external debug interface for the programmable IC 602. Trace interface 668B can provide a port to receive debug, e.g., trace, information from the processing sub-system 610 or the programmable logic sub-system 630.

As shown, each of interfaces 660, 662, 666, and 668 can be coupled to a multiplexer 670. Multiplexer 670 provides a plurality of outputs that can be directly routed or coupled to external pins of the programmable IC 602, e.g., balls of the package within which the programmable IC 602 is disposed. For example, I/O pins of programmable IC 602 can be shared among interfaces 660, 662, 666, and 668. A user can configure multiplexer 670, via a configuration data stream to select which of interfaces 660-668 are to be used and, therefore,

coupled to I/O pins of programmable IC 602 via multiplexer 670. The I/O sub-system 650, may also include a fabric multiplexer I/O (FMIO) interface (not shown) to connect interfaces 662-668 to programmable logic circuits of the programmable logic sub-system. Additionally or alternatively, the programmable logic sub-system 630 can be configured to implement one or more I/O circuits within programmable logic. In some implementations, the programmable IC 602 may also include a sub-system 640 having various circuits for power and/or safety management. For example, the sub-system 640 may include a power management unit 646 configured to monitor and maintain one or more voltage domains used to power the various sub-systems of the programmable IC 602. In some implementations, the power management unit 646 may disable power of individual sub-systems, when idle, to reduce power consumption, without disabling power to sub-systems in use.

The sub-system 640 may also include safety circuits to monitor the status of the sub-systems to ensure correct operation. For instance, the sub-system 640 may include one or more real-time processors 642 configured to monitor the status of the various sub-systems (*e.g.,* as indicated in status registers 644). The real-time processors 642 may be configured to perform a number of tasks in responses to detecting errors. For example, for some errors, the real-time processors 642 may generate an alert in response to detecting an error. As another example, the real-time processors 642 may reset a sub-system to attempt to restore the sub-system to correct operation. The sub-system 640 includes a switch network 648 that may be used to inter connect various sub-systems. For example, the switch network 648 may be configured to connect the various sub-systems 610, 630, and 640 to various interfaces of the I/O sub-system 650. In some applications, the switch network 648 may also be used to isolate the real-time processors 642 from the sub-systems that are to be monitored. Such isolation may be required by certain application standards (*e.g.*, IEC-61508 SIL3 or ISO-26262 standards) to ensure that the real-time processors 642 are not affected by errors that occur in other sub-systems.

The disclosure generally relates to power management control of circuits.

For example, an apparatus may be disclosed that includes a processing sub-system and a power management sub-circuit. Such an apparatus may include: a processing sub-system, including: a plurality of processor circuits; and an interrupt control circuit configured to, in response to a peripheral interrupt, initiate performance of a task indicated by the peripheral interrupt by at least one of the plurality of processor circuits, wherein the processing sub-system is configured to generate a power-down control signal in response to suspension of the plurality of processor circuits; a proxy interrupt control circuit configured and arranged to generate a power-up control signal in response to receiving a peripheral interrupt and power to the processing sub-system being disabled; and a power management circuit configured and arranged to: disable power to the processing sub-system, including the interrupt control circuit, in response to the power-down control signal; and enable power to the processing sub-system in response to the power-up control signal.

In some such apparatus, the processing sub-system is further configured to, in response to one of the plurality of processor circuits being idle for a threshold period of time, suspend the one of the processor circuits.

In some such an apparatus, the processing sub-system is configured to suspend the one of the plurality of processor circuits by generating a first power-gating control signal; and the power management circuit is configured to disable power to the one of the plurality of processor circuits in response to the first power-gating control signal.

In some such apparatus, the processing sub-system is further configured to, in response to suspension of the plurality of processor circuits, enable the proxy interrupt control circuit prior to generating the power-down control signal.

In some such apparatus, the interrupt control circuit is configured and arranged to generate the power-down control signal in response to an input control signal.

In some such apparatus, the interrupt control circuit is configured to generate the power-down control signal in response to the suspension of the plurality of processor circuits.

In some such apparatus, one of the plurality of processor circuits is configured to generate the power-down control signal in response to the suspension of the plurality of processor circuits.

A system is also disclosed.

Such a system may include: a first sub-system including: a shared circuit; a plurality of processor circuits configured to perform one or more operations using the shared circuit; and an interrupt control circuit configured to: in response to a peripheral interrupt, initiate performance of a task indicated by the peripheral interrupt by at least one of the plurality of processor circuits, wherein the first sub-system is configured to generate a power-down control signal in response to suspension of the plurality of processor circuits; a second sub-system including a circuit configured to perform one or more operations using the shared circuit; and a third sub-system including: a proxy interrupt control circuit configured and arranged to generate a power-up control signal in response to receiving a peripheral interrupt and power to the first sub-system being disabled; and a power management circuit configured and arranged to: disable power to the first sub-system, including the interrupt control circuit, in response to the power-down control signal and the shared circuit being unused by the first and second sub-systems; and enable power to the first sub-system in response to the power-up control signal.

In some such system, the second sub-system is configured to, in response to the shared circuit being unused by the second sub-system, provide a respective power-down authorization signal to the power management circuit.

In some such system, the second sub-system includes programmable logic circuits.

In some such system, the shared circuit includes a memory controller; and the plurality of processor circuits and the second sub-system are each configured to access a memory using the memory controller.

In some such system, the third sub-system includes a circuit configured to access the memory using the memory controller of the first sub-system.

In some such system, the first sub-system is further configured to, in response to one of the plurality of processor circuits being idle for a threshold period of time, suspend the one of the plurality of processor circuits.

In some such system, the first sub-system is configured to suspend the one of the plurality of processor circuits by generating a first power-gating control signal; and the power management circuit is configured to disable power to the

one of the plurality of processor circuits in response to the first power-gating control signal.

In some such system, the power management circuit is further configured to enable power to the one of the plurality of processor circuits in response to a second power-ungating control signal.

In some such system, the interrupt control circuit is further configured to enable the proxy interrupt control circuit prior to generating the power-down control signal.

A method for operating a power management circuit is also disclosed.

In one example, such a method may include: using a power management circuit: providing power to a first sub-system and a second sub-system, wherein the second sub-system is configured to perform one or more operations using a shared circuit of the first sub-system; and in response to a power-down request signal from the first sub-system: continuing to provide power to the first sub-system while the shared circuit is being unused by the second sub-system; and in response to the shared circuit being unused by the second sub-system, removing power from the first sub-system.

In some such method, the method further includes: using the second sub-system, generating a power-down authorization signal in response to the power-down request signal and the shared circuit being unused by the second sub-system.

In some such method, the method further includes: using a proxy interrupt controller, monitoring a data-bus for peripheral interrupts, and generating a power-up control signal in response to the peripheral interrupt; and using the power management circuit, providing power to the first sub-system.

In some such method, the method further includes: enabling the proxy interrupt controller prior to removing power from the first sub-system; and disabling the proxy interrupt controller in response to providing power to the first sub-system.

The methods and circuits are thought to be applicable to a variety of systems and applications. Other aspects and features will be apparent to those skilled in the art from consideration of the specification. For example, though aspects and features may in some cases be described in individual figures, it will

be appreciated that features from one figure can be combined with features of another figure even though the combination is not explicitly shown or explicitly described as a combination. It is intended that the specification and drawings be considered as examples only, with a true scope of the invention being indicated by the following claims.

CLAIMS

What is claimed is:

1. An apparatus comprising:

a processing sub-system, including:

a plurality of processor circuits; and

an interrupt control circuit configured to, in response to a peripheral interrupt, initiate performance of a task indicated by the peripheral interrupt by at least one of the plurality of processor circuits, wherein the processing sub-system is configured to generate a power-down control signal in response to suspension of the plurality of processor circuits;

a proxy interrupt control circuit configured and arranged to generate a power-up control signal in response to receiving a peripheral interrupt and power to the processing sub-system being disabled; and

a power management circuit configured and arranged to:

disable power to the processing sub-system, including the interrupt control circuit, in response to the power-down control signal; and

enable power to the processing sub-system in response to the power-up control signal.

2. The apparatus of claim 1, wherein the processing sub-system is further configured to, in response to one of the plurality of processor circuits being idle for a threshold period of time, suspend the one of the processor circuits.

3. The apparatus of claim 2, wherein:

the processing sub-system is configured to suspend the one of the plurality of processor circuits by generating a first power-gating control signal; and

the power management circuit is configured to disable power to the one of the plurality of processor circuits in response to the first power-gating control signal.

4. The apparatus of any of claims 1-3, wherein the processing sub-system is further configured to, in response to suspension of the plurality of processor

circuits, enable the proxy interrupt control circuit prior to generating the power-down control signal.

5. The apparatus of claim 1, wherein the interrupt control circuit is configured and arranged to generate the power-down control signal in response to an input control signal.

6. The apparatus of claim 1, wherein the interrupt control circuit is configured to generate the power-down control signal in response to the suspension of the plurality of processor circuits.

7. The apparatus of claim 1, wherein one of the plurality of processor circuits is configured to generate the power-down control signal in response to the suspension of the plurality of processor circuits.

8. A method, comprising:
using a power management circuit:
providing power to a first sub-system and a second sub-system, wherein the second sub-system is configured to perform one or more operations using a shared circuit of the first sub-system; and
in response to a power-down request signal from the first sub-system:
continuing to provide power to the first sub-system while the shared circuit is being unused by the second sub-system; and
in response to the shared circuit being unused by the second sub-system, removing power from the first sub-system.

9. The method of claim 8, further comprising:
using the second sub-system, generating a power-down authorization signal in response to the power-down request signal and the shared circuit being unused by the second sub-system.

10. The method of claim 8, further comprising:

using a proxy interrupt controller, monitoring a data-bus for peripheral interrupts, and generating a power-up control signal in response to the peripheral interrupt; and

using the power management circuit, providing power to the first sub-system.

11. The method of claim 10, further comprising,

enabling the proxy interrupt controller prior to removing power from the first sub-system; and

disabling the proxy interrupt controller in response to providing power to the first sub-system.

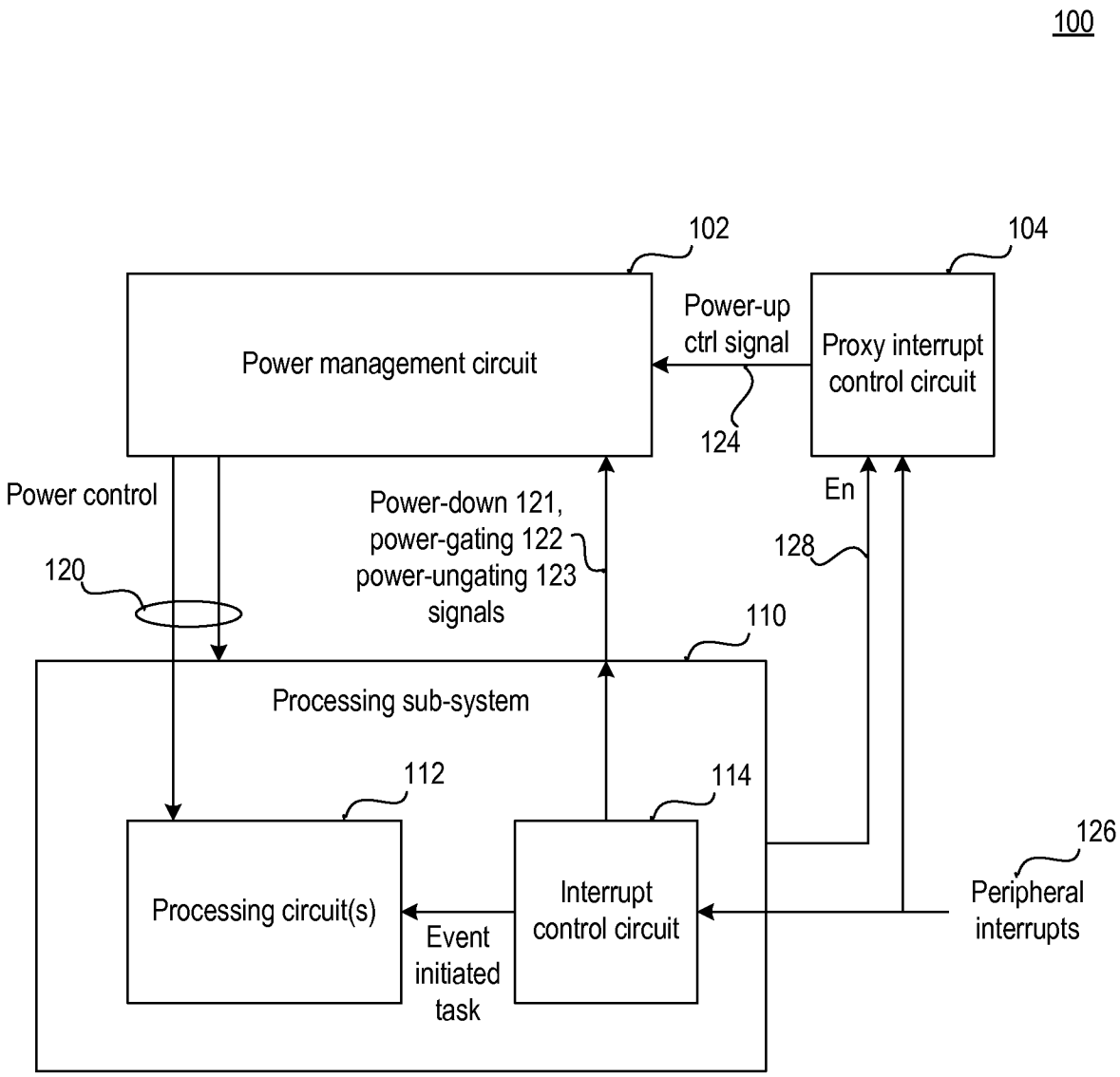
100
102
104
Power management circuit
Power-up
ctrl signal
Proxy interrupt
control circuit
124
Power control
120
Power-down 121,
power-gating 122
power-ungating 123
signals
En
128
110
Processing sub-system
112
114
126
Processing circuit(s)
Event
initiated
task
Interrupt
control circuit
Peripheral
interrupts

FIG. 1

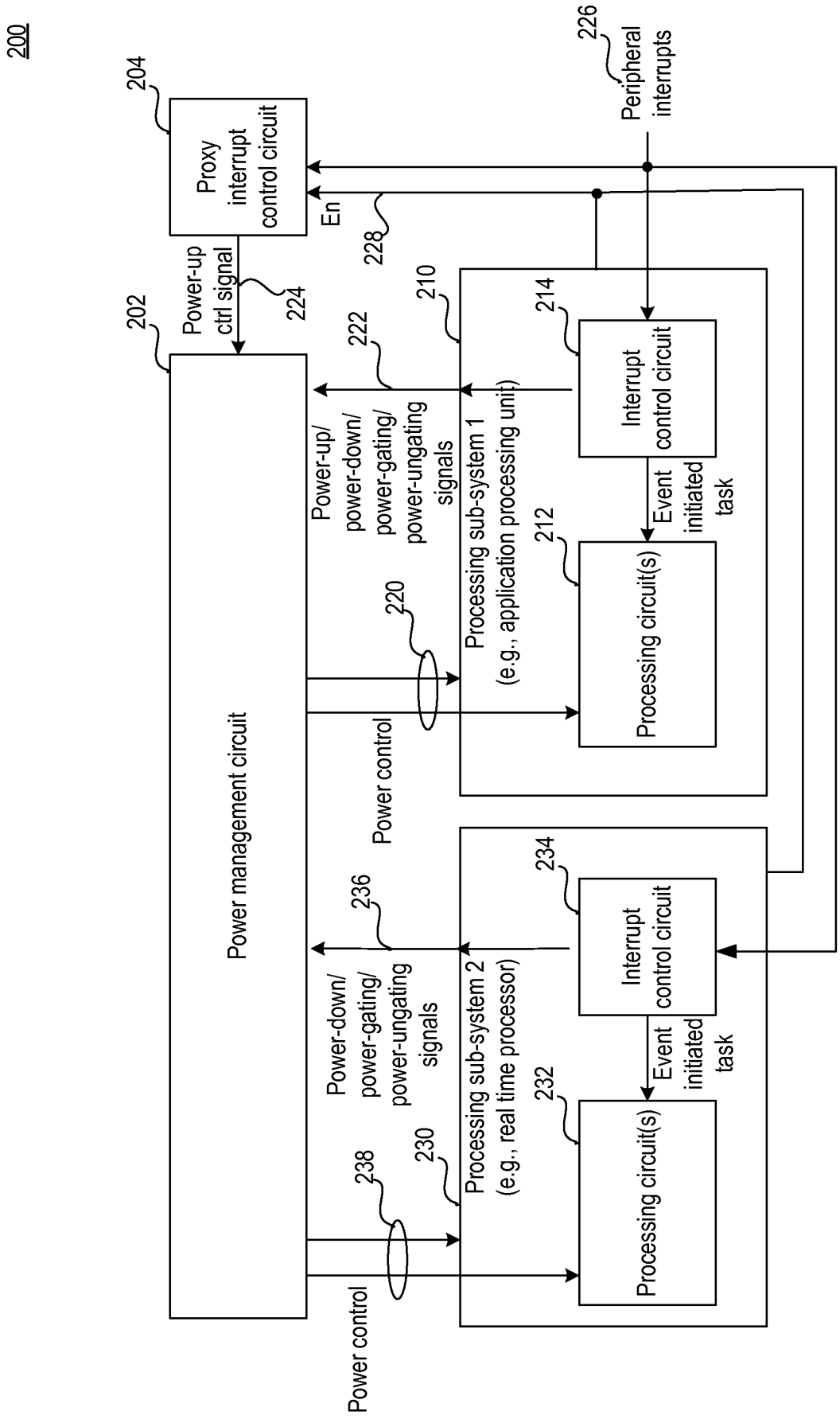
200
204
Proxy interrupt control circuit
226
Peripheral interrupts
En
228
Power-up ctrl signal
224
202
Power management circuit
222
210
214
Interrupt control circuit
Power-up/ power-down/ power-gating/ power-ungating signals
Processing sub-system 1 (e.g., application processing unit)
Event initiated task
212
Processing circuit(s)
220
Power control
234
236
Interrupt control circuit
Power-down/ power-gating/ power-ungating signals
Processing sub-system 2 (e.g., real time processor)
Event initiated task
232
Processing circuit(s)
238
230
Power control

FIG. 2

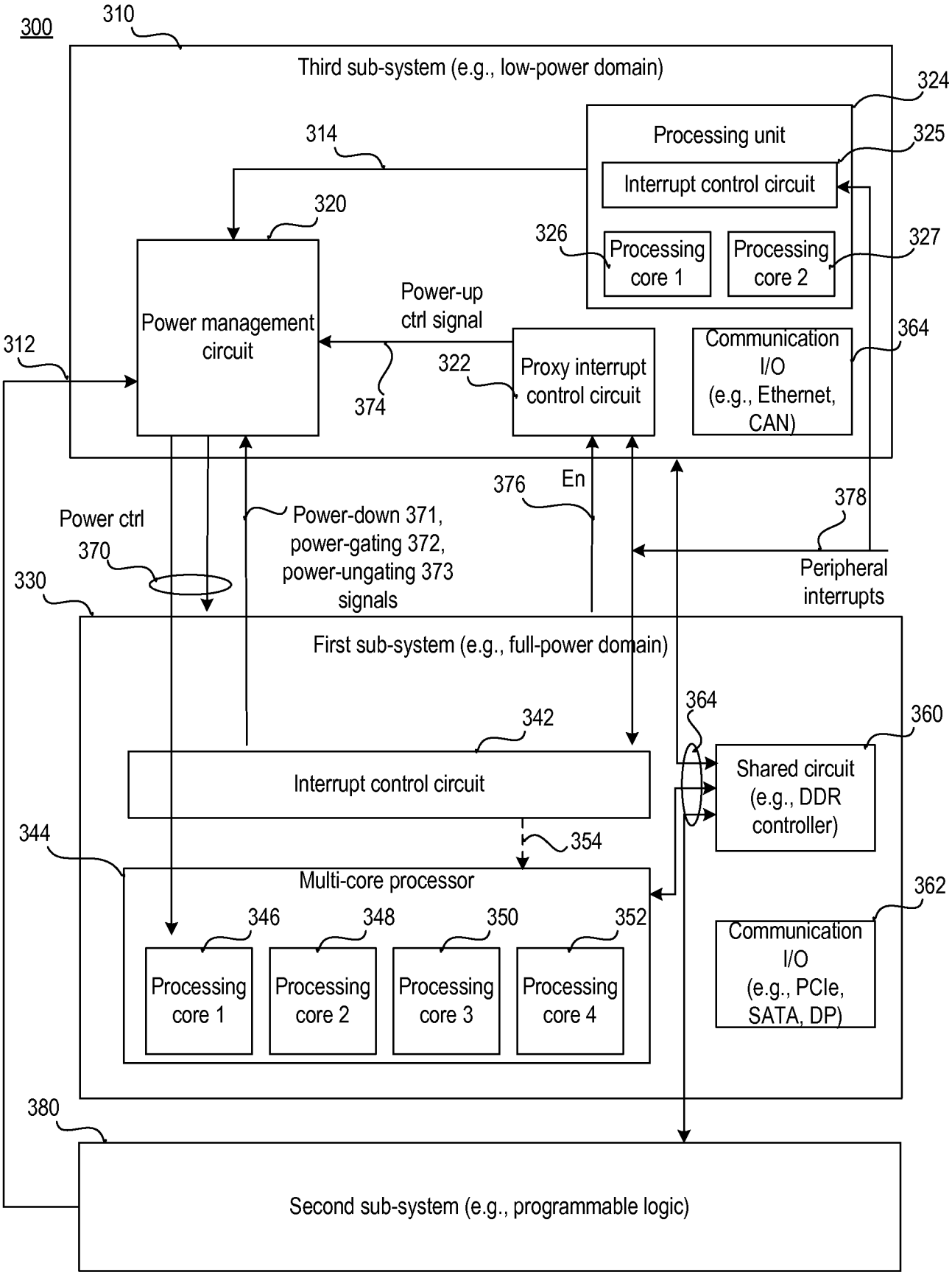
300
310
Third sub-system (e.g., low-power domain)
324
Processing unit
325
Interrupt control circuit
314
320
326
Processing core 1
Processing core 2
327
Power-up ctrl signal
Power management circuit
312
322
Proxy interrupt control circuit
374
Communication I/O (e.g., Ethernet, CAN)
364
376
En
378
Power ctrl
370
Power-down 371, power-gating 372, power-ungating 373 signals
Peripheral interrupts
330
First sub-system (e.g., full-power domain)
342
364
360
Interrupt control circuit
Shared circuit (e.g., DDR controller)
344
354
Multi-core processor
346
348
350
352
362
Processing core 1
Processing core 2
Processing core 3
Processing core 4
Communication I/O (e.g., PCIe, SATA, DP)
380
Second sub-system (e.g., programmable logic)

FIG. 3

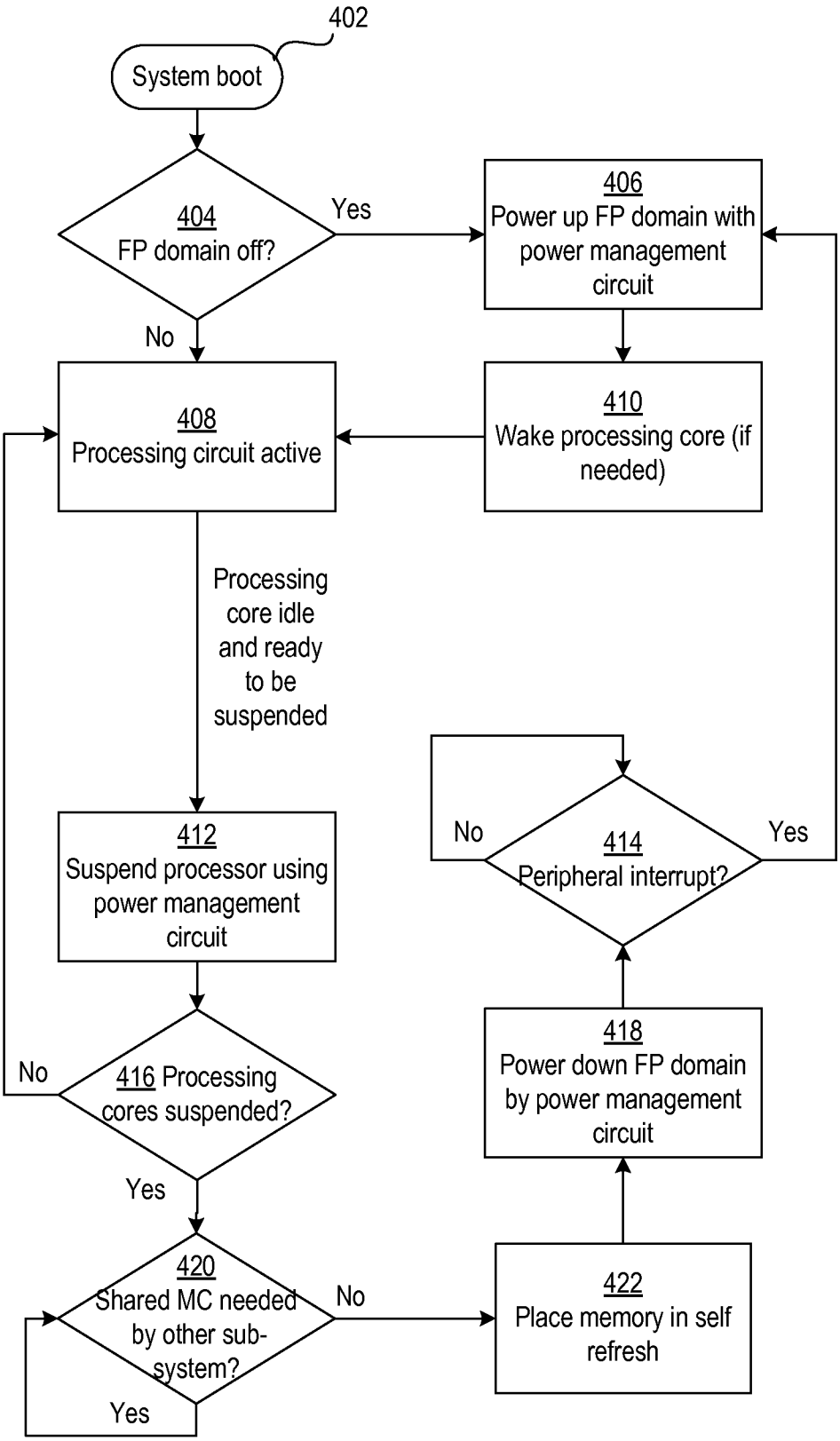
402
System boot
404
FP domain off?
Yes
No
406
Power up FP domain with power management circuit
408
Processing circuit active
410
Wake processing core (if needed)
Processing core idle and ready to be suspended
412
Suspend processor using power management circuit
414
Peripheral interrupt?
No
Yes
416 Processing cores suspended?
No
Yes
418
Power down FP domain by power management circuit
420
Shared MC needed by other sub-system?
No
Yes
422
Place memory in self refresh

FIG. 4

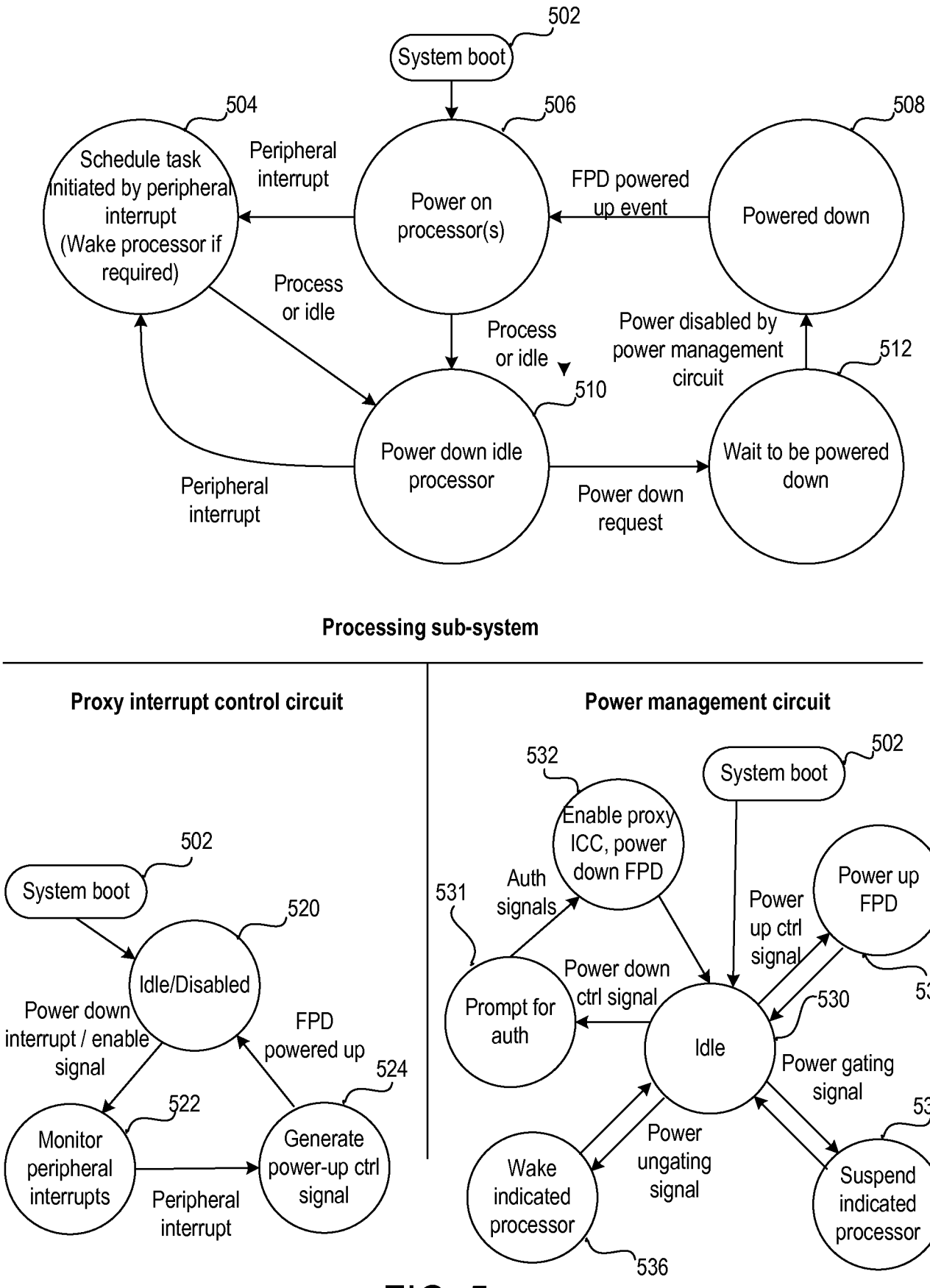
502
System boot
504
Schedule task initiated by peripheral interrupt (Wake processor if required)
Peripheral interrupt
506
Power on processor(s)
FPD powered up event
508
Powered down
Process or idle
Process or idle
Power disabled by power management circuit
512
510
Power down idle processor
Wait to be powered down
Peripheral interrupt
Power down request
Processing sub-system
Proxy interrupt control circuit
502
System boot
520
Idle/Disabled
Power down interrupt / enable signal
FPD powered up
524
522
Monitor peripheral interrupts
Generate power-up ctrl signal
Peripheral interrupt
Power management circuit
532
Enable proxy ICC, power down FPD
502
System boot
531
Auth signals
Power up FPD
Power up ctrl signal
534
Power down ctrl signal
Prompt for auth
530
Idle
Power gating signal
538
Power ungating signal
Wake indicated processor
Suspend indicated processor
536

FIG. 5

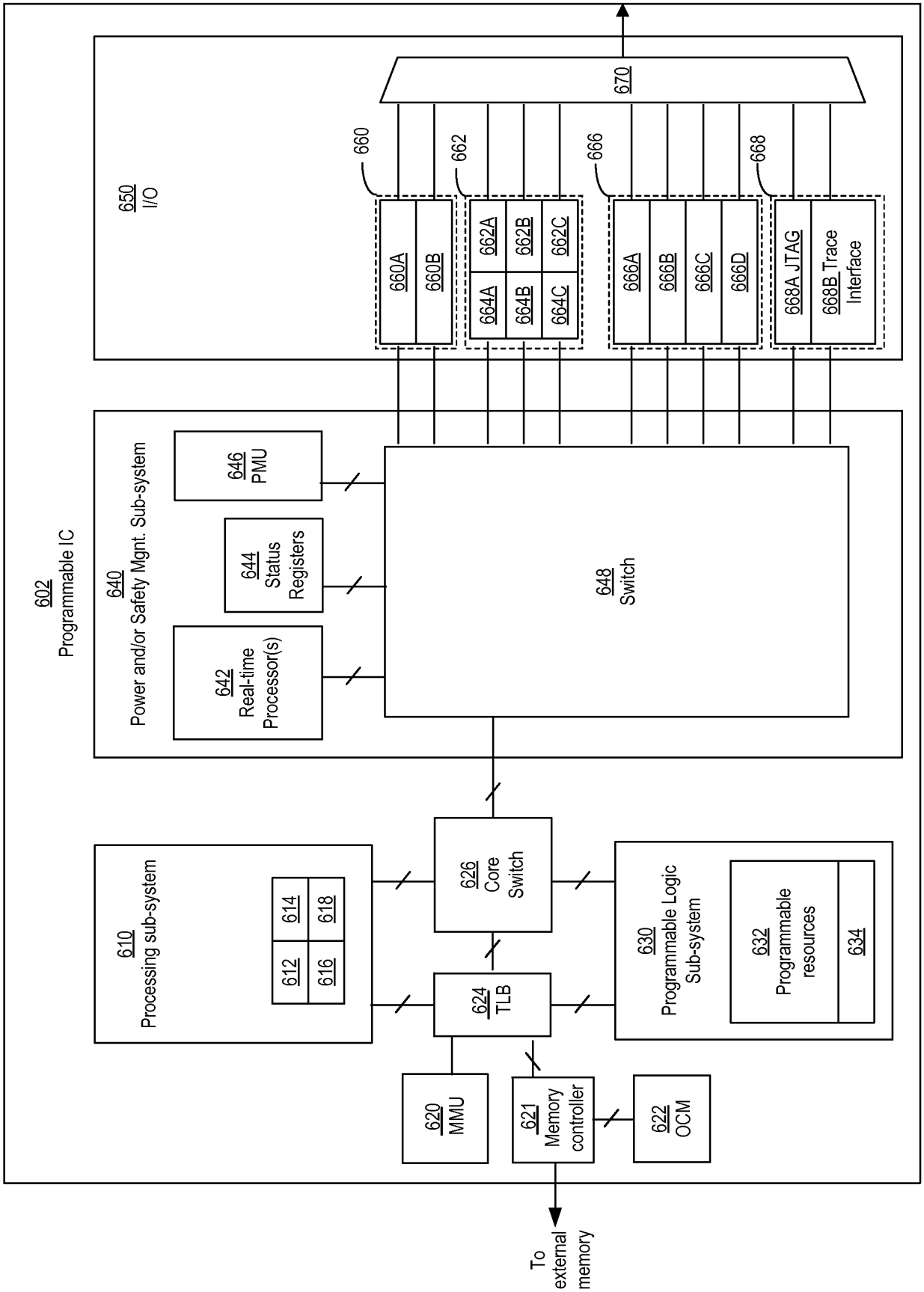
602
Programmable IC
650
I/O
660
662
666
668
670
660A
660B
662A
662B
662C
664A
664B
664C
666A
666B
666C
666D
668A JTAG
668B Trace Interface
640
Power and/or Safety Mgnt. Sub-system
646
PMU
644
Status Registers
642
Real-time Processor(s)
648
Switch
610
Processing sub-system
612
614
616
618
626
Core Switch
624
TLB
630
Programmable Logic Sub-system
632
Programmable resources
634
620
MMU
621
Memory controller
622
OCM
To external memory

FIG. 6

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2015/045569

A. CLASSIFICATION OF SUBJECT MATTER
INV. G06F13/24 G06F1/32
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2014/181557 A1 (BRANOVER ALEXANDER J [US] ET AL) 26 June 2014 (2014-06-26) paragraph [0009] - paragraph [0010]; claims 1-11; figures 1-3 paragraph [0019] - paragraph [0029] -----	1-7
A	US 2012/047402 A1 (CHEN XUFENG [US] ET AL) 23 February 2012 (2012-02-23) paragraph [0016] - paragraph [0024] paragraph [0028] - paragraph [0039] -----	1-7

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 October 2015	29/01/2016

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Toader, Elena Lidia

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/045569

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-7

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-7

   Saving power for independent circuits in a processing subsystem

   ---

2. claims: 8-11

   Saving power for dependent circuits in processing subsystems

   ---

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2015/045569

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2014181557 A1	26-06-2014	NONE	
US 2012047402 A1	23-02-2012	CN 103124941 A	29-05-2013
		EP 2609482 A2	03-07-2013
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		KR 20130045402 A	03-05-2013
		US 2012047402 A1	23-02-2012
		WO 2012027284 A2	01-03-2012