(12) UK Patent Application (19) GB (11) 2 070 857 A

(21) Application No 8041342
(22) Date of filing 29 Dec 1980
(30) Priority data
(31) 54/169935
(32) 26 Dec 1979
(33) Japan (JP)
(43) Application published 9 Sep 1981
(51) INT CL³
H01L 27/12
G09F 9/30
H01L 29/78
(52) Domestic classification
H1K 1CA 1EA 4C11 4C14 4H1A 4H3A 9D1 9D2 CAA
G5C A310 A342 A350 HG
(56) Documents cited
GB 2056770 A
GB 2052154 A
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GB 1465244
GB 1447849
(58) Field of search
H1K

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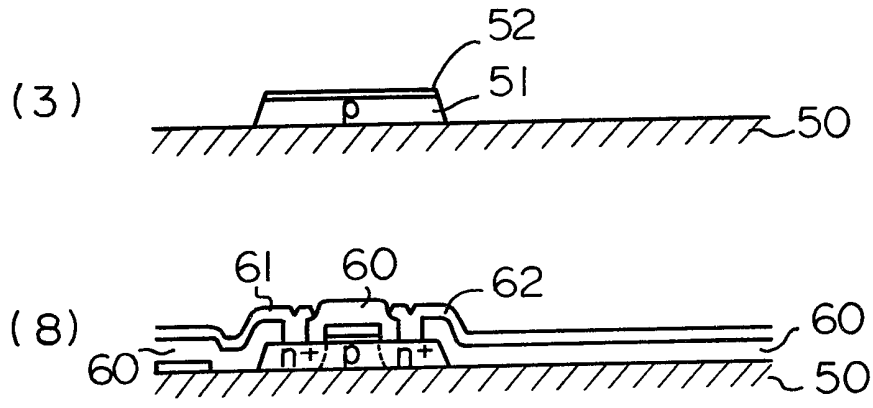
(54) **Method of forming display panel substrates having switching elements provided thereon**

(57) In a method of forming substrates for display panels of liquid crystal, electro-chromism, electro-luminescence type, etc, having switching elements provided individually for each display element, the switching elements are formed from a thin film of a semiconductor 51, which is irradiated by a high energy beam 53 such as an electron beam or laser beam. Subsequently a layer of insulating material 52 is provided over the semiconductor film to provide a gate insulating film, a gate layer of conducting material 54, 55 is provided over the gate insulating layer, a patterned insulating film 60 is provided over said gate layer and a patterned conducting film 61, 62 is formed over said patterned insulating film. The substrate 50 may be formed of quartz or glass.

Fig. 4



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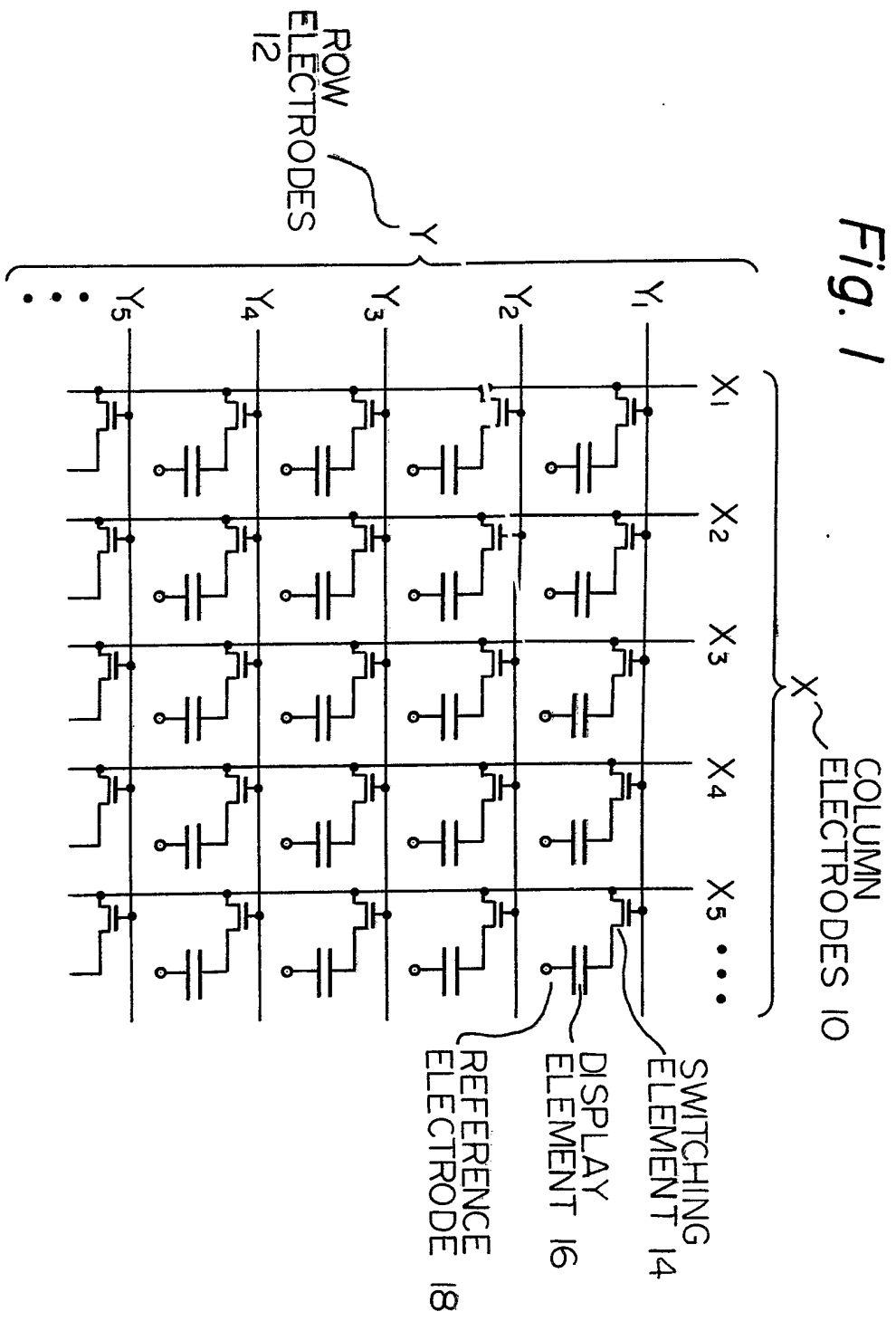
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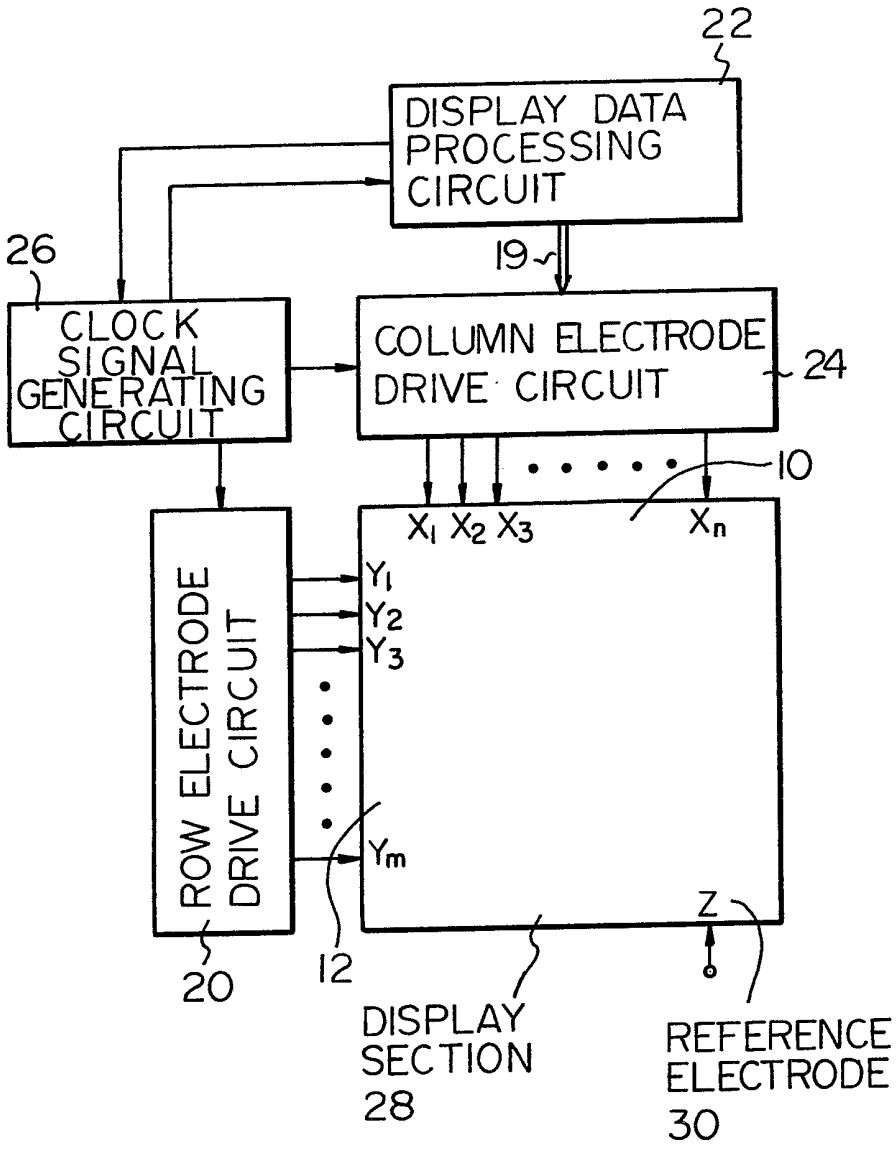
Y2
Y3
Y4
Y5
X1
X2
X3
X4
X5
X
COLUMN ELECTRODES 10
SWITCHING ELEMENT 14
DISPLAY ELEMENT 16
REFERENCE ELECTRODE 18

Fig. 1

Fig. 2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DISPLAY DATA PROCESSING CIRCUIT
19
26
CLOCK SIGNAL GENERATING CIRCUIT
COLUMN ELECTRODE DRIVE CIRCUIT
24
10
X1 X2 X3
Xn
ROW ELECTRODE DRIVE CIRCUIT
Y1
Y2
Y3
Ym
Z
20
12
DISPLAY SECTION 28
REFERENCE ELECTRODE 30

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Fig. 3

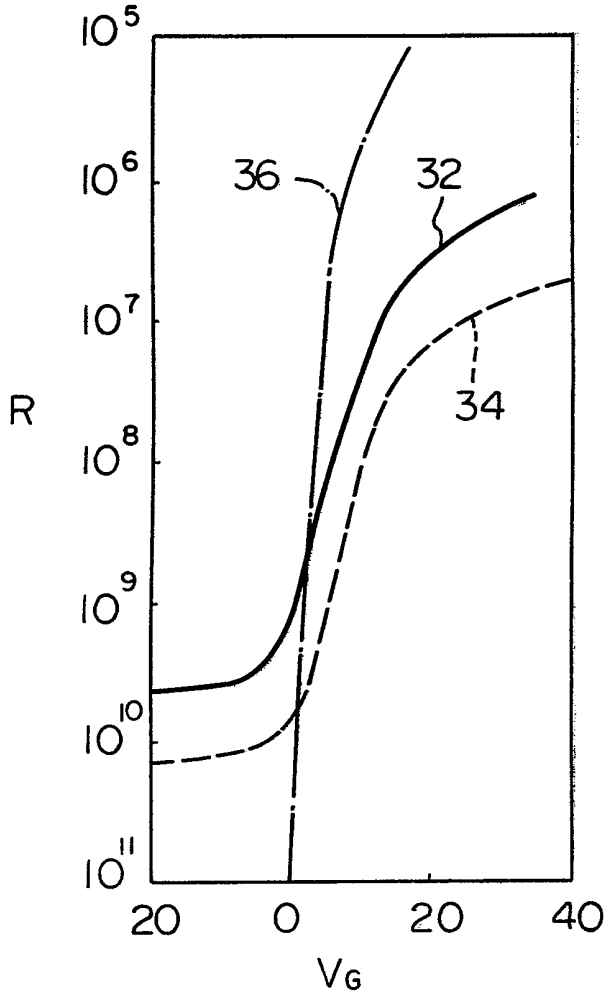
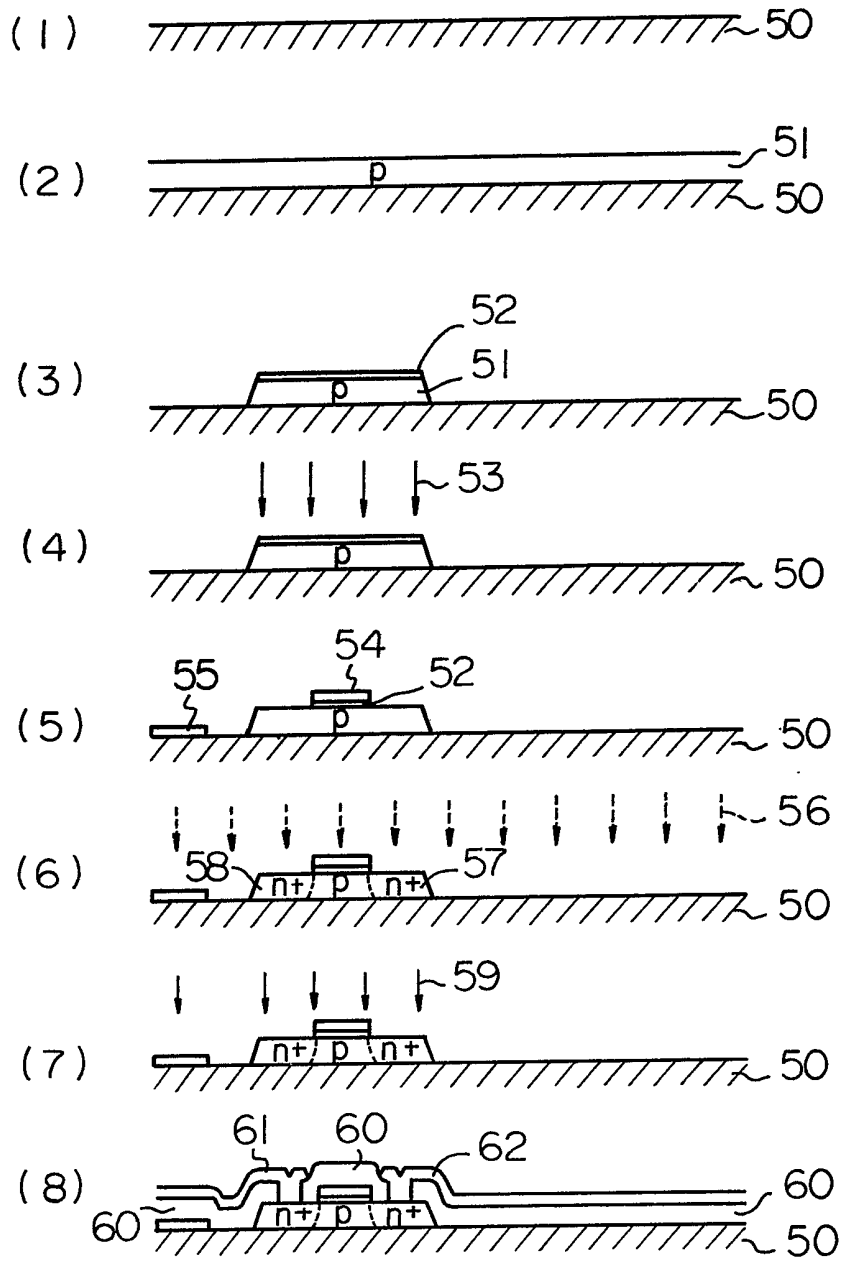


Fig. 4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p
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(3)
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(5)
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p
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(6)
56
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n+
p
n+
57
50
(7)
59
n+
p
n+
50
(8)
61
60
62
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n+
p
n+
60
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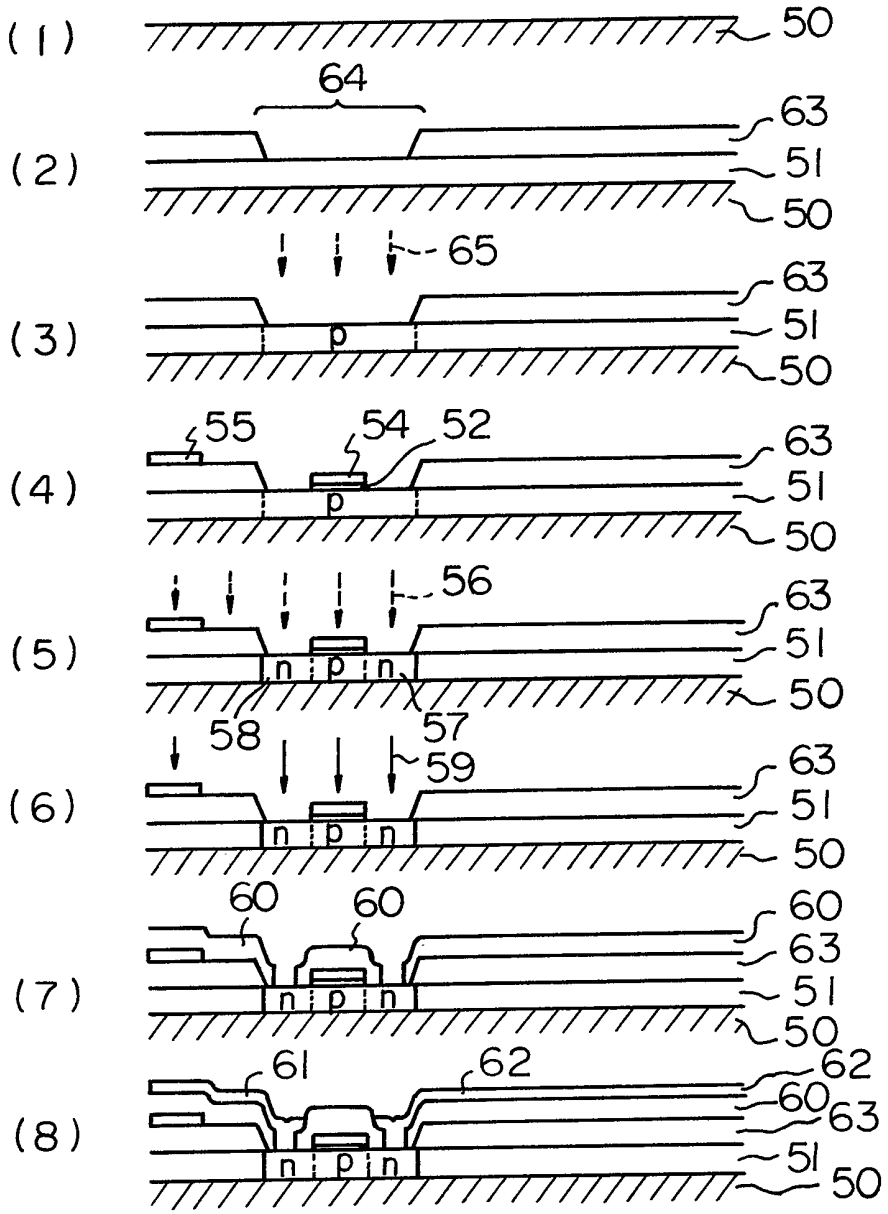
4 · 1(8)

Fig. 5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n p n
50
60
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(7)
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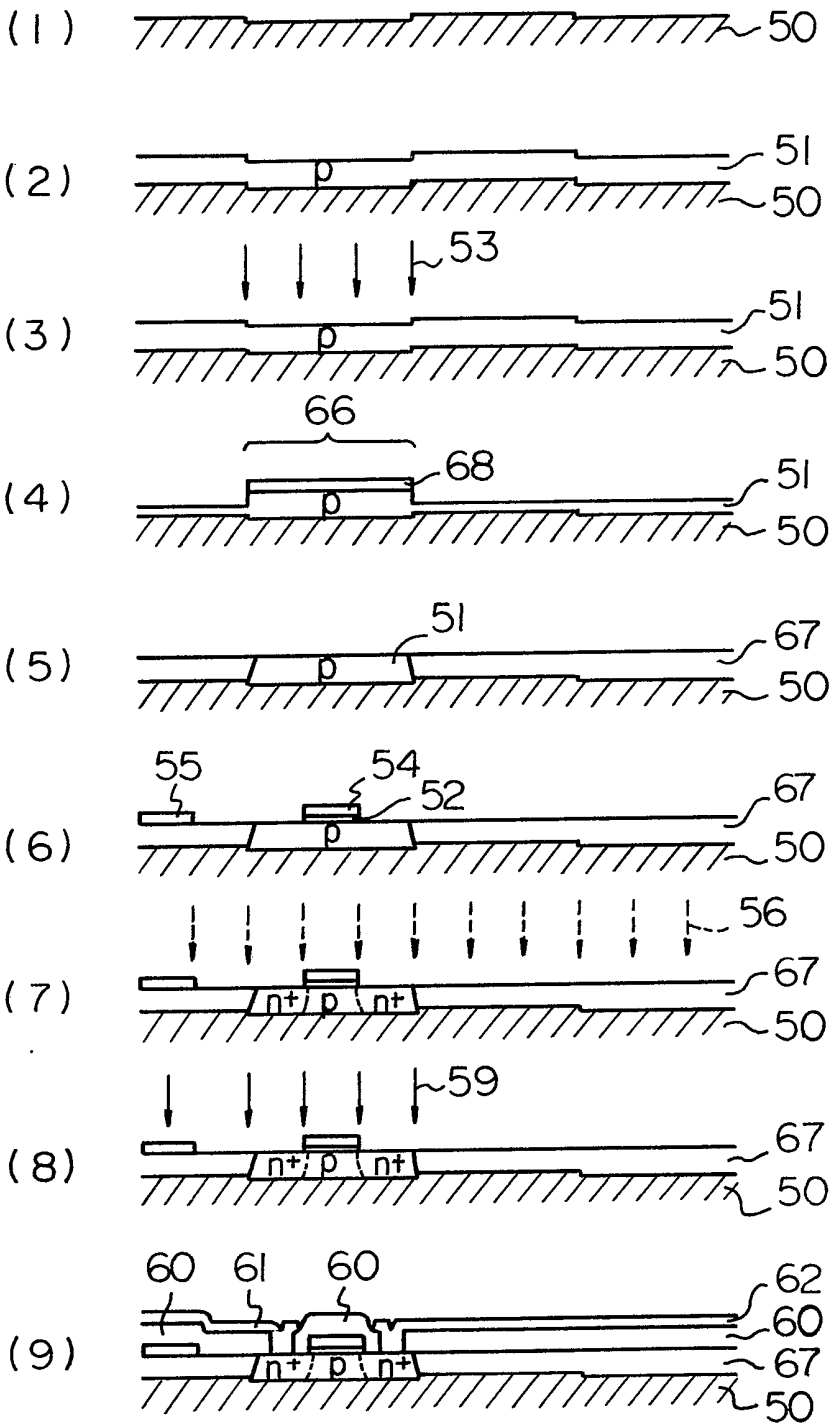
51
n p n
50
61
62
(8)
62
60
63
51
n p n
50

Fig. 6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(7)
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n+
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(8)
59
67
n+
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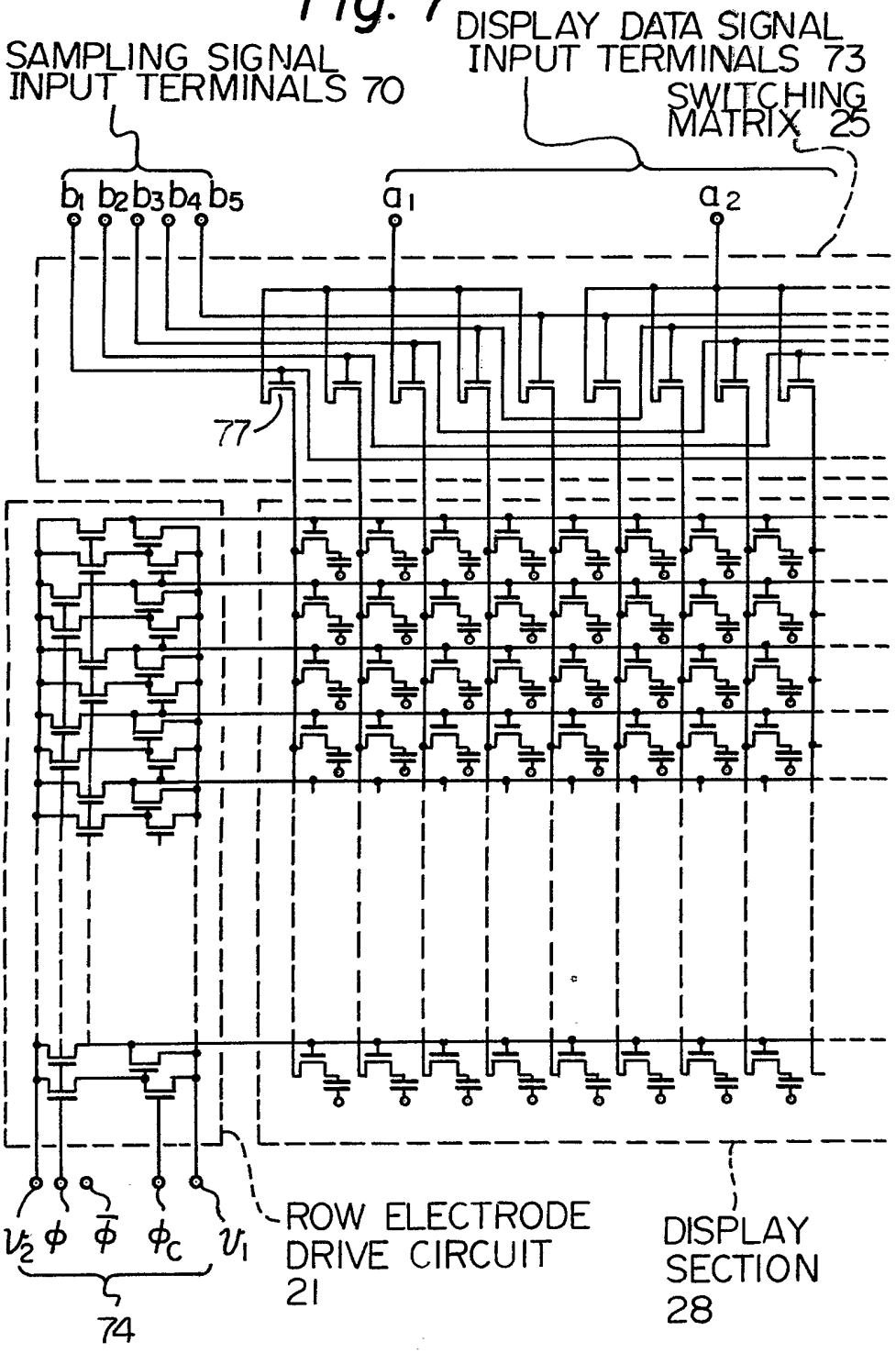
n+
50
(9)
60
61
60
62
60
67
n+
p
n+
50

Fig. 7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DISPLAY DATA SIGNAL INPUT TERMINALS 73
SWITCHING MATRIX 25
b1 b2 b3 b4 b5
a1
a2
77
ROW ELECTRODE DRIVE CIRCUIT 21
DISPLAY SECTION 28
74

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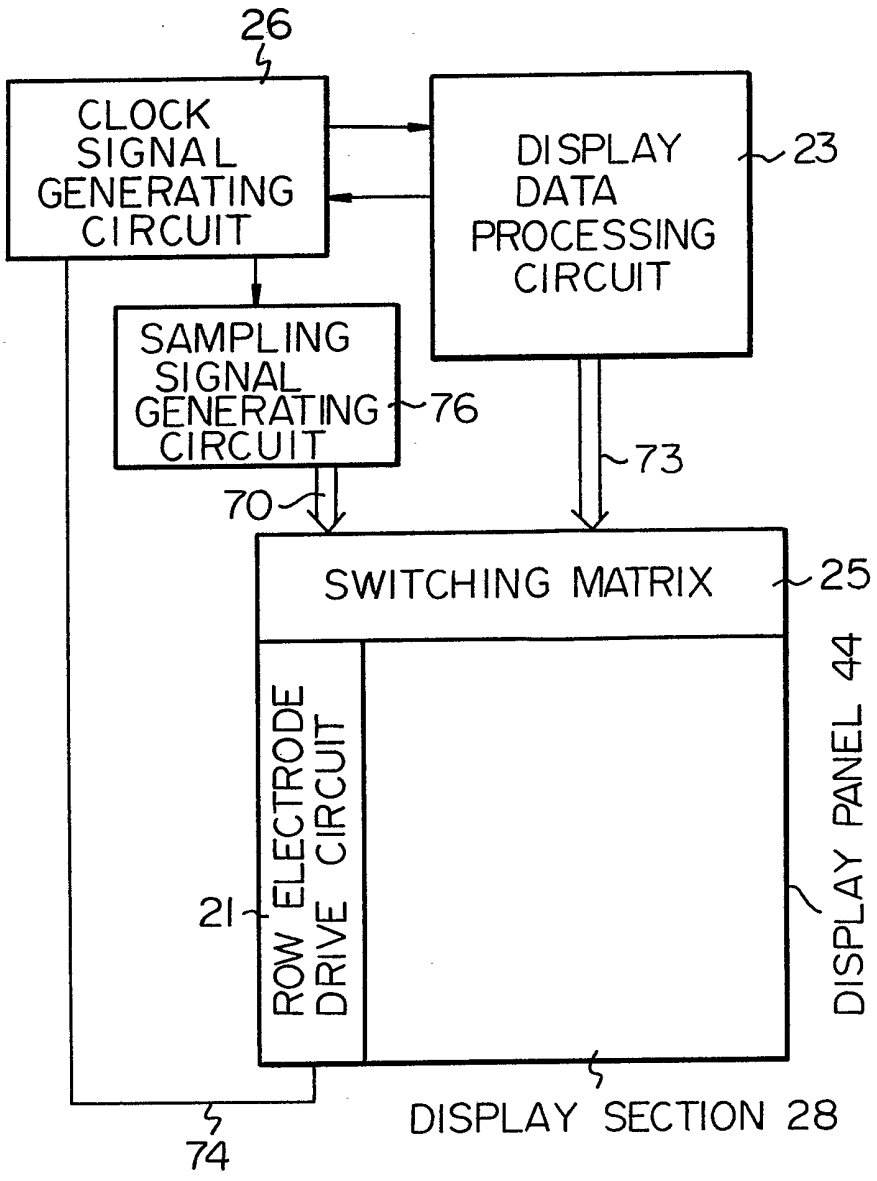
Fig. 8



SPECIFICATION

Method of forming display panel substrates having switching elements provided thereon

Various types of electro-optical display panels have come into widespread use for a number of different applications, which include electronic wristwatches, calculators, computers, flat-screen television receivers, and so on. Such display panels include liquid crystal, electro-luminescent, electro-chromic, plasma discharge types, etc, and their use is expected to increase rapidly in the future. In the case of a display panel for such applications as television receivers, computer terminal equipment, etc, in which a high degree of display density is required, display panels of matrix type are generally used, in order to reduce as far as possible the number of leads which connect the display panel to other circuitry. Initially, the performance of such display panels was limited, because of the occurrence of cross-talk inteference, resulting from such factors as capacitative coupling between various electrodes of the matrix. However, this problem was substantially solved by the adoption of display panels of matrix type in which an individual switching element is provided to control each of the display elements of the matrix. Such a method, which will be referred to herein, for convenience, as the "built-in switching element method was first proposed by B. J. Leichner et al (Proc. IEEE, Vol. 59, Nov. 1971, P. 1566 to 1579). A great deal of research has been carried out upon this method, which is especially suited to matrix-type liquid crystal display panels. Such display panels bring the advantages of low power consumption, low operating voltages, compactness, etc, which are usually associated with liquid crystal displays. However, until now no method of manufacturing such display panels has been disclosed which is completely satisfactory with respect to various important requirements. These requirements include, preferably, low cost of manufacture, ease of manufacture, ability to use substrates consisting of a transparent material, switching elements having a suitably high level of OFF resistance and low level of ON resistance, etc. The various conventional methods of forming integrated circuits containing switching elements such as thin film transistors, e.g. evaporative deposition of semiconductor and conductor regions, are not suited to the requirements for providing uniform characteristics over a display panel substrate which has a large area and a relatively low density of elements. In addition, some of the prior art methods which have been proposed for manufacturing such display panel substrates have the disadvantage that the material which must be used as the basic substrate is expensive and/or non-transparent. A display panel having a non-transparent substrate is obviously not suitable for display panels of transmission type or reflection type. There have been prior art proposals to utilize a thin film of a semiconductor such as amorphous silicon or polycrystalline silicon in order to form the switching elements of such a display panel substrate. However, the switching elements thus formed display poor electrical characteristics, due basically to the mobility of the majority carriers of the semiconductor being low.

There is therefore a requirement for some method of forming the substrates of display panels of matrix type, having built-in switching elements, which will eliminate the various disadvantages of prior art methods, as briefly described above. Such a method is disclosed by the present invention.

According to the present invention, there is provided a method of manufacturing a substrate for an electro-optical display panel, comprising the steps of: preparing a substrate base; forming a thin film of a semiconductor material on surface of said substrate base; irradiating said semiconductor film by a radiation beam; forming a layer of an electrically insulating material over said semiconductor film to thereby provide a gate insulating layer; forming a gate layer, comprising a layer of conducting material, over said gate insulating layer; forming a patterned insulating film over said gate layer; and forming a patterned conducting film over said patterned insulating film.

In the attached drawings:

Fig. 1 is a circuit diagram of a portion of the display section of a display panel of the built-in switching element type;

Fig. 2 is an overall block diagram of a display system which includes a display panel;

Fig. 3 is a graph showing the switching characteristics of a switching element produced according to the present invention and a switching element produced according to prior art methods;

Fig. 4, Fig. 5 and Fig. 6A and B are diagrams illustrating the various stages of forming a display panel substrate according to the present invention, for three examples of the method of the present invention;

Fig. 7 is a circuit diagram of a display panel which utilizes switching elements formed by the method of the present invention, such as can be produced by the processes illustrated in Fig. 4, 5 and 6, and

Fig. 8 is an overall block diagram of a display system which includes a display panel such as that of Fig. 7.

Before describing the present invention in detail, with specific embodiments, a brief description of the basic features of a display panel of the built-in switching element type will be given. Fig. 1 is a circuit diagram illustrating a part of such a display panel. Reference numeral 10 denotes a set of column electrodes (i.e. vertically arranged bus lines), while numeral 12 denotes a set of row electrodes (i.e. horizontally arranged bus lines). These row and column electrodes are connected to a matrix array of switching elements (a typical one of which is designated by numeral 14) and display elements (one of which is denoted by numeral 16). If we assume that this is a liquid crystal display panel, then the display element

16 comprises a conductive region (a display electrode) which is electrically connected to the column electrode X_5 when the potential of the row electrode Y_1 is such that the switching element 14 is in the conducting state, a reference electrode which is formed on the opposing substrate to that on which the switching elements and display electrodes are formed, and a region of liquid crystal lying between the display electrode and the reference electrode. The reference electrode generally comprises a conductive layer formed over the entire area of one substrate, and connected to a fixed reference potential. Drive signals are sequentially applied to each of the row electrodes Y_1, Y_2, . . . in turn, to thereby temporarily set the switching elements of each row in the conductive state. While the switching elements of a particular row are in the conducting state, a corresponding set of display data signals are applied to the column electrodes X_1, X_2, . . . , to thereby input display data to the display elements. After the switching elements return to the non-conducting state, the potentials of the display electrodes are held constant, due to the isolation provided by the switching element, until the corresponding row is again scanned by the row drive signals. In effect, the display signal is stored in the display element, between successive scans of the row electrodes, due to the capacitance of each display element.

Referring now to Fig. 2, a block diagram is shown therein of a display system which includes a display panel of the built-in switching element type. Here, reference numeral 26 denotes a clock signal generating circuit, which generates timing signals to control the operation of a row electrode drive circuit 20 and a column electrode drive circuit 24. Row electrode drive circuit 20 serves to generate scanning signals to sequentially select each of the set of row electrodes 12, as described above. Column electrode 24 serves to apply display data signals to the column electrodes 10 at appropriate timings, these display data signals being produced in accordance with display data generated by a display data processing circuit 22.

It is a feature of a display panel of the built-in switching element type that, due to the isolation provided by the switching elements, cross-talk effects are virtually non-existent. In addition, there is virtually no limit on the maximum number of display elements which can be provided with such a display panel. However, practicable manufacture of such a display panel has not yet been achieved. This has been due to the lack of a suitable method of manufacturing substrates for such display panels, with the necessary switching elements provided thereon. Various methods of manufacturing such substrates have in fact been proposed in the prior art. For example, Lewis T. Lipton et al have proposed the use of a monocrystalline silicon substrate as such a display panel substrate, with the switching elements comprising field-effect transistors (FETs) formed in the silicon. (See SID 78, Digest, P. 96, 1978). This method can provide switching elements having satisfactory characteristics, however the manufacture of monocrystalline silicon substrates is extremely expensive. In addition, since such a substrate is non-transparent, the number of display cell operating modes which can be used with such a substrate are severely limited.

Because of this, various methods have been proposed whereby substrates can be produced which are transparent. Such methods include, for example, vacuum evaporative deposition of a compound semiconductor such as CdSe (e.g. see Fang-Chen Luo, T. P. Brody, et al, SID 78 Digest, P.94, 1978). Another proposal has been to use a film of amorphous silicon, formed by a glow-discharge dissolution technique (see P. G. LeComber, W. E. Spear et al, Electronics Letters, 15, P.179, 1979). However, such methods present problems with respect to difficulties of manufacture and unsatisfactory characteristics of the switching elements, so that practical realization of display panels using such methods have not been achieved. For example, grain boundary effects are extremely important, in relation to the characteristics of switching elements which are formed of a polycrystalline semiconductor film prepared by evaporative deposition of CdSe. For this reason, it is desirable to be able to form a film in which the grain diameter is uniform, over a large area. However, it is difficult to form a film having such properties. In addition, if the slant evaporative deposition method of forming a thin semiconductor film is used, it is necessary to align the substrate upon which the deposition is to be performed in a direction facing the evaporation source. As a result, it is difficult to process a number of such substrates in a single manufacturing stage. Furthermore, in the case of a thin film of amorphous silicon which is formed by the glow discharge dissolution process, the distribution of the plasma is extremely important. Because of this, only a limited number of substrates can be processed during a single manufacturing stage, with the latter method. For the above reasons, it can be seen that the prior art methods which have been proposed for forming such substrates, which are based upon conventional methods of integrated circuit manufacture, are not suitable for practical manufacture of substrates for display panels of the built-in switching element type, and do not produce switching elements which are suitable for use in such display panels. It is necessary for the switching elements used in such display panels to satisfy the following criteria. The first of these criteria is that it must be possible to form a display section (i.e. an array of switching elements and display element electrodes) upon the display panel. The second criterion is that it must be possible to provide peripheral circuitry upon the display panel. The first of these criteria is the minimum which must be satisfied in order to construct a display panel. If only the first criterion is met, but not the second, then it is necessary to provide all of the peripheral circuitry (i.e. the circuitry which supplies the row and column drive signals, such as circuits 20 and 24 of the example in Fig. 2) externally to the display panel. If the total number of row and column electrodes is of the order of several hundred, then the problem of providing interconnecting leads between such external peripheral circuitry and the display panel becomes very severe, and a number of different integrated

circuit modules or chips must be interconnected in order to realize a display system. If, on the other hand, at least a part of the peripheral circuitry can be provided directly upon the display panel, then such problems can be considerably reduced, as will be described hereinafter. In order to achieve a practicable display panel of the built-in switching element type, therefore, it is highly desirable that both of the criteria stated above can be met.

The first of these criteria is determined by the following factors:

(a) It must be possible to write in or to erase display data (i.e for one row of the display element matrix) during a selection period (i.e. the period during which the switching elements of that row are in the conductive state). For practicable durations of such a selection period, i.e. of reasonably short duration, it is therefore necessary that the resistance of each switching element in the ON state (Ron) must be sufficiently low, in order to rapidly charge or discharge the capacitance of the display element.

(b) It must be possible to retain display data which has been written into the display elements, in the intervals between successive selection periods, i.e. the OFF resistance (Roff) of the switching elements must be sufficiently high.

(c) The potential which must be applied to the switching elements to set them in the non-conducting state (which we shall designate as Voff), and the potential which must be applied to set them in the conducting state must not be excessively great.

In the following, the capacitance of a display element (i.e. the capacitance arising between a display electrode and the opposing reference electrode) will be designated as C_{lc}, the stray capacitance associated with a display element as C_s, and the sum of these capacitances simply as C. The frame frequency for scanning the row and column electrodes will be designated as F, and the number of row electrodes as M. The switching time (i.e. the time required to charge or discharge the display element during a selection period), which will be designated as t_s, is given by Ron × C, and the time interval during which a row is in the selected state (i.e. the selection period) will be designated simply as t, and must be smaller than $1/(F \times m)$. According to requirement (a) above, t_s must be smaller than t, resulting in the relation:

$$\text{Ron} \; 1/(F \times m \times C) \quad \ldots\ldots(1)$$

The duration of the non-selection interval is given by:

$$(m-1)/(F \times m) \fallingdotseq 1/F$$

The duration for which the display data will be retained by the switching element is given by Roff × C.

Thus, it can be seen that requirement (b) above results in the relation:

$$\text{Roff} > 1/(F \times C_{lc}) \quad \ldots\ldots(2)$$

The conditions for meeting requirement (c) above will be set in part by the type of peripheral circuit elements used. However, these voltages should be as low as possible.

The second criterion stated above, i.e. for providing peripheral circuitry on the display panel, is affected by the type of peripheral circuitry which is involved. In the case of the row drive circuit, e.g. circuit 20 of Fig. 2, this only serves to produce successive scanning signals having a pulse width of t. However, the column drive circuit, e.g. circuit 24 of Fig. 2, is more complex, and normally performs a serial/parallel conversion upon display data. It is therefore necessary to ensure that the time required for each serial/parallel conversion, t_{sp}, is shorter than the selection period t. If the number of column electrodes is n, and the number of serial signal lines (connected to the column drive circuit to input display data in serial form) is designated as s, then the response speed Ron × C* of the switching elements in the serial/parallel conversion circuit of the column drive circuit must meet the condition:

$$\text{Ron} \times C^* < t_{sp} \times (s/n)$$

In addition, as stated above, the following conditions must be met:

$$t_{sp} \leqslant t \qquad \text{and} \qquad t \leqslant 1/F \times m$$

so that:

$$\text{Ron} < s/(F \times m \times n \times C^*) \quad \ldots\ldots(3)$$

In order to form the column drive circuit upon the display panel substrate, the above conditions (1) to (3) must be met, as a minimum.

Referring now to Fig. 3, the switching characteristics of thin film transistors formed by conventional techniques are shown. The solid-line curve 32 represents the characteristics of transistors formed using a film of CdSe, while the broken-line cirve represents the characteristics of transistors formed using amorphous silicon. The transistor gate voltage is plotted along the horizontal axis, while the impedance of the switching element (i.e. between drain and source) is plotted on the vertical axis. If we assume a display panel for which the display section area is 10 cm square, the number of row and column electrodes are each 500, for which C_{lc} is 0.2 pf, and for which C is 1pf, and the frame frequency F is 50 Hz, then from requirement (1) above:

$$\text{Ron} < 4 \times 10^7 \text{ ohms}$$

Also, from requirement (2) above:

$$\text{Roff} > 10^{10} \text{ ohms}$$

If we assume that $C^* \fallingdotseq 0.2$ pf, and $s \fallingdotseq 5$, then from requirement (3):

$$\text{Ron} < 2 \times 10^6 \text{ ohms.}$$

In the case of a CdSe transistor, Roff is low, so that the first condition stated above is not met. In the case of an amorphous silicon transistor, the value of Ron is close to the permissible limit, for values of Von greater than 40 V. It is possible to vary the switching characteristics by changing the dimensions of the transistor and the gate oxide layer. It is also possible, by varying certain parameters, to modify the conditions (1) to (3) stated above. However, it is only with the greatest difficulty that it would be possible to meet the first basic criterion stated above, whereby the switching transistors are provided on the display section substrate, and there is no possibility of meeting the second basic criterion, for providing peripheral circuitry upon the display panel substrate.

One of the reasons for the poor switching characteristics of CdSe and amorphous silicon (abbreviated hereinafter to a-Si) transistors is that the carrier mobility in such a semiconductor film is low. This is indicated by the way in which the characteristic curves shown in Fig. 3 (i.e. 32 and 34) slope, in other

words the change from the OFF state to the ON state of such a switching element is relatively gradual. If on the other hand the carrier mobility of the semiconductor is high, then there is a large change in the impedance of the switching element for a relatively small change in the control gate voltage Vg.

For monocrystalline silicon, for example, the carrier mobility is from 10^3 to 10^2 cm^2/V.sec, approximately. For CdSe, on the other hand, the carrier mobility is no more than 10 cm^2/V.sec, while for a-Si, the carrier mobility is no greater than 10^{-1} to 10^{-2} cm^2/V secm approximately. It is because of this low degree of carrier mobility that the switching characteristics of thin-film CdSe or a-Si transistors are so poor, with Ron being excessively high, and with it being necessary to apply high values of Von and Voff.

Another cause of these poor switching characteristics is unsatisfactory control of impurity concentration. A suitably high value for the OFF resistance of a MOS FET formed from monocrystalline silicon can be obtained, because of the isolation which is provided by a reverse-biased PN junction. However, with a CdSe transistor, it is not possible to provide PN junctions within the switching element, due to the fact that control of impurity concentration is extremely poor for CdSe. It is possible to provide PN junctions within an a-Si transistor. However, it is difficult to produce effective PN junctions, having a high density of levels within the energy band gap. As a result, as can be seen from the low-voltage operating regions of the characteristics of Fig. 3, a finite amount of leakage current flows between the drain and source of such a transistor in the OFF state, so that it is not possible to provide a suitably high value of Roff.

The present invention comprises a method of producing display panel substrates which is inexpensive, and which provides substrates having elements with improved characteristics, whereby the various problems described above, which arise with display panels of the prior art, are eliminated.

Figure 4 is a diagram of an embodiment of the method of the present invention. In step (1) of Fig. 4, a plate of a suitable material is denoted by numeral 50, upon which the various elements and electrodes will be formed. For clarity of description, in the following description and also in the appended claims, a member such as plate 50 will be referred to as a "substrate base", while the term "substrate" will be used to refer to a completed assemblage upon which switching elements and electrodes have been formed. With the present invention, the substrate base 50 can be made of any of a wide variety of materials. For example, in the case of a display panel of transmission type, the substrate base can be made of fused quartz, or inexpensive glass, so as to be transparent. In step (2) of Fig. 4, a thin film of a semiconductor is formed upon substrate base 50. Such materials as polycrystalline silicon, or amorphous silicon, can be used as this semiconductor. If the subsequent processing stages permit, it is preferable that control of impurity concentration be performed within this semiconductor film. In the present embodiment, a P-type polycrystalline silicon thin film is formed by chemical vapor deposition of a mixture of SiH_4 and B_2H_6 gases.

In step (3), coating of an insulating film over flim 51 is performed, and then patterning is performed so as to leave only desired regions of film 51, which will subsequently become the channel regions of the switching elements, with an insulating film 52 provided over each region. Performing this patterning process in stage (3) serves to enhance the effectiveness of the beam irradiation processing which will be performed in the next step (4). In addition, desired characteristics can be produced in particular small regions, by forming such regions during this patterning step. Furthermore, by providing the insulating film 52 over the channel regions prior to the beam irradiation step (4), it is possible to closely control the effects produced by the irradiation process, through suitable choice of the thickness of the insulating film 52 and of the type of irradiating beam. For example, if an Ar laser is used to provide the irradiating beam, and a layer of polycrystalline silicon 800 Å thick, oxidised by means of heat treatment, is used as the gate insulating film, then the insulating film can act as an anti-reflective coating with respect to the beam. This serves to enhance the effectiveness of the irradiation process.

In step (4) of Fig. 4, the irradiation processing is performed. Various types of beam sources can be used for this irradiation, including lasers, flash lamps, sunlight, infra-red beams, etc. It is also possible to use an electron beam for this purpose. The irradiation can be performed either on a continuous basis (i.e. using a CW beam source), or can be on a pulsed basis. If a CW Argon laser is used, and if the operating conditions are set at a spot size of 100 μm, and a beam power of approximately 10 watts, then it is possible to irradiate only regions which have been formed by patterning, (e.g. 51 and 52 in part (2) of Fig. 4), while other areas are not irradiated. Alternatively it is possible to irradiate the entire area of the substrate, within a short time, by employing high-speed scanning of the beam.

In step (5), formation of a gate film 54 and a connecting lead film 55 is performed. In this embodiment, after deposition of a conductive material such as a polycrystalline film formed by the CVD method, the latter film is formed into gate regions such as 54, and wiring regions 55, by a patterning process. In step (6), processing is performed of regions adjacent to the gate areas, which are to form the source and drain portions of the switching elements. N-type regions which will form the drain 57 and source 58 are produced by means of a self-aligning process, which employs implantation of phosphorus ions.

In step (7), activation is performed of the regions in which ion implantation was carried out in step (6), i.e. activation of the implanted impurities. This is done by irradiation with a beam 59, as in step (4).

Steps (6) and (7) are not absolutely essential to the method of the present invention. However, they serve to produce switching devices which have superior characteristics.

Step (8) is a process in which a patterned insulating film 60 and patterned conducting films 61 and 62

are formed. It is necessary to provide an insulating film upon the display panel substrate in order to provide a base for the conducting pattern. The latter pattern comprises a wiring pattern conducting film 61 and display electrode conducting film 62. For a display panel of reflection type, these conducting films can be metallic, and can consist of Al, Mo, An, Ag, etc. In the case of a transmission type of display, the conducting films can consist of a transparent conductive film of In_2O_3, SnO_2, etc.

Fig. 5 and Fig. 6 show other embodiments of methods of constructing display panel substrates according to the present invention. In (1) of Fig. 5, a substrate base 50 is indicated, which can be of a material such as has been discussed for the first embodiment of Fig. 4. In step (2), a semiconductor film 51 is formed on substrate base 50, and an insulating film 63 is formed over this. A mask aperture 64 is provided in film 63, to leave a stabilized region of film 51. In this embodiment, semiconductor layer 51 comprises a layer of silicon, which is formed by a plasma CVD process, with hydrogen being contained in the silicon film. The masking insulating film 63 is formed by deposition of SiO_2, by the CVD process.

In step (3), doping with an impurity is performed in the active region as indicated by numeral 64. In this embodiment, doping is performed by implantation of boron ions.

In step (4), the gate insulating film 52, gate film 54, and connecting conductor film 55 are formed. SiO_2 is used for gate insulating film 52, while Si is used to form the gate film and the connecting conductor film 55.

In step (5), conduction types of both of the source region 58 and the drain region 57 (i.e. regions 58, 57 which are within the active region but outside the gate region) are controlled. The conduction types of the regions 57 and 58 are provided by doping with phosphorus ions 56.

In step (6), beam irradiation of the semiconductor film is performed. In the embodiment, the second harmonic of a Q-switched YAG laser is used as a beam source. The semiconductor film comprises amorphous silicon, with added hydrogen, which is formed into a polycrystalline layer as a result of the irradiation with the laser beam. Since the grain boundaries within the semiconductor film are terminated by dangling bonds, formed by hydrogen atoms, the film has electrical characteristics which are ideal for forming switching elements. In this embodiment, the Q-switched laser beam is used to irradiate only the activation regions, i.e. the regions in which switching elements are formed.

In step (7), an insulating film 60 is formed, to provide insulation for the interconnecting conductors (e.g. to provide insulation at the crossovers between row and column electrodes). Apertures are left in this film 60 above the drain and source regions, and any other regions to which electrical contact must subsequently be established.

In step (8), interconnecting conductor film 61 and display electrode film 62 are formed. The display electrode film 62 can comprise a metallic film, or a layer of semiconductor material.

In this embodiment, a layer of non-doped semiconductor is used to provide an insulating film between the switching elements (i.e. film 63), and the beam irradiation is performed only over the regions in which switching elements are to be formed. In these respects, therefore, this embodiment differs somewhat from that of Fig. 4. However, basically, these manufacturing methods are very similar.

Referring now to the embodiment of Fig. 6, step (1) therein shows a substrate base 51, on the upper surface of which are provided a plurality of regularly arranged recessed areas. In step (2), a film of semiconductor (which is P-type, in this example) is formed over substrate base 51.

In step (3), beam irradiation is performed. In this example, irradiation is shown as being performed only over regions in which switching elements are to be performed, as indicated by numeral 53.

In step (4), a film of heat-resistant resist 68 is formed over active region 66. This resist material can comprise for example Si_3N_4. Partial etching of regions other than the active regions is then performed.

In step (5), oxidation is performed of regions other than the active region 66, to form an insulating oxidised film 67. The heat-resistant resist film 66 is then removed.

In step (6), deposition and patterning are performed, to provide a gate insulation film 52 and a gate electrode film 54, together with a connecting conductor film 55.

In step (7), doping of the drain and source regions is performed.

In step (8), beam irradiation is performed of the regions where doping was carried out in step (7).

In step (9), after deposition of an insulating film of material such as SiO_2, to form film 60, an interconnecting conductor film 61 and a display electrode film 62 are formed, to connect to the drain and source regions (i.e. in this example, the N-type regions) of the switching element. This stage corresponds to steps (7) and (8) of the embodiment of Fig. 5, and the comments made with respect to those steps of the latter embodiment are equally applicable to that of Fig. 6.

It is a feature of the embodiment of Fig. 6 that a LOCOS (local oxidisation of silicon) process is used to provide insulation between the various elements, and also to provide a high degree of surface flatness in the finished substrate. Another particular feature of this embodiment is the use of a set of regularly spaced recessed areas in the base substrate surface, within which the switching element regions are formed. By using this LOCOS process, differences in level between the various elements on the display panel substrate are reduced. Another advantage of using these recessed regions in the substrate base is that the directions of the axes of crystallization in the polycrystalline film that is formed by the irradiation process are held within a limited range. This serves to ensure more stable characteristics for the switching elements which are formed by this method.

Referring now to Fig. 3 once more, numeral 36 therein denotes the switching characteristics of a switching element formed by the method of the present invention, as described in the above embodi-

ments. It can be seen that these are a considerable improvement over the characteristics which can be obtained by prior art methods, such as are indicated by numerals 32 and 34.

Because of the improved switching characteristics of elements formed upon a display panel substrate according to the method of the present invention, it becomes possible to simultaneously form all or part of the peripheral circuitry for the display panel directly upon the same substrate base as the display section, i.e. the array of display electrodes and their switching elements. An example of this is shown in the circuit diagram of Fig. 7 and block diagram of Fig. 8. Fig. 7 is a partial circuit diagram of a display panel, in which numeral 28 denotes a display section, comprising an array of switching elements and display elements, numeral 21 denotes a row electrode drive circuit, and numeral 25 denotes a switching matrix which controls the supply of display data signals to the column electrodes of the display section 28. Row electrode drive circuit 21 comprises a dynamic shift register, which utilizes stray capacitances for its operation. Scanning signals are applied sequentially to the row electrodes of display section 28, in response to clock signals ϕ, ϕ and ϕ_c, which are supplied from a clock signal generating circuit 26 shown in Fig. 8, together with fixed potentials V_1 and V_2, collectively designated by numeral 74. The switching elements in switching matrix 25, such as element 77, are selectively rendered conducting in response to sampling signals which are applied to a set of sampling signal input terminals 70, from sampling signal generating circuit 76. In this way, the display data signals, produced by display data processing circuit 23, are distributed to the column electrodes of display section 28 in a time-sharing manner.

It can be seen from this example that, by forming at least a part of the peripheral drive circuitry for a display panel directly upon the same substrate base on which the display element matrix is formed, using the method of the present invention, the number of interconnecting leads between the display panel and external circuitry can be very substantially reduced. This makes possible the manufacture of display panels having a considerably higher density and number of display elements than has been possible with prior art panels.

As described with the above embodiments, it is possible to produce a liquid crystal display panel having, for example, 400 × 400 display elements, utilizing a substrate manufactured according to the method of the present invention, which requires only approximately 50 interconnecting leads between the display panel and external circuitry. In addition, since the drive voltage requirements are low, such a display panel is very advantageous from the aspect of portability. These advantages of a display panel manufactured according to the method of the present invention are based upon the effective use of beam irradiation.

The most important requirements for a display panel are that the element density can be low, but that the display area is large. This differs from the requirements for conventional LSI integrated circuitry, where the area involved is low, but high element density is the principal objective. The most important points for a method of manufacturing such display panels are:

A. A practicable type of substrate, preferably transparent, must be used.

B. The display elements must be uniform in their characteristics and free from defects, even over a large display area.

C. The manufacturing cost should be low, even for display panels of large area.

D. The grade of the switching element should be high, to be utilized for the display panel.

Since stabilization of the semiconductor film by beam irradiation is performed on a localized basis, there are no problems with regard to the dispersion of doping impurities, or danger of damage to the substrate base caused by the activation process. Thus, a wide variety of materials can be used for the substrate base. This enables the substrate to be made transparent, by using an easily worked material such as quartz glass, or an even less expensive material such as soda lime glass. If necessary, the substrate can be coated with SiO_2, MgF_2, TiO_2, Al_2O_3, or other suitable substance.

By comparison with the beam irradiation process of the present invention, other processes such as heat-treatment methods provide a lower degree of surface regularity and a higher proportion of defects, when used to produce a display panel substrate of large area. In addition, with such a heat-treatment process, it is difficult to provide a uniform temperature distribution over a large area. However, with the beam irradiation process, since scanning of the beam can be employed, stable and uniform processing of a large area can be achieved.

In addition, irradiation by the beam of the display panel substrate can be performed in a non-continuous manner, i.e. the beam can be made to irradiate only those portions of the substrate in which switching elements are to be formed. This enables the time required for processing a substrate to be reduced, which is very advantageous for the manufacture of display panel substrates having a large area and a low density of elements. In the case of the prior art heat-treatment processes, the time required to process a substrate is determined entirely by the total area to be processed, irrespective of whether the element density is high or low, i.e. it is necessary to process areas where this is required and also those areas where processing is not actually necessary.

The switching characteristics of switching elements produced by the method of the present invention are almost identical to those which can be obtained by using monocrystalline semiconductor material, and these switching elements are ideally suited for use on display panel substrates.

From the above description, it can be understood that the method of the present invention for manufacturing display panel substrates provides important advantages over prior art methods, with respect to the characteristics of switching elements produced thereby, stability, cost, etc.

Substrates produced according to the method of the present invention are particularly advantageous

for use with devices which employ the electro-optical effects of liquid crystal, and are applicable to liquid crystal display devices employing various operating modes, including the twisted nematic mode, guest-host mode, dynamic scattering mode, phase-change mode, birefringence mode, etc. In addition, since the method of the present invention enables a transparent substrate to be used, the display panel can be of transmission type or reflection type. Substrates produced according to the method of the present invention are also applicable to electro-chromism and electro-luminescent types of display panel.

The present invention enables substrates to be produced which are of very high quality and can be of virtually any since. The present invention is therefore applicable to the production of high-precision display panels for use in electronic wristwatches, for example. The method of the present invention is also highly applicable to the manufacture of display panels for flat-type television receivers, computer terminal displays, etc.

From the preceding description, it will be apparent that the objectives set forth for the present invention are effectively attained. Since various changes and modifications to the above construction may be made without departing from the spirit and scope of the present invention, it is intended that all matter contained in the above description or shown in the accompanying drawings shall be interpreted as illustrative, and not in a limiting sense. The appended claims are intended to cover all of the generic and specific features of the invention described herein.

CLAIMS

1. A method of manufacturing a substrate for an electro-optical display panel, comprising the steps of:
preparing a substrate base;
forming a thin film of a semiconductor material on surface of said substrate base;
irradiating said semiconductor film by a radiation beam;
forming a layer of an electrically insulating material over said semiconductor film to thereby provide a gate insulating layer;
forming a gate layer, comprising a layer of conducting material, over said gate insulating layer;
forming a patterned insulating film over said gate layer; and
forming a patterned conducting film over said patterned insulating film.

2. A method of manufacturing a substrate according to claim 1, wherein said substrate base is formed of glass.

3. A method of manufacturing a substrate according to claim 1, wherein said substrate base is formed of fused quartz.

4. A method of manufacturing a substrate according to claim 1, wherein said semiconductor film comprises polycrystalline silicon.

5. A method of manufacturing a substrate according to claim 1, wherein said semiconductor film comprises a thin film of silicon containing hydrogen.

6. A method of manufacturing a substrate according to claim 1, wherein said semiconductor thin film comprises a film of amorphous silicon.

7. A method of manufacturing a substrate according to claim 1, wherein patterning of said semiconductor thin film is performed prior to said step of irradiating said semiconductor thin film.

8. A method of manufacturing a substrate according to claim 1, wherein said irradiation of said semiconductor thin film is performed in a non-continuous manner, and is limited to a plurality of predetermined regions of said semiconductor thin film.

9. A method of manufacturing a substrate according to claim 1, wherein said step of forming a gate insulating layer is performed prior to said step of irradiating with a radiation beam.

10. A method of manufacturing a substrate according to claim 1, wherein said thin film of a semiconductor material is doped with impurities when formed over said substrate base.

11. A method of manufacturing a substrate according to claim 1, wherein both said step of forming a gate layer and said step of forming said gate insulating layer are performed prior to said step of irradiation.

12. A method of manufacturing a substrate according to claim 1, wherein impurities are added to at least a portion of a regions adjacent to said gate insulating layer prior to said step of irradiating the semiconductor film to form semiconductor regions of different majority carrier type to that of a region of said semiconductor film lying below said gate insulating layer.

13. A method of manufacturing a substrate according to claim 1, wherein said radiation beam comprises a laser beam.

14. A method of manufacturing a substrate according to claim 1, wherein said radiation beam comprises a continuous wave type of laser beam.

15. A method of manufacturing a substrate according to claim 1, wherein said radiation beam comprises a pulse type of laser beam.

16. A method of manufacturing a substrate according to claim 1, wherein said radiation beam comprises an electron beam.

17. A method of manufacturing a substrate according to claim 1, wherein said radiation beam is produced by a flash lamp.

18. A method of manufacturing a substrate according to claim 1, wherein said radiation beam comprises an infra-red light beam.

19. A method of manufacturing a substrate according to claim 1, and further comprising a step of forming a passivation layer, following said step of forming a patterned conducting film over said patterned insulating film.

20. A method of manufacturing a substrate according to claim 1, wherein said electro-optical display panel utilizes the electro-optical properties of liquid crystal.

21. A method of manufacturing a substrate according to claim 1, wherein said electro-optical display panel utilizes the property of electro-chromism.

22. A method of manufacturing a substrate sub-

stantially as shown and described with reference to the accompanying drawings.

Printed for Her Majesty's Stationery Office by The Tweeddale Press Ltd., Berwick-upon-Tweed, 1981.
Published at the Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.