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(54) METHOD FOR PRODUCTION OF CONTACTS ON A WAFER

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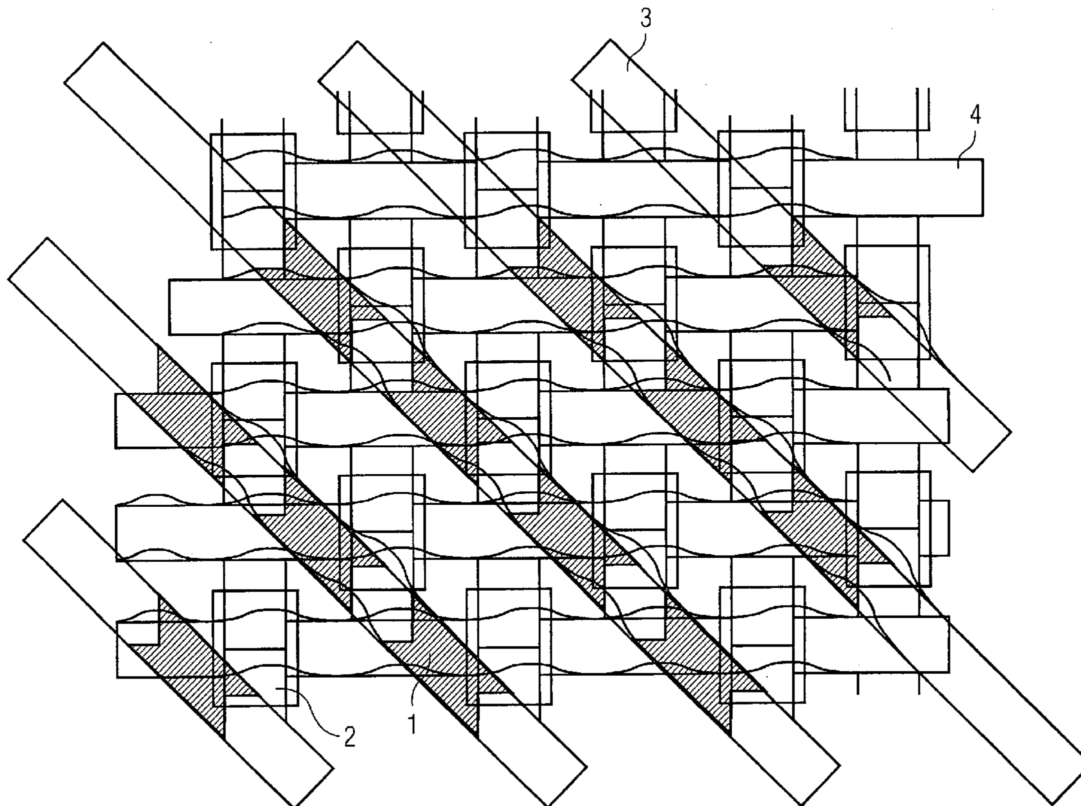
(57) **ABSTRACT**

The invention relates to a method for production of contacts on a wafer, preferably with the aid of a lithographic process. The preferred embodiment provides a method which overcomes the disadvantages of the complex point/hole lithography process, and which avoids any increase in the process complexity. This method is achieved in that a strip structure extending over two layers is used to structure the contacts. The strip structure in the first layer is rotated at a predetermined angle with respect to the strip structure in the second layer, and the contacts are formed in the mutually overlapping areas of the strip structures in the two layers.



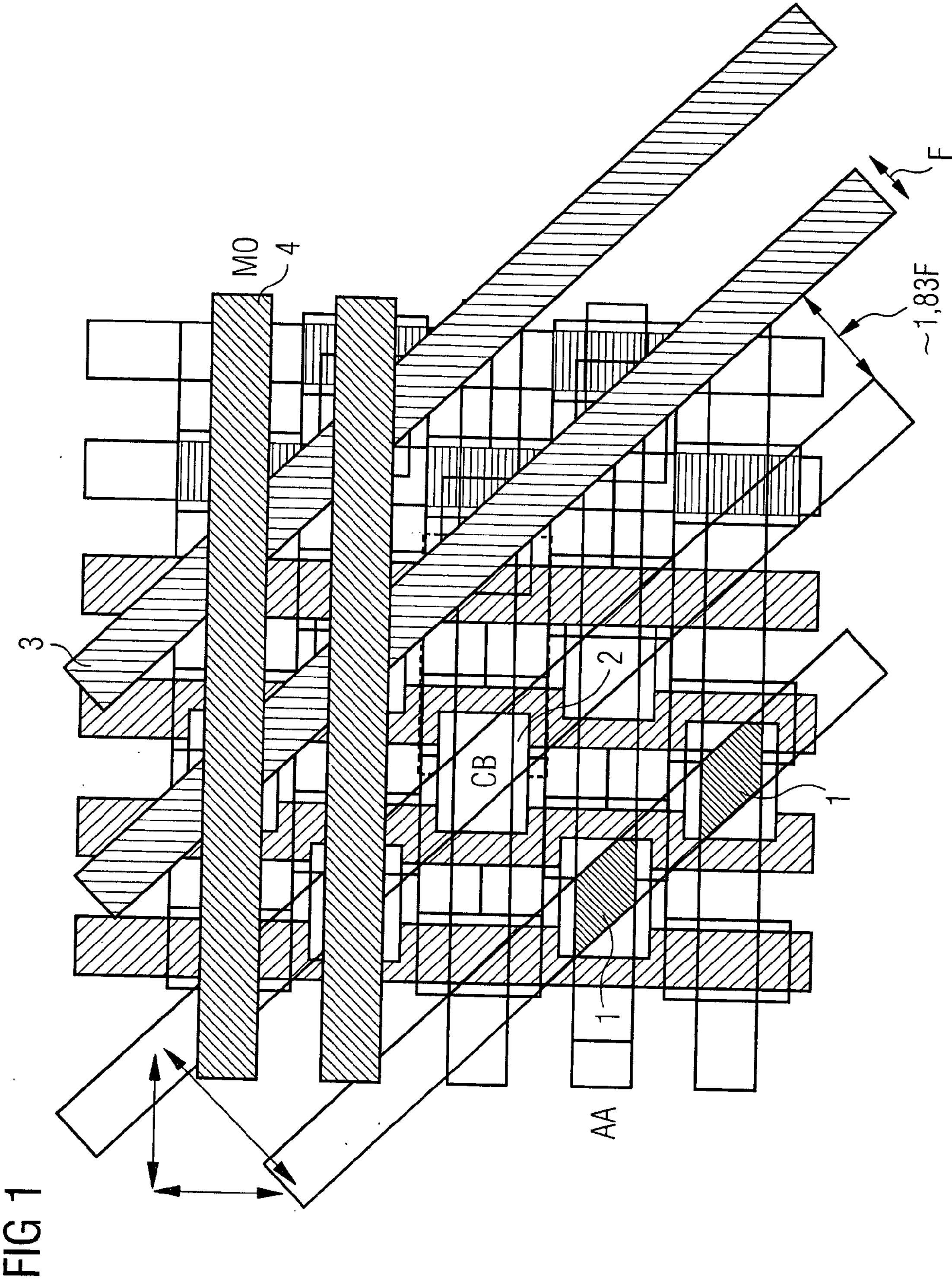


FIG 1

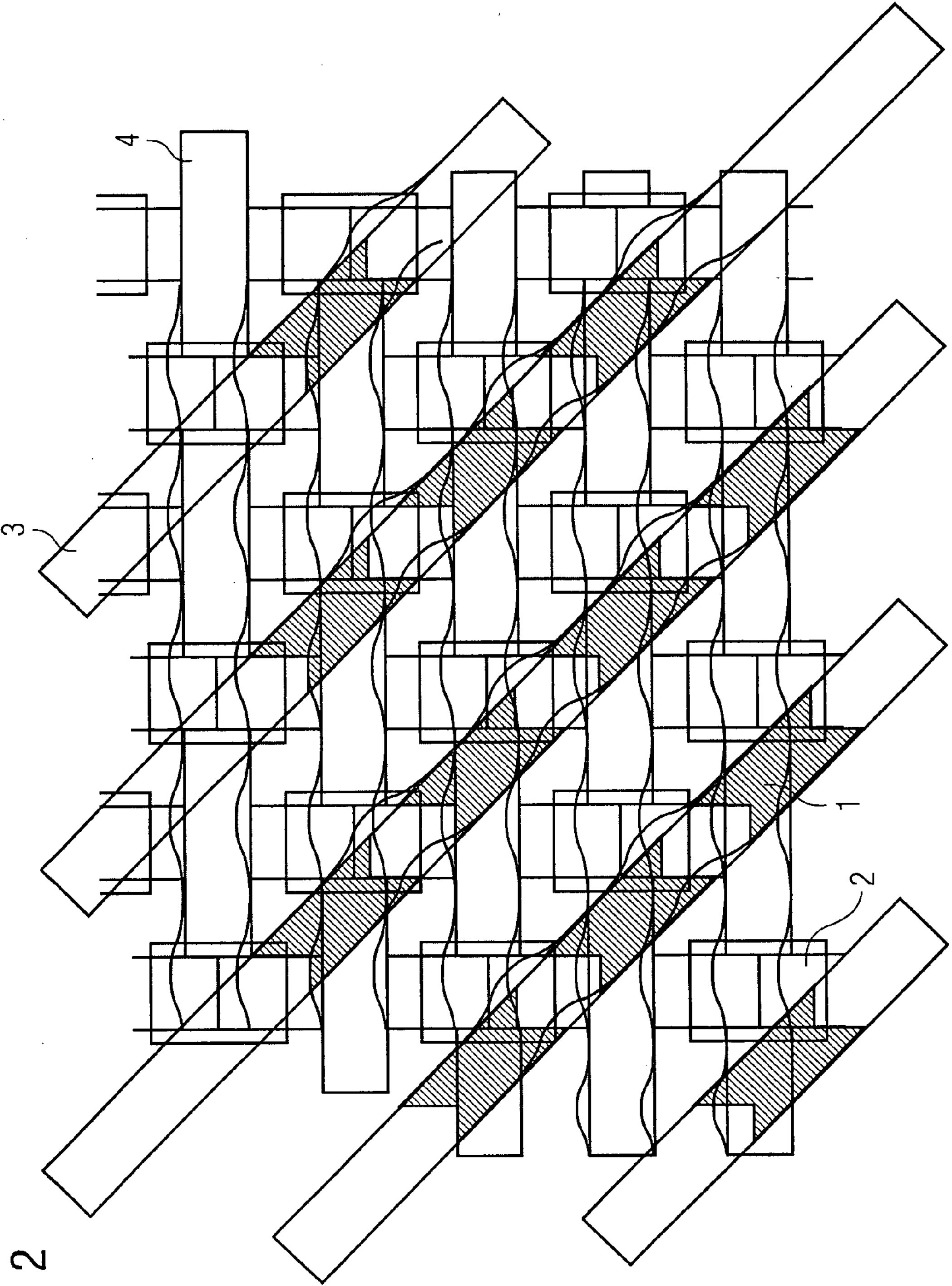


FIG 2

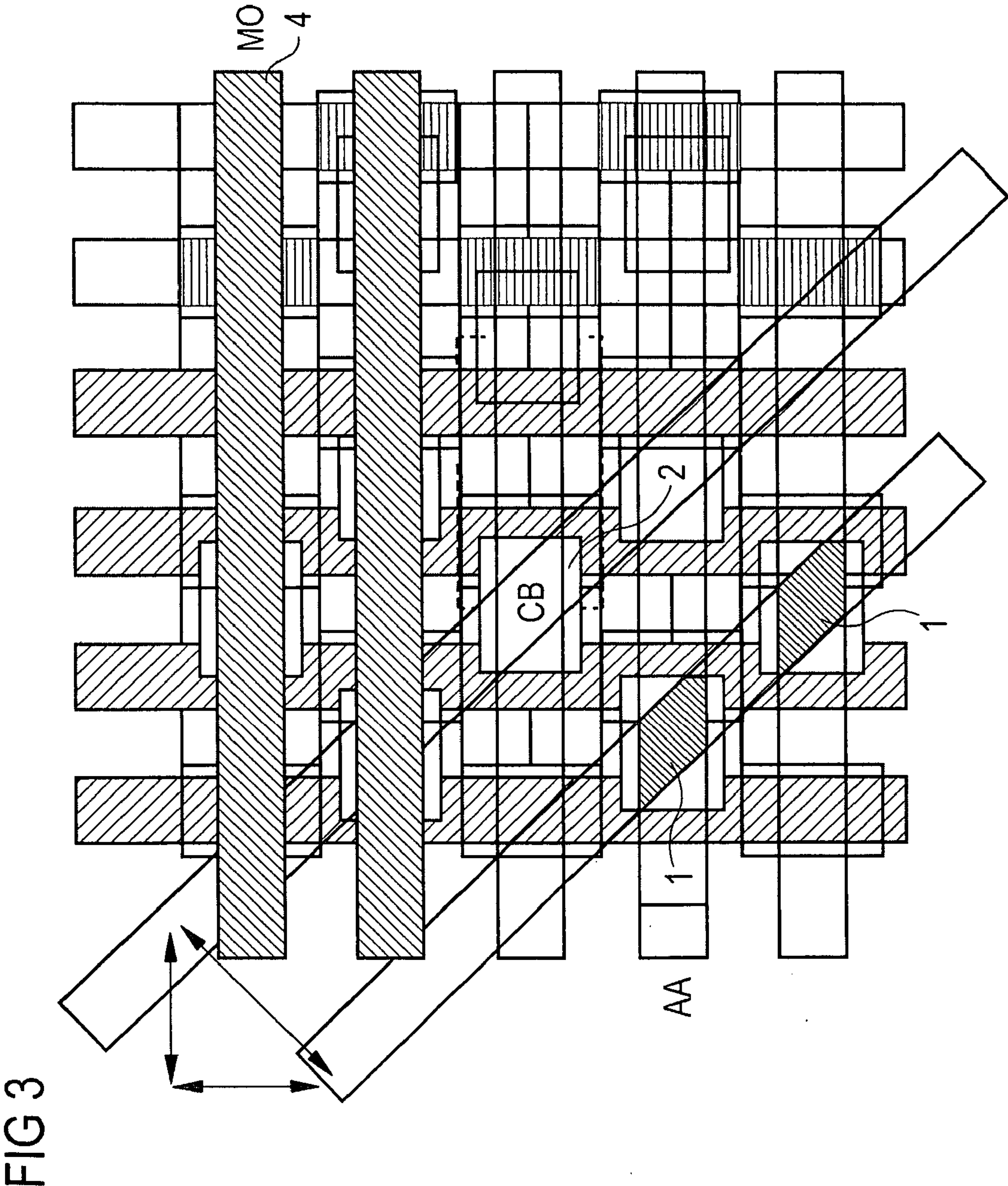


FIG 3

METHOD FOR PRODUCTION OF CONTACTS ON A WAFER

[0001] This application is a continuation of U.S. patent application Ser. No. 10/739,477, filed Dec. 18, 2003, which is now U.S. Pat. No. 7,094,674, issued Aug. 22, 2006, and which claims the benefit of German Application No. 102 59 634.4-33, which was filed Dec. 18, 2002, which application is incorporated herein by reference.

TECHNICAL FIELD

[0002] The invention relates to a method for production of contacts on a wafer, and more preferably to a method for production of contacts on a wafer with the aid of a lithographic process.

BACKGROUND

[0003] When memory cells are produced in matrix-like arrangements, it is necessary to make contact between each cell and a row and a column line. In order to produce these connections, the cells have to be provided with contacts, which are electrically conductively connected to the lines.

[0004] As is described in U.S. Pat. No. 5,482,894 and international application WO 01/09946 A1, when manufacturing DRAM circuits according to the prior art, contacts in the cell array are produced by using a plug/hole mask in a lithographic process. After an exposure and development process, holes are etched in the dielectric between the first metallization layer and the diffusion layer. The etching is in this case carried out selectively for gate encapsulation.

[0005] The hole masks that are required for this method are difficult to produce lithographically with the necessary size and accuracy. A further disadvantage occurs as the contact holes become smaller. The subsequent selective etching of the holes as far as the gate encapsulation is more difficult for small structures.

[0006] WO 01/09946 A1 describes a method for production of integrated semiconductor components. The necessary contacts are produced first by forming the desired contact as a sacrificial poly-silicon DOT, then by embedding this DOT in BPSG in a subsequent process, and by later removing the sacrificial poly-silicon once again. The contact holes are then filled with a conductive material, thus forming a conductive connection.

[0007] In this method, the distance between the structures is very small, owing to the progress in the miniaturization of the memory structures and the use of a checkerboard design. This improves the capability to form resist feet between the resist DOTs that are produced. A disadvantage of the method is that the resist DOTs which are required in the meantime are relatively high, as isolated structures, and can easily fall down.

SUMMARY OF THE INVENTION

[0008] A preferred embodiment of the invention provides a method that overcomes the disadvantages of the complex plug/hole lithography process, and that avoids any increase in the process complexity.

[0009] The preferred embodiment provides a method of forming a semiconductor device, such as a dynamic random access memory. A surface, e.g., a silicon substrate, includes a plurality of contacts, e.g., bitline contacts, laid out in a matrix of rows and columns. A first plurality of strips is formed over the surface. Each strip in the first plurality is disposed along a diagonal of the matrix. A second plurality of strips is formed over the surface and over the first plurality of strips. Each strip in the second plurality is disposed along a row of the matrix. Contacts can be formed by removing portions of the first plurality of strips not underlying the second plurality of strips.

[0010] One advantageous embodiment of the invention provides for the production of strip structures by means of a lithographic process, using a first and a second exposure mask, each mask having a parallel strip structure.

[0011] Another advantageous embodiment of the invention provides for the strip structure to be corrugated or to be provided with corrections in selected areas in a layer which are predetermined by the chip design.

[0012] A further embodiment of the invention provides for the parallel strip structure in one layer to have a greater distance between one strip center and an adjacent strip center than the strip structure in another layer.

[0013] Another embodiment of the invention provides for the width of the strips in one strip structure to be the same as that of the width of the strips in another strip structure, and for the space between the strips of one strip structure to be greater than the space between the strips in another strip structure.

[0014] A further embodiment of the invention provides for a rotated strip structure wherein the rotated strip structure has the greater space between the strips.

[0015] Another embodiment of the invention provides for the contacts to be formed by over-etching the space between the M0 strip structures, with the CB strip structures being cut through.

[0016] A further embodiment of the invention provides for the M0 strip structure to form row lines for the memory cells which are arranged in the same row.

[0017] Another advantageous embodiment of the invention provides for positive resist or negative resist to be used for the lithography step.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

[0019] **FIG. 1** shows a structure layer on the wafer by means of strip structures in various layers; and

[0020] **FIG. 2** shows two layers of the parallel strip structures with a corrugated strip profile.

[0021] **FIG. 3** shows the structure of **FIG. 1** after further processing.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

[0022] The making and using of the presently preferred embodiments are discussed in detail below. It should be appreciated, however, that the present invention provides

many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative of specific ways to make and use the invention, and do not limit the scope of the invention.

[**0023**] Aspects of the present invention will now be described. The preferred embodiment will first be described textually. A specific example will then be discussed with respect to **FIG. 1**.

[**0024**] According to the present invention, the preferred embodiment method is achieved by using strip structures extending over two layers for the structuring of the contacts. The strip structure in the first layer is rotated at a predetermined angle with respect to the strip structure in the second layer, and the contacts are formed in the mutually overlapping areas of the strip structures in the two layers. An example of the structure is shown in **FIG. 1**, which will be discussed in greater detail below.

[**0025**] In this case, a strip structure is used in one layer and is aligned at an angle of, for example, 45 degrees with respect to the base layer of the chips. This strip structure is designed using a checkerboard arrangement such that the strips lie over the CB (bitline contact) surfaces of the memory cells. The cells are electrically connected to one another by means of these strips. A second layer, which is arranged above the first layer, is aligned in the direction of the base layer of the chips. This alignment of the layers results in areas which are covered not only by the strip structure in the first layer but also by the strip structure in the second layer. In a subsequent method step, the strip structure of the lower, rotated layer is cut through at those points which are not covered by the upper strip structure, and the overlapping portion is used to form the desired contacts to a structure which is located deeper on the wafer. An appropriate configuration of the uppermost strip structure allows it to connect the contacts that are produced to one another, for example as a row line.

[**0026**] The strips are formed by using two exposure masks. Once a number of preparatory method steps have been completed, for example those used for the production of DRAM memory cells, a positive or negative resist is applied. Then a first exposure mask is used in a lithographic method step to produce the first parallel strip structure which, after the development process and depending on the photoresist that is used, corresponds to the CB tracks or the trenches between the tracks. The tracks or trenches are placed at an angle of 45 degrees with respect to the base layer of the chips. After a number of method steps, the uppermost metallization layer (M0) is structured. This layer is also in the form of strips, with the alignment of these strips, with respect to the base layer of the chips, being zero degrees.

[**0027**] The contact is formed at the points at which the parallel strips of the two structures overlap. This assumes that the strip structures be placed at an angle to one another. In the preferred embodiment, the angle between the strip structures is 45 degrees. Angles other than that of 45 degrees may also be used, so long as the chosen angle allows contact to be made at the necessary points. Each memory cell design will determine what angles can be used.

[**0028**] After the structuring of the metallization layer M0 (e.g., the level of metal closest to the semiconductor body), the CB tracks which are located underneath it are cut through by over-etching the space between the M0 tracks, so that the contacts remain as CB plugs. The process of cutting through by means of M0 over-etching is possible since the CB tracks lead over encapsulated GC (gate contact) tracks by virtue of the checkerboard design in the M0 intermediate space, so that the etching need not be continued as far as the substrate.

[**0029**] In the checkerboard design used for producing the contacts, the distances between adjacent structures become even smaller by doubling the number of contacts. In order to reduce the increased risk of a short circuit between the structures resulting from this effect, for example the shortening of the distance between the CB layer and the AA (active area) layer or else between adjacent cells, the linear profile of the strips may be modified to a corrugated profile as shown in **FIG. 2**. A further possibility is to use partially regular corrections of the strips in accordance with the requirements of the respective chip design.

[**0030**] The distance between the parallel strips, also referred to as the pitch, is measured from the track center of one strip to the track center of an adjacent strip. Due to the chip design, for a layer which is rotated 45 degrees, the distance increases by the square root of two. If the width of the strips with respect to the other layer remains the same, the free space between the strips is thus increased.

[**0031**] The M0 strip structure may also form row lines for the memory cells which are arranged in the same row. The memory cells which are arranged in a matrix make contact with a row line and a column line, with the function of the row line being provided by the M0 strip structure, which is structured according to the method provided herein.

[**0032**] Referring now to **FIG. 1**, the preferred method provided herein is based on the assumption that the structures of the individual memory cells have been formed in a checkerboard arrangement and that the contacts **1** which are required for writing to and reading from the individual cells are to be formed.

[**0033**] In the preferred embodiment, the contacts **1** are formed on the surfaces **2**, which are identified by "CB". In order to produce the contact structures, a structure comprising parallel strips is formed by means of a first exposure mask using a lithographic process. These parallel strips form tracks which lead over the CB surfaces of the memory cells and connect them to one another at an angle of 45 degrees to the basic grid. This structure of the CB tracks **3** is formed from a resist track or trench, depending on the resist that is used, after an exposure and development process, and is formed by appropriate subsequent process steps, depending on the requirements for the chip.

[**0034**] Once this layer has been formed, a further lithographic process step is carried out, in which a second exposure mask is used. This likewise has a parallel strip structure, with the distance between the strips being less than that in the first mask. The strips are aligned in the base layer of the chips, that is at an angle of zero degrees. After a further exposure and development process, as well as the corresponding necessary further method steps, the M0 tracks **4** as illustrated in **FIG. 1** are produced. In a subsequent method step, over-etching of the space between the M0 tracks **4** leads to cutting through the CB tracks **3** located

underneath it in the rotated layer at the points which are not covered by the upper M0 strip structure **4**, and thus formation of the contacts **1** for the CB contact surfaces **2** at the points at which the two strip structures overlap.

[**0035**] These M0 tracks **4** in the uppermost metallization layer produce the connection for the contacts **1** located underneath it for the memory cells as a row line in a memory matrix, and need not be provided by further method steps following the contact formation.

[**0036**] In addition to the production of the contacts by means of a lithographic process, it is also possible for the necessary structures, for example the conductor tracks for a contact-making layer, to be applied directly or for exposure of a photoresist layer to be carried out using a laser rather than by using an exposure mask.

[**0037**] While this invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications and combinations of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to persons skilled in the art upon reference to the description. It is therefore intended that the appended claims encompass any such modifications or embodiments.

What is claimed is:

1. A method for producing contacts on a wafer, the method comprising:

providing a first strip structure of a first layer that overlies a second strip structure of a second layer, wherein the first strip structure is rotated at a predetermined angle with respect to the second strip structure; and

forming contacts in mutually overlapping areas of the first strip structure and the second strip structure by using the first strip structure as a mask to etch portions of the second strip structure that do not underlie the first strip structure.

2. The method of claim 1, wherein the contacts are formed without the use of any plug/hole mask.

3. The method of claim 1, wherein the first and second strip structures are formed by means of a lithographic process using a first and a second exposure mask, wherein each exposure mask has a parallel strip structure.

4. The method of claim 1, wherein the predetermined angle is a 45 degree angle.

5. The method of claim 1, wherein at least one of the first strip structure and/or second strip structure is corrugated in selected areas.

6. The method of claim 1, wherein the first and second strip structures are provided with corrections that are predetermined by a chip design in selected areas of a layer.

7. The method of claim 1, wherein the first strip structure comprises a plurality of parallel strips wherein the second strip structure comprises a plurality of parallel strips.

8. The method of claim 7, wherein the first strip structure has a different distance between one strip center and an adjacent strip center than a distance between one strip center and an adjacent strip center of the second strip structure.

9. The method of claim 8, wherein a width of the strips in the first strip structure is the same as a width of the strips in the second strip structure and wherein a space between the strips of the first strip structure is different than a space between the strips of the second strip structure.

10. The method of claim 9, wherein the space between the strips of the first strip structure is greater than the space between the strips of the second strip structure.

11. The method of claim 1, wherein forming the contacts comprises over-etching regions between strips in the second layer.

12. The method of claim 11, wherein the M0 metallization layer forms a row line for memory cells arranged in a same row.

13. A method of making a semiconductor device, the method comprising:

forming a plurality of memory cells in a checkerboard pattern, each memory cell including a contact region;

forming a plurality of conductive lines, each conductive line in the first plurality electrically coupling the contact region of each memory cell along a diagonal line of the checkerboard pattern;

forming a second plurality of conductive lines over the first plurality, each conductive line of the second plurality overlying a row of the memory cells;

using the second plurality of conductive lines as a mask, etching exposed portions of the first plurality of conductive lines such that for each row, the contact regions of that row are coupled together by an associated one of the conductive lines of the second plurality, the associated conductive line being coupled to the contact region by remaining portions of the first plurality of conductive lines.

14. The method of claim 13, wherein forming conductive lines comprises forming trenches.

15. The method of claim 13, wherein the memory cells comprises dynamic random access memory (DRAM) cells.

16. The method of claim 15, wherein the contact region comprises a bitline contact region.

17. The method of claim 13, wherein the second plurality of conductive lines extend at a 45 degree angle with respect to the first plurality of conductive lines.

18. The method of claim 13, wherein the first plurality of conductive lines has a first pitch and the second plurality of conductive lines has a second pitch that is different than the first pitch.

19. The method of claim 13, wherein the second plurality of conductive lines comprises a plurality of corrugated lines.

20. The method of claim 13, wherein the second plurality of conductive lines is formed in an M0 metallization layer.

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