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(54) **Title:** OPTICAL BENCH APPARATUS AND FABRICATION METHOD THEREFOR FOR HETEROGENEOUS LASER INTEGRATION

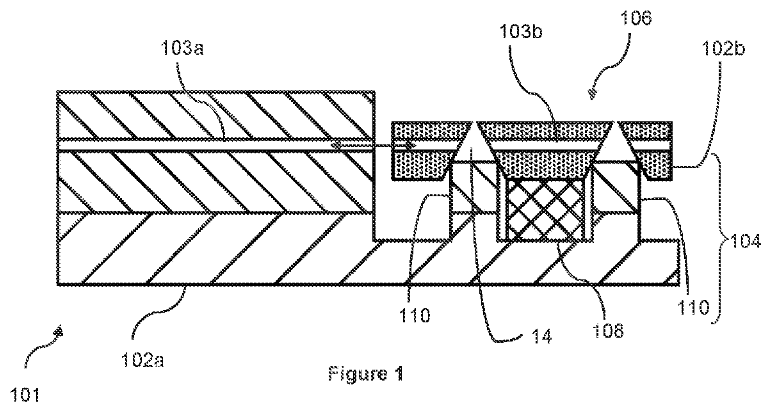

Figure 1

(57) **Abstract:** The present invention relates to an optical bench apparatus (100) for a heterogeneous laser integration. The optical bench apparatus (100) comprises a first chip (101) including a first substrate (102a), a first waveguide and an optical bench (104) formed on at least one portion of the first substrate (102a). At least one vertical alignment pillar (110) is formed on at least one portion of the optical bench (104). An active chip (106) is formed with a second waveguide. Furthermore, the present invention relates to a method for fabricating the optical bench apparatus.

OPTICAL BENCH APPARATUS AND FABRICATION METHOD THEREFOR FOR HETEROGENEOUS LASER INTEGRATION

FIELD OF THE INVENTION

The disclosures made herein relate generally to an optical apparatus, and more particularly to an optical bench apparatus and a method for fabricating an optical bench apparatus for a heterogeneous laser integration.

BACKGROUND OF THE INVENTION

In general, silicon photonics enables the realization of various passive and active optical components, such as optical waveguides, splitters, filters, wavelength multiplexer (mux)/Demultiplexer (demux), modulators etc. However, due to the silicon's material property of having an indirect bandgap, it is poorly suited for making light sources such as laser or light emitting diodes. This requires compound semiconductor material systems such as Gallium Arsenide (GaAs) or Indium Phosphide (InP). As such, to realize a complete photonic integrated circuit (PIC), several techniques have been implemented to integrate light emitters onto a single chip with other active and passive functionalities. Flip chip bonding integration is one such technology, in which light emitter chips are flipped upside down and solder-bonded onto a common substrate called optical bench, and the light is coupled between them through precisely aligned waveguides. The technique is also an important packaging technology to allow passive alignment between optical chips that is both cost effective, more reliable and make

integration multiple chips on one optical bench possible. However, it has an inherit issue of semiconductor material systems (e.g., silicon material system) not being able to emit light.

United States Patent Publication No.: US 2016/0291265 A1 discloses optical alignment of two semiconductor chips to form a hybrid semiconductor device. One of the chips is flip-chip mounted in a recess formed in a main face of the other chip. Even though the said process allows quick and accurate alignment of the chips, the process of flipping needs complex and space consuming setup, which increases the cost and complexity of the manufacturing process.

Hence, there is a need for an optical bench apparatus and fabricating method therefor allowing quicker and more accurate alignment of the chips without a need for complex and space consuming setups.

SUMMARY OF THE INVENTION

The present invention relates to an optical bench apparatus for heterogeneous laser integration. The optical bench apparatus comprises a first chip including a first substrate, a first waveguide and an optical bench on at least one portion of the first substrate and an active chip (106) formed with a second waveguide. At least one vertical alignment pillar is formed on at least one portion of the optical bench. At least one cavity is formed at a bottom portion of the active chip (106), wherein each cavity is configured to receive a top portion of a

corresponding vertical alignment pillar when the active chip is placed on the optical bench, such that the waveguides are aligned with one another to form an optical path between the first chip and the active chip.

In a preferred embodiment, the first substrate is a silicon-on-silicon substrate. The optical bench includes two Silicon dioxide (SiO_2) layers and a silicon device layer sandwiched between the SiO_2 layers.

More preferably, a thickness of the silicon device layer is in range of 220 nm to 340 nm and is top-cladded with 3 to 4 μm of SiO_2.

In one embodiment, the active chip comprises at least one of an edge-emitting laser and a photodetector.

Furthermore, the active chip and the optical bench are bonded using adhesives, wherein the adhesives include at least one of a solder paste and a metal solders.

Furthermore, the present invention relates to a method for fabricating an optical bench apparatus. The method comprises the steps of forming a first chip including a first substrate, a first waveguide and an optical bench, forming an active chip including a second waveguide and placing the active chip on the optical bench. The optical bench is on at least one portion of the first substrate

and at least one vertical alignment pillar is on at least one portion of the optical bench. The step of forming the active chip includes forming at least one cavity at a bottom portion of the active chip, wherein each cavity is configured to receive a top portion of a corresponding vertical alignment pillar when the active chip is placed on the optical bench, such that the waveguides are aligned with one another to form an optical path between the first chip and the active chip.

BRIEF DESCRIPTION OF THE ACCOMPANYING DRAWINGS

The present invention will be fully understood from the detailed description given herein below and the accompanying drawings which are given by way of illustration only, and thus are not limitative of the present invention, wherein:

FIGURE 1 shows a longitudinal sectional side view of an optical bench apparatus, according to one embodiment of the present invention.

FIGURE 2 shows a longitudinal sectional top view of an optical bench apparatus, according to one embodiment of the present invention.

FIGURE 3 is an example flow chart illustrating a method for fabricating the optical bench apparatus, according to one embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Detailed description of preferred embodiments of the present invention is disclosed herein. It should be understood, however, that the embodiments are

merely exemplary of the present invention, which may be embodied in various forms. Therefore, the details disclosed herein are not to be interpreted as limiting, but merely as the basis for the claims and for teaching one skilled in the art of the invention. The numerical data or ranges used in the specification are not to be construed as limiting. The following detailed description of the preferred embodiments will now be described in accordance with the attached drawings, either individually or in combination.

Accordingly, the embodiment herein is to provide an optical bench apparatus for a heterogeneous laser integration. The optical bench apparatus includes an optical bench formed on at least one portion of a first substrate and an active chip formed on at least one portion of a second substrate. At least one cavity is formed at a bottom portion of the active chip. At least one vertical alignment pillar is formed on at least one portion of the optical bench. When the active chip is placed on the optical bench, each cavity receives a corresponding pillar, such that a waveguide in the active chip is automatically aligned with a waveguide in the first chip, so as to provide an optical light path alignment between the two chips.

In the proposed optical bench apparatus, the optical bench apparatus including with one or multiple deeply etched pillars on the optical bench, together with an active chip with etched through cavities. Hence, the precision in optical light path alignment is achieved via the fabricated vertical alignment pillars on

the optical bench matched and aligned with the cavities on the active chip. In the proposed optical bench apparatus, the alignment between the active chip and optical bench is automatically achieved by the vertical pillars fabricated on the optical bench and the cavities fabricated on the active chip, through any conventional wafer process e.g. lithography and deep etching. Furthermore, since the cavities are formed at the bottom portion of the active chip, the active chip can be easily aligned with the optical bench without a need for flipping the active chip before mounting, which in turn avoids a need for a flipping chamber altogether while enabling easy visual alignment check, and thus minimizing cost, complexity and space requirements for the entire process.

The proposed optical bench apparatus creates a better heat dissipation channel from the bonded chip to the silicon optical bench substrate through the deep-etch recess and solder paste, which is typically an excellent heat conducting material. In the optical bench apparatus, the active chip does not need to be flipped (as required for common flip chip process), and hence, visual alignment check can be done.

Referring now to the drawings and more particularly to **FIGURE 1** through **FIGURE 2**, where similar reference characters denote corresponding features consistently throughout the figures, there are shown preferred embodiments.

FIGURE 1 and **FIGURE 2** illustrate a longitudinal sectional side view and longitudinal sectional top view of an optical bench apparatus (100), according to one embodiment of the present invention. The optical bench apparatus (100) includes a first chip (101) formed with a first substrate (102a), a first waveguide (103a) and an optical bench (104) (also called as single hosting chip), an active chip (106) and adhesives. Preferably, the first substrate (102a) is a silicon-on-silicon substrate. The active chip (106) can include, for example, but not limited to an edge-emitting laser and a photodetector. The adhesives can include, for example, but not limited to a solder paste (108) and metal solders.

The optical bench (104) is formed on at least one portion of the first substrate (102a). The active chip (106) and the optical bench (104) are bonded using the adhesives. The optical bench (104) is formed by a silicon device layer sandwiched between two silicon dioxide (SiO_2) layers. The bottom SiO_2) layer is a 3 μm thick and the top SiO_2 layer is 3 to 4 μm thick. Furthermore, thickness of the silicon device layer is in range of 220 nm to 340 nm. The at least one vertical alignment pillar (110) is formed on at least one portion of the first substrate (102a) and the at least one cavity (112) is formed at a bottom portion of the active chip (106). A shape of the at least one vertical alignment pillar (110) can be a circular shape, rectangular shape, a square shape or the like. The active chip (106) includes a second substrate (102b), wherein each cavity (112) is formed at bottom of the second substrate (102b).

Each cavity (112) is configured to receive at least top portion of the corresponding vertical alignment pillar (110). One or more sidewalls of each cavity (112) configured such that the top portion of the vertical alignment pillar (110) abuts against the sidewalls of the cavity (112) as shown in FIGURE 1, to stop the vertical alignment pillar (110) from being further inserted inside the cavity (112).

The active chip (106) is bonded onto the optical bench (104), so as to provide a heat dissipation channel in the optical bench apparatus (100) as well as to form an electrical connection between the two chips (101, 106).

In an embodiment, after the standard optical device's fabrication process of both the active chip (106) and the first chip (101), the active chip (106), equipped with the cavities (11) designed precisely to match with the vertical pillars (110) on the optical bench (104), are aligned using a die attached machine (not shown) and the active chip (106) and the optical bench (104) are bonded together using adhesives that can include solder paste (108) or metal solders, as shown in **FIGURE 1**.

In an embodiment, the proposed optical bench apparatus (100) can be used to bond and integrate one or multiple chips, or a single chip with array of multiple devices (not shown), onto the optical bench (104).

FIGURE 2 is an example flow chart (S200) illustrating a method for fabricating the optical bench apparatus (100), according to one embodiment of the present invention. The method comprises the steps of: forming a first chip (201) including a first waveguide and an optical bench, forming an active chip (202) including a second waveguide and placing the active chip on the optical bench (203), such that the two waveguides are aligned to form an optical path between the two chips. While forming the active chip, at least one cavity is formed at a bottom portion of the active chip, wherein each cavity is configured to receive a top portion of a corresponding vertical alignment pillar on the optical bench, when the active chip is placed on the optical bench, such that the waveguides are aligned with one another to form the optical path.

The first chip includes a first substrate, wherein the optical bench is on at least one portion of the first substrate and at least one vertical alignment pillar is on at least one portion of the optical bench. Preferably, the first substrate is a silicon-on-silicon substrate.

The optical bench includes two Silicon dioxide (SiO_2) layers and a silicon device layer sandwiched between the SiO_2 layers. Preferably, thickness of the silicon device layer is in a range of 220 nm to 340 nm. The silicon device layer is top-cladded with 3 to 4 μm of SiO_2. The active chip includes at least one of an edge-emitting laser and a photodetector.

The active chip is bonded to the optical bench using adhesives, wherein the adhesives include at least one of a solder paste and a metal solders e.g. gold tin solder.

In one embodiment, multiple deeply etched pillars are formed on the optical bench by any conventional fabrication process. Similarly, the cavities are etched at the bottom portion of the active chip through any conventional process. The pillars and the cavities are configured in such a way that each cavity receives at least a top portion of the corresponding pillar when the active chip is placed on the optical bench. One or more sidewalls of each cavity are configured to abut the top portion of the vertical alignment pillar when a predetermined length of the top portion of the pillar is inserted into the cavity.

By this way, the present invention ensures proper positioning of the active chip with respect to the optical bench, and thus realizing precise alignment between the waveguides without a need for flip mounting the active chip, which in turn avoids a need for a flipping chamber or assembly and thereby allowing quicker and more accurate alignment of the chips without a need for complex and space consuming setups.

The proposed method can be used to create a better heat dissipation channel from the bonded active chip to the first substrate (102a) through a deep-etch recess and the solder paste (108), which is typically an excellent heat

conducting material. Since the cavities are formed at the bottom portion of the active chip, there is no need to flip the active chip while aligning it with the first chip, while enabling easy visual alignment check.

The proposed method provides a high precision requirement ($<\pm 0.5$ um) than flip chip alignment between the active chip and the optical bench.

The terminology used herein is for the purpose of describing particular example embodiments only and is not intended to be limiting. As used herein, the singular forms "a", "an" and "the" may be intended to include the plural forms as well, unless the context clearly indicates otherwise. The terms "comprises", "comprising", “including” and “having” are inclusive and therefore specify the presence of stated features, integers, steps, operations, elements and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components and/or groups thereof. The method steps, processes and operations described herein are not to be construed as necessarily requiring their performance in the particular order discussed or illustrated, unless specifically identified as an order of performance. It is also to be understood that additional or alternative steps may be employed. The use of the expression “at least” or “at least one” suggests the use of one or more elements, as the use may be in one of the embodiments to achieve one or more of the desired objects or results.

CLAIMS

We claim:

1. An optical bench apparatus (100) for a heterogeneous laser integration, comprises:

   i. a first chip (101) including a first substrate (102a), a first waveguide (103a) and an optical bench (104) formed on at least one portion of the first substrate (102a), wherein at least one vertical alignment pillar (110) is formed on at least one portion of the optical bench (104); and

   ii. an active chip (106) formed with a second waveguide (103b), characterized in that:

   at least one cavity (112) is formed at a bottom portion of the active chip (106), wherein each cavity (112) is configured to receive a top portion of a corresponding vertical alignment pillar (110) when the active chip (106) is placed on the optical bench (104), such that the waveguides (103a, 103b) are aligned with one another to form an optical path between the first chip (101) and the active chip (106).

2. The optical bench apparatus (100) as claimed in claim 1, wherein the first substrate (102a) is a silicon-on-silicon substrate.

3. The optical bench apparatus (100) as claimed in claim 1, wherein the optical bench (104) includes two Silicon dioxide (SiO_2) layers and a silicon device layer sandwiched between the SiO_2 layers.

4. The optical bench apparatus (100) as claimed in claim 3, wherein a thickness of the silicon device layer is in the range of 220 nm to 340 nm.

5. The optical bench apparatus (100) as claimed in claim 3, wherein the silicon device layer is top-cladded with 3 to 4 μm of SiO_2.

6. The optical bench apparatus (100) as claimed in claim 1, wherein the active chip (106) comprises at least one of an edge-emitting laser and a photodetector.

7. The optical bench apparatus (100) as claimed in claim 1, wherein the active chip (106) and the optical bench (104) are bonded using adhesives, wherein the adhesives include at least one of a solder paste (108) and metal solders.

8. A method for fabricating an optical bench apparatus (100), comprises:
   i. forming a first chip (101) including a first substrate (102a), a first waveguide (103a) and an optical bench (104), wherein the optical bench (104) is on at least one portion of the first substrate (102a)

and at least one vertical alignment pillar (110) is on at least one portion of the optical bench (104);

ii. forming an active chip (106) including a second waveguide (103b); and

iii. placing the active chip (106) on the optical bench (104),

characterized in that the step of forming the active chip (106) includes:

forming at least one cavity (112) at a bottom portion of the active chip (106), wherein each cavity (112) is configured to receive a top portion of a corresponding vertical alignment pillar (110) when the active chip (106) is placed on the optical bench (104), such that the waveguides (13a, 103b) are aligned with one another to form an optical path between the first chip (101) and the active chip (106).

9. The method as claimed in claim 8, wherein the first substrate (102a) is a silicon-on-silicon substrate.

10. The method as claimed in claim 8, wherein the optical bench (104) includes two Silicon dioxide (SiO_2) layers and a silicon device layer sandwiched between the SiO_2 layers.

11. The method as claimed in claim 9, wherein a thickness of the silicon device layer is in range of 220 nm to 340 nm.

12. The method as claimed in claim 9, wherein the silicon device layer is top-cladded with 3 to 4 μm of SiO_2.

13. The method as claimed in claim 8, wherein the active chip (106) comprises at least one of an edge-emitting laser and a photodetector.

14. The method as claimed in claim 8, comprising the step of bonding the active chip (106) and the optical bench (104) using adhesives, wherein the adhesives include at least one of a solder paste (108) and a metal solders.

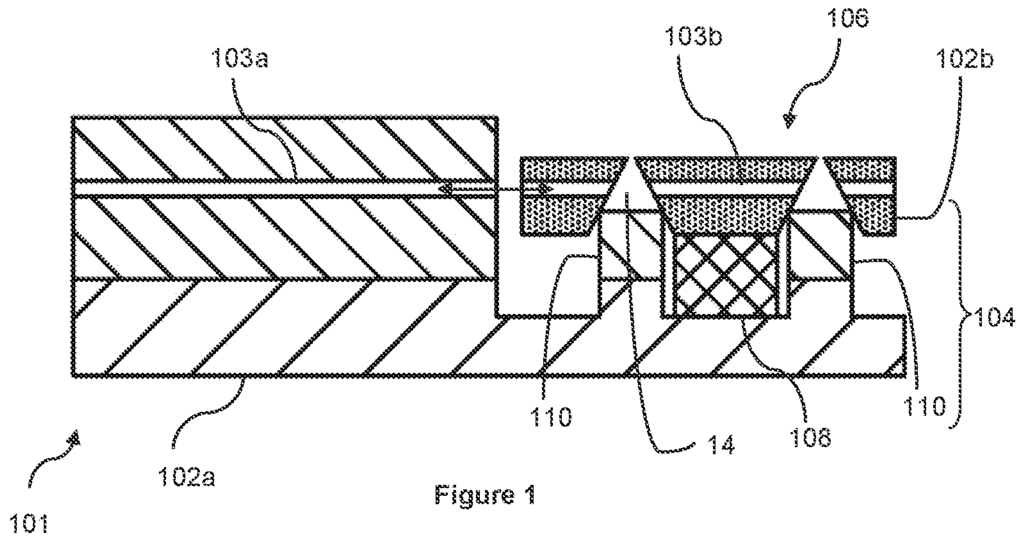

Figure 1

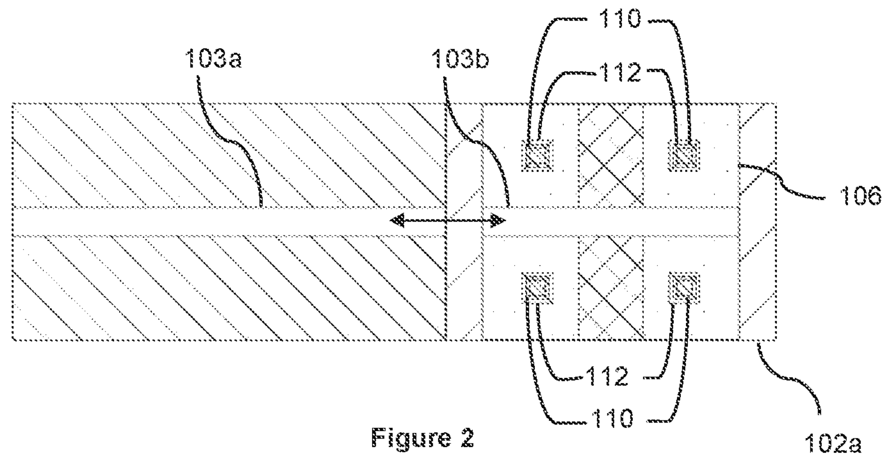

Figure 2

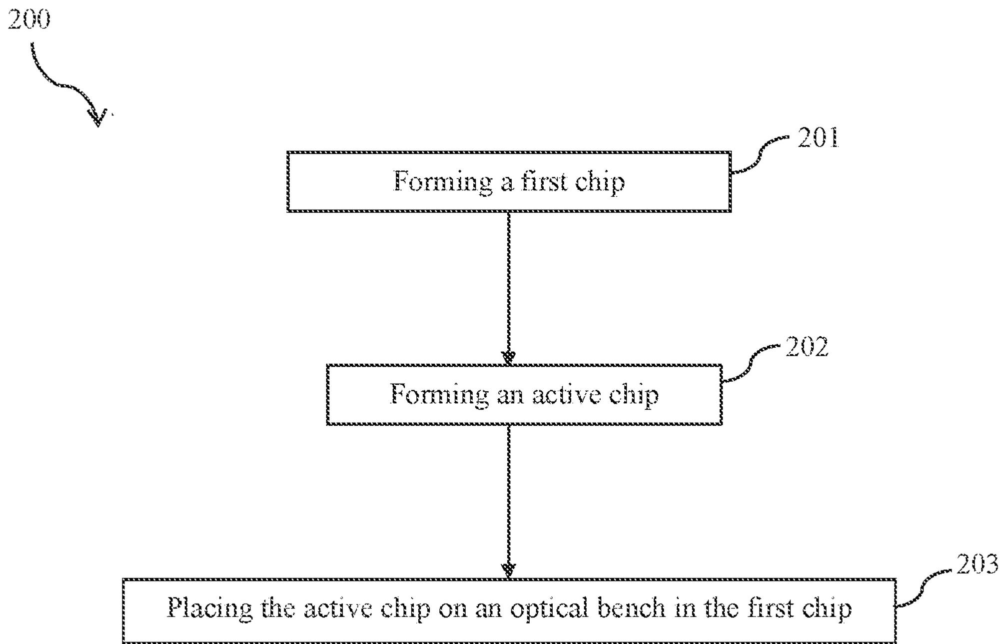

Figure 3

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SG2022/050262

A. CLASSIFICATION OF SUBJECT MATTER

G02B 6/42(2006.01)i; **H01S 5/02**(2006.01)i; **H01S 5/00**(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G02B 6/42(2006.01); G02B 6/136(2006.01); G02B 6/26(2006.01); H01J 5/02(2006.01); H01L 21/60(2006.01); H01L 27/146(2006.01); H01L 31/0236(2006.01); H01L 31/0352(2006.01)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: optical bench, chip alignment, pillar, cavity

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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A	US 2015-0063747 A1 (ACACIA COMMUNICATIONS INC.) 05 March 2015 (2015-03-05) paragraphs [0025]-[0037]; and figures 1-6	1-14
A	US 2017-0194522 A1 (SHIH-YUAN WANG et al.) 06 July 2017 (2017-07-06) paragraphs [0171]-[0347]; and figures 1-117	1-14
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☐ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:
- "A" document defining the general state of the art which is not considered to be of particular relevance
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- "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- "O" document referring to an oral disclosure, use, exhibition or other means
- "P" document published prior to the international filing date but later than the priority date claimed
- "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
- "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
- "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
- "&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
30 May 2023	**31 May 2023**

Name and mailing address of the ISA/KR	Authorized officer
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INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
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