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(54) **HYBRID WAFER DICING APPROACH USING A SPATIALLY MULTI-FOCUSED LASER BEAM LASER SCRIBING PROCESS AND PLASMA ETCH PROCESS**

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(51) **Int. Cl.**

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H01L 21/3065	(2006.01)
B23K 26/067	(2006.01)
H01L 21/308	(2006.01)

(52) **U.S. Cl.**

CPC ***H01L 21/82*** (2013.01); ***B23K 26/064*** (2015.10); ***B23K 26/0673*** (2013.01); ***H01L 21/3081*** (2013.01); ***H01L 21/3086*** (2013.01); ***H01L 21/30655*** (2013.01)

(58) **Field of Classification Search**

None

See application file for complete search history.

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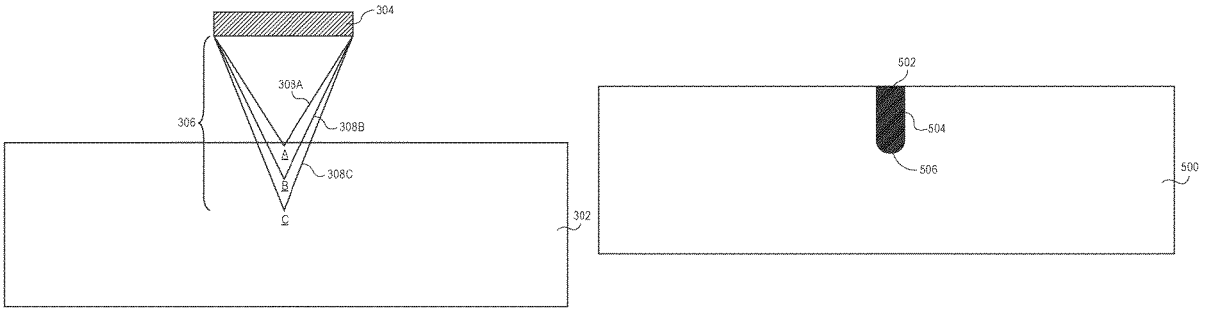
(57) **ABSTRACT**

Methods of dicing semiconductor wafers, each wafer having a plurality of integrated circuits, are described. In an example, a method of dicing a semiconductor wafer having a plurality of integrated circuits involves forming a mask above the semiconductor wafer, the mask composed of a layer covering and protecting the integrated circuits. The mask is then patterned with a spatially multi-focused laser beam laser scribing process to provide a patterned mask with gaps, exposing regions of the semiconductor wafer between the integrated circuits. The semiconductor wafer is then plasma etched through the gaps in the patterned mask to singulate the integrated circuits.

14 Claims, 10 Drawing Sheets



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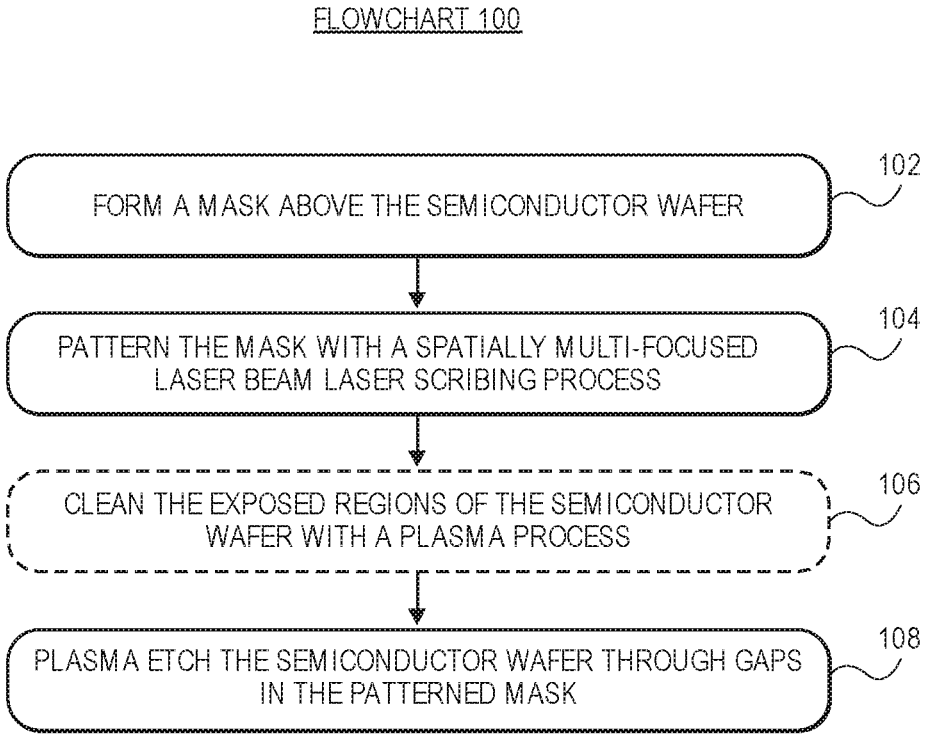

FLOWCHART 100
FORM A MASK ABOVE THE SEMICONDUCTOR WAFER
102
PATTERN THE MASK WITH A SPATIALLY MULTI-FOCUSED LASER BEAM LASER SCRIBING PROCESS
104
CLEAN THE EXPOSED REGIONS OF THE SEMICONDUCTOR WAFER WITH A PLASMA PROCESS
106
PLASMA ETCH THE SEMICONDUCTOR WAFER THROUGH GAPS IN THE PATTERNED MASK
108

FIG. 1

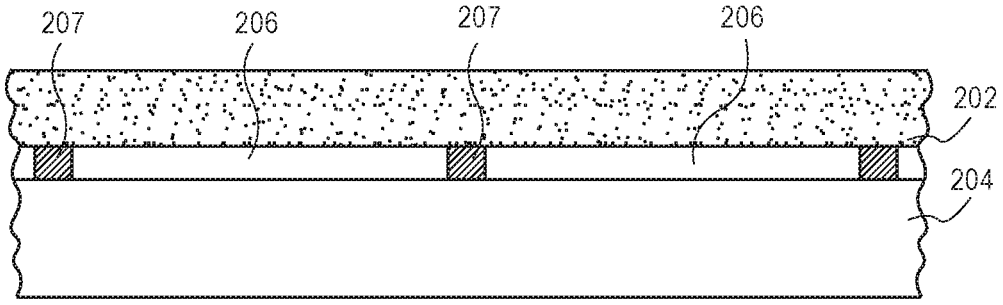


FIG. 2A

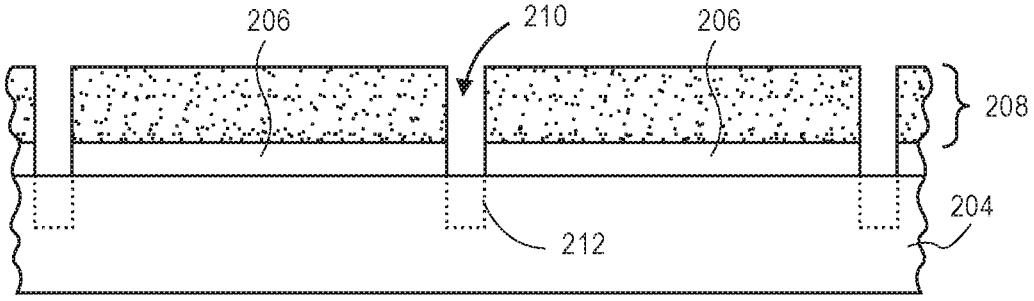


FIG. 2B

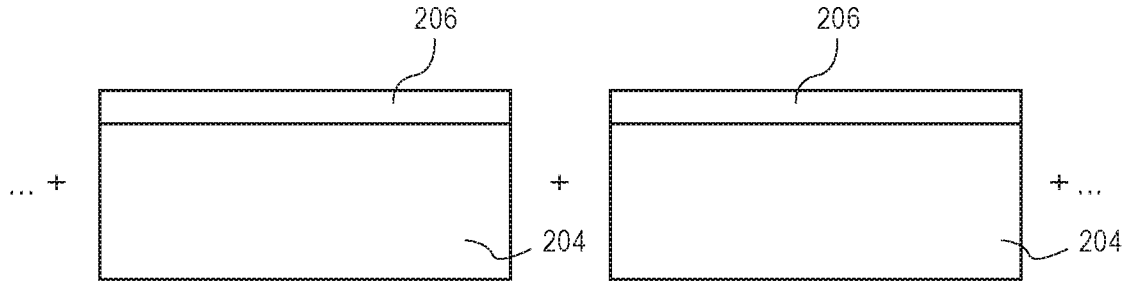


FIG. 2C

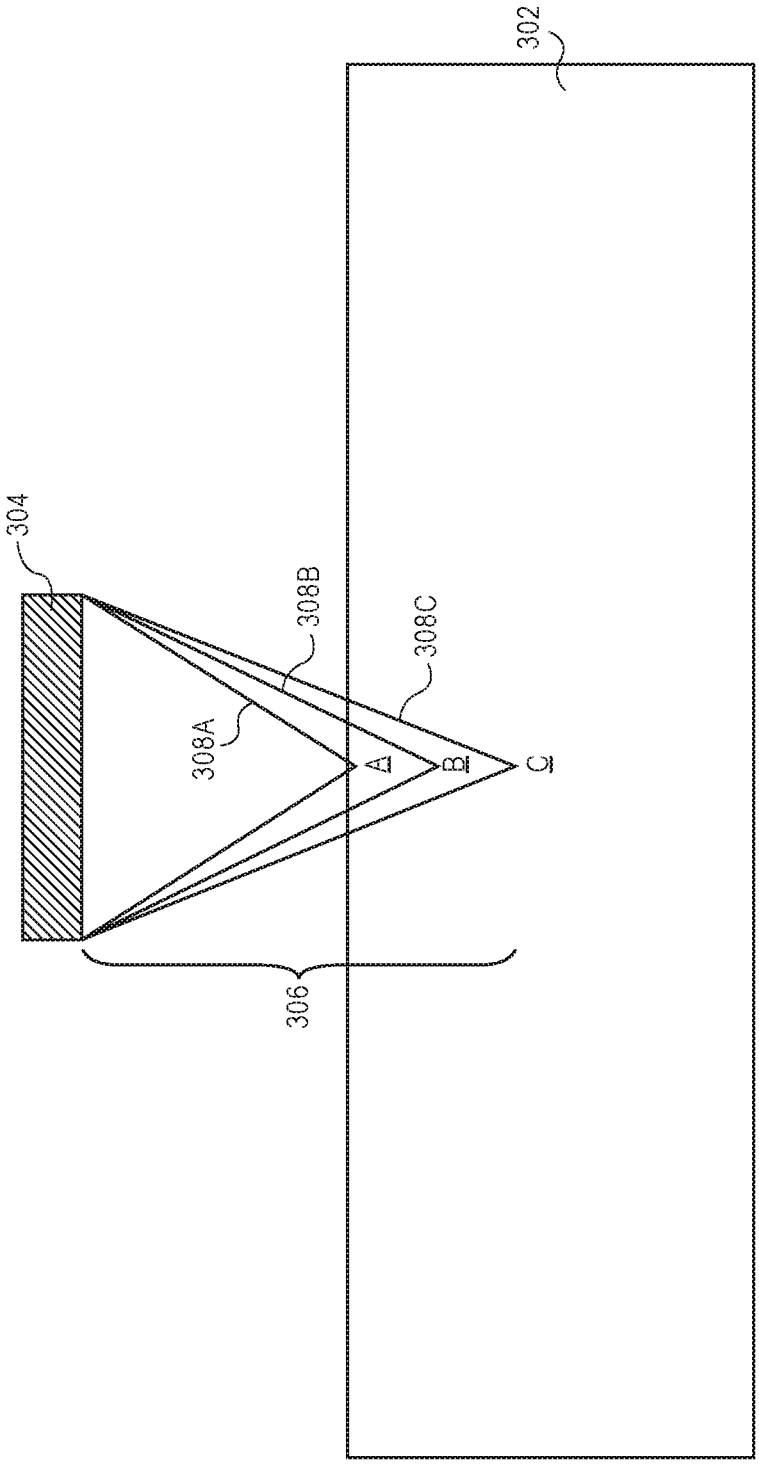


FIG. 3

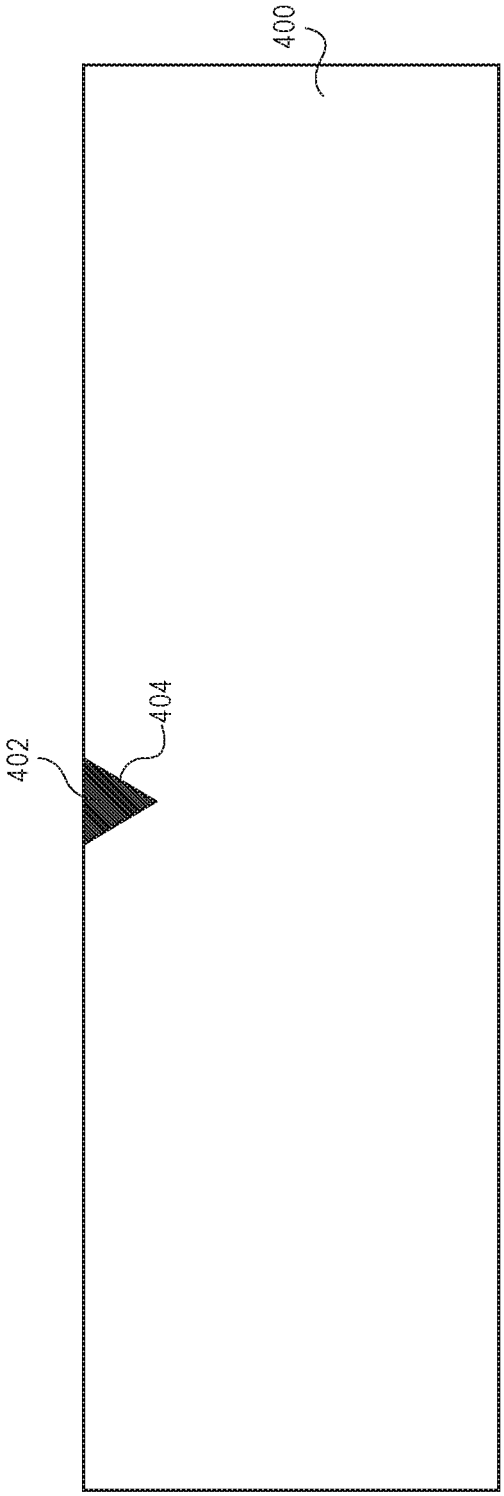


FIG. 4

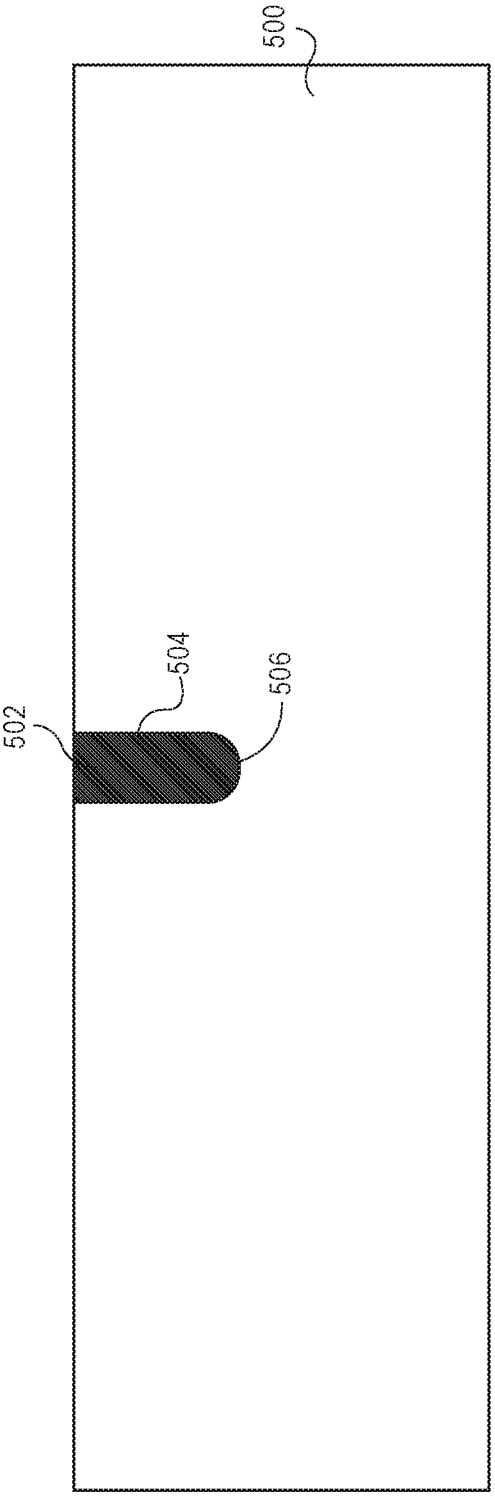
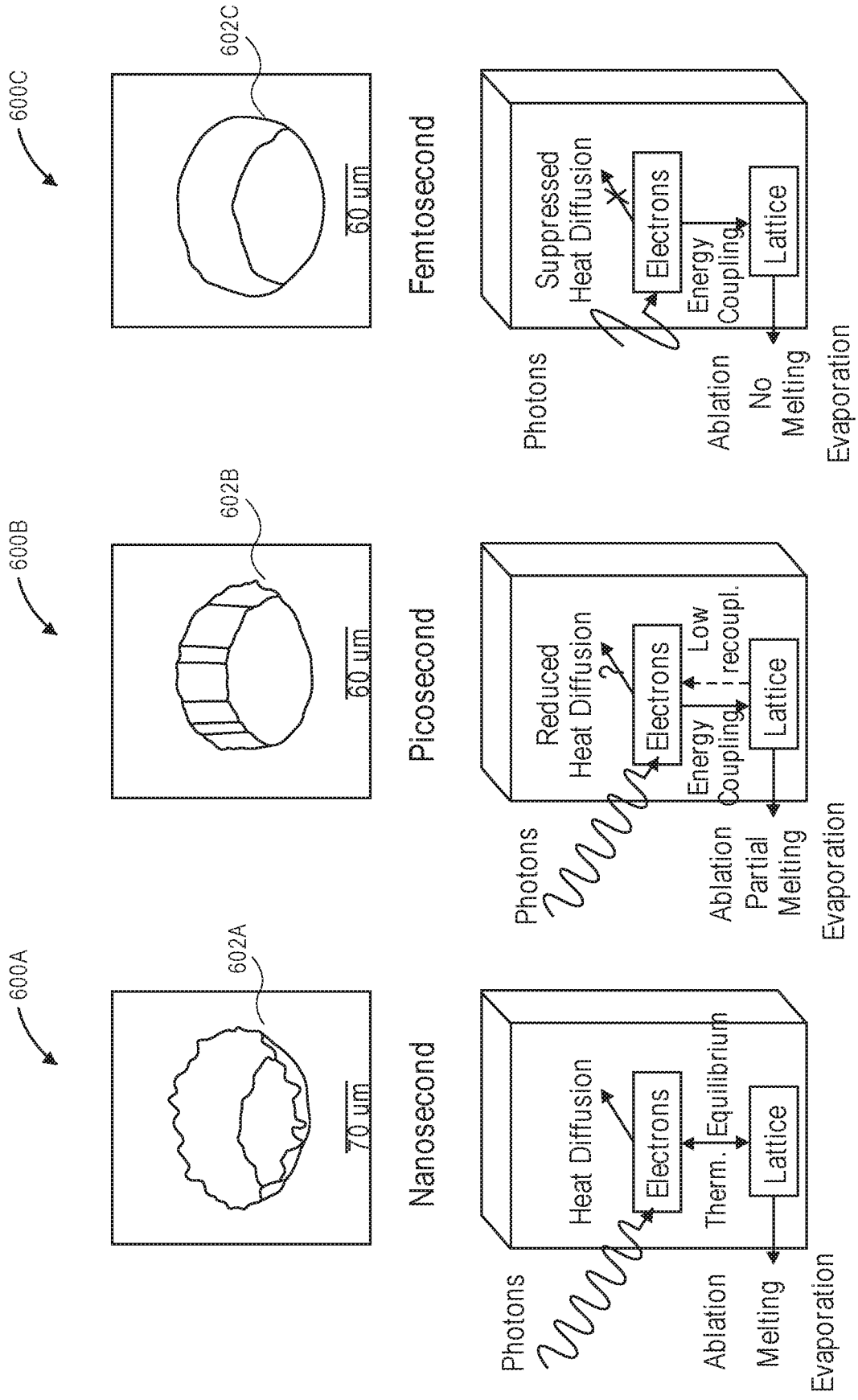


FIG. 5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602A
70 um
Nanosecond
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Electrons
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Lattice
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Melting
Evaporation
600B
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Picosecond
Photons
Reduced Heat Diffusion
Electrons
Energy Coupling
Low recoupl.
Lattice
Ablation
Partial Melting
Evaporation
600C
602C
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Femtosecond
Photons
Suppressed Heat Diffusion
Electrons
Energy Coupling
Lattice
Ablation
No Melting
Evaporation

FIG. 6

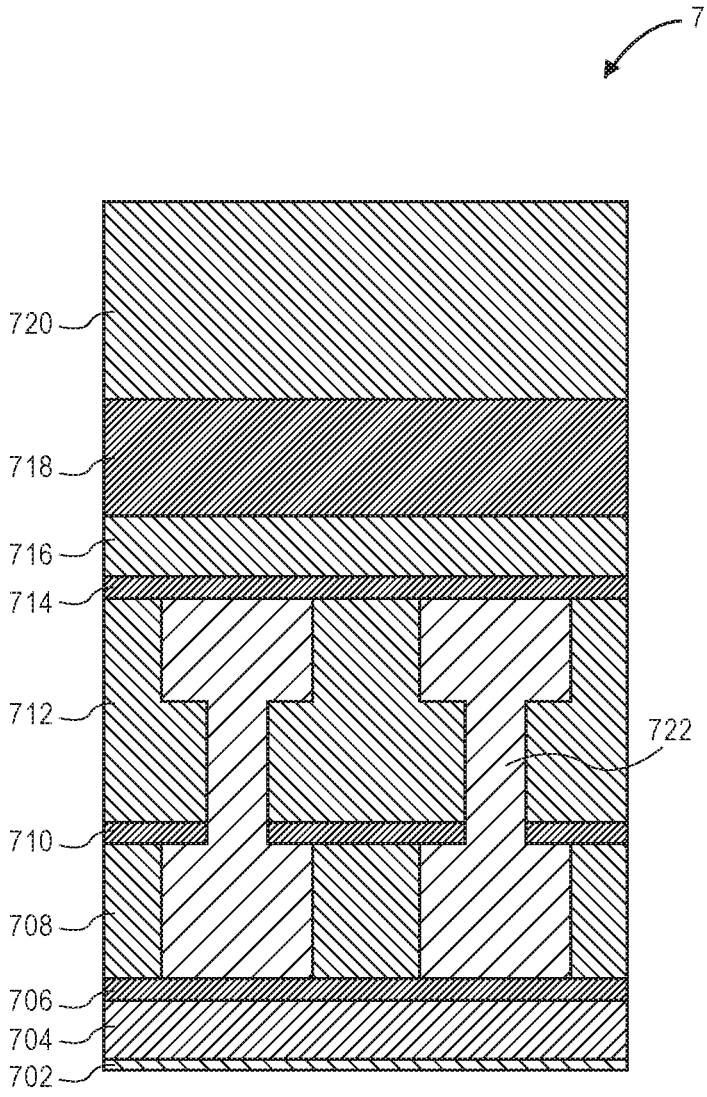


FIG. 7

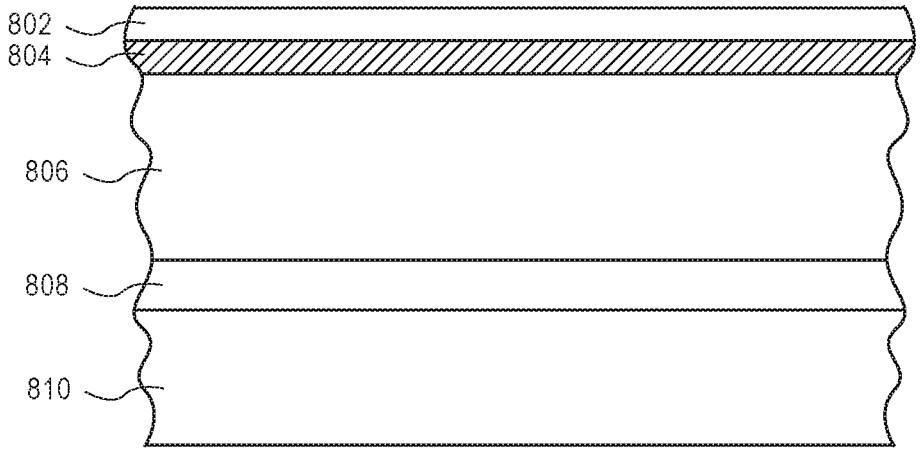


FIG. 8A

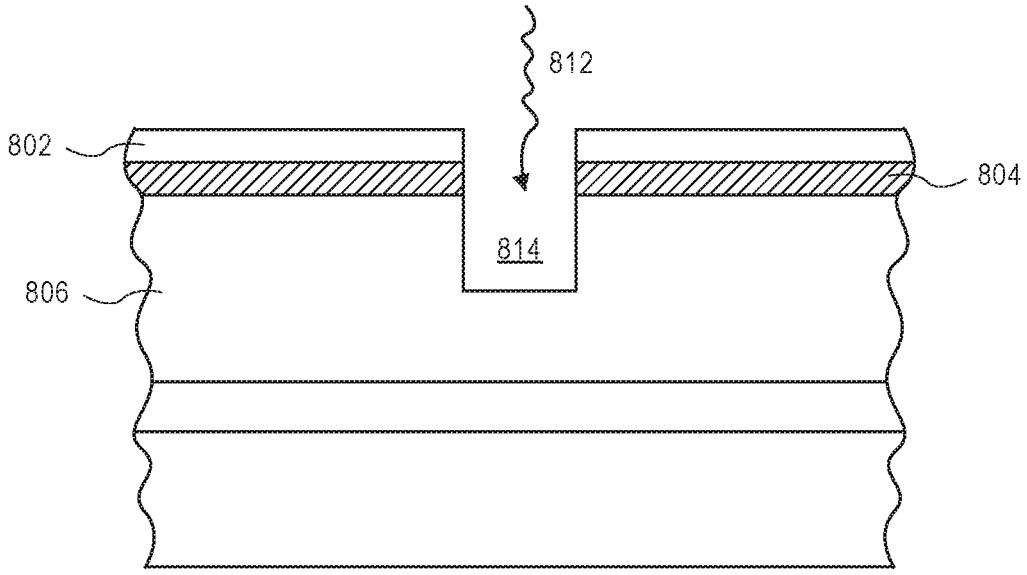


FIG. 8B

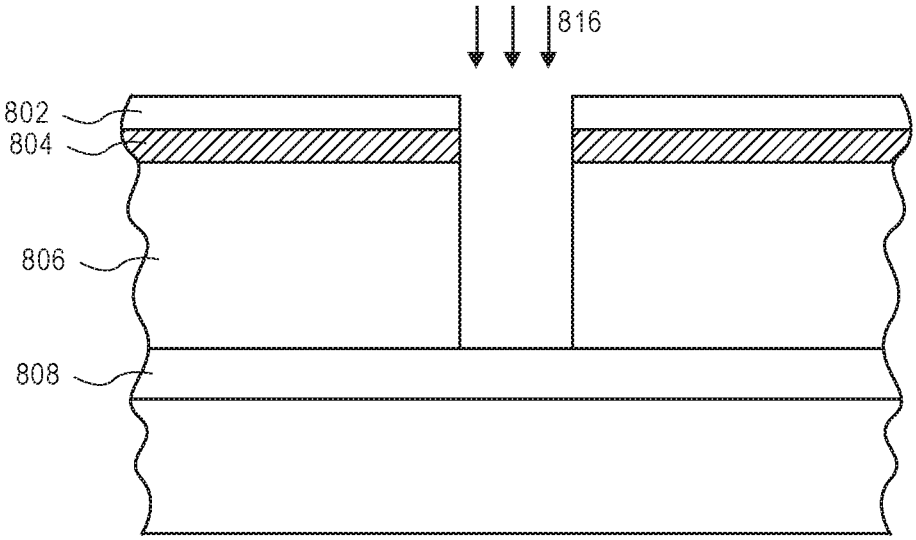


FIG. 8C

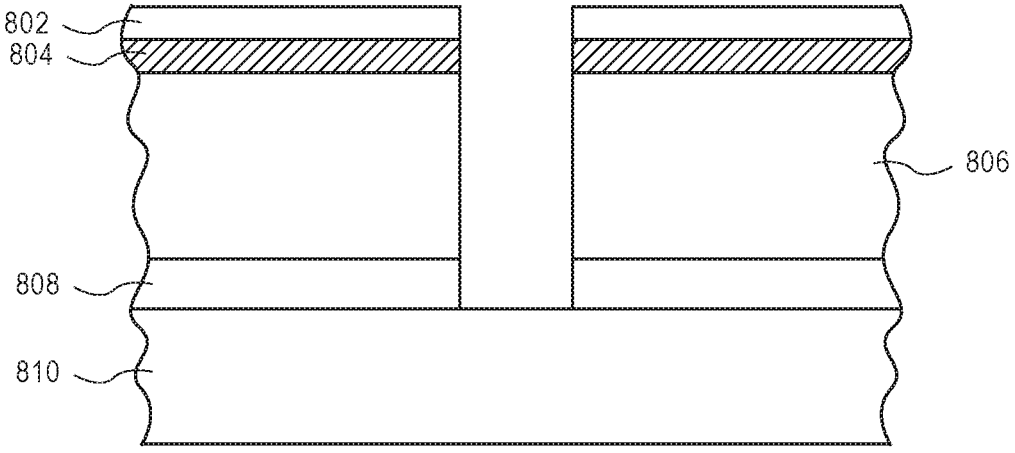
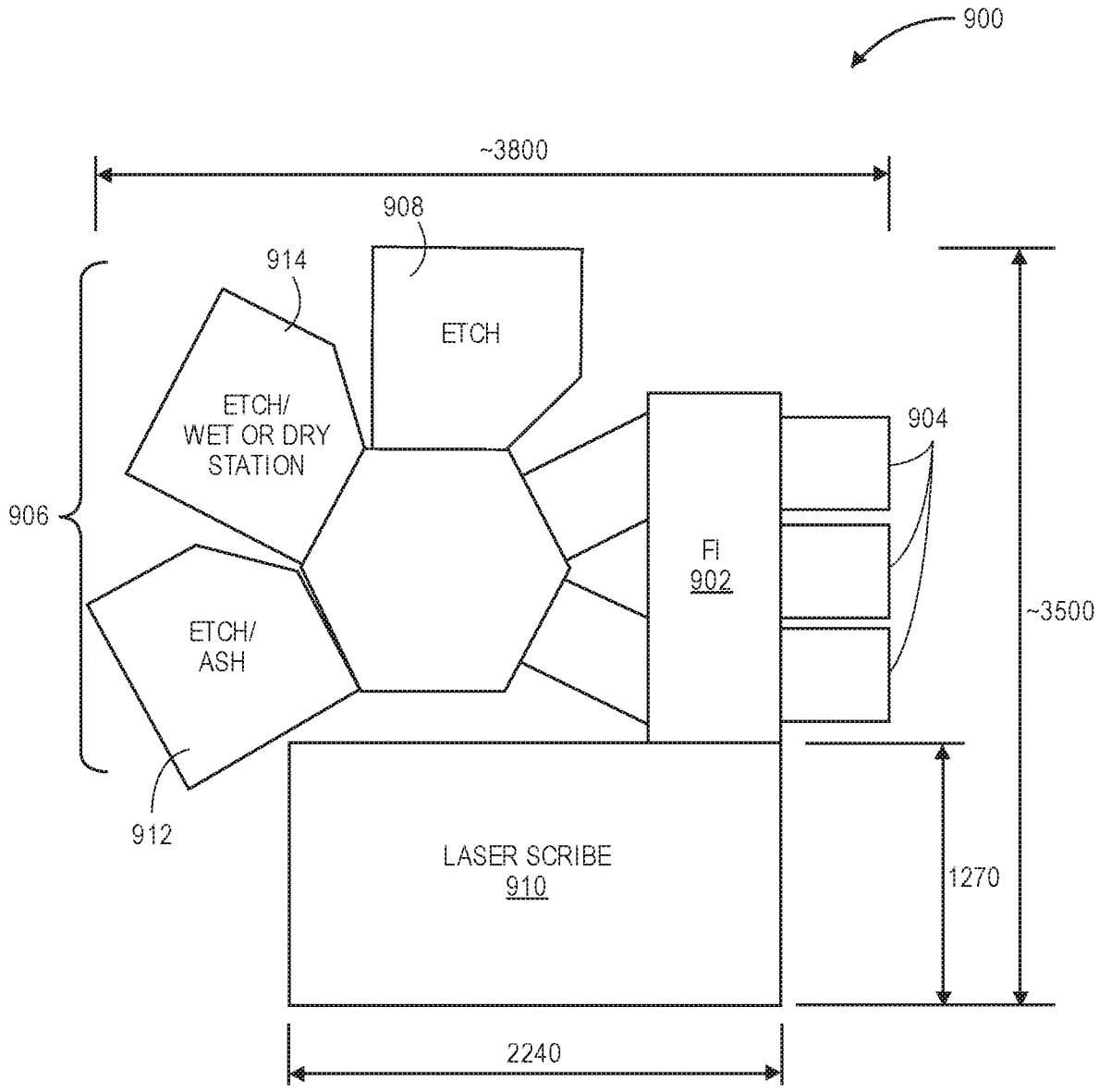


FIG. 8D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908
914
ETCH
ETCH/
WET OR DRY
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FI
902
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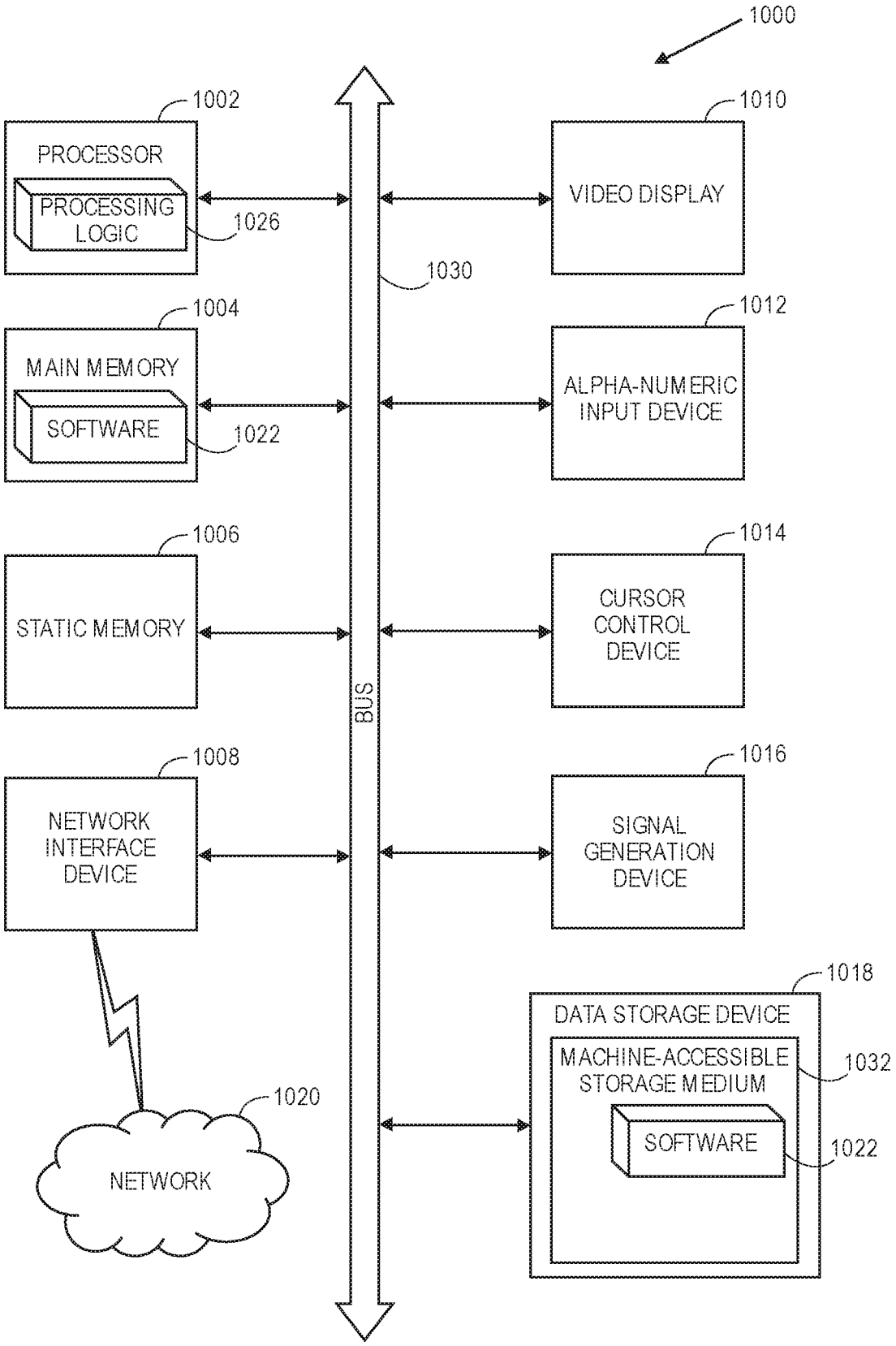
ETCH/
ASH
912
LASER SCRIBE
910
1270
2240

FIG. 9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1026
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MAIN MEMORY
SOFTWARE
1022
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STATIC MEMORY
1008
NETWORK INTERFACE DEVICE
1020
NETWORK
BUS
1030
1010
VIDEO DISPLAY
1012
ALPHA-NUMERIC INPUT DEVICE
1014
CURSOR CONTROL DEVICE
1016
SIGNAL GENERATION DEVICE
1018
DATA STORAGE DEVICE
MACHINE-ACCESSIBLE STORAGE MEDIUM
1032
SOFTWARE
1022

FIG. 10

HYBRID WAFER DICING APPROACH USING A SPATIALLY MULTI-FOCUSED LASER BEAM LASER SCRIBING PROCESS AND PLASMA ETCH PROCESS

BACKGROUND

1) Field

Embodiments of the present disclosure pertain to the field of semiconductor processing and, in particular, to methods of dicing semiconductor wafers, each wafer having a plurality of integrated circuits thereon.

2) Description of Related Art

In semiconductor wafer processing, integrated circuits are formed on a wafer (also referred to as a substrate) composed of silicon or other semiconductor material. In general, layers of various materials which are either semiconducting, conducting or insulating are utilized to form the integrated circuits. These materials are doped, deposited and etched using various well-known processes to form integrated circuits. Each wafer is processed to form a large number of individual regions containing integrated circuits known as dice.

Following the integrated circuit formation process, the wafer is "diced" to separate the individual die from one another for packaging or for use in an unpackaged form within larger circuits. The two main techniques that are used for wafer dicing are scribing and sawing. With scribing, a diamond tipped scribe is moved across the wafer surface along pre-formed scribe lines. These scribe lines extend along the spaces between the dice. These spaces are commonly referred to as "streets." The diamond scribe forms shallow scratches in the wafer surface along the streets. Upon the application of pressure, such as with a roller, the wafer separates along the scribe lines. The breaks in the wafer follow the crystal lattice structure of the wafer substrate. Scribing can be used for wafers that are about 10 mils (thousandths of an inch) or less in thickness. For thicker wafers, sawing is presently the preferred method for dicing.

With sawing, a diamond tipped saw rotating at high revolutions per minute contacts the wafer surface and saws the wafer along the streets. The wafer is mounted on a supporting member such as an adhesive film stretched across a film frame and the saw is repeatedly applied to both the vertical and horizontal streets. One problem with either scribing or sawing is that chips and gouges can form along the severed edges of the dice. In addition, cracks can form and propagate from the edges of the dice into the substrate and render the integrated circuit inoperative. Chipping and cracking are particularly a problem with scribing because only one side of a square or rectangular die can be scribed in the <110> direction of the crystalline structure. Consequently, cleaving of the other side of the die results in a jagged separation line. Because of chipping and cracking, additional spacing is required between the dice on the wafer to prevent damage to the integrated circuits, e.g., the chips and cracks are maintained at a distance from the actual integrated circuits. As a result of the spacing requirements, not as many dice can be formed on a standard sized wafer and wafer real estate that could otherwise be used for circuitry is wasted. The use of a saw exacerbates the waste of real estate on a semiconductor wafer. The blade of the saw is approximate 15 microns thick. As such, to insure that cracking and other damage surrounding the cut made by the saw does not harm the integrated circuits, three to five hundred microns often must separate the circuitry of each of the dice. Furthermore, after cutting, each die requires substantial cleaning to remove particles and other contaminants that result from the sawing process.

Plasma dicing has also been used, but may have limitations as well. For example, one limitation hampering implementation of plasma dicing may be cost. A standard lithography operation for patterning resist may render implementation cost prohibitive. Another limitation possibly hampering implementation of plasma dicing is that plasma processing of commonly encountered metals (e.g., copper) in dicing along streets can create production issues or throughput limits.

SUMMARY

Embodiments of the present disclosure include methods of, and apparatuses for, dicing semiconductor wafers.

In an embodiment, a method of dicing a semiconductor wafer having a plurality of integrated circuits involves forming a mask above the semiconductor wafer, the mask composed of a layer covering and protecting the integrated circuits. The mask is then patterned with a spatially multi-focused laser beam laser scribing process to provide a patterned mask with gaps, exposing regions of the semiconductor wafer between the integrated circuits. The semiconductor wafer is then plasma etched through the gaps in the patterned mask to singulate the integrated circuits.

In another embodiment, a method of dicing a semiconductor wafer including a plurality of integrated circuits involves laser scribing the semiconductor wafer with a spatially multi-focused laser beam laser scribing process to singulate the integrated circuits.

In another embodiment, a system for dicing a semiconductor wafer having a plurality of integrated circuits includes a factory interface. The system also includes a laser scribe apparatus coupled with the factory interface and having a laser assembly configured to provide a spatially multi-focused laser beam. The system also includes a plasma etch chamber coupled with the factory interface.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a Flowchart representing operations in a method of dicing a semiconductor wafer including a plurality of integrated circuits, in accordance with an embodiment of the present disclosure.

FIG. **2**A illustrates a cross-sectional view of a semiconductor wafer including a plurality of integrated circuits during performing of a method of dicing the semiconductor wafer, corresponding to operation **102** of the Flowchart of FIG. **1**, in accordance with an embodiment of the present disclosure.

FIG. **2**B illustrates a cross-sectional view of a semiconductor wafer including a plurality of integrated circuits during performing of a method of dicing the semiconductor wafer, corresponding to operation **104** of the Flowchart of FIG. **1**, in accordance with an embodiment of the present disclosure.

FIG. **2**C illustrates a cross-sectional view of a semiconductor wafer including a plurality of integrated circuits during performing of a method of dicing the semiconductor wafer, corresponding to operation **108** of the Flowchart of FIG. **1**, in accordance with an embodiment of the present disclosure.

FIG. **3** illustrates a cross-sectional view of a laser-scribing process using a multi-focused laser beam, in accordance with an embodiment of the present disclosure.

FIG. **4** illustrates a cross-sectional view of a laser-scribed trench in a substrate where the laser-scribed trench is formed with a single-focus laser beam.

FIG. **5** illustrates a cross-sectional view of a laser-scribed trench in a substrate where the laser-scribed trench is formed with a multi-focused laser beam, in accordance with an embodiment of the present disclosure.

FIG. **6** illustrates the effects of using a laser pulse width in the femtosecond range, picoseconds range, and nanosecond range, in accordance with an embodiment of the present disclosure.

FIG. **7** illustrates a cross-sectional view of a stack of materials that may be used in a street region of a semiconductor wafer or substrate, in accordance with an embodiment of the present disclosure.

FIGS. **8**A-**8**D illustrate cross-sectional views of various operations in a method of dicing a semiconductor wafer, in accordance with an embodiment of the present disclosure.

FIG. **9** illustrates a block diagram of a tool layout for laser and plasma dicing of wafers or substrates, in accordance with an embodiment of the present disclosure.

FIG. **10** illustrates a block diagram of an exemplary computer system, in accordance with an embodiment of the present disclosure.

DETAILED DESCRIPTION

Methods of dicing semiconductor wafers, each wafer having a plurality of integrated circuits thereon, are described. In the following description, numerous specific details are set forth, such as spatially multi-focused laser beam laser scribing approaches and plasma etching conditions and material regimes, in order to provide a thorough understanding of embodiments of the present disclosure. It will be apparent to one skilled in the art that embodiments of the present disclosure may be practiced without these specific details. In other instances, well-known aspects, such as integrated circuit fabrication, are not described in detail in order to not unnecessarily obscure embodiments of the present disclosure. Furthermore, it is to be understood that the various embodiments shown in the Figures are illustrative representations and are not necessarily drawn to scale.

A hybrid wafer or substrate dicing process involving an initial laser scribe and subsequent plasma etch may be implemented for die singulation. The laser scribe process may be used to cleanly remove a mask layer, organic and inorganic dielectric layers, and device layers. The laser etch process may then be terminated upon exposure of, or partial etch of, the wafer or substrate. The plasma etch portion of the dicing process may then be employed to etch through the bulk of the wafer or substrate, such as through bulk single crystalline silicon, to yield die or chip singulation or dicing. More specifically, one or more embodiments are directed to implementing a spatially multi-focused laser beam laser scribing process for, e.g., dicing applications.

Spatially multi-focused laser beams for wafer dicing using a hybrid laser scribing and plasma etch approach are described. To provide context, a laser scribing process may require precise focusing depth control. Currently, most scribing applications have only one focal depth setting. Uneven trench formation may result from a scribe process based on such a process. Embodiments described herein are directed to multi-focal processing in a single scribing pass. A controlled groove/trench profile can be achieved from such a scribe process.

To provide further context, a hybrid technology combining laser scribing and plasma etching can enable precise thin semiconducting device die cutting from a silicon (Si) wafer. Use of an ultra-short pulse laser can be an essential component in achieving fine scribing of a die street for subsequently singulating a wafer with a plasma etching process. The spatial profile of laser scribing can dictate the cleanness and smoothness of a singulated device die.

A single laser beam scribing process is typically associated with formation of a cone shaped opening on the surface of a Si substrate. Such a cone shape trench can undesirably provide for an uneven trench which may be less suitable for the subsequent plasma etch process. For example, for high quality of die singulation, a uniform and deep initial scribing trench may be beneficial or even essential. Embodiments described herein involve use of a multi-focused laser scribing process used to generate a deep and uniform cylindrical shaped trench opening.

Implementation of embodiments described herein can provide for a suitable scribing trench which can enable etching rate and profile uniformity during a plasma dicing process that follows initial opening or scribing by laser scribing. Advantages of implementing one or more of the embodiments described herein can include one or more of: (1) achieving a precisely controlled and refined trench profile, (2) using a diffractive optical element (DOE) to manage the cleanness and smoothness of an opening trench for a subsequent etching process, (3) a flexible scribing configuration scribing, e.g., the combination of DOE and optics can be arranged to provide a proper beam path for controlling a scribing process, (4) achieving high product quality by improving a scribed trench profile, and/or (5) adjustability of a scribed trench to match the kerf width and depth according to requirement of a subsequent etching process.

In accordance with one or more embodiments of the present disclosure, a multi-focused laser beam is created by the combination of optical elements and differential optical elements with additional optics, such as one or more lenses. The number and beam separation of multi-focused laser beams can be controlled by a diffractive optics order. In addition, beam delivery optics can be used to reconfigure the laser scribing system, to provide for a proper beam path inside the system. By controlling the overlap of multiple laser beam spots, scan speed, laser beam wavelength, etc., the proper scribed trench quality can be generated on a scribed substrate.

In an embodiment, a precisely controlled laser scribing profile enables a high quality singulated device die, as well as cost-effectiveness for the etching process. By contrast, previous implementations have involved laser usage in wafer singulation where beams only focus on a single point instead of on multiple planes. Such arrangements are significantly less configurable without fine-tuned flexibly, and can lead to increased expense required for the subsequent etching process.

Additionally, in a hybrid wafer or substrate dicing process involving an initial laser scribe and subsequent plasma etch of a coated wafer, a femtosecond laser may be applied to remove the mask and device layers on the dicing street until the silicon substrate is exposed. A plasma etch follows to separate dies to realize die singulation. Typically, a single-focus beam is used for the femtosecond laser scribing

process. However, a single-focus beam may limit process flexibility and/or trench profile control.

In accordance with one or more embodiments of the present disclosure, a scribing laser beam is multiply-focused for improving laser scribing process in hybrid laser dicing. As such, in an aspect of the present disclosure, a combination of a spatially multi-focused laser beam laser scribing process with a plasma etching process may be used to dice a semiconductor wafer into singulated integrated circuits. FIG. **1** is a Flowchart **100** representing operations in a method of dicing a semiconductor wafer including a plurality of integrated circuits, in accordance with an embodiment of the present disclosure. FIGS. **2A-2C** illustrate cross-sectional views of a semiconductor wafer including a plurality of integrated circuits during performing of a method of dicing the semiconductor wafer, corresponding to operations of Flowchart **100**, in accordance with an embodiment of the present disclosure.

Referring to operation **102** of Flowchart **100**, and corresponding FIG. **2A**, a mask **202** is formed above a semiconductor wafer or substrate **204**. The mask **202** is composed of a layer covering and protecting integrated circuits **206** formed on the surface of semiconductor wafer **204**. The mask **202** also covers intervening streets **207** formed between each of the integrated circuits **206**.

In accordance with an embodiment of the present disclosure, forming the mask **202** includes forming a layer such as, but not limited to, a photo-resist layer or an I-line patterning layer. For example, a polymer layer such as a photo-resist layer may be composed of a material otherwise suitable for use in a lithographic process. In one embodiment, the photo-resist layer is composed of a positive photo-resist material such as, but not limited to, a 248 nanometer (nm) resist, a 193 nm resist, a 157 nm resist, an extreme ultraviolet (EUV) resist, or a phenolic resin matrix with a diazonaphthoquinone sensitizer. In another embodiment, the photo-resist layer is composed of a negative photo-resist material such as, but not limited to, poly-cis-isoprene and poly-vinyl-cinnamate.

In another embodiment, forming the mask **202** involves forming a layer deposited in a plasma deposition process. For example, in one such embodiment, the mask **202** is composed of a plasma deposited Teflon or Teflon-like (polymeric CF_2) layer. In a specific embodiment, the polymeric CF_2 layer is deposited in a plasma deposition process involving the gas C_4F_8.

In another embodiment, forming the mask **202** involves forming a water-soluble mask layer. In an embodiment, the water-soluble mask layer is readily dissolvable in an aqueous media. For example, in one embodiment, the water-soluble mask layer is composed of a material that is soluble in one or more of an alkaline solution, an acidic solution, or in deionized water. In an embodiment, the water-soluble mask layer maintains its water solubility upon exposure to a heating process, such as heating approximately in the range of 50-160 degrees Celsius. For example, in one embodiment, the water-soluble mask layer is soluble in aqueous solutions following exposure to chamber conditions used in a laser and plasma etch singulation process. In one embodiment, the water-soluble mask layer is composed of a material such as, but not limited to, polyvinyl alcohol, polyacrylic acid, dextran, polymethacrylic acid, polyethylene imine, or polyethylene oxide. In a specific embodiment, the water-soluble mask layer has an etch rate in an aqueous solution approximately in the range of 1-15 microns per minute and, more particularly, approximately 1.3 microns per minute.

In another embodiment, forming the mask **202** involves forming a UV-curable mask layer. In an embodiment, the mask layer has a susceptibility to UV light that reduces an adhesiveness of the UV-curable layer by at least approximately 80%. In one such embodiment, the UV layer is composed of polyvinyl chloride or an acrylic-based material. In an embodiment, the UV-curable layer is composed of a material or stack of materials with an adhesive property that weakens upon exposure to UV light. In an embodiment, the UV-curable adhesive film is sensitive to approximately 365 nm UV light. In one such embodiment, this sensitivity enables use of LED light to perform a cure.

In an embodiment, semiconductor wafer or substrate **204** is composed of a material suitable to withstand a fabrication process and upon which semiconductor processing layers may suitably be disposed. For example, in one embodiment, semiconductor wafer or substrate **204** is composed of a group IV-based material such as, but not limited to, crystalline silicon, germanium or silicon/germanium. In a specific embodiment, providing semiconductor wafer **204** includes providing a monocrystalline silicon substrate. In a particular embodiment, the monocrystalline silicon substrate is doped with impurity atoms. In another embodiment, semiconductor wafer or substrate **204** is composed of a material such as, e.g., a material substrate used in the fabrication of light emitting diodes (LEDs).

In an embodiment, semiconductor wafer or substrate **204** has disposed thereon or therein, as a portion of the integrated circuits **206**, an array of semiconductor devices. Examples of such semiconductor devices include, but are not limited to, memory devices or complimentary metal-oxide-semiconductor (CMOS) transistors fabricated in a silicon substrate and encased in a dielectric layer. A plurality of metal interconnects may be formed above the devices or transistors, and in surrounding dielectric layers, and may be used to electrically couple the devices or transistors to form the integrated circuits **206**. Materials making up the streets **207** may be similar to or the same as those materials used to form the integrated circuits **206**. For example, streets **207** may be composed of layers of dielectric materials, semiconductor materials, and metallization. In one embodiment, one or more of the streets **207** includes test devices similar to the actual devices of the integrated circuits **206**.

Referring to operation **104** of Flowchart **100**, and corresponding FIG. **2B**, the mask **202** is patterned with a spatially multi-focused laser beam laser scribing process to provide a patterned mask **208** with gaps **210**, exposing regions of the semiconductor wafer or substrate **204** between the integrated circuits **206**. As such, the laser scribing process is used to remove the material of the streets **207** originally formed between the integrated circuits **206**. In accordance with an embodiment of the present disclosure, patterning the mask **202** with the spatially multi-focused laser beam laser scribing process includes forming trenches **212** partially into the regions of the semiconductor wafer **204** between the integrated circuits **206**, as depicted in FIG. **2B**.

Diffractive optical elements (DOE) optics can be used to generate a uniform deep trench with multi-focusing. As an example, FIG. **3** illustrates a cross-sectional view of a laser-scribing process using a multi-focused laser beam, in accordance with an embodiment of the present disclosure.

Referring to FIG. **3**, a diffractive optical element **304** is located above a substrate **302**. The diffractive optical element **304** provides a beam **306** having a first portion **308**A with a first focus depth A in substrate **302**. The diffractive optical element **304** simultaneously provides the beam **306** having a second portion **308**B with a second focus depth B

in substrate **302**. The depth B is vertically beneath the depth A. In a particular embodiment, the diffractive optical element **304** simultaneously provides the beam **306** having a third portion **308**C with a third focus depth C in substrate **302**. The depth C is vertically beneath the depth B. It is to be appreciated that yet further beam portions may be provided with corresponding additional focus depths.

Thus, with reference again to FIG. **3**, in an embodiment, a spatially multi-focused laser beam laser scribing process provides a first beam portion **308**A focused at a first depth A in a semiconductor wafer **302**, and a second beam portion **308**B focused at a second depth B in the semiconductor wafer **302**, where the second depth B is vertically beneath the first depth A. In one such embodiment, the spatially multi-focused laser beam laser scribing process further provides a third beam portion **308**C focused at a third depth C in the semiconductor wafer **302**, where the third depth C is vertically beneath the second depth B.

In an embodiment, a spatially multi-focused laser beam laser scribing process involves passing a laser beam through a diffractive optical element (DOE), such as diffractive optical element **304**. In an embodiment, a spatially multi-focused laser beam laser scribing process involves using a Gaussian source laser beam. In an such embodiment, scribing using the spatially multi-focused laser beam laser scribing process involves scribing with a spatially multi-focused femto-second based laser beam.

It is to be appreciated that embodiments described herein may be contrasted to laser scribing involving differentiated leading and trailing beam portions. For example, in an embodiment, beam portions **308**A, **308**B and **308**C of FIG. **3** are vertically aligned and not temporally spaced. It is also to be appreciated that the different depths A, B, C etc. are achieved in a single pass as opposed to additively in multiple passes.

A uniform scribed trench can be generated by a laser scribing process using multi-focus optics, such as the laser scribing process described above in association with FIG. **3**. For comparative, FIG. **4** illustrates a cross-sectional view of a laser-scribed trench in a substrate where the laser-scribed trench is formed with a single-focus laser beam.

Referring to FIG. **4**, a substrate **400** is scribed with a single-focus laser beam to form a trench **402**. Trench **402** has tapered or sloped sidewalls **404** and a pointed or vertex bottom. Such a trench **402** may be considered a non-uniform trench and may pose difficulty in a subsequent plasma etching process.

By contrast to FIG. **4**, FIG. **5** illustrates a cross-sectional view of a laser-scribed trench in a substrate where the laser-scribed trench is formed with a multi-focused laser beam, in accordance with an embodiment of the present disclosure.

Referring to FIG. **5**, a substrate **500** is scribed with a multi-focused laser beam to form a trench **402**. Trench **502** has essentially vertical sidewalls **504** and can have a rounded bottom **506**. Such a trench **502** may be considered a uniform or substantially uniform trench and may enable a highly uniform subsequent plasma etching process.

In an embodiment, a femtosecond-based laser is used as a source for a spatially multi-focused laser beam scribing process. For example, in an embodiment, a laser with a wavelength in the visible spectrum plus the ultra-violet (UV) and infra-red (IR) ranges (totaling a broadband optical spectrum) is used to provide a femtosecond-based laser pulse, which has a pulse width on the order of the femtosecond (10^{-15} seconds). In one embodiment, ablation is not, or is essentially not, wavelength dependent and is thus suitable for complex films such as films of the mask **202**, the streets **207** and, possibly, a portion of the semiconductor wafer or substrate **204**.

FIG. **6** illustrates the effects of using a laser pulse width in the femtosecond range, picosecond range, and nanosecond range, in accordance with an embodiment of the present disclosure. Referring to FIG. **6**, by using a laser beam in the femtosecond range, heat damage issues are mitigated or eliminated (e.g., minimal to no damage **602**C with femtosecond processing of a via **600**C) versus longer pulse widths (e.g., significant damage **602**A with nanosecond processing of a via **600**A). The elimination or mitigation of damage during formation of via **600**C may be due to a lack of low energy recoupling (as is seen for picosecond-based laser ablation of **600**B/**602**B) or thermal equilibrium (as is seen for nanosecond-based laser ablation), as depicted in FIG. **6**.

Laser parameters selection, such as beam profile, may be critical to developing a successful laser scribing and dicing process that minimizes chipping, microcracks and delamination in order to achieve clean laser scribe cuts. The cleaner the laser scribe cut, the smoother an etch process that may be performed for ultimate die singulation. In semiconductor device wafers, many functional layers of different material types (e.g., conductors, insulators, semiconductors) and thicknesses are typically disposed thereon. Such materials may include, but are not limited to, organic materials such as polymers, metals, or inorganic dielectrics such as silicon dioxide and silicon nitride.

A street between individual integrated circuits disposed on a wafer or substrate may include the similar or same layers as the integrated circuits themselves. For example, FIG. **7** illustrates a cross-sectional view of a stack of materials that may be used in a street region of a semiconductor wafer or substrate, in accordance with an embodiment of the present disclosure.

Referring to FIG. **7**, a street region **700** includes the top portion **702** of a silicon substrate, a first silicon dioxide layer **704**, a first etch stop layer **706**, a first low K dielectric layer **708** (e.g., having a dielectric constant of less than the dielectric constant of 4.0 for silicon dioxide), a second etch stop layer **710**, a second low K dielectric layer **712**, a third etch stop layer **714**, an undoped silica glass (USG) layer **716**, a second silicon dioxide layer **718**, and a layer of photoresist **720**, with relative thicknesses depicted. Copper metallization **722** is disposed between the first and third etch stop layers **706** and **714** and through the second etch stop layer **710**. In a specific embodiment, the first, second and third etch stop layers **706**, **710** and **714** are composed of silicon nitride, while low K dielectric layers **708** and **712** are composed of a carbon-doped silicon oxide material.

Under conventional laser irradiation (such as nanosecond-based irradiation), the materials of street **700** behave quite differently in terms of optical absorption and ablation mechanisms. For example, dielectrics layers such as silicon dioxide, is essentially transparent to all commercially available laser wavelengths under normal conditions. By contrast, metals, organics (e.g., low K materials) and silicon can couple photons very easily, particularly in response to nanosecond-based irradiation. In an embodiment, a spatially multi-focused laser beam laser scribing process is used to pattern a layer of silicon dioxide, a layer of low K material, and a layer of copper by ablating the layer of silicon dioxide prior to ablating the layer of low K material and the layer of copper.

In case that the spatially multi-focused laser beam is a femtosecond-based laser beam, in an embodiment, suitable femtosecond-based laser processes are characterized by a

high peak intensity (irradiance) that usually leads to non-linear interactions in various materials. In one such embodiment, the femtosecond laser sources have a pulse width approximately in the range of 10 femtoseconds to 500 femtoseconds, although preferably in the range of 100 femtoseconds to 400 femtoseconds. In one embodiment, the femtosecond laser sources have a wavelength approximately in the range of 1570 nanometers to 200 nanometers, although preferably in the range of 540 nanometers to 250 nanometers. In one embodiment, the laser and corresponding optical system provide a focal spot at the work surface approximately in the range of 3 microns to 15 microns, though preferably approximately in the range of 5 microns to 10 microns or between 10-15 microns.

In an embodiment, the laser source has a pulse repetition rate approximately in the range of 200 kHz to 10 MHz, although preferably approximately in the range of 500 kHz to 5 MHz. In an embodiment, the laser source delivers pulse energy at the work surface approximately in the range of 0.5 uJ to 100 uJ, although preferably approximately in the range of 1 uJ to 5 uJ. In an embodiment, the laser scribing process runs along a work piece surface at a speed approximately in the range of 500 mm/sec to 5 m/sec, although preferably approximately in the range of 600 mm/sec to 2 m/sec.

The scribing process may be run in single pass only, or in multiple passes, but, in an embodiment, preferably 1-2 passes. In one embodiment, the scribing depth in the work piece is approximately in the range of 5 microns to 50 microns deep, preferably approximately in the range of 10 microns to 20 microns deep. In an embodiment, the kerf width of the laser beam generated is approximately in the range of 2 microns to 15 microns, although in silicon wafer scribing/dicing preferably approximately in the range of 6 microns to 10 microns, measured at the device/silicon interface.

Laser parameters may be selected with benefits and advantages such as providing sufficiently high laser intensity to achieve ionization of inorganic dielectrics (e.g., silicon dioxide) and to minimize delamination and chipping caused by underlayer damage prior to direct ablation of inorganic dielectrics. Also, parameters may be selected to provide meaningful process throughput for industrial applications with precisely controlled ablation width (e.g., kerf width) and depth. In an embodiment, a spatially multi-focused laser beam laser scribing process is suitable to provide such advantages.

It is to be appreciated that the dicing or singulation process could be stopped after the above described laser scribing in a case that the laser scribing is used to pattern the mask as well as to scribe fully through the wafer or substrate in order to singulate the dies. Accordingly, further singulation processing would not be required in such a case. However, the following embodiments may be considered in cases where laser scribing alone is not implemented for total singulation.

Referring now to optional operation **106** of Flowchart **100**, an intermediate post mask-opening cleaning operation is performed. In an embodiment, the post mask-opening cleaning operation is a plasma-based cleaning process. In a first example, as described below, the plasma-based cleaning process is reactive to the regions of the substrate **204** exposed by the gaps **210**. In the case of a reactive plasma-based cleaning process, the cleaning process itself may form or extend trenches **212** in the substrate **204** since the reactive plasma-based cleaning operation is at least somewhat of an etchant for the substrate **204**. In a second, different, example, as is also described below, the plasma-based cleaning process is non-reactive to the regions of the substrate **204** exposed by the gaps **210**.

In accordance with a first embodiment, the plasma-based cleaning process is reactive to exposed regions of the substrate **204** in that the exposed regions are partially etched during the cleaning process. In one such embodiment, Ar or another non-reactive gas (or the mix) is combined with SF_6 for a highly-biased plasma treatment for cleaning of scribed openings. The plasma treatment using mixed gases Ar+SF_6 under high-bias power is performed for bombarding mask-opened regions to achieve cleaning of the mask-opened regions. In the reactive breakthrough process, both physical bombardment from Ar and SF_6 along with chemical etching due to SF_6 and F-ions contribute to cleaning of mask-opened regions. The approach may be suitable for photoresist or plasma-deposited Teflon masks **202**, where breakthrough treatment leads to fairly uniform mask thickness reduction and a gentle Si etch. Such a breakthrough etch process, however, may not be best suited for water soluble mask materials.

In accordance with a second embodiment, the plasma-based cleaning process is non-reactive to exposed regions of the substrate **204** in that the exposed regions are not or only negligible etched during the cleaning process. In one such embodiment, only non-reactive gas plasma cleaning is used. For example, Ar or another non-reactive gas (or the mix) is used to perform a highly-biased plasma treatment both for mask condensation and cleaning of scribed openings. The approach may be suitable for water-soluble masks or for thinner plasma-deposited Teflon **202**. In another such embodiment, separate mask condensation and scribed trench cleaning operations are used, e.g., an Ar or non-reactive gas (or the mix) highly-biased plasma treatment for mask condensation is first performed, and then an Ar+SF_6 plasma cleaning of a laser scribed trench is performed. This embodiment may be suitable for cases where Ar-cleaning is not sufficient for trench cleaning due to too thick of a mask material. Cleaning efficiency is improved for thinner masks, but mask etch rate is much lower, with almost no consumption in a subsequent deep silicon etch process. In yet another such embodiment, three-operation cleaning is performed: (a) Ar or non-reactive gas (or the mix) highly-biased plasma treatment for mask condensation, (b) Ar+SF_6 highly-biased plasma cleaning of laser scribed trenches, and (c) Ar or non-reactive gas (or the mix) highly-biased plasma treatment for mask condensation. In accordance with another embodiment of the present disclosure, a plasma cleaning operation involves first use of a reactive plasma cleaning treatment, such as described above in the first aspect of operation **106**. The reactive plasma cleaning treatment is then followed by a non-reactive plasma cleaning treatment such as described in association with the second aspect of operation **106**.

Referring to operation **108** of Flowchart **100**, and corresponding FIG. **2**C, the semiconductor wafer **204** is etched through the gaps **210** in the patterned mask **208** to singulate the integrated circuits **206**. In accordance with an embodiment of the present disclosure, etching the semiconductor wafer **204** includes ultimately etching entirely through semiconductor wafer **204**, as depicted in FIG. **2**C, by etching the trenches **212** initially formed with the spatially multi-focused laser beam laser scribing process.

In an embodiment, patterning the mask with the laser scribing process involves forming trenches in the regions of the semiconductor wafer between the integrated circuits, and plasma etching the semiconductor wafer involves extending

the trenches to form corresponding trench extensions. In one such embodiment, each of the trenches has a width, and each of the corresponding trench extensions has the width.

In accordance with an embodiment of the present disclosure, the resulting roughness of mask opening from laser scribing can impact die sidewall quality resulting from the subsequent formation of a plasma etched trench. Lithographically opened masks often have smooth profiles, leading to smooth corresponding sidewalls of a plasma etched trench. By contrast, a conventional laser opened mask can have a very rough profile along a scribing direction if improper laser process parameters are selected (such as spot overlap, leading to rough sidewall of plasma etched trench horizontally). Although the surface roughness can be smoothened by additional plasma processes, there is a cost and throughput hit to remedying such issues. Accordingly, embodiments described herein may be advantageous in providing a smoother scribing process and/or more reliable trench formation process from the laser scribing portion of the singulation process.

In an embodiment, etching the semiconductor wafer **204** includes using a plasma etching process. In one embodiment, a through-silicon via type etch process is used. For example, in a specific embodiment, the etch rate of the material of semiconductor wafer **204** is greater than 25 microns per minute. An ultra-high-density plasma source may be used for the plasma etching portion of the die singulation process. An example of a process chamber suitable to perform such a plasma etch process is the Applied Centura® Silvia™ Etch system available from Applied Materials of Sunnyvale, Calif., USA. The Applied Centura® Silvia™ Etch system combines the capacitive and inductive RF coupling, which gives much more independent control of the ion density and ion energy than was possible with the capacitive coupling only, even with the improvements provided by magnetic enhancement. This combination enables effective decoupling of the ion density from ion energy, so as to achieve relatively high density plasmas without the high, potentially damaging, DC bias levels, even at very low pressures. This results in an exceptionally wide process window. However, any plasma etch chamber capable of etching silicon may be used. In an exemplary embodiment, a deep silicon etch is used to etch a single crystalline silicon substrate or wafer **204** at an etch rate greater than approximately 40% of conventional silicon etch rates while maintaining essentially precise profile control and virtually scallop-free sidewalls. In a specific embodiment, a through-silicon via type etch process is used. The etch process is based on a plasma generated from a reactive gas, which generally a fluorine-based gas such as SF_6, C_4F_8, CHF_3, XeF_2, or any other reactant gas capable of etching silicon at a relatively fast etch rate. In an embodiment, the mask layer **208** is removed after the singulation process, as depicted in FIG. **2**C. In another embodiment, the plasma etching operation described in association with FIG. **2**C employs a conventional Bosch-type dep/etch/dep process to etch through the substrate **204**. Generally, a Bosch-type process consists of three sub-operations: deposition, a directional bombardment etch, and isotropic chemical etch which is run through many iterations (cycles) until silicon is etched through.

Accordingly, referring again to Flowchart **100** and FIGS. **2**A-**2**C, wafer dicing may be preformed by initial ablation using a spatially multi-focused laser beam laser scribing process to ablate through a mask layer, through wafer streets (including metallization), and partially into a silicon substrate. Die singulation may then be completed by subsequent through-silicon deep plasma etching. A specific example of a materials stack for dicing is described below in association with FIGS. **8**A-**8**D, in accordance with an embodiment of the present disclosure.

Referring to FIG. **8**A, a materials stack for hybrid laser ablation and plasma etch dicing includes a mask layer **802**, a device layer **804**, and a substrate **806**. The mask layer, device layer, and substrate are disposed above a die attach film **808** which is affixed to a backing tape **810**. In an embodiment, the mask layer **802** is a water soluble layer such as the water soluble layers described above in association with mask **202**. The device layer **804** includes an inorganic dielectric layer (such as silicon dioxide) disposed above one or more metal layers (such as copper layers) and one or more low K dielectric layers (such as carbon-doped oxide layers). The device layer **804** also includes streets arranged between integrated circuits, the streets including the same or similar layers to the integrated circuits. The substrate **806** is a bulk single-crystalline silicon substrate.

In an embodiment, the bulk single-crystalline silicon substrate **806** is thinned from the backside prior to being affixed to the die attach film **808**. The thinning may be performed by a backside grind process. In one embodiment, the bulk single-crystalline silicon substrate **806** is thinned to a thickness approximately in the range of 50-100 microns. It is important to note that, in an embodiment, the thinning is performed prior to a laser ablation and plasma etch dicing process. In an embodiment, the photo-resist layer **802** has a thickness of approximately 5 microns and the device layer **804** has a thickness approximately in the range of 2-3 microns. In an embodiment, the die attach film **808** (or any suitable substitute capable of bonding a thinned or thin wafer or substrate to the backing tape **810**) has a thickness of approximately 20 microns.

Referring to FIG. **8**B, the mask **802**, the device layer **804** and a portion of the substrate **806** are patterned with a spatially multi-focused laser beam laser scribing process **812** to form trenches **814** in the substrate **806**. Referring to FIG. **8**C, a through-silicon deep plasma etch process **816** is used to extend the trench **814** down to the die attach film **808**, exposing the top portion of the die attach film **808** and singulating the silicon substrate **806**. The device layer **804** is protected by the mask layer **802** during the through-silicon deep plasma etch process **816**.

Referring to FIG. **8**D, the singulation process may further include patterning the die attach film **808**, exposing the top portion of the backing tape **810** and singulating the die attach film **808**. In an embodiment, the die attach film is singulated by a laser process or by an etch process. Further embodiments may include subsequently removing the singulated portions of substrate **806** (e.g., as individual integrated circuits) from the backing tape **810**. In one embodiment, the singulated die attach film **808** is retained on the back sides of the singulated portions of substrate **806**. Other embodiments may include removing the mask layer **802** from the device layer **804**. In an alternative embodiment, in the case that substrate **806** is thinner than approximately 50 microns, the spatially multi-focused laser beam laser scribing process **812** is used to completely singulate substrate **806** without the use of an additional plasma process.

A single process tool may be configured to perform many or all of the operations in a spatially multi-focused laser beam ablation and plasma etch singulation process. For example, FIG. **9** illustrates a block diagram of a tool layout for laser and plasma dicing of wafers or substrates, in accordance with an embodiment of the present disclosure.

Referring to FIG. **9**, a process tool **900** includes a factory interface **902** (FI) having a plurality of load locks **904** coupled therewith. A cluster tool **906** is coupled with the factory interface **902**. The cluster tool **906** includes one or more plasma etch chambers, such as plasma etch chamber **908**. A laser scribe apparatus **910** is also coupled to the factory interface **902**. The overall footprint of the process tool **900** may be, in one embodiment, approximately 3500 millimeters (3.5 meters) by approximately 3800 millimeters (3.8 meters), as depicted in FIG. **9**.

In an embodiment, the laser scribe apparatus **910** houses a laser assembly configured to provide a spatially multi-focused laser beam. In one such embodiment, the laser assembly is configured to provide the spatially multi-focused laser beam having a first beam portion focused at a first depth, and a second beam portion focused at a second depth, the second depth vertically beneath the first depth, e.g., as is described in association with FIG. **3**. In a further such embodiment, the laser assembly is configured to provide a third beam portion focused at a third depth, the third depth vertically beneath the second depth, e.g., as is also described in association with FIG. **3**. In an embodiment, the laser assembly includes a diffractive optical element (DOE). In an embodiment, the laser assembly includes a Gaussian source laser beam. In an embodiment, the laser assembly includes a femto-second source laser beam.

In an embodiment, the laser is suitable for performing a laser ablation portion of a hybrid laser and etch singulation process, such as the laser ablation processes described above. In one embodiment, a moveable stage is also included in laser scribe apparatus **910**, the moveable stage configured for moving a wafer or substrate (or a carrier thereof) relative to the laser. In a specific embodiment, the laser is also moveable. The overall footprint of the laser scribe apparatus **910** may be, in one embodiment, approximately 2240 millimeters by approximately 1270 millimeters, as depicted in FIG. **9**.

In an embodiment, the one or more plasma etch chambers **908** is configured for etching a wafer or substrate through the gaps in a patterned mask to singulate a plurality of integrated circuits. In one such embodiment, the one or more plasma etch chambers **908** is configured to perform a deep silicon etch process. In a specific embodiment, the one or more plasma etch chambers **808** is an Applied Centura® Silvia™ Etch system, available from Applied Materials of Sunnyvale, Calif., USA. The etch chamber may be specifically designed for a deep silicon etch used to create singulate integrated circuits housed on or in single crystalline silicon substrates or wafers. In an embodiment, a high-density plasma source is included in the plasma etch chamber **908** to facilitate high silicon etch rates. In an embodiment, more than one etch chamber is included in the cluster tool **906** portion of process tool **900** to enable high manufacturing throughput of the singulation or dicing process.

The factory interface **902** may be a suitable atmospheric port to interface between an outside manufacturing facility with laser scribe apparatus **910** and cluster tool **906**. The factory interface **902** may include robots with arms or blades for transferring wafers (or carriers thereof) from storage units (such as front opening unified pods) into either cluster tool **906** or laser scribe apparatus **910**, or both.

Cluster tool **906** may include other chambers suitable for performing functions in a method of singulation. For example, in one embodiment, in place of an additional etch chamber, a deposition chamber **912** is included. The deposition chamber **912** may be configured for mask deposition on or above a device layer of a wafer or substrate prior to laser scribing of the wafer or substrate. In one such embodiment, the deposition chamber **912** is suitable for depositing a photo-resist layer. In another embodiment, in place of an additional etch chamber, a wet/dry station **914** is included. The wet/dry station may be suitable for cleaning residues and fragments, or for removing a mask, subsequent to a laser scribe and plasma etch singulation process of a substrate or wafer. In yet another embodiment, in place of an additional deep silicon etch chamber, a plasma etch chamber is included and is configured for performing a plasma-based cleaning process. In an embodiment, a metrology station is also included as a component of process tool **900**.

Embodiments of the present disclosure may be provided as a computer program product, or software, that may include a machine-readable medium having stored thereon instructions, which may be used to program a computer system (or other electronic devices) to perform a process according to embodiments of the present disclosure. In one embodiment, the computer system is coupled with process tool **900** described in association with FIG. **9**. A machine-readable medium includes any mechanism for storing or transmitting information in a form readable by a machine (e.g., a computer). For example, a machine-readable (e.g., computer-readable) medium includes a machine (e.g., a computer) readable storage medium (e.g., read only memory ("ROM"), random access memory ("RAM"), magnetic disk storage media, optical storage media, flash memory devices, etc.), a machine (e.g., computer) readable transmission medium (electrical, optical, acoustical or other form of propagated signals (e.g., infrared signals, digital signals, etc.)), etc.

FIG. **10** illustrates a diagrammatic representation of a machine in the exemplary form of a computer system **1000** within which a set of instructions, for causing the machine to perform any one or more of the methodologies described herein, may be executed. In alternative embodiments, the machine may be connected (e.g., networked) to other machines in a Local Area Network (LAN), an intranet, an extranet, or the Internet. The machine may operate in the capacity of a server or a client machine in a client-server network environment, or as a peer machine in a peer-to-peer (or distributed) network environment. The machine may be a personal computer (PC), a tablet PC, a set-top box (STB), a Personal Digital Assistant (PDA), a cellular telephone, a web appliance, a server, a network router, switch or bridge, or any machine capable of executing a set of instructions (sequential or otherwise) that specify actions to be taken by that machine. Further, while only a single machine is illustrated, the term "machine" shall also be taken to include any collection of machines (e.g., computers) that individually or jointly execute a set (or multiple sets) of instructions to perform any one or more of the methodologies described herein.

The exemplary computer system **1000** includes a processor **1002**, a main memory **1004** (e.g., read-only memory (ROM), flash memory, dynamic random access memory (DRAM) such as synchronous DRAM (SDRAM) or Rambus DRAM (RDRAM), etc.), a static memory **1006** (e.g., flash memory, static random access memory (SRAM), MRAM, etc.), and a secondary memory **1018** (e.g., a data storage device), which communicate with each other via a bus **1030**.

Processor **1002** represents one or more general-purpose processing devices such as a microprocessor, central processing unit, or the like. More particularly, the processor **1002** may be a complex instruction set computing (CISC) microprocessor, reduced instruction set computing (RISC)

microprocessor, very long instruction word (VLIW) microprocessor, processor implementing other instruction sets, or processors implementing a combination of instruction sets. Processor **1002** may also be one or more special-purpose processing devices such as an application specific integrated circuit (ASIC), a field programmable gate array (FPGA), a digital signal processor (DSP), network processor, or the like. Processor **1002** is configured to execute the processing logic **1026** for performing the operations described herein.

The computer system **1000** may further include a network interface device **1008**. The computer system **1000** also may include a video display unit **1010** (e.g., a liquid crystal display (LCD), a light emitting diode display (LED), or a cathode ray tube (CRT)), an alphanumeric input device **1012** (e.g., a keyboard), a cursor control device **1014** (e.g., a mouse), and a signal generation device **1016** (e.g., a speaker).

The secondary memory **1018** may include a machine-accessible storage medium (or more specifically a computer-readable storage medium) **1032** on which is stored one or more sets of instructions (e.g., software **1022**) embodying any one or more of the methodologies or functions described herein. The software **1022** may also reside, completely or at least partially, within the main memory **1004** and/or within the processor **1002** during execution thereof by the computer system **1000**, the main memory **1004** and the processor **1002** also constituting machine-readable storage media. The software **1022** may further be transmitted or received over a network **1020** via the network interface device **1008**.

While the machine-accessible storage medium **1032** is shown in an exemplary embodiment to be a single medium, the term "machine-readable storage medium" should be taken to include a single medium or multiple media (e.g., a centralized or distributed database, and/or associated caches and servers) that store the one or more sets of instructions. The term "machine-readable storage medium" shall also be taken to include any medium that is capable of storing or encoding a set of instructions for execution by the machine and that cause the machine to perform any one or more of the methodologies of the present disclosure. The term "machine-readable storage medium" shall accordingly be taken to include, but not be limited to, solid-state memories, and optical and magnetic media.

In accordance with an embodiment of the present disclosure, a machine-accessible storage medium has instructions stored thereon which cause a data processing system to perform a method of dicing a semiconductor wafer having a plurality of integrated circuits. The method includes forming a mask above the semiconductor wafer, the mask composed of a layer covering and protecting the integrated circuits. The mask is then patterned with a spatially multi-focused laser beam laser scribing process to provide a patterned mask with gaps, exposing regions of the semiconductor wafer between the integrated circuits. The semiconductor wafer is then plasma etched through the gaps in the patterned mask to singulate the integrated circuits.

Thus, hybrid wafer dicing approaches using a spatially multi-focused laser beam and plasma etch process have been disclosed.

What is claimed is:

1. A method of dicing a semiconductor wafer comprising a plurality of integrated circuits, the method comprising:

forming a mask above the semiconductor wafer, the mask comprising a layer covering and protecting the integrated circuits;

patterning the mask with a spatially multi-focused laser beam laser scribing process to provide a patterned mask with gaps, exposing regions of the semiconductor wafer between the integrated circuits, wherein patterning the mask with the spatially multi-focused laser beam laser scribing process comprises forming trenches in the regions of the semiconductor wafer between the integrated circuits, the trenches comprising essentially vertical sidewalls; and

plasma etching the semiconductor wafer through the gaps in the patterned mask to singulate the integrated circuits.

2. The method of claim **1**, wherein the spatially multi-focused laser beam laser scribing process provides a first beam portion focused at a first depth in the semiconductor wafer, and a second beam portion focused at a second depth in the semiconductor wafer, the second depth vertically beneath the first depth.

3. The method of claim **2**, wherein the spatially multi-focused laser beam laser scribing process provides a third beam portion focused at a third depth in the semiconductor wafer, the third depth vertically beneath the second depth.

4. The method of claim **1**, wherein the spatially multi-focused laser beam laser scribing process comprises passing a laser beam through a diffractive optical element (DOE).

5. The method of claim **1**, wherein the spatially multi-focused laser beam laser scribing process comprises using a Gaussian source laser beam.

6. The method of claim **5**, wherein the spatially multi-focused laser beam laser scribing process comprises using a femto-second source laser beam.

7. The method of claim **1**, wherein scribing with the spatially multi-focused laser beam laser scribing process comprises scribing with a spatially multi-focused femto-second based laser beam.

8. The method of claim **1**, wherein plasma etching the semiconductor wafer comprises extending the trenches to form corresponding trench extensions.

9. A method of dicing a semiconductor wafer comprising a plurality of integrated circuits, the method comprising:

laser scribing the semiconductor wafer with a spatially multi-focused laser beam laser scribing process to singulate the plurality of integrated circuits, wherein the laser scribing with the spatially multi-focused laser beam laser laser scribing process comprises forming trenches in regions of the semiconductor wafer between the integrated circuits, the trenches comprising essentially vertical sidewalls.

10. The method of claim **9**, wherein the spatially multi-focused laser beam laser scribing process provides a first beam portion focused at a first depth in the semiconductor wafer, and a second beam portion focused at a second depth in the semiconductor wafer, the second depth vertically beneath the first depth.

11. The method of claim **10**, wherein the spatially multi-focused laser beam laser scribing process provides a third beam portion focused at a third depth in the semiconductor wafer, the third depth vertically beneath the second depth.

12. The method of claim **10**, wherein the spatially multi-focused laser beam laser scribing process comprises passing a laser beam through a diffractive optical element (DOE).

13. The method of claim **10**, wherein the spatially multi-focused laser beam laser scribing process comprises using a Gaussian source laser beam.

14. The method of claim **10**, wherein the spatially multi-focused laser beam laser scribing process comprises using a femto-second source laser beam.

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