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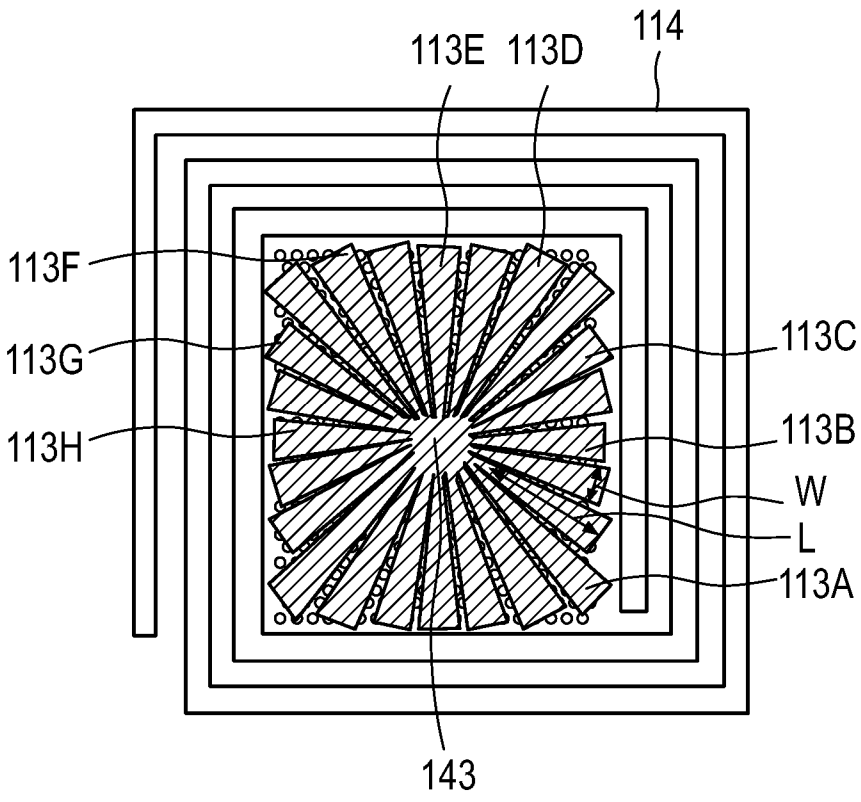

(57) Abstract: The present invention relates to a chip with a chip substrate and comprising a network of trench capacitors, which trench capacitors comprise electrodes and an intermediate dielectric extending in a direction perpendicular to a main chip surface. The trench capacitors are coupled by a pattern of interconnects, which pattern is designed to withstand a generation of eddy currents in the interconnects.

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Integrated low-loss capacitor-array structure

FIELD OF THE INVENTION

The present invention relates to a chip with a chip substrate and comprising a network of trench capacitors, and to a chip assembly comprising such a chip.

BACKGROUND OF THE INVENTION

It has always been a desire in the electronics industry to have access to a so-called `miniaturized' switched DC-to-DC converter. In order to achieve this, it is well known that the switching frequency must go up to very high values because the size of the necessary passives scales inversely with the switching frequency, i.e., the higher the switching frequency, the smaller must be the device.

A problem with increasing the switching frequency is that with many passives, the parasitic components, in particular the equivalent series inductance (ESL) and the equivalent series resistance (ESR) of the capacitors, become dominant over the intended function of the component. In practice, for non-integrated passives, this sets a limit to an achievable switching frequency of about 25 MHz. This, therefore, sets a clear limitation to the degree of miniaturization that can be achieved through the route of increasing the switching frequency.

As an alternative route to miniaturizing a switched DC-to-DC converter, a way must be found to miniaturize the necessary passives without reducing their component value.
JP 08330517 A, published in the form of a patent abstract, describes an integrated circuit device that decreases an occupation area required by an integrated circuit that comprises a MIM capacitor and a spiral inductor in an interconnect stack of an integrated circuit device. The inductor has an inner space left by its spiral-shaped arrangement of conductor traces. A MIM plate capacitor is arranged in this inner space.

However, the capacity that can be achieved with this structure is rather small. Furthermore, this structure does not allow achieving high switching frequencies required for instance for operating a switched DC-to-DC converter in integrated technology.

SUMMARY OF THE INVENTION

In a first aspect of the present invention, therefore, a chip is provided with a chip substrate and with a network of trench capacitors. The trench capacitors comprise electrodes and an intermediate dielectric extending in a direction substantially perpendicular to a main chip surface. In the chip of the first aspect of the invention, the trench capacitors are coupled by a pattern of interconnects, which pattern is designed to withstand a generation of eddy currents in the interconnects.

Individual integrated trench capacitors can be fabricated to exhibit a very low ESL and ESR. Integrated trench capacitors in principle allow achieving high capacitance densities by coupling the trench capacitors in parallel with the pattern of interconnects, which therefore is done in one embodiment of the chip of the present invention. Providing the network of trench capacitors in the form of an array of parallel trench capacitors should enable integration of a DC-to-DC converter or filter function in integrated technology, with a desired capacity for operation at switching frequencies on the order of 100 MHz.

However, the inventors found that particularly eddy currents are relevant for the performance of a combination of interconnects and networks of capacitive elements such as trench capacitors. This applies in particular to an embodiment of a combination of an integrated trench capacitor array with one or more integrated inductors on the same chip or on different chips in a chip assembly. Here it results in a reduction of the achievable maximum switching frequency, blocking a realization of a miniaturized integrated switched DC-to-DC converter requiring operation at switching frequencies higher than 25 MHz. Therefore, a straightforward integration of inductors and conductors does not provide a viable solution.

The chip of the first aspect of the invention is based on the recognition that a combination of an trench capacitor array with one or more integrated inductors on the same chip or on different chips in a chip assembly reduces the quality factor of the inductors substantially, which results in a reduction of the achievable maximum switching frequency. As is known in the art per se, the quality factor Q of an inductor is the ratio of its inductive reactance $2\pi fL$, f being the switching frequency and L the inductance, to its ohmic resistance R at a given frequency f, and is a measure of its efficiency. The higher the Q factor of the inductor, the closer it approaches the behavior of an ideal, lossless inductor. In the chip of the present invention, the quality factor of the inductors is high because the generation of eddy currents

in interconnects of the capacitor array is suppressed. Eddy currents in the interconnects would be, in a hypothetical absence of countermeasures present on the chip of the invention, induced by an exposure of interconnects to a magnetic field component varying in time and oriented substantially perpendicular to the main chip surface. Such magnetic field component can for instance be created by an inductor on the same chip, or by an inductor on a different chip in a chip assembly. Eddy currents are avoided partly or in total in the interconnects of the chip of the invention by providing a suitable structure of the interconnects, as will be explained by way of embodiments further below.

In the chip of the present aspect of the invention, therefore, a high quality factor of the inductor is achieved, be it arranged on the same chip or on a different chip of a chip assembly. As a consequence, operational switching frequencies become available that are suitable for an integrated switched DC-DC converter in a chip or chip assembly that also comprises an integrated inductor, be it as a part of the DC-to-DC converter or as a part of a different integrated circuit, such as a filter.

With the chip of the invention, the equivalent series inductance of the array of trench capacitors is below 1 Microhenry at operation frequencies of 50 MHz and above. Note that eddy currents and other parasitic elements are expected to be too high above an upper limit of a switching frequency of 200 MHz even with the chip of the invention. The lower limit of the switching frequency is given by size requirements for the passive components.

In the following, embodiments of the chip of the invention will be described. The embodiments can be combined with each other, unless described as forming alternatives to each other.

Trench capacitors may be defined in the chip substrate in a front-end process or on the substrate, i.e., in a back-end process. Preferably, the trenches are defined in the chip substrate, which allows deeper trenches and thus larger capacitance densities. A network of trench capacitors that is coupled in parallel usually has a connection through top or second electrodes of the trench capacitors. These top electrodes extend also on the substrate. In a variant to a cylindrical trench shape, the trench capacitors have the shape of pillars in a trench, such as described in the application EP 06 300 422.0 (PH005852) that is included herein by reference. Particularly when using pillars, there may be a further connection

through the bottom or first electrodes, up to the level where it is difficult to determine whether it relates to a capacitor structure comprising trenches and/or channels or a plurality of capacitors in trenches that are coupled in parallel. The term 'network of trench capacitors' is intended to cover all these embodiments.

Different concepts are suitable for withstanding the generation of eddy currents in the interconnects. In one embodiment, the pattern of interconnects comprises interconnects, which are stripe-shaped and electrically isolated from each other either along their full stripe length or in a first stripe section along the stripe length, which first stripe section has a smaller extension than the full stripe length. The stripe shape is advantageous for avoiding a large extension of eddy currents and thus keeps their influence small.

The interconnects of this embodiment can extend in parallel to each other. However, even better suppression of eddy currents is achieved in an embodiment if the interconnects do not extend in parallel. One particularly suitable pattern of interconnects comprises a plurality of stripe-shaped interconnects, which extend radially with reference to a reference point, for instance with reference to a center interconnect. The center interconnect is advantageously arranged on a magnetic field line extending from a center of an inductor.

Preferably, a distance between neighboring stripe-shaped interconnects is equal over substantially the complete length of the interconnects. This modification maximizes the surface area that may be used for the definition of trench capacitors. For the example of interconnects extending radially, these stripe-shaped interconnects of this embodiment have a length along a radial direction and a width in a direction perpendicular to the radial direction. The width of the stripe-shaped interconnects preferably increases with increasing distance to the center interconnect. This modification maximizes the surface area that may be used for the definition of trench capacitors.

An inductor typically has coil windings extending in parallel to the main chip surface. The coil windings are in one embodiment arranged in one plane to provide a planar inductor. In a variant, the coil windings are arranged at different distances to the main chip surface to provide a non-planar inductor, for instance on different metallization levels. The use of the metallization levels for the inductor has the further advantage that the highly conductive metal layers can be used to create an inductor with a relatively good parasitic

resistance/inductance ratio R/L. The maximum allowable ratio of R/L depends on the semiconductor device formed by the chip or chip assembly comprising the chip, and particularly on the quality of any transistors or diodes that are included in the semiconductor device, e.g. a DC-to-DC converter. Suitably, the ratio is less than 0.05 Ω/nH. Advantageously, the ratio is 0.02 Ω/nH or less. This latter value is still achievable when the inductor is not integrated in the same chip as the network of trench capacitors.

The total layout of a combination of an integrated network of trench capacitors and an integrated inductor can be optimized further by placing the required trench capacitors inside the inductor. In an advantageous embodiment, the network of trench capacitors and the pattern of interconnects are laterally arranged within an outer edge of the integrated inductor. This embodiment simplifies the design so as to reduce eddy currents and parasitics to a minimum. A very good R/L ratio can be obtained in this embodiment for a given total area.

Suppression of eddy currents is useful not only in an embodiment, wherein the chip itself comprises an integrated inductor. This advantage can also be achieved if the inductor as the source of the changing magnetic field is located on an external chip in a chip assembly. Here, the network of trench capacitors is positioned such with respect to the inductor that the trench capacitors are located within a perpendicular projection of an outer edge of the inductor on a first chip to the main chip surface of the second chip containing the trench capacitors.

Suitably, the inductor is defined in the same metallization as mentioned above for the pattern of interconnects of the trench capacitors. This embodiment has the advantage that the connections between capacitor and inductor are defined properly, so that the parasitic impedance and resistance is small.

For further reducing the impedance, the interconnect pattern of one embodiment comprises interconnects, which couple a group of more than two trench capacitors, which trench capacitors, in a top view of the chip, are hidden by the interconnects. One such interconnect may cover, in perpendicular projection, several trench capacitors. It thus not merely extends between a first and a second trench capacitor. It is the interconnect to which several trench capacitors are connected, and as seen in top view, under which several capacitors are hidden. This shape reduces the inherent impedance.

In an embodiment with an integrated inductor extending in parallel to the main chip surface and with stripe-shaped interconnects, which extend radially from a center interconnect, the inductor preferably has at least one coil winding that defines a central axis extending substantially perpendicular to the main chip surface with respect to the coil winding, and the center interconnect is arranged such that it is crossed by the central axis.

The distribution of the trench capacitors is preferably not homogeneous. Suitably, the trench capacitors are concentrated in an area that is remote from the center, e.g. near to the inductor. More specifically, the trench capacitors are arranged within a first and a second capacitor area of the chip surface, of which the first area is located inside the second area, and the number of trench capacitors per unit area is larger in the second capacitor area than in the first capacitor area.

According to a second aspect of the invention, a chip assembly is provided that comprises a first chip, which includes a semiconductor device, and a second chip, wherein the second chip is a chip according to the first aspect of the invention or one of its embodiments disclosed in this specification and in the claims.

The chip assembly of the second aspect of the invention shares the advantages of the chip of the first aspect of the invention.

In the following, embodiments of the chip assembly of the invention, which is also referred to in short as the assembly, will be described. The embodiments can be combined with each other, unless described as forming alternatives to each other.

One group of embodiments concerns the arrangement of the inductor relative to the network of trench capacitors. As was mentioned before, in an embodiment, where the second chip contains an integrated inductor in parallel arrangement with the main chip surface of the first chip, the trench capacitors and the pattern of interconnects of the second chip are preferably laterally arranged within a perpendicular projection of an outer edge of the integrated planar inductor onto the main chip surface of the second chip.

In a further embodiment, the assembly comprises an encapsulation, and the inductor is defined as a metal pattern that is coupled to the second chip with bumps. Such an inductor is

known from WO 2003/85729 A. The metal pattern can thus be provided in any desired thickness and against reasonable costs. However, there is most probably a need for an additional assembly step that needs to be compatible with other assembly steps.

In a third embodiment, the chip assembly comprises a multilayer carrier substrate, to which the first and the second chip are assembled, in which carrier substrate the inductor is defined. This multilayer carrier substrate is for instance a tape or laminate of the type in use for ball grid array packages. Definition of an inductor herein is for instance disclosed in US 6,310,386, but for another purpose.

Another group of embodiments of the chip assembly further concerns the application case of a DC-to-DC converter. In this group of embodiments a DC-DC converter is defined in the chip assembly. This localized and integrated DC-DC converter has the function of up-conversion or down-conversion of the supply voltage to an application voltage. Power consumption is therein reduced due to several factors. First of all, the application voltage may be specific for the operation of the first chip, and more specific than in case of a separately assembled DC-DC converter. The application voltage may also be regulated. Such better specified application voltage is usually lower, resulting in lower power consumption. Secondly, currents are reduced due to the use of the localized DC-DC converter, which also results in lower power consumption. Additionally, the DC-DC converter forms an adequate isolation in the standby mode.

The DC-to-DC converter is preferably configured for operation with a switching frequency in the range of 50-200 MHz. Advantageously, the switching frequency of the DC-DC converter is above 80 MHz and below 150 MHz. Good results have been obtained with a switching frequency of 90-110 MHz. The parasitics as expressed in the equivalent series inductance of the network of trench capacitors, is then preferably less than 40 pH, more preferably even less than 30 pH. This is also achievable with the technology of trench capacitors, particularly if the overall capacitance is 20 nF or more.

Several topologies of an inductive DC-DC converter are known in the art, such as buck converters, buck-boost converters and cuk converters. These are therewith particularly suitable for larger output currents, upwards from 5 mA. All such inductive topologies have a filter to obtain essentially direct current at its input and output terminals.

In a preferred embodiment of the invention, the DC-DC converter comprises an output filter that is defined as a series notch circuit. The inductor and the capacitor of the series notch circuit are designed such as to create a notch at the switching frequency of the DC-DC converter. Such a series notch circuit is attractive, as it tends to have a small voltage ripple. This small voltage ripple allows reduction of the inductor size, since not the inductor itself, but the voltage ripple is a specification to DC-DC converter.

The use of a series notch circuit as part of a DC-DC converter requires accurate matching of these inductor and capacitor, or alternatively, adjustment of the switching frequency to the value of the notch in the series notch circuit. The prior art needed adjustment of the switching frequency, which is not desired. This adjustment was needed due to variations in the values of discrete capacitors and inductors of about 15 %. In the present invention, the notch can be designed adequately, and no adjustments of the switching frequency are needed. This is achieved due to manufacture with an accuracy of more than 95 % and even 98 % or more. In a further extension hereof, the output filter comprises a cascade of notch filters, which is tuned both to the switching frequency and its second harmonic. Appropriate matching of the inductor and the capacitor is then mandatory, as the harmonic is always an integer multiple of the fundamental switching frequency. By integrating the inductor and the capacitor into the second chip, a matching of both is achieved with a tolerance of less than 1 %, in most cases even in the order of 0.1 %.

In another or additional extension, the output filter comprises a cascade of one or more notch filters and a low-pass filter. Such a cascade appears to have superior performance.

The network of trench capacitors forms a circuit element of a DC-to-DC converter integrated on either one of the first and second chips or on both chips. The active components are suitably integrated in the first chip. However, alternatively, they may be defined in the second chip together with the network of trench capacitors. In the latter case, it is preferable that the substrate is defined into a high-ohmic area and a low-ohmic area. The active elements are then arranged in the low-ohmic area. A typical low-ohmic semiconductor material has a resistivity in the order of 100mΩ·cm. The trench capacitors and the overlying inductor are defined in and respectively on the high-ohmic area. High-ohmic is understood herein to have a resistivity of more than 1kΩ·cm. Such high-ohmic substrate is advantageous

for the performance of the inductor and also to allow low-cost manufacture of trench capacitors. Herein, a surface zone of the semiconductor substrate in the trench is used as the first electrode.

In order to make the assembly as small as possible, it is suitable that the first chip overlies the inductor at least partially. Then, it is preferred to apply a shielding between the inductor and active elements within the first chip. The shielding may be defined in the first chip, in the second chip, or in a separate metal layer in the encapsulation. In case it is present in the second chip, one suitable possibility constitutes the use of the second surface of the substrate. This second surface is then not only shielding surface, but also the surface to which the first chip will be assembled. Most suitably, use is made of a shield as disclosed in WO-A 2004/055839, which is included herein by reference. Such a shield is defined in relation to the inductor, which is situated in an inductor plane. The inductor is designed to be substantially symmetrical with respect to a mirror plane perpendicular to the inductor plane. The shield is defined in a ground shield plane that is oriented in parallel to the inductor plane. The shield comprises a plurality of electrically conductive tracks that have an orientation perpendicular to the mirror plane. The advantage of this shield is that loop currents are prevented and that a reduction in the effective self-inductance is therewith prevented.

In an advantageous embodiment, the localized DC-DC converter is used in an assembly that operates on the basis of a first and a second supply voltage. Such first and second supply voltage may be used within the first chip. Alternatively, these are used with a first chip and a third chip, both of which comprise semiconductor or semiconductor alike devices, but need different supply voltages. Due to the integration of the DC-DC converter, the assembly can be provided with a single supply voltage as input. This means that the interface of assembly to an external board may be reduced to a single pin or a plurality of coupled pins. This is evidently advantageous for simplifying design. It furthermore allows supply of a packaged assembly that may be used as any standard device without any further modification of a printed circuit board. This embodiment could be applied as well with a DC-DC converter in a switched capacitor topology.

In a most advantageous modification of this embodiment, the first chip and the third chip comprise different types of semiconductor (alike) devices. The first chip is for instance a

driver IC, while the third chip is a light emitting diode, a sensor, a MEMS-component. In case of a driver IC, this suitably is designed to drive the third chip.

In a further advantageous modification, the assembly comprises more than one DC-DC converter so as to provide different voltage islands in the assembly with different supply voltages. This modification is for instance desired, if the needed voltages are rather different. Then the design of a single DC-DC converter would not fit for both voltage islands. This modification may also be desired in case that a proper isolation is needed between the voltage islands. This may even be the case if the assembly does not have a third chip. For instance, with an IC as a first chip, different voltage islands may be present for mostly digital core functionality and for mostly mixed-signal peripheral functionality. It is not needed herein, that both DC-DC converters are of the same type, e.g. one DC-DC converter may be an inductive one, allowing larger output current, while a second DC-DC converter is a switched capacitor type, which can be miniaturized further.

In an even further modification, the integrated DC-DC converter is made reconfigurable. In this manner, one DC-DC converter can be used for up-conversion and for down-conversion. Additionally, the ratio between the input voltage and the output voltage may be tuned. While a conventional ratio is in the range of 0.5-2, or 0.25-4, larger ratios are achievable due to the integration. A larger ratio is for instance 0.1-10, or 2-10. The larger ratios are achievable, as a larger number of capacitors is needed. The ESL requirement is increasingly more difficult to achieve with discrete capacitors, but can be achieved with the network of trench capacitors. A particularly preferred version of reconfigurability makes use of trench capacitors with a second dielectric and a third electrode, wherein at least one of the electrodes and particularly the intermediate one is switchable. The switching allows to tune the capacitance density of the capacitor. This concept is described in application EP 05 110 488.3, which is herein included by reference.

The invention further relates to the embodiment of the second chip with the network of trench capacitors that is provided with a pattern of interconnects that is designed so as to limit eddy currents therein. Such eddy currents would have been generated therein otherwise by a nearby inductor that is part of the DC-DC converter of which the network of trench capacitors is also part.

The design of the present chip is very suitable and needed in view of the requirements of the DC-DC converter with a switching frequency of 50-200 MHz. However, the design may be used advantageously also for filters for other specific functions that are to be integrated.

Embodiments of the invention are also defined in the dependent claims

BRIEF DESCRIPTION OF THE DRAWINGS

These and other aspects of the invention will be apparent from and elucidated with reference to the embodiment(s) described hereinafter. In the following drawings

Fig. 1 shows a cross sectional view of an embodiment of the chip of the invention;

Fig. 2 shows a combination of an inductor and of a pattern of interconnects in a top view according to a further embodiment of the chip of the invention;

Fig. 3 shows a combination of an inductor and of a pattern of interconnects in a top view

Fig. 4 to 6 show different embodiments of an assembly according to the invention

DETAILED DESCRIPTION OF EMBODIMENTS

Fig. 1 shows an embodiment of the chip 100, that is provided with a vertical interconnect extending from the first surface 101 to the second surface 103. This embodiment comprises a network of the trench capacitors 102, which are exposed at the first surface 101. This embodiment further shows a vertical interconnect 30. Both the vertical interconnect 30 and the network of capacitors 102 have in this embodiment a plurality of trenches, 21, 311, 312, 313. Although not shown, it is suitable that the network of trench capacitors 102 comprises many individual trenches 21, that may be defined on mutually differing distances.

The vertical interconnect 30 comprises a first part 31 and a second part 32 of wider dimensions. As will become clear from the further discussion, the first part 31 is made by anisotropic etching from the first surface 101, and the second part 32 is made by etching from the second surface 103, and particularly wet-chemical etching. The chip 100 comprises in at its surfaces at the first and second surface 101, 103 as well as in the trenches 21, 31, 32 a couple of layers. Not shown here are first conductive surfaces that constitute the bottom electrode of the vertical trench capacitor 102. Shown is a layer 112 of dielectric material, that is present at nearly the complete surface. On top of the layer 112 of dielectric material, a

layer of electrically conductive material is present. This layer – not shown – fills the trench. This layer is for instance polysilicon, but may alternatively be another (conducting) material such as copper, sol-gel deposited silver, aluminum. At the first surface 101 the trench capacitor 102 and the vertical interconnect 30 are provided with a further metallization of AlCu in this case. The layers 112 and 13 can be used as interconnect layers, and may be mutually separated at certain positions by an insulating layer. The second part 32 of the interconnect has its surface covered with a layer 14, in this case of electroplated copper. The copper extends at the second surface 103 of the substrate 104 and forms the wiring pattern. The layer 14 may fill the second part of the interconnect 30.

The chip 100 is further provided with an inductor 114. The inductor 114 comprises a first winding 114A and a second winding 114B. The inductor 114 is suitably defined on an isolating layer, which is in this example the layer 112 of dielectric material, that is also used within the trench capacitor.

An inductor generates eddy currents in nearby electrical tracks. In order to limit the eddy currents in the trench capacitor network 102, the network 102 is provided with an optimized pattern of interconnects 113A, 113B. The pattern will be shown in more detail with respect to Fig 2 and 3.

Fig. 2 shows in a top view the combination of inductor 114 and pattern of interconnects 113. As shown herein, the pattern of interconnects 113 comprises a plurality of interconnects 113A-113D extending in parallel, which each of those has a limited width. Each of the interconnects is thus essentially stripe-shaped. The network of trench capacitors 102 is defined below the interconnects 113. The interconnects 113A-113D cross the inductor in a second conductive layer, in case of integration of the inductor 114 and the interconnects 113A-113D in a single metallization layer in the second chip 100. The layer of polysilicon is suitable for such crossing. The same is true for the input 115 of the inductor 114. The output 116 of the inductor is also shown in this Fig 6, as well as an interconnect line 117. This interconnect line couples the interconnects 113A-113D and forms the input of the trench capacitor network 102. The output of the trench capacitor network 102 is not shown herein; it is lead to ground directly. While the layer of polysilicon may extend over the complete surface, it is suitably patterned in accordance with the pattern of interconnects 113.

Fig 3 shows in a top view a second embodiment of the inductor 114 and the pattern of interconnects 113. As will be further explained with reference to the following figures, the inductor 114 and the pattern of interconnects 113 need not to be defined in a single metallization layer or even within the same chip. The inductor 114 in particular may be located elsewhere. According to this embodiment, the pattern of interconnects 113 is defined with reference to a center 143. The individual interconnects 113 extend radially from this center 143. The center 143 furthermore couples all interconnects together. The center 143 is defined with reference to the inductor 114. In this manner, the interconnects extend substantially perpendicularly to any eddy currents. The eddy currents are caused by the main current flowing through the inductor 114 around the center 143.

Length L and width W can be defined with respect to each individual interconnect 113A-H. The length direction is herein chosen parallel to the radial extending from the center. The width direction is oriented perpendicularly to the length. In a preferred embodiment, the width W of the interconnect 113A-H increases with the distance to the center 143 of the network 102. The advantage hereof is that the distance between neighboring interconnects 113A, 113B is kept constant. Another advantage is that the available surface area may be used most efficiently, as the non-interconnected area is kept as small as possible.

Fig. 4 to 6 show several embodiments of the assembly 200 of the invention. Generally, the assembly 200 comprises the second chip 100 with the network of trench capacitors 102, a first chip 150, and optionally a further assembly element such as an encapsulation, a carrier substrate. The assembly further comprises any elements needed for mutual interconnection and for interconnection to a printed circuit board, as are known per se to the skilled person in the field of assembly.

Fig. 4 shows in diagrammatical cross-sectional view an assembly 200 that comprises a leadframe with a heatsink 210 and contact pads 211, 212. The first chip 150 and the second chip 100 are assembled to the leadframe in a double flip-chip configuration: the first chip, generally an integrated circuit, is attached to the heat sink 210 with an adhesive 221. Thereafter, the second chip 100 is provided, which is attached both to the first chip 150 and to the contact pads 211, 212 with solder bumps 231, 232 of different diameter. The second chip 100 comprises in this embodiment both the network of trench capacitors 102 with the interconnects 113A, 113B, and the inductor 114. The interconnects 113 and the inductor 114

are suitably defined in the same layer that is used for the definition of the contact pads and/or the underbump metallization 198, 199. The assembly 200 is further provided with a dielectric encapsulation 220, which is an epoxy moulding material in particular. Space between the first chip 150 and the second chip 100 may be filled with an underfill. A shielding is suitably implemented in the first chip 150.

Fig. 5 shows in diagrammatical cross-sectional view a second embodiment of the assembly 200. This assembly 200 comprises a carrier substrate 250 in addition to the first chip 150 and the second chip 100. Such a carrier substrate is for instance an FR-4 based multilayer substrate or alternatively a metallized polyimide tape. Such carrier substrates are known to the skilled person from the field of ball grid array packages. The present example shows a multilayer substrate with an inner metal layer wherein the inductor 114 is defined. The integration of the inductor of the DC-DC converter in the multilayer substrate is not needed, but advantageous from a cost perspective. The trench capacitors 102 are still provided with an optimized interconnect 113. Both the first chip 150 and the second chip 100 are herein assembled to the carrier substrate 250 with bumps, but wirebonds could be used alternatively, particularly for the first chip 150. This however is deemed not advantageous, as the wirebonds have an ESL that might limit the switching frequency. This is particularly the case when the switches of the DC-DC converter are defined in the first chip 150 instead of in the second chip 100.

Fig. 6 shows a third embodiment of the assembly 200 in diagrammatical cross-sectional view. The second chip 100 acts herein as the carrier substrate of the assembly, and is provided with vertical interconnects 30. The resulting assembly 200 may be of small size. The inductor 114 is in this embodiment defined within the encapsulation 220 and coupled to the second chip 100 with bumps 231. As will be understood, this embodiment of the inductor 114 could be used also in combination with the carrier substrate 250 shown in Fig. 5. The stacked die assembly of this Fig. 6 may also be combined with a carrier substrate as shown in Fig. 5.

While the invention has been illustrated and described in detail in the drawings and foregoing description, such illustration and description are to be considered illustrative or exemplary and not restrictive; the invention is not limited to the disclosed embodiments.

Other variations to the disclosed embodiments can be understood and effected by those skilled in the art in practicing the claimed invention, from a study of the drawings, the disclosure, and the appended claims. In one variant, the trench capacitors are formed by other trench elements such as batteries or via.

In the claims, the word "comprising" does not exclude other elements or steps, and the indefinite article "a" or "an" does not exclude a plurality. The mere fact that certain measures are recited in mutually different dependent claims does not indicate that a combination of these measured cannot be used to advantage.

Any reference signs in the claims should not be construed as limiting the scope.

CLAIMS:

1. A chip with a chip substrate and comprising a network of trench capacitors, which trench capacitors comprise electrodes and an intermediate dielectric extending in a direction perpendicular to a main chip surface, wherein the trench capacitors are coupled by a pattern of interconnects, which pattern is designed to withstand a generation of eddy currents in the interconnects.

2. The chip of claim 1, wherein the pattern of interconnects comprises interconnects, which are stripe-shaped and electrically isolated from each other either along their full stripe length or in a first stripe section along the stripe length, which first stripe section has a smaller extension than the full stripe length.

3. The chip of claim 2, wherein the interconnects extend in parallel to each other.

4. The chip of claim 2, wherein the pattern of interconnects comprises a plurality of stripe-shaped interconnects, which extend radially from a center interconnect.

5. The chip of claim 1, wherein the chip comprises an integrated inductor extending in parallel to the main chip surface.

6. The chip of claim 5 in combination with claim 3 or 4, wherein trench capacitors and the pattern of interconnects are laterally arranged within an outer edge of the integrated inductor.

7. The chip of claim 1, wherein the interconnect pattern comprises interconnects, which couple a group of more than two trench capacitors, which trench capacitors, in a top view of the chip, are hidden by the interconnects.

8. The chip of claims 4 to 6, wherein the inductor has at least one coil winding that defines a central axis extending perpendicular to the main chip surface with respect to the

coil winding, and wherein the center interconnect is arranged such that it is crossed by the central axis.

9. The chip of claim 4, wherein the stripe-shaped interconnects have a length along a radial direction and a width in a direction perpendicular to the radial direction, and wherein the width of the stripe-shaped interconnects increases with increasing distance to the center interconnect.

10. The chip of claim 4, wherein the trench capacitors are arranged within a first and a second capacitor area of the chip surface, of which the first area is located inside the second area, and wherein a number of trench capacitors per unit area is larger in the second capacitor area than in the first capacitor area.

11. The chip of claim 4, wherein the inductor and the interconnects are arranged on an identical metal level.

12. A chip assembly comprising a first chip, which includes a semiconductor device, and a second chip, wherein the second chip is a chip according to claim 1.

13. The chip assembly of claim 12, wherein the second chip contains an integrated inductor in parallel arrangement with the main chip surface of the first chip, and wherein the trench capacitors and the pattern of interconnects of the second chip are laterally arranged within a perpendicular projection of an outer edge of the integrated planar inductor onto the main chip surface of the second chip.

14. The chip assembly of claim 12, in which a DC-DC converter is defined, which is configured for operation with a switching frequency in the range of 50-200 MHz and which comprises an output filter with an inductor and with said network of trench capacitors in the second chip.

15. The chip assembly of claim 12, further comprising an encapsulation wherein the inductor is defined as a metal pattern that is coupled to the second chip with bumps.

16. The chip assembly of claim 12, wherein the second chip is a chip according to claim 5.

17. The chip assembly of claim 12, further comprising a multilayer carrier substrate to which the first and the second chip are assembled, in which carrier substrate the inductor is defined.

18. The chip assembly of claim 12, wherein the array of trench capacitor forms a circuit element of a DC-to-DC converter integrated on either one of the first and second chips or on both chips.

19. The chip assembly of claim 18, wherein the DC-to-DC converter comprises a filter that includes at least one inductor and the network of trench capacitors.

FIG. 1

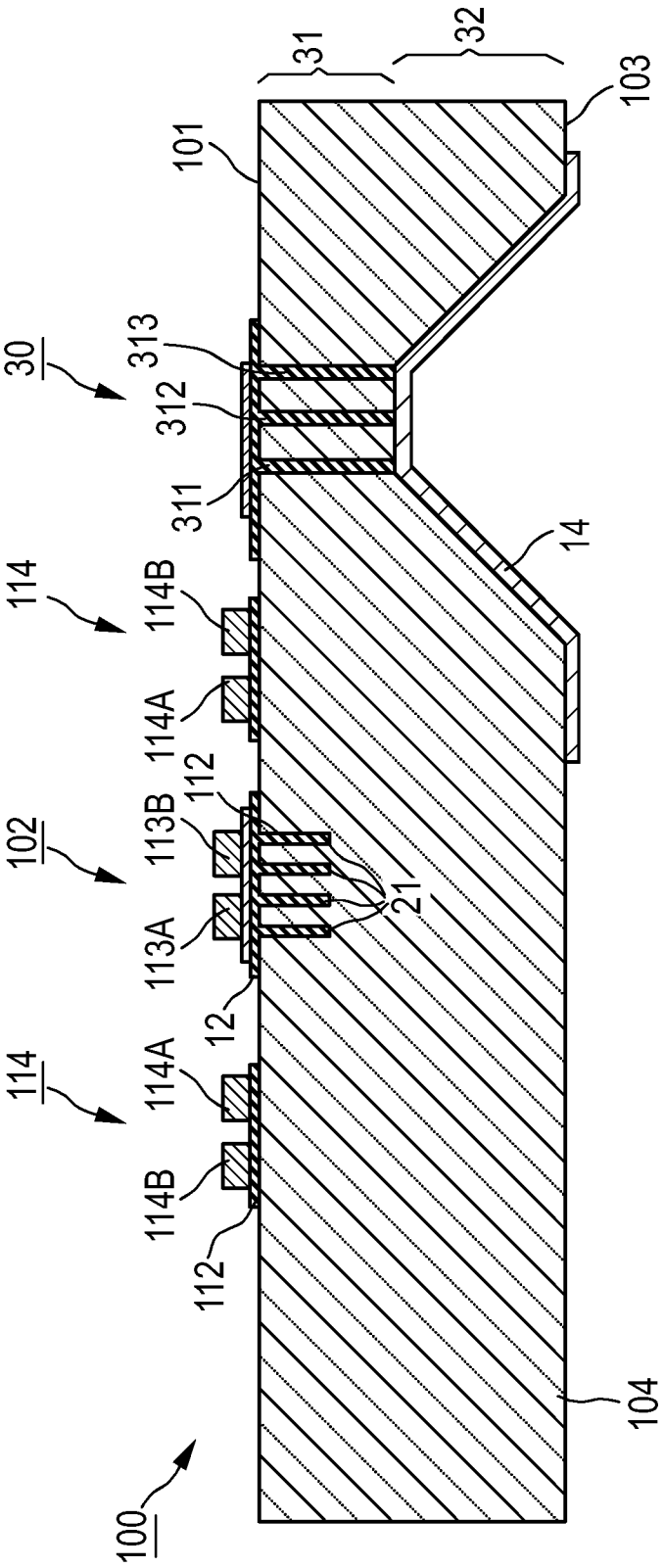
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FIG. 2

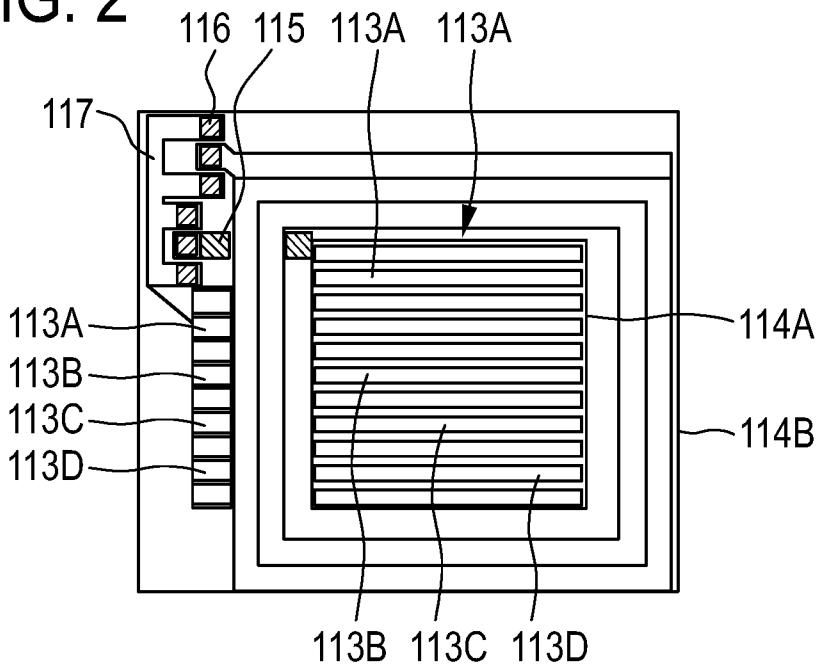
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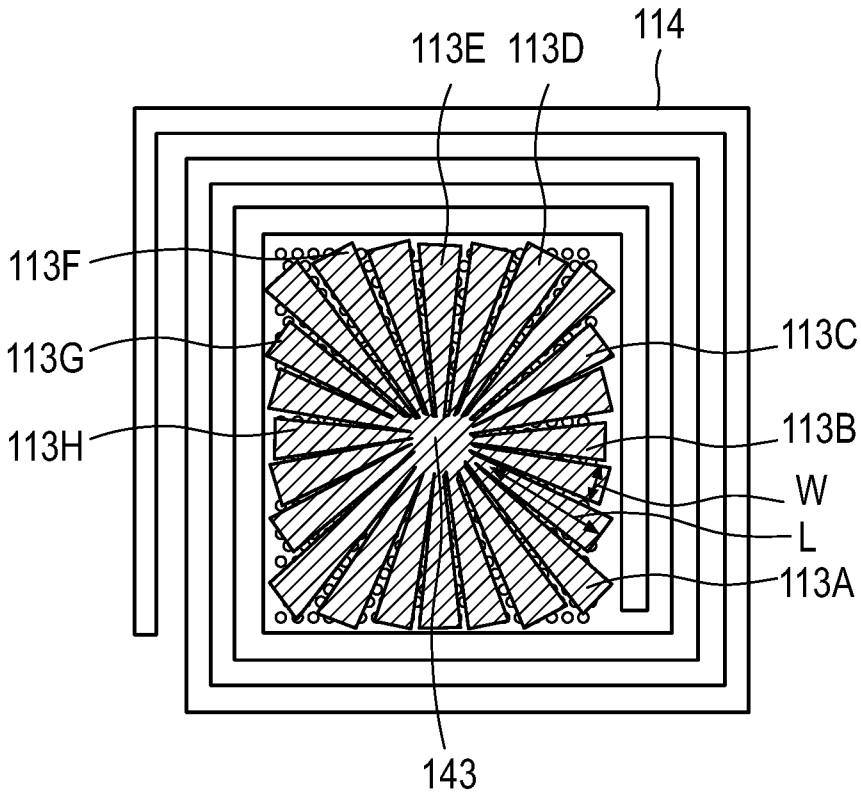
FIG. 3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113H
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W
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113A
143

FIG. 4

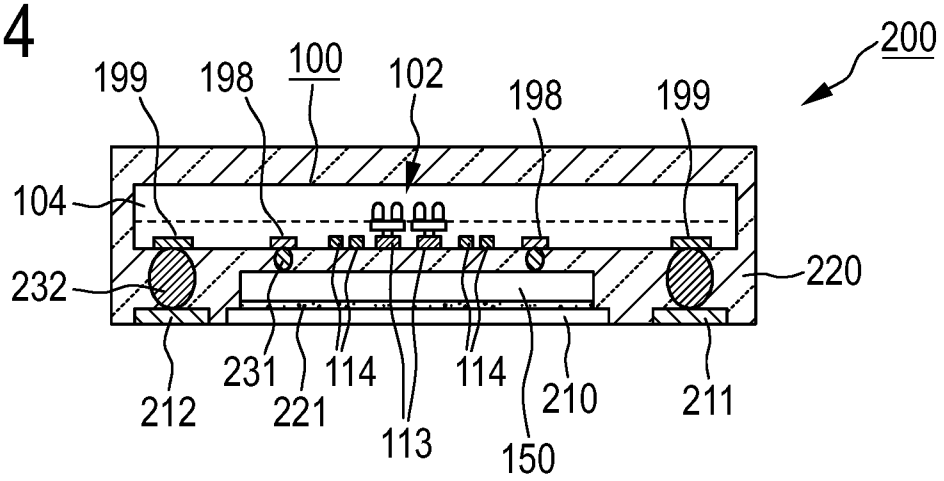


FIG. 5

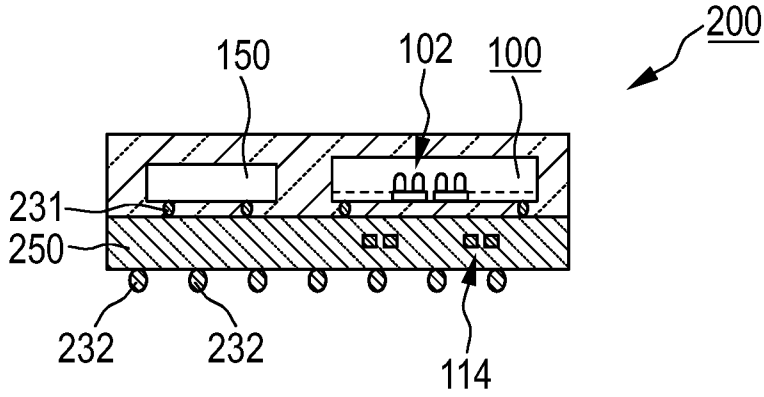
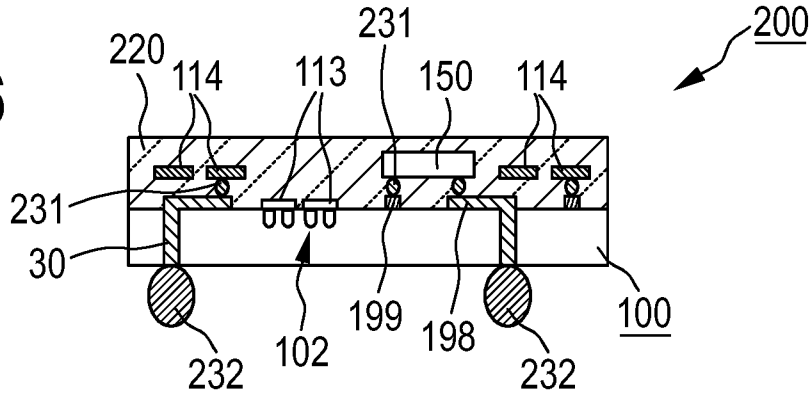


FIG. 6



INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2007/054595

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L23/522 H01L25/16 H01L27/08

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L H01G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, INSPEC, COMPENDEX, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 September 2007	10/10/2007

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Crampin, Nicola

INTERNATIONAL SEARCH REPORT

International application No
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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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