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(54) **Title:**
A PHOTODETECTOR AND A METHOD OF FORMING THE SAME

(57) **Abstract:**
A PHOTODETECTOR AND A METHOD OF FORMING THE SAME ABSTRACT 5 According to embodiments of the present invention, a photodetector is provided. The photodetector includes a substrate, a waveguide formed on a surface of the substrate, a first metal layer formed on a first side of the waveguide, wherein a first interface is defined between the waveguide and the first metal layer, and a silicide layer formed on a second side of the waveguide, wherein a second interface is defined between the 10 waveguide and the silicide layer, and wherein the second side is opposite to the first side, and wherein at least one of the first interface and the second interface is at least substantially perpendicular to the surface of the substrate. Various embodiments further provide a method of forming the photodetector. 15 Figure 3A

A PHOTODETECTOR AND A METHOD OF FORMING THE SAME

ABSTRACT

5   According to embodiments of the present invention, a photodetector is provided. The photodetector includes a substrate, a waveguide formed on a surface of the substrate, a first metal layer formed on a first side of the waveguide, wherein a first interface is defined between the waveguide and the first metal layer, and a silicide layer formed on a second side of the waveguide, wherein a second interface is defined between the waveguide and the silicide layer, and wherein the second side is opposite to the first side,

10   and wherein at least one of the first interface and the second interface is at least substantially perpendicular to the surface of the substrate. Various embodiments further provide a method of forming the photodetector.

15   Figure 3A

A PHOTODETECTOR AND A METHOD OF FORMING THE SAME

Cross-Reference To Related Application

5 **[0001]** This application claims the benefit of priority of Singapore patent application No. 201103211-7, filed 5 May 2011, the content of it being hereby incorporated by reference in its entirety for all purposes.

Technical Field

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[0002] Various embodiments relate to a photodetector and a method of forming the photodetector.

Background

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[0003] The continuous increase in speed and bandwidth of modern electronic circuits requires integration of optical devices to overcome the interconnection bottleneck. However, the conventional silicon (Si) electronic photonic integrated circuits (EPICs) face a critical challenge of the dimension mismatch between the micrometer scales of 20 diffraction-limited optical devices and nanometer scales of electronic devices.

[0004] Plasmonics, which deals with surface plasmon polariton (SPP) excitation and propagation at metal-dielectric interfaces, can confine light far beyond the diffraction limit, thus showing a great potential to bridge the dimension mismatch between the electronics and photonics. A number of ultra-compact plasmonic devices have been 25 proposed or demonstrated to generate, guide, modulate, and detect the SPP signals. A plasmon detector is one of the blocks of integrated plasmonic circuits. Up to date, the fabrication of most plasmonic devices requires a non-standard CMOS technology, e.g., (1) Au or Ag, - which are not CMOS-compatible material, is commonly used as the metal; (2) a special process, such as electron beam lithography, is usually required to 30 fabricate the nanostructure; and (3) a unique active material, such as CdSe quantum dot (QD), Ge, or GaAs, etc, is required for the active plasmonic devices.

[0005] However, in the view of practical implementation of plasmonic devices in the existing Si EPICs, it is highly desirable to use fully CMOS compatible materials (e.g. Al, Cu, or silicide, etc.) and industry-standard lithographic process. Recently, horizontal Al/SiO$_2$/Si/SiO$_2$/Al and Cu/SiO$_2$/Si/SiO$_2$/Cu nanoplasmonic slot waveguides were demonstrated using the standard CMOS technology to exhibit high coupling efficiency to the conventional Si dielectric waveguide and very low bending loss. The Cu-waveguide has lower propagation loss than the Al-counterpart, indicating that it is a promising plasmonic waveguide for various plasmonic devices. A nanoplasmonic modulator based on the above horizontal plasmonic waveguide was proposed. It is therefore necessary to develop a detector to convert the SPP signal propagating along the plasmonic waveguide directly to the electrical signal to provide a complete plasmo-electronic nanocircuit.

[0006] In Si photonics, germanium is commonly used to detect the 0.8-eV photons (i.e. at the communication wavelength of 1550 nm). Because Ge has a relatively small absorption coefficient of ~0.046 μm^{-1} at 1550 nm, a thick or long Ge active layer is required for the sufficient light absorption. To shrink the detector into nanometer scale, - which is required for nanoplasmonic detectors, a precise cavity or antenna structure should be developed to confine the light into a very small volume. However, although high-quality Ge film can be grown on Si, the heteroepitaxy of Ge on Si is an expensive and tough process. It also makes the whole fabrication flow of integrated circuits complex and/or difficult, especially accompanied with the fabrication of a pretty nanocavity or antenna structure.

[0007] Silicide Schottky barrier detector (SBD) is an attractive alternative for infrared detection, in which light is absorbed by silicide and the photoexcited carriers in the silicide layer can emit over the Schottky barrier (Φ_B) to be collected as photocurrent. It can detect photons of energy (hv) between Φ_B and the Si bandgap (1.12 eV). Because silicide typically has a very large absorption coefficient, e.g. ~20.66 μm^{-1} for TaSi$_2$ at 1550 nm, the silicide SBD requires a much thinner or shorter silicide layer for light absorption than the Ge-counterpart. More importantly, the silicide SBD can be easily fabricated using the standard CMOS technology. However, the silicide SBD suffers a major shortcoming of low responsivity mainly due to its low internal quantum efficiency. Reducing the barrier height Φ_B and thinning down the silicide thickness to much less than

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the hot carrier attenuation length can improve the internal quantum efficiency. However, the former leads to a large dark current unless the detector is operated at cryogenic temperature and the latter reduces the light absorption. Regarding the first problem, a suitable Φ_B should be selected to compromise the responsivity and the dark current. However, as Φ_B is mainly determined by the silicide itself, it can be tuned over very limited range by an applied voltage. To alleviate the second problem, one can use an optical cavity and/or put the silicide layer on the Si waveguide. A 2-nm-thick PtSi/p-Si Schottky detector ($\Phi_B \sim 0.21$ eV) having an optical cavity was demonstrated with a responsivity up to ~0.25 A/W at 1.5 μm, but it operated at 40 K. A Si waveguide-based NiSi$_2$/p-Si Schottky detector ($\Phi_B \sim 0.53$ eV) can operate at room temperature with the dark current of ~3 nA, but its responsivity is only ~4.6 mA/W. To meet the requirement for Si-EPIC application, the responsivity of silicide SBD needs to be substantially improved while keeping the dark current low enough to operate at room temperature.

Summary

[0008] According to an embodiment, a photodetector is provided. The photodetector may include a substrate, a waveguide formed on a surface of the substrate, a first metal layer formed on a first side of the waveguide, wherein a first interface is defined between the waveguide and the first metal layer, and a silicide layer formed on a second side of the waveguide, wherein a second interface is defined between the waveguide and the silicide layer, and wherein the second side is opposite to the first side, and wherein at least one of the first interface or the second interface is at least substantially perpendicular to the surface of the substrate.

[0009] According to an embodiment, a method of forming a photodetector is provided. The method may include providing a substrate, forming a waveguide on a surface of the substrate, forming a first metal layer on a first side of the waveguide, wherein a first interface is defined between the waveguide and the first metal layer, and forming a silicide layer on a second side of the waveguide, wherein a second interface is defined between the waveguide and the silicide layer, and wherein the second side is opposite to

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the first side, and wherein at least one of the first interface or the second interface is at least substantially perpendicular to the surface of the substrate.

Brief Description of the Drawings

[0010] In the drawings, like reference characters generally refer to the same parts throughout the different views. The drawings are not necessarily to scale, emphasis instead generally being placed upon illustrating the principles of the invention. In the following description, various embodiments of the invention are described with reference to the following drawings, in which:

[0011] FIG. 1A shows a schematic block diagram of a photodetector, while FIG. 1B shows a simplified cross-sectional representation of the photodetector of the embodiment of FIG. 1A, according to various embodiments.

[0012] FIG. 2 shows a flow chart illustrating a method of forming a photodetector, according to various embodiments.

[0013] FIG. 3A shows a schematic perspective view of a photodetector, according to various embodiments.

[0014] FIG. 3B shows a schematic cross-sectional view of the photodetector of the embodiment of FIG. 3A along the line A1-A1'.

[0015] FIG. 3C shows a schematic cross-sectional view of the photodetector of the embodiment of FIG. 3A along the line A2-A2'.

[0016] FIG. 3D shows a schematic cross-sectional view of the photodetector of the embodiment of FIG. 3A along the line A3-A3'.

[0017] FIGS. 4A to 4M show the top or cross-sectional views of a fabrication process to manufacture a photodetector, according to various embodiments.

[0018] FIG. 4N shows a cross sectional transmission electron microscopy (XTEM) image of a front view of a photodetector, according to various embodiments.

[0019] FIG. 4O shows a cross sectional transmission electron microscopy (XTEM) image of a front view of a nanoplasmonic waveguide of the embodiment of FIG. 4N.

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[0020] FIG. 4P shows a cross sectional transmission electron microscopy (XTEM) image of a front view of a nanoplasmonic waveguide of a photodetector, according to various embodiments.

[0021] FIG. 5 shows a map of calculated propagation loss as a function of the real and imaginary index of the silicide.

[0022] FIGS. 6A and 6B show respectively the y-component magnetic field (H_y) distributions along the waveguide (z-direction) and the x-component electric field (E_x) along a cross section of the waveguide for a silicide having a complex index of $1.0 + 1.5i$.

[0023] FIGS. 6C and 6D show respectively the y-component magnetic field (H_y) distributions along the waveguide (z-direction) and the x-component electric field (E_x) along a cross section of the waveguide for a silicide having a complex index of $4.0 + 5.0i$.

[0024] FIG. 7A shows a schematic of a band diagram of a silicide/Si/silicide structure under a positive bias, according to various embodiments.

[0025] FIG. 7B shows a plot 720 of internal quantum efficiency (η_i) of a thin-film silicide/Si Schottky-barrier photodetector of various embodiments, for different Schottky barrier heights (Φ_B).

[0026] FIGS. 8A and 8B show respective plots of calculated absorption (A) and external quantum efficiency (η_e) as a function of TaSi$_2$ thickness (W_{TaSi2}), according to various embodiments.

[0027] FIG. 9 shows a plot of calculated propagation loss (α) and absorption (A) as a function of silicon (Si) core width (W_{Si}), according to various embodiments.

[0028] FIG. 10 shows a plot of calculated propagation loss (α) and absorption (A) as a function of silicon nitride (Si$_3$N$_4$) isolator width (W_{SiN}), according to various embodiments.

Detailed Description

[0029] The following detailed description refers to the accompanying drawings that show, by way of illustration, specific details and embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and

structural, logical, and electrical changes may be made without departing from the scope of the invention. The various embodiments are not necessarily mutually exclusive, as some embodiments can be combined with one or more other embodiments to form new embodiments.

[0030] Embodiments described in the context of one of the methods or devices are analogously valid for the other method or device. Similarly, embodiments described in the context of a method are analogously valid for a device, and vice versa.

[0031] In the context of various embodiments, the phrase "at least substantially" may include "exactly" and a variance of +/- 5% thereof. As an example and not limitations, "A is at least substantially same as B" may encompass embodiments where A is exactly the same as B, or where A may be within a variance of +/- 5%, for example of a value, of B, or vice versa.

[0032] In the context of various embodiments, the term "about" or "approximately" as applied to a numeric value encompasses the exact value and a variance of +/- 5% of the value.

[0033] As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items.

[0034] Various embodiments may be related to a plasmonic detector or photodetector for integration in electronic photonic plasmonic integrated circuits, for example to directly convert surface plasmon polariton (SPP) signal to electric signal. A circuit or device incorporating the photodetector of various embodimens may be provided. The circuit with the detector may be used in applications for communication, bio-sensor, etc.

[0035] Various embodiments may provide a Schottky barrier nanoplasmonic detector or photodetector and a method for forming the same. Various embodiments may provide a silicide Schottky barrier detector (e.g. photodetector) integrated in a horizontal nanoplasmonic slot waveguide. Various embodiments may provide an integrated plasmonic detector or photodetector, which is fully CMOS compatible and offers a very high speed.

[0036] Various embodiments may provide an integrated silicide Schottky barrier detector designed to electrically detect surface plasmons propagating along a horizontal metal/insulator/Si/insulator/metal nanoplasmonic waveguide (e.g. slot waveguide), for

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example at the telecommunication wavelength of 1.55 μm. In various embodiments, ultrathin silicide layers may be inserted between the Si core and the insulators to absorb the optical power effectively, and the silicide/Si Schottky barrier height of the silicide/Si/silicide structure with a very narrow Si core may be substantially tuned by an applied voltage through the Schottky effect. The mechanism of a silicide Schottky barrier detector is based on (Φ_B < hv < E_g), where Φ_B refers to the Schottky barrier height, hv refers to the photon energy and E_g refers to the bandgap (e.g. Si bandgap).

[0037] Various embodiments may provide a plasmonic photodetector (e.g. a silicide SPP structure) directly integrated in a horizontal plasmonic waveguide to detect surface plasmon polariton (SPP) signal propagating along a plasmonic waveguide (e.g. having a Si waveguide or core) of the photodetector. The photodetector may have a horizontal silicide/Si/silicide metal-semiconductor-metal (MSM) structure integrated in a horizontal metal/insulator/Si/insulator/metal plasmonic or nanoplasmonic waveguide. The light confinement within the photodetector provides an effective absorption. In various embodiments, the Schottky barrier of the photodetector may be tunable, due to the metal-semiconductor-metal (MSM) structure with a very narrow semiconductor (e.g. Si) core width, by an applied voltage. The photodetector may have a high speed due to the ultracompact structure. Various embodiments may further provide an easy and fully Si-CMOS compatible fabrication process, as compared to other SPP detectors (e.g. Ge or GaAs based).

[0038] FIG. 1A shows a schematic block diagram of a photodetector 100, while FIG. 1B shows a simplified cross-sectional representation of the photodetector 100 of the embodiment of FIG. 1A, according to various embodiments.

[0039] The photodetector 100 includes a substrate 102, a waveguide (e.g. a Si waveguide or core) 104 formed on a surface of the substrate 102, a first metal layer 106 formed on a first side of the waveguide 104, wherein a first interface is defined between the waveguide 104 and the first metal layer 106, and a silicide layer 108 formed on a second side of the waveguide 104, wherein a second interface is defined between the waveguide 104 and the silicide layer 108, and wherein the second side is opposite to the first side, and wherein at least one of the first interface or the second interface is at least substantially perpendicular to the surface of the substrate 102. In FIG. 1A, the line

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represented as 110 is illustrated to show the relationship between the different components, which may include electrical coupling and/or mechanical coupling and/or optical coupling. In FIG. 1B, it should be appreciated that the positions of the first metal layer 106 and the silicide layer 108 may be interchangeable.

[0040] In various embodiments, the first interface may be at least substantially perpendicular to the surface of the substrate 102, or the second interface may be at least substantially perpendicular to the surface of the substrate 102, or both the first interface and the second interface may be at least substantially perpendicular to the surface of the substrate 102.

[0041] In various embodiments, the photodetector 100 may further include a second metal layer formed adjacent to the first metal layer 106, and a third metal layer formed adjacent to the silicide layer 108. The second metal layer and the third metal layer may be formed on the surface of the substrate 102.

[0042] In various embodiments, the photodetector 100 may further include a first dielectric layer formed between the first metal layer 106 and the second metal layer, and a second dielectric layer formed between the silicide layer 108 and the third metal layer. The first dielectric layer may be formed partially in a longitudinal direction of the waveguide 104, and wherein the second dielectric layer may be formed partially in the longitudinal direction of the waveguide 104.

[0043] FIG. 2 shows a flow chart 200 illustrating a method of forming a photodetector, according to various embodiments.

[0044] At 202, a substrate is provided.

[0045] At 204, a waveguide is formed on a surface of the substrate.

[0046] At 206, a first metal layer is formed on a first side of the waveguide, wherein a first interface is defined between the waveguide and the first metal layer.

[0047] At 208, a silicide layer is formed on a second side of the waveguide, wherein a second interface is defined between the waveguide and the silicide layer, and wherein the second side is opposite to the first side.

[0048] In various embodiments, the photodetector is formed such that at least one of the first interface or the second interface is at least substantially perpendicular to the surface of the substrate. In various embodiments, the first interface may be at least substantially

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perpendicular to the surface of the substrate, or the second interface may be at least substantially perpendicular to the surface of the substrate, or both the first interface and the second interface may be at least substantially perpendicular to the surface of the substrate.

5   [0049] In various embodiments, the method may further include forming a second metal layer adjacent to the first metal layer, and forming a third metal layer adjacent to the silicide layer. In various embodiments, forming the second metal layer may include forming the second metal layer on the surface of the substrate and forming the third metal layer may include forming the third metal layer on the surface of the substrate.

10   [0050] In various embodiments, the method may further include forming a first dielectric layer between the first metal layer and the second metal layer, and forming a second dielectric layer between the silicide layer and the third metal layer. In various embodiments, forming the first dielectric layer may include forming the first dielectric layer partially in a longitudinal direction of the waveguide, and forming the second

15   dielectric layer may include forming the second dielectric layer partially in the longitudinal direction of the waveguide.

[0051] In the context of various embodiments, the first metal layer (e.g. 106) may be another silicide layer. In the context of various embodiments, the silicide layer (e.g. 108) and the other silicide layer (e.g. equivalent to 106) may include an at least substantially

20   same material or different materials. Each of the silicide layer (e.g. 108) and the other silicide layer may include a material having a complex refractive index, wherein the complex refractive index has a real index and an imaginary index, and wherein the real index may be between about 1 and about 6 (e.g. between about 1 and about 4, between about 1 and about 2 or between about 3 and about 6) and the imaginary index may be

25   between about 0 and about 5.5 (e.g. between about 0 and about 4, between about 0 and about 2, or between about 3 and about 5.5).

[0052] In the context of various embodiments, each of the silicide layer (e.g. 108) and the other silicide layer may include a material selected from a group consisting of cobalt silicide (CoSi), nickel silicide (NiSi), titanium silicide (TiSi), palladium silicide (PdSi),

30   hafnium silicide (HfSi), niobium silicide (NbSi), platinum silicide (PtSi), vanadium silicide (VSi), tantalum silicide (TaSi) and any combinations thereof.

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[0053] In the context of various embodiments, a first Schottky barrier (e.g. a first silicide diode) may be formed at the first interface, and a second Schottky barrier (e.g. a second silicide diode) may be formed at the second interface. One of the first Schottky barrier or the second Schottky barrier may be forward biased, and the other Schottky barrier may be reverse biased when a voltage is applied between the first metal layer (e.g. 106) and the silicide layer (e.g. 108).

[0054] In the context of various embodiments, each of the second metal layer and the third metal layer may include copper (Cu), aluminium (Al), gold (Au), silver (Ag) or any alloys of these materials.

[0055] In the context of various embodiments, the first metal layer (e.g. 106) has a first permittivity, the silicide layer (e.g. 108) has a second permittivity, the first dielectric layer has a third permittivity and the second dielectric layer has a fourth permittivity, wherein the third permittivity and the fourth permittivity may be lower than the first permittivity and the second permittivity. In the context of various embodiments, the first permittivity and the second permittivity may be lower than a permittivity of a material of the waveguide (e.g. 104).

[0056] In the context of various embodiments, each of the first dielectric layer and the second dielectric layer may include silicon oxide, silicon nitride, silicon oxynitride, hafnium oxide, hafnium oxynitride or any other high-κ dielectric materials.

[0057] In the context of various embodiments, each of the first dielectric layer and the second dielectric layer may have a width of between about 1 nm and about 40 nm, e.g. between about 1 nm and about 20 nm, between about 1 nm and about 10 nm or between about 10 nm and about 40 nm.

[0058] In the context of various embodiments, each of the first metal layer (e.g. 106) and the silicide layer (e.g. 108) may have a width of between about 1 nm and about 10 nm, e.g. between about 1 nm and about 5 nm, between about 1 nm and about 3 nm or between about 5 nm and about 10 nm.

[0059] In the context of various embodiments, the waveguide (e.g. 104) may include a semiconductor. In various embodiments, the waveguide (e.g. 104) may include silicon.

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[0060] In the context of various embodiments, each of the first side of the silicon waveguide and the second side of the silicon waveguide may be silicon (110) crystal planes.

[0061] In the context of various embodiments, the waveguide (e.g. 104) may include a slot waveguide or a rib waveguide.

[0062] In the context of various embodiments, the waveguide (e.g. 104) may have a width of between about 10 nm and about 100 nm, e.g. between about 10 nm and about 80 nm, between about 10 nm and about 50 nm, between about 10 nm and about 30 nm, between about 30 nm and about 100 nm or between about 50 nm and about 100 nm.

[0063] In the context of various embodiments, the waveguide (e.g. 104) may have a height of between about 100 nm and about 500nm, e.g. between about 100 nm and about 300nm, between about 100 nm and about 200nm, or between about 300 nm and about 500nm.

[0064] In the context of various embodiments, the photodetector (e.g. 100) may have an absorption length of between about 0.5 μm and about 10 μm, e.g. between about 0.5 μm and about 5 μm, between about 0.5 μm and about 2 μm, between about 2 μm and about 10 μm, or between about 5 μm and about 10 μm.

[0065] In the context of various embodiments, the terms "dielectric", "isolator" and "insulator" may be interchangeably used.

[0066] In the context of various embodiments, a MSM structure means a metal-semiconductor-metal structure, which is a term normally used in the silicide photodetector field, while a MDM structure means a metal-dielectric-metal structure, which is a term normally used in the plasmonic waveguide field. In the context of various embodiments, the terms (MSM) and (MDM) may be equivalent and/or may be interchangeably used.

[0067] FIG. 3A shows a schematic perspective view of a photodetector 300, according to various embodiments. The photodetector 300 may be a plasmonic waveguide based silicide Schottky barrier detector.

[0068] The photodetector 300 includes a substrate 302, for example a silicon-on-insulator (SOI) or a buried oxide (BOX), e.g. SiO_2 of a SOI. The photodetector 300 further includes a waveguide 304, e.g. a slot waveguide or a rib waveguide, formed on or over

the substrate, e.g. on the surface 303 of the substrate 302. The waveguide 304 may be part of a plasmonic waveguide. The waveguide 304 may include a semiconductor, e.g. silicon (Si). In various embodiments, the waveguide 304 may include or may be a silicon core. The photodetector 300 further includes a silicide layer 306 formed on one side of the waveguide 304, defining an interface between the waveguide 304 and the silicide layer 306, and a silicide layer 308 formed on another side of the waveguide 304, defining an interface between the waveguide 304 and the silicide layer 308. The silicide layers 306, 308 are formed on opposite sides of the waveguide 304. The respective interfaces between the waveguide 304 and the silicide layer 306, and between the waveguide 304 and the silicide layer 308 are formed or oriented at least substantially perpendicular to the surface 303 of the substrate 302. In various embodiments, the waveguide 304 may have a width of between about 10 nm and about 100 nm, e.g. between about 10 nm and about 80 nm, between about 10 nm and about 50 nm, between about 10 nm and about 30 nm, between about 30 nm and about 100 nm or between about 50 nm and about 100 nm.

[0069] In various embodiments, each of the silicide layers 306, 308, may be used as an absorbing layer or material, for example for detecting surface plasmon polariton (SPP) signal.

[0070] In various embodiments, each of the silicide layers 306, 308 may have or may be of a material having a complex refractive index, where the complex refractive index may have a real index of between about 1 and about 6 (e.g. between about 1 and about 4, between about 1 and about 2 or between about 3 and about 6) and an imaginary index of between about 0 and about 5.5 (e.g. between about 0 and about 4, between about 0 and about 2, or between about 3 and about 5.5).

[0071] In various embodiments, the silicide layer 306 may have the same material as that of the silicide layer 308 or both silicide layers 306, 308 may have different materials, i.e. different silicide materials. The material of each of the silicide layers 306, 308 may include but not limited to cobalt silicide (CoSi), nickel silicide (NiSi), titanium silicide (TiSi), palladium silicide (PdSi), hafnium silicide (HfSi), niobium silicide (NbSi), platinum silicide (PtSi), vanadium silicide (VSi), tantalum silicide (TaSi) or any combinations thereof.

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[0072] In various embodiments, each of the silicide layers 306, 308 may extend through the absorber region 310 and the contact region 312 of the plasmonic detector portion 313. In various embodiments, each of the silicide layers 306, 308 may not extend to the plasmonic waveguide portion 314.

[0073] In various embodiments, each of the silicide layers 306, 308 may have a width of between about 1 nm and about 10 nm, e.g. between about 1 nm and about 5 nm, between about 1 nm and about 3 nm or between about 5 nm and about 10 nm.

[0074] In various embodiments, any one of the silicide layers 306, 308 may be a metal layer (e.g. a first metal layer).

[0075] The photodetector 300 may further include a metal layer (e.g. a second metal layer) 316 formed adjacent to the silicide layer 306. The photodetector 300 may further include a metal layer (e.g. a third metal layer) 318 formed adjacent to the silicide layer 308.

[0076] Each of the metal layers 316, 318 are formed on the surface 303 of the substrate 302. Each of the metal layers 316, 318 may extend through the absorber region 310, the contact region 312 and the plasmonic waveguide portion 314. Each of the metal layers 316, 318 may be in direct contact with the silicide layers 306, 308 respectively, for example in the contact region 312.

[0077] In various embodiments, the metal layer 316 may have the same material as that of the metal layer 318 or both metal layers 316, 318 may have different materials. The material of each of the metal layers 316, 318 may include but not limited to copper (Cu), aluminium (Al), gold (Au), silver (Ag) and alloys of these materials.

[0078] The photodetector 300 may further include a dielectric layer (e.g. a first dielectric layer) 320 formed between the silicide layer 306 and the metal layer 316. The dielectric layer 320 may be formed at least partially or extending partially in a longitudinal direction (z-direction as illustrated in FIG. 3A) of the waveguide 304. The photodetector 300 may further include a dielectric layer (e.g. a second dielectric layer) 322 formed between the silicide layer 308 and the metal layer 318. The dielectric layer 322 may be formed at least partially or extending partially in a longitudinal direction (z-direction as illustrated in FIG. 3A) of the waveguide 304. In various embodiments, each of the dielectric layers 320, 322 may extend through the plasmonic

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waveguide portion 314 and the absorber region 310. In various embodiments, each of the dielectric layers 320, 322 may not extend to the contact region 312. In various embodiments, each of the dielectric layers 320, 322 may have a width of between about 1 nm and about 40 nm, e.g. between about 1 nm and about 20 nm, between about 1 nm and about 10 nm or between about 10 nm and about 40 nm.

[0079] In various embodiments, the dielectric layer 320 may have the same material as that of the dielectric layer 322 or both dielectric layers 320, 322 may have different materials. The material of each of the dielectric layers 320, 322 may include but not limited to silicon oxide (SiO$_x$), silicon nitride (SiN), silicon oxynitride (SiON), hafnium oxide (HfO$_2$), hafnium oxynitride (HfON) or any other high-κ dielectric materials.

[0080] In various embodiments, the respective permittivities of the dielectric layers 320, 322 may be lower than the respective permittivities of the silicide layers 306, 308. In various embodiments, the respective permittivities of the silicide layers 306, 308 may be lower than a permittivity of the waveguide 304.

[0081] As shown in FIG. 3A, a voltage, as represented by 330 may be applied to the contact region 312, between the metal layer 316 and the metal layer 318. Therefore, a voltage may be applied between the silicide layer 306 and the silicide layer 308.

[0082] In various embodiments, respective Schottky barriers (or silicide diodes) may be formed at the respective interfaces between the waveguide 304 and the silicide layer 306, and between the waveguide 304 and the silicide layer 308. In various embodiments, the respective Schottky barriers may be oppositely biased, e.g. one Schottky barrier is forward biased while the other is reversed biased, e.g. when the voltage 330 is applied.

[0083] In various embodiments, the photodetector 300 may detect the SPP signal propagating along the metal 316/dielectric 320/Si 304/dielectric 322/metal 318 structure in the plasmonic waveguide portion 314, based on the two silicide layers 320, 322, placed on opposite sidewalls of the Si waveguide 304 in the absorber region 310 of the plasmonic detector portion 313.

[0084] While not shown, a cladding layer (e.g. SiO$_2$) may be provided over the photodetector 300 to encapsulate the photodetector 300. In other words, the photodetector 300 may be embedded in a cladding layer of for example SiO$_2$.

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[0085] FIG. 3B shows a schematic cross-sectional view of the photodetector 300 of the embodiment of FIG. 3A along the line A1-A1', at the plasmonic waveguide portion 314. At the plasmonic waveguide portion 314, the photodetector 300 includes a plasmonic waveguide structure or arrangement of "metal / isolator (or dielectric) / waveguide (e.g. Si) / isolator (or dielectric) / metal".

[0086] Each of or any one of the interfaces defined between the dielectric layer 320 and the waveguide 304, between the dielectric layer 322 and the waveguide 304, between the metal layer 316 and the dielectric layer 320, and between the metal layer 318 and the dielectric layer 322, may be at least substantially perpendicular to the surface 303 of the substrate 302.

[0087] The waveguide 304, the metal layers 316, 318 and the dielectric layers 320, 322 may have at least substantially similar heights, h1. In various embodiments, h1 may depend on the height of the waveguide (e.g. Si) 304, which may be between about 100 nm and about 500nm, e.g. between about 100 nm and about 300nm, between about 100 nm and about 200nm, or between about 300 nm and about 500nm.

[0088] FIG. 3C shows a schematic cross-sectional view of the photodetector 300 of the embodiment of FIG. 3A along the line A2-A2', at the absorber region 310. At the absorber region 310, the photodetector 300 has a plasmonic detector structure or arrangement of "metal / isolator (or dielectric) / silicide / waveguide (e.g. Si) / silicide / isolator (or dielectric) / metal".

[0089] Each of or any one of the interfaces defined between the silicide layer 306 and the dielectric layer 320, between the silicide layer 308 and the dielectric layer 322, between the metal layer 316 and the dielectric layer 320, and between the metal layer 318 and the dielectric layer 322, may be at least substantially perpendicular to the surface 303 of the substrate 302.

[0090] The waveguide 304, the silicide layers 306, 308, the metal layers 316, 318 and the dielectric layers 320, 322 may have at least substantially similar heights, h2. The height, h2, may be at least substantially same as h1.

[0091] FIG. 3D shows a schematic cross-sectional view of the photodetector 300 of the embodiment of FIG. 3A along the line A3-A3', at the contact region 312. At the contact

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region 312, the photodetector 300 has a structure or arrangement of "metal / silicide / waveguide (e.g. Si) / silicide / metal".

[0092] Each of or any one of the interfaces defined between the silicide layer 306 and the metal layer 316, and between the silicide layer 308 and the metal layer 318 may be at least substantially perpendicular to the surface 303 of the substrate 302.

[0093] The waveguide 304, the silicide layers 306, 308, and the metal layers 316, 318 may have at least substantially similar heights, h3. The height, h3, may be at least substantially same as h1 and h2.

[0094] The absorber region 310 may have a length or absorption length, L_{abs}, of between about 0.5 µm and about 10 µm, e.g. between about 0.5 µm and about 5 µm, between about 0.5 µm and about 2 µm, between about 2 µm and about 10 µm, or between about 5 µm and about 10 µm. The contact region 312 may have a length, L_{con}, of between about 0.2 µm and about 20 µm, e.g. between about 0.2 µm and about 10 µm, between about 0.2 µm and about 5 µm, between about 1 µm and about 20 µm, between about 1 µm and about 5 µm, between about 5 µm and about 20 µm or between about 10 µm and about 20 µm.

[0095] As illustrated in FIGS. 3A to 3D, the photodetector 300 may be a silicon (Si) waveguide-based silicide Schottky barrier detector (SBD) having a horizontal structure or arrangement, i.e. the waveguide 304, the silicide layers 306, 308, the metal layers 316, 318 and the dielectric layers 320, 322 may be arranged one after the other in the x-direction illustrated.

[0096] In one embodiment, the metal layers 316, 318, may be copper (Cu), and the dielectric layers 320, 322 may be silicon oxide (SiO_2). Therefore, the photodetector 300 may have a horizontal plasmonic waveguide structure of $Cu/SiO_2/Si/SiO_2/Cu$ in the plasmonic waveguide portion 314. At the absorber region 310, respective thin silicide layers 306, 308 may be inserted or formed between the Si core waveguide 304 and the respective dielectric layers 320, 322 on opposite sides of the Si core waveguide 304 to form a horizontal structure of $Cu/SiO_2/silicide/Si/silicide/SiO_2/Cu$. The absorber region 310 may have a length, L_{abs}, to absorb surface plasmon polariton (SPP) signals propagating along the plasmonic waveguide of $Cu/SiO_2/Si/SiO_2/Cu$.

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[0097] At the contact region 312, at the rear of the photodetector 300, a horizontal structure of Cu/silicide/Si/silicide/Cu is provided to form the electrode terminals.

[0098] FIGS. 4A to 4M show the top or cross-sectional views of a fabrication process to manufacture a photodetector, according to various embodiments. The fabrication parameters may be determined during the processing.

[0099] The fabrication process begins with a silicon-on-insulator (SOI) wafer. The SOI wafer includes a layer of silicon (Si) on an insulator (SiO_2) layer. A silicon oxide (SiO_2)/silicon nitride (SiN)/silicon oxide (SiO_2) hard mask is then deposited on the SOI wafer. The silicon oxide (SiO_2)/silicon nitride (SiN)/silicon oxide (SiO_2) hard mask may be deposited using a plasma-enhanced chemical vapour deposition (PECVD) process sequentially. The SiO_2 layers may result in a better waveguide profile while the SiN layer may be used as a stopping layer for a chemical mechanical polishing (CMP) process to be carried out in a later process. However, it should be appreciated that a single mask layer (e.g. SiO_2) may instead be used.

[0100] The hard mask is then patterned and the silicon layer of the SOI wafer may then be etched based on the hard mask, thereby transferring the pattern of the hard mask onto the silicon layer for patterning a waveguide. In the etching process, the SiO_2/SiN/SiO_2 hard mask is first dry etched using a photoresist as a mask. The photoresist is then stripped or removed. The silicon layer of the SOI wafer may then be dry etched down to the SiO_2 insulator layer of the SOI wafer based on the etched SiO_2/SiN/SiO_2 hard mask to form a waveguide. This etching process may provide a good profile of the waveguide. During the etching process, the upper SiO_2 layer of the hard mask may be removed and after the etching process, the SiN layer and the lower SiO_2 layer of the hard mask may be maintained over the silicon waveguide. The SiN layer may be used as a stopping layer for a chemical mechanical polishing (CMP) process to be carried out in a later process.

[0101] FIGS. 4A and 4B show the top and cross-sectional views respectively of the structure 400 that may be obtained. The structure 400 includes a silicon layer 402, which has been patterned to form a waveguide, on a SiO_2 layer 404. The structure further includes a SiN layer 406 over the silicon waveguide 402. While not shown in FIG. 4B, it should be appreciated that the lower SiO_2 layer of the hard mask is present between the silicon layer 402 and the SiN layer 406. For illustration and clarity purposes, the SiN hard

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mask layer 406 is not shown in the schematic top view of the structure 400 of FIG. 4A. FIG. 4A further shows a scanning electron image (SEM) image 408 of a portion, as highlighted by the dotted box 410, of the structure 400.

[0102] Subsequently, deposition of silicon nitride (SiN) may be carried out over the structure 400, followed by deposition of silicon oxide (SiO_2) over the structure 400. The silicon nitride (SiN) and the silicon oxide (SiO_2) may be deposited using a plasma-enhanced chemical vapour deposition (PECVD) process sequentially. A window is then opened on the deposited SiO_2, by depositing and patterning a photoresist over the deposited SiO_2, and dry etching the deposited SiO_2 using the photoresist as the mask, and using the deposited SiN as an etch stop layer.

[0103] FIGS. 4C and 4D show the top and cross-sectional views respectively of the structure 420 that may be obtained. The structure 402 includes a layer of deposited SiN 422, which includes the SiN hard mask 406 over the top of the silicon waveguide 402. The SiN layer 422 is deposited on the sidewalls of the silicon waveguide 402 and also on the surface of the SiO_2 layer 404 of the SOI wafer. The structure 420 further includes the SiO_2 layer 424 deposited over the SiN layer 422, with a window, as represented by the box 426, that is opened on the SiO_2 layer 424 to provide access to the silicon waveguide 402. For illustration and clarity purposes, the SiN layer 422 and the SiO_2 layer 424 are not shown in the schematic top view of the structure 420 of FIG. 4C. FIG. 4C further shows a scanning electron image (SEM) image 428 of a portion, as highlighted by the dotted box 430, of the structure 420.

[0104] Subsequently, a thin layer of SiO_2 is deposited within the window 426. FIG. 4E shows the cross-sectional view of the structure 440 that may be obtained. The structure 440 includes a layer of SiO_2 442 deposited within the window 426, over the layer of SiN 422.

[0105] Silicide window opening is then performed, by depositing and patterning a photoresist over the silicon waveguide 402, followed by dry etching of the SiO_2 layer 442, stripping or removal of the photoresist, and wet etching of the SiN layer 422.

[0106] FIGS. 4F and 4G show respectively the top view of the structure 450 and the cross-sectional view of the structure 450 that may be obtained within the silicide window, as represented by the box 452, that is opened, where the SiO_2 layer 442 has been etched

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away. A part of the SiN 422 over the silicon waveguide 402 remains as the SiN 422 on the sidewall of the silicon waveguide 402 is thinner than the SiN 422 over the top of the silicon waveguide 402. For illustration and clarity purposes, the SiN layer 422 and the SiO$_2$ layer 424 are not shown in FIG. 4F.

[0107] A metal (e.g. tantalum (Ta), nickel (Ni), etc) may then be deposited on the sidewalls of the silicon waveguide 402 within the silicide window 452, followed by silicidation by a rapid thermal annealing (RTA) process to form thin silicide on the sidewalls of the silicon waveguide 402, and then selective wet etching of the un-reacted metal. The self-aligned silicide (SALICIDE) process may be used for forming the silicides on the sidewalls of the silicon waveguide 402.

[0108] FIG. 4H shows the cross-sectional view of the structure 454 that may be obtained, including silicide layers 456, 458, formed on the sidewalls of the silicon waveguide 402 within the silicide window 452.

[0109] A thin layer of SiN may then be deposited to surround the silicon waveguide 402 within the silicide window 452, thereby encapsulating the silicide layers 456, 458. FIG. 4I shows the cross-sectional view of the structure 460 that may be obtained. The SiN layer 462 includes the SiN layer 422 and the thin layer of SiN deposited that encapsulates the silicide layers 456, 458 over the sidewalls of thesilicon waveguide 402.

[0110] Contact region window opening is then performed, by depositing and patterning a photoresist over the SiN layer 462, and dry etching of the SiN layer 462 using the photoresist as the mask. FIG. 4J shows the top view of the structure 466 that may be obtained, showing the contact region window, as represented by the box 468, that is opened. For illustration and clarity purposes, the SiO$_2$ layer 424, the silicide layers 456, 458 and the SiN layer 462 are not shown in FIG. 4F. Similar to the process of silicide window opening, after the contact region window opening process, a part of the SiN 462 over the silicon waveguide 402 remains as the SiN 462 over the sidewalls of the silicon waveguide 402 is thinner than the SiN 462 over the top of the silicon waveguide 402.

[0111] A metal (e.g. tantalum (Ta), nickel (Ni), etc) may then be deposited on the sidewalls of the silicon waveguide 402 within the contact region window 468, followed by silicidation by a rapid thermal annealing (RTA) process to form thick silicides on the sidewalls of the silicon waveguide 402, and then selective wet etching of the un-reacted

metal. The self-aligned silicide (SALICIDE) process may be used for forming the silicides on the sidewalls of the silicon waveguide 402.

[0112] FIG. 4K shows the cross-sectional view of the structure 470 that may be obtained, including silicide layers 472, 474, formed on the sidewalls of the silicon waveguide 402 within the contact region window 468. The thick silicide layers 472, 474, may prevent diffusion of metal (e.g. Cu) that is to be deposited in a later process between the silicide layers 472, 474 and the SiO₂ layer 424.

[0113] Subsequently, a metal (e.g. copper (Cu)) may be deposited over the entire structure that has been processed as described above, followed by a planarization process, for example a chemical mechanical planarization or polishing (CMP) to remove a portion of the deposited metal, and stopping on the SiN 462. The SiN 462 over the top of the silicon waveguide 402 is maintained to minimise or avoid electrical short.

[0114] FIG. 4L shows the cross-sectional view of the structure 480 that may be obtained, at the portion within the silicide window 452, to form an absorber region (e.g. 310 of FIG. 3A). The structure 480 includes the deposited metal (e.g. Cu) 482.

[0115] FIG. 4M shows the cross-sectional view of the structure 481 that may be obtained, at the portion within the contact region window 468, to form a contact region (e.g. 312 of FIG. 3A). The structure 481 includes the deposited metal (e.g. Cu) 482.

[0116] Subsequently, one or more metal (e.g. aluminium (Al)) electrodes or contacts may be formed, for example at the contact region (e.g. 312 of FIG. 3A).

[0117] FIG. 4N shows a cross sectional electron transmission microscopy (XTEM) image 483 of a front view of a photodetector, according to various embodiments, at a nanoplasmonic waveguide portion of the photodetector. The photodetector includes a nanoplasmonic waveguide including a Si core 496 (e.g. equivalent to 402) and a layer of Cu 484 (e.g. equivalent to 482) surrounding the Si core 496. The nanosplamonic waveguide is formed on a layer of SiN 485 (e.g. equivalent to 462) over a SiO₂ layer 486 (e.g. equivalent to 404), and is surrounded by a SiO₂ layer 487 (e.g. equivalent to 424).

[0118] FIG. 4O shows a cross sectional transmission electron microscopy (XTEM) image 488 of a front view of the nanoplasmonic waveguide of the embodiment of FIG. 4N, at the portion within the dotted ellipse illustrated in FIG. 4N. The XTEM image 488 shows a nanoplasmonic waveguide including a Si core 496 surrounded by a

dielectric layer of SiO$_2$ 489 and a metal layer of Cu 484. The Si core 496 may have a width of about 50 nm at the central portion.

[0119] FIG. 4P shows a cross sectional transmission electron microscopt (XTEM) image 490 of a front view of a nanoplasmonic waveguide of a photodetector, according to various embodiments, at a nanoplasmonic waveguide portion of the photodetector. The XTEM image 490 shows a nanoplasmonic waveguide including a Si core 492 surrounded by a dielectric layer of HfO$_2$ 493 and a metal layer of Al 494. The Si core 496 may have a width of about 85 nm at the central portion.

[0120] Various embodiments may provide one or more of the following advantages: (i) As the silicide layers may be fabricated using the self-aligned silicide (SALICIDE) process, and that the thicknesses of the silicide layers may be precisely or more accurately controlled, e.g. by the temperature for solid-phase reaction, the fabrication of the photodetector of various embodiments is easy and straightforward, and is fully Si-CMOS compatible; (ii) The metal-semiconductor waveguide-metal structure with a semiconductor layer that is sufficicently thin to be fully depleted enables a broader tuning range of the Schottky barrier height, Φ_B, by an applied voltage through the Schottky effect; (iii) By selecting a silicide with suitable optical parameters, the SPP model may be concentrated in the thin silicide layers to be quickly absorbed, even if the silicide layers are very thin (e.g. approximately 2 nm) and short (e.g. approximately 1 μm). The small areas of the silicide layers may result in only a small or reduced dark current, and/or may tolerate a low Schottky barrier height, Φ_B, to improve the responsivity of the photodetector; (iv) The photodetector of various embodiments may offer very high speed due to its ultra-compact structure, and (v) The photodetector of various embodiments may offer high responsivity.

[0121] A 2-dimensional (2-D) optical simulation method for the photodetector of various embodiments will now be described. The simulation may be carried out using the software FullWAVE from RSOFT. The FullWAVE software is based on a finite-difference time-domain (FDTD) method.

[0122] For the optical simulation method, a very fine and non-uniform grid (e.g. about 0.5 nm at the bulk and about 0.1 nm near the interface) is set, to capture the field change around the very thin silicide layers (e.g. 306, 308). As a 3-D FDTD simulation with such

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a fine grid size needs a very long computational time, the 2-D FDTD simulation used may offer simplification, which corresponds to an infinite height of the photodetector (e.g. 300, FIGS. 3A to 3D), for example in the direction of the y-axis as shown in FIGS. 3A to 3D.

[0123] While the height dependence of plasmonic slot waveguides may become weak with increasing height, for example for a height of 0.3 µm and above, the 2-D simplification may not cause any significant error for the photodetector of various embodiments having a height of approximately 0.34 µm (e.g. h1, h2, h3).

[0124] A fundamental 1550 nm (1.55 µm) transverse electric (TE) mode light (the electric field is parallel to the x-axis) may be launched at the plasmonic slot waveguide to propagate through the photodetector. A perfectly matched layer may be used to attenuate the field within its region without back reflection. The perfectly matched layer is a boundary condition used in simulation, which means that light is substantially or totally absorbed without reflection at this layer.

[0125] Copper (Cu) is used as the metal as it a metal used in CMOS technology and that Cu-waveguide has a much lower propagation loss than the Al-counterpart. The complex refractive index of Cu at about 1.55 µm is about $0.606 + 8.92i$. The isolator or dielectric may be silicon oxide (SiO_2) or silicon nitride (Si_3N_4), with the refractive indices of about 1.44 and 2.0, respectively. The refractive index for silicon (Si) is about 3.45.

[0126] Different silicides have different complex refractive indices ($n + ki$, where n is the real component and k is the imaginary component). The n and k values for various silicides at about 1550 nm are listed in Table 1 below, which are mostly measured on the Si (100) surface, while the silicide layers in the photodetector of various embodiments are on the Si (110) surfaces (i.e. on the sidewalls of the Si waveguide). Both the electrical and optical properties of silicides may depend on the orientation. However, the possible orientation dependence is ignored in the simulation due to a lack of optical and electrical information on the Si (110) surface.

[0127] A part of Si may be consumed or used to form silicide through solid phase reaction of as-deposited metal on Si, with Si. The amount of consumed Si may depend on the silicide itself. For the simulation, a ($W_{silicide}/2$)-thick Si is assumed to be consumed on one side of the Si waveguide to form a $W_{silicide}$-thick silicide for all silicides, i.e., the Si

core width (W_{Si}) in the plasmonic waveguide portion (e.g. 314, FIG. 3A) becomes ($W_{Si} - W_{silicide}$) in the plasmonic detector portion (e.g. 313, FIG. 3A).

[0128] The absorption or power absorption of the photodectector of various embodiments will now be described, using the structure Cu / isolator / silicide / Si / silicide / isolator / Cu as a non-limiting example. Based on the embodiments of FIGS. 3A to 3D, the absorber region 310 has a Cu / isolator / silicide / Si / silicide / isolator / Cu structure, which may be regarded as a plasmonic waveguide.

[0129] In order to calculate the propagation loss, the parameters of the plasmonic waveguide may be set as follows: the width, $W_{silicide}$, of each silicide layer is about 5 nm (which is formed from part of the Si core and the metal deposited on each side of the Si core), the width, W_{Si}, of the Si core is about 50 nm (thus, the actual Si core width is about 45 nm as about 2.5 nm of the Si core may be consumed on each side to form a part of a respective silicide layer) and the isolator is SiO_2 with a width, W_{SiO2}, of about 10 nm. The n and k values of the silicide may vary from 1 to 6 and 0 to 5.5, respectively, which include most silicides.

[0130] FIG. 5 shows a map 500 of calculated propagation loss (in dB/μm) as a function of the real and imaginary index of the silicide, for a Cu / SiO_2 (10 nm) / silicide (5 nm) / Si (45 nm) / silicide (5 nm) / SiO_2 (10 nm) / Cu plasmonic waveguide. The positions corresponding to different silicides, as listed in Table 1 below, are indicated in the map 500. As illustrated in FIG. 5, the propagation loss of the waveguide with silicide depends on not only the imaginary index of silicide, but also the real index of silicide. While not wishing to be bound by any theory, this behavior may be explained by the continuity of electric displacement normal to the interfaces, e.g. the interface between the Si core and the silicide. For comparison, the corresponding plasmonic waveguide without silicide layers has a propagation loss of approximately 0.85 dB/μm.

[0131] FIGS. 6A and 6B show respectively the y-component magnetic field (H_y) distributions along the waveguide (z-direction) and the x-component electric field (E_x) along a cross section of the waveguide for a silicide having a complex index of 1.0 + 1.5i.

[0132] FIGS. 6C and 6D show respectively the y-component magnetic field (H_y) distributions along the waveguide (z-direction) and the x-component electric field (E_x) along a cross section of the waveguide for a silicide having a complex index of 4.0 + 5.0i.

[0133] Due to the continuity of electric displacement normal to the interfaces, the boundary conditions are : $\varepsilon_{Si}E_x(Si^-) = |\varepsilon_{silicide}|E_x(silicide^+)$ and $|\varepsilon_{silicide}|E_x(silicide^-) = \varepsilon_{SiO2}E_x(SiO_2^-)$, where $\varepsilon_{silicide}$ $(=\varepsilon'+\varepsilon''i=(n+ki)^2=(n^2-k^2)+(2nk)i)$ is the silicide permittivity and $|\varepsilon_{silicide}|$ $(=\sqrt{\varepsilon'^2+\varepsilon''^2})$ is its absolute value, ε_{Si} (= 11.9) and ε_{SiO2} (= 2.0) are the permittivity of Si and SiO$_2$, respectively.

[0134] In the embodiment where the silicide index is 1.0 + 1.5i, $|\varepsilon_{silicide}|$ = 3.5 is smaller than ε_{Si}, thus the electric field is confined in the silicide and the SiO$_2$ regions, as shown in FIG. 6B, thus leading to a quick attenuation of the propagating SPP mode, as shown in FIG. 6A.

[0135] In the embodiment where the silicide index is 4.0 + 5.0i, the electric field in the silicide layer is smaller than that in the Si layer due to a large $|\varepsilon_{silicide}|$ of 41, as shown in FIG. 6D. The silicide behaves as a metal for the plasmonic device or photodetector and the waveguide has a relatively low propagation loss, as shown in FIG. 6C.

[0136] In contrast to a conventional waveguide where the propagation loss should be small, the propagation loss of the waveguide with silicide or silicide layer(s) of the photodetector of various embodiments should be large for light absorption. Therefore, among the silicides listed in Table 1 below, TaSi$_2$ may be used for the photodetector of various embodiments as it has the lowest $|\varepsilon_{silicide}|$, where TaSi$_2$ is also a silicide used in the standard CMOS technology. Moreover, based on the above analysis, it is expected that the permittivity (hence, the refractive index) of the isolator should be high.

[0137] A map of propagation loss as a function of the real and imaginary index of the silicide, for a Cu/SiN/silicide/Si/silicide/SiN/Cu plasmonic waveguide has also been generated (result not shown), which is similar to map 500 of FIG. 5, but with a larger propagation loss. For example, the maximum propagation loss increases from about 20 dB/μm to about 35 dB/μm, and the propagation loss of TaSi$_2$-waveguide increases from about 4.07 dB/μm to about 7.87 dB/μm by replacing SiO$_2$ with Si$_3$N$_4$ as the dielectric or isolator. Therefore, in various embodiments of the photodetector, Si$_3$N$_4$ may be chosen as the isolator and TaSi$_2$ may be chosen as the silicide.

[0138] A silicide with a smaller permittivity may provide a larger propagation loss. The optical property of silicide may be majorly determined by the silicide itself. It is expected

that alloying of two or three silicides, i.e. ternary or quaternary silicides formed by co-deposited metals with Si, may have different optical properties as compared to individual silicides. For example, $Co_{1-x}Ni_xSi_2$ has electrical properties (e.g. Schottky barrier height and resistivity) between that of $CoSi_2$ and NiSi. It may be possible to obtain a silicide with a low $|\varepsilon_{silicide}|$, owing to the huge number of ternary or quaternary silicides with different component ratios that may be possible. Based on the map 500 of FIG. 5, an ideal silicide may be defined for a silicide that is located at around the maximum propagation loss region, e.g. a silicide having a complex index of about $1 + 1.5i$.

[0139] The propagation loss of a plasmonic waveguide with silicide may be caused by light absorption in the Cu, isolator, silicide, and Si regions, where the absorption in the silicide region contributes to a photocurrent. For a L_{abs}-long waveguide, the effective absorption (A) may be expressed as:

$$A = \gamma_C \cdot \left(1 - 10^{-\alpha \cdot L_{abs}}\right) \cdot ratio \qquad \text{(Equation 1),}$$

where γ_C is the coupling efficiency from the plasmonic waveguide portion (e.g. 314) to the plasmonic detector portion (e.g. 313), α is the propagation loss in unit dB/μm, L_{abs} (e.g. 310, FIG. 3A) is the waveguide length in unit μm, and ratio is the power absorbed in silicide over the total power absorbed.

[0140] Table 1 shows the calculated optical properties for a 1-μm-long Cu / SiN (10 nm) / silicide (5 nm) / Si(45 nm) / silicide (5 nm) / SiN (10 nm) / Cu waveguide at a wavelength of about 1550 nm for different silicides.

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Table 1

	Index		Calculated optical properties				Φ_n	ρ
	n	k	α (dB/μm)	ratio	γ_C	A	(eV)	($\mu\Omega\cdot$cm)
CoSi$_2$	0.91	6.62	2.05	0.25	0.99	0.095	0.67	9-20
Ni$_3$Si	5.90	5.15	2.81	0.45	1.00	0.212	N.A.	70-106
Ni$_2$Si	3.76	3.87	4.27	0.54	0.99	0.331	0.66	30-60
NiSi	1.54	4.73	3.61	0.48	0.99	0.263	0.66	14-20
TiSi$_2$	2.06	4.13	4.74	0.57	0.99	0.369	0.60	11-15
Pd$_2$Si	3.75	5.14	3.44	0.48	0.99	0.258	0.74	13-18
HfSi$_2$	4.05	2.04	4.43	0.56	0.99	0.354	0.60	>60
NbSi$_2$	3.18	2.61	6.02	0.64	0.99	0.472	0.62	22-50
PtSi	3.09	4.25	4.35	0.54	0.99	0.337	0.88	25-35
VSi$_2$	4.14	2.15	4.32	0.55	0.99	0.343	0.54	34-59
TaSi$_2$	2.47	2.55	7.87	0.71	0.99	0.590	0.60	20-50
Ideal	1.00	1.50	27.51	0.90	0.98	0.887	N.A.	N.A.

where: n = real component of the complex refractive index,

k = imaginary component of the complex refractive index,

α = propagation loss,

ratio = power absorbed in silicide over the total power absorbed,

γ_C = coupling efficiency from the plasmonic waveguide portion to the plasmonic detector portion,

A = effective absorption,

Φ_n = electron Schottky barrier height. The corresponding hole Schottky barrier height (Φ_p) may be approximately calculated as: $\Phi_p \approx E_g - \Phi_n$, where E_g ($\approx$ 1.12 eV) is the Si band gap, and

ρ = resistivity of silicide.

[0141] The complex permittivity is related to n and k, where $\varepsilon = \varepsilon' + \varepsilon'' i = (n + ki)^2$, where ε' is the real part and ε'' is the imaginary part of the permittivity. As may be observed from Table 1, a smaller permittivity of silicide increases not only the propagation loss, but also the ratio of the power absorbed in the silicide layer due to power confinement. In addition, Table 1 shows that the SPP mode propagating along the

metal/isolator/Si/isolator/metal plasmonic waveguide portion may effectively couple into the plasmonic detector portion. Therefore, the silicide material of the photodetector of various embodiments may be appropriately chosen as the permittivity of the silicide material may affect the performance of the photodetector.

[0142] The internal quantum efficiency and the external quantum efficiency of the plasmonic photodetector of various embodiments, based on the Scales' model [C. Scales and P. Berini, "*Thin-film Schottky barrier photodetector models*", IEEE J. Quantum Electronics 46 (5), 633-643 (2010)], will now be described.

[0143] The photodetector of various embodiments has a metal-semiconductor-metal structure. FIG. 7A shows a schematic of a band diagram 700 of a silicide/Si/silicide structure under a positive bias, according to various embodiments. Under a positive bias (V), the left silicide/Si Schottky contact 702 may be reversely biased and the right silicide/Si Schottky contact 704 may be forwardly biased for electrons, and vice versa for holes. In FIG. 7A, "t" represents the silicide thickness.

[0144] In the photodetector of various embodiments, the left silicide layer of the silicide/Si Schottky contact 702 and the right silicide layer of the silicide/Si Schottky contact 704 may be assumed to absorb power equally. The hot electrons excited in the left silicide layer emits through Φ_n to be collected by the right silicide layer, and the hot holes excited in the right silicide layer emits through Φ_p to be collected by the left silicide layer. The hot electrons and holes may both contribute to the photocurrent.

[0145] In various embodiments, due to the narrow Si width, the Si layer may be fully depleted under bias and the constant electric field across the Si layer may be given by V/W_{Si} (=biasing voltage/width of silicon layer).

[0146] The applied voltage may lead to both Φ_n and Φ_p lowering. The decrease of both Φ_n and Φ_p may be predicted by the Schottky effect based on Equation 2 below:

$$\Delta\Phi = \sqrt{\frac{eV}{4\pi\varepsilon_0\varepsilon_{Si}W_{Si}}} \qquad \text{(Equation 2)},$$

where e is the electron charge, ε_0 is the permittivity of vacuum and ε_{Si} is the permittivity of silicon (Si). Based on Equation 2, for an embodiment where W_{Si} is about 45 nm and V is about 1 V, $\Delta\Phi$ is approximately 0.05 eV.

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[0147] For embodiments of a photodetector using TaSi$_2$, Φ_n is approximately 0.6 eV and Φ_p is aproximately 0.5 eV. Therefore, the effective barrier heights, for Φ_n and Φ_p, under a 1 V bias may become approximately 0.55 eV and approximately 0.45 eV, respectively. Lower effective Φ_n and Φ_p may be obtained at a higher bias voltage and/or a narrower Si width. The Schottky barrier height for electron (Φ_n) is different to the Schottky barrier height for hole (Φ_p). For a particular silicide/Si diode, $\Phi_n + \Phi_p$ is approximately 1.12 eV (where 1.12 eV is the energy bandgap of Si). Based on this, the TaSi$_2$ silicide may be assumed to have Φ_n of about 0.55 eV and Φ_p of about 0.45 eV, after taking the voltage induced barrier height lowering effect into consideration.

[0148] FIG. 7B shows a plot 720 of internal quantum efficiency (η_i) of a thin-film silicide/Si Schottky-barrier photodetector of various embodiments, for different Schottky barrier heights (Φ_B), calculated based on the Scales' model [C. Scales and P. Berini, "Thin-film Schottky barrier photodetector models", IEEE J. Quantum Electronics 46 (5), 633-643 (2010)]. The plot 720 shows the calculated η_i as a function of t/L (where t is the silicide thickness and L is the hot carrier attenuation length), at $h\nu$ (photon energy, where h is the Planck constant and ν is frequency) of about 0.8 eV, for $\Phi_B = 0.42$ eV 722, $\Phi_B = 0.45$ eV 724, $\Phi_B = 0.5$ eV 726, $\Phi_B = 0.55$ eV 728 and $\Phi_B = 0.59$ eV 730. As shown in FIG. 7B, η_i increases with Φ_B lowering (i.e. decrease in Φ_B) and/or silicide thickness thinning (i.e. decrease in the silicide thickness, t). Therefore, the barrier height may be tuned by an applied voltage, thus improving the internal efficiency. When t/L approaches 0 (i.e. $t/L \rightarrow 0$), the maximum η_i reaches or approaches to $\eta'_{i,\infty} \cong (h\nu - \Phi_B)/h\nu$.

[0149] The external quantum efficiency (η_e) may be a function of η_i, and may be given as $\eta_e = A \cdot \eta_i$, where A refers to the effective absorption (see for example Table 1), which is equivalent to the absorptance shown, for example, in FIGS. 8A, 9 and 10.

[0150] FIGS. 8A and 8B show respective plots 800, 820, of calculated absorption (or absorptance) (A) and external quantum efficiency (η_e) as a function of TaSi$_2$ thickness or width (W$_{TaSi2}$), according to various embodiments, for a photodetector having a structure of (Cu/SiN/TaSi$_2$/Si/TaSi$_2$/SiN/Cu). Other parameters may be set as: Si thickness or width, W$_{Si}$, of (50 nm – W$_{TaSi2}$), SiN isolator width, W$_{SiN}$, of about 10 nm, absorber region length, L$_{abs}$, of about 1 μm or about 2 μm, hot carrier attenuation length, L,

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assumed to be about 100 nm, Schottky height barrier, Φ_B, of about 0.45 eV or about 0.55 eV, and hv of about 0.8 eV.

[0151] The plot 800 shows the absorptance result 802 for L_{abs} = 1 μm and the absorptance result 804 for L_{abs} = 2 μm.

[0152] The plot 820 shows the η_e result 822 for L_{abs} = 1 μm and Φ_B = 0.45 eV, the η_e result 824 for L_{abs} = 2 μm and Φ_B = 0.45 eV, the η_e result 826 for L_{abs} = 1 μm and Φ_B = 0.55 eV and the η_e result 828 for L_{abs} = 2 μm and Φ_B = 0.55 eV.

[0153] As shown in FIGS. 8A and 8B, for L_{abs} = 1 μm, an increase in A and a decrease in η_i leads to a maximum η_e at W_{TaSi2} of about 2 - 3 nm (e.g. see results 822, 826). With an increase in L_{abs}, A increases and η_e is generally limited by η_i, thus η_e monotonically increases, as W_{TaSi2} decreases (e.g. see results 824, 828).

[0154] In embodiments of a TaSi$_2$-photodetector, with W_{TaSi2} = 2 nm, L_{abs} = 2 μm and W_{Si} = 50 nm, at 1 V bias (thus, $\Phi_n \approx$ 0.55 eV and $\Phi_p \approx$ 0.45 eV), the overall η_e ($= (\eta_e(electron) + \eta_e(hole))/2$) is approximately 0.056, as may be observed from FIG. 8B, which corresponds to a responsivity of approximately 0.07 A/W at about 1550 nm. In various embodiments, the responsivity may increase with an increase in the bias voltage, due to Φ_B lowering. However, the dark current may increase. In the photodetector of various embodiments, silicide layers may be provided on either side of a waveguide. Therefore, a pair of silicide layers may interface with respective opposite sides of the waveguide and may be regarded as two silicide diodes, with one silicide diode for electrons and the other silicide diode for holes. The overall η_e may be calculated as ($(\eta_e(electron) + \eta_e(hole))/2$). For the electron diode, the barrier height Φ_B may be assumed to be about 0.55 eV, and based on the η_e result 828 for W_{TaSi2} = 2 nm and L_{abs} = 2 μm, η_e(electron) is approximately 0.027. For the hole diode, the barrier height Φ_B may be assumed to be about 0.45 eV, and based on the η_e result 824 for W_{TaSi2} = 2 nm and L_{abs} = 2 μm, η_e(hole) is approximately 0.085. Accordingly, the overall η_e is approximately 0.056 [(=0.027+0.085)/2].

[0155] Where an ideal silicide is adopted, the absorptance, A, is approximately 0.69 for L_{abs} = 1 μm and $W_{silicide}$ = 2 nm. The overall η_e may be about 0.08 and the responsivity

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may be 0.1 A/W at a bias voltage of about 1 V, assuming the ideal silicide has at least substantially the same barrier height as $TaSi_2$.

[0156] FIG. 9 shows a plot 900 of calculated propagation loss (α) and absorption (or absorptance) (A) as a function of silicon (Si) core width (W_{Si}), according to various embodiments, for a photodetector having a structure of ($Cu/SiN/TaSi_2/Si/TaSi_2/SiN/Cu$). The effective width of the Si core is ($W_{Si} - W_{TaSi2}$). Other parameters may be set as: W_{TaSi2} of about 3 nm, W_{SiN} of about 10 nm, and L_{abs} of about 1 μm.

[0157] The plot 900 shows the propagation loss result 902 and the power absorption 904 of the photodetector in the absorber region (e.g. 310). The plot 900 also shows the propagation loss result 906 for a corresponding plasmonic waveguide without silicide (i.e. $Cu/SiN/Si/SiN/Cu$), for comparison.

[0158] As shown in FIG. 9, both propagation loss 902 and the power absorption 904 increase, e.g. increase monotonically, as W_{Si} decreases. This shows that L_{abs} may be reduced with a decrease in W_{Si} to maintain a particular absorption. As shown in FIG. 9, the propagation loss 906 of a conventional plasmonic slot waveguide (i.e. without silicide layers) also increases with a decrease in W_{Si}.

[0159] In various embodiments, the photodetector of various embodiments may be designed or fabricated with W_{Si} of about 50 nm, as a near or substantially rectangle profile may be obtained using industry-standard lithographic process for a Si core with a width, W_{Si}, of about 50 nm and a height of about 340 nm.

[0160] FIG. 10 shows a plot 1000 of calculated propagation loss (α) and absorption (or absorptance) (A) as a function of silicon nitride (Si_3N_4) isolator width (W_{SiN}), according to various embodiments, for a photodetector having a structure of ($Cu/SiN/TaSi_2/Si/TaSi_2/SiN/Cu$). Other parameters may be set as: W_{TaSi2} of about 3 nm, W_{Si} of about 50 nm, and L_{abs} of about 1 μm.

[0161] The plot 1000 shows the propagation loss result 1002 and the power absorption 1004 of the photodetector in the absorber region (e.g. 310). The plot 1000 also shows the propagation loss result 1006 for a corresponding plasmonic waveguide without silicide (i.e. $Cu/SiN/Si/SiN/Cu$), for comparison.

[0162] As shown in FIG. 10, reducing the Si_3N_4 width (W_{SiN}) may increase the propagation loss 1002 and the power absorption 1004. In addition, as shown in FIG. 10,

reducing W_{SiN} also increases the propagation loss 1006 of the conventional plasmonic slot waveguide (i.e. without silicide layers). This shows that L_{abs} may be reduced with a decrease or thinning down of W_{SiN} to maintain a particular power absorption, which may lead to a smaller dark current and a higher detector speed.

[0163] The estimated dark current and speed of the photodectector of various embodiments will now be described, based on calculation.

[0164] The photodetector of various embodiments may effectively be two Schottky diodes connected or coupled to each other back-to-back, for example one Schottky diode may be forward-biased while the other may be reversed-biased, when a biasing voltage is applied to the photodetector.

[0165] The total dark current, I_{dark}, is composed of both electron current and hole current, and may be expressed as

$$I_{dark} = (L_{abs} + L_{con}) \cdot height \cdot T^2 \left(A_n^{**} \cdot \exp\left(-\frac{e \cdot \Phi_n}{k \cdot T}\right) + A_p^{**} \cdot \exp\left(-\frac{e \cdot \Phi_p}{k \cdot T}\right) \right) \quad \text{(Equation 3)},$$

where L_{abs} is the absorber region length, L_{con} is the contact region length, height refers to the waveguide height (e.g. h1 as illustrated in FIG. 3B), T is the absolute temperature, k is the Boltzmann constant, A_n^{**} is the effective Richardson constant for electrons (e.g. 117 A·cm^{-2}·K^{-2} for electrons in Si), A_p^{**} is the effective Richardson constant for holes (e.g. 32 A·cm^{-2}·K^{-2} for holes in Si), e is the electron charge (approximately 1.602 × 10^{-19} C), Φ_n is the electron Schottky barrier height, and Φ_p is the hole Schottky barrier height.

[0166] For a 2 μm long and 2 nm thick TaSi$_2$-detector, integrated in a 50 nm wide Si core in a metal-semiconductor-metal (MSM) structure) (or equivalently a metal-dielectric-metal (MDM)) plasmonic waveguide, as described above with a responsivity of about 0.07 A/W, the dark current, I_{dark}, may be calculated to be approximately 66 nA at room temperature under a bias voltage of about 1 V. The minimum detectable power, S_{min} (sensitivity) in dBm, which is defined as 1 dB above the optical power (in dBm) that generates a photocurrent equal to the dark current, I_{dark}, may be calculated to be approximately -29 dBm. For the ideal silicide-detector as described above with a responsivity of about 0.07 A/W, the dark current, I_{dark}, may be approximately 39 nA (due to a short L_{abs}) and S_{min} may be approximately -33 dBm.

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[0167] The speed of a photodetector may be determined by the transit time of excited carriers across the Si core and the RC delay. Assuming a drift velocity of carriers of about 1×10^7 cm/s in Si, the transit time may be estimated to be about 0.5 ps for $W_{Si} = 50$ nm, corresponding to a Terahertz (THz) cutoff frequency. The speed of the photodetector of various embodiments may be limited by the RC delay, which may be defined as

$$f_{max} = \frac{1}{2\pi \times RC}$$ (Equation 4),

where f_{max} refers to the maximum frequency or cutoff frequency, R refers to resistance and C refers to capacitance.

[0168] Based on a simple parallel-plate model, the capacitance, C of the $TaSi_2$-detector as described above may be calculated to be approximately 1.75 fF. Assuming a resistivity, ρ of about 40 $\mu\Omega$·cm, a 2-μm-long 2-nm-thick $TaSi_2$ film may have a resistance, R of about 1.3 kΩ. Therefore, the cutoff frequency or speed, f_{max}, of the $TaSi_2$-detetctor as described above may be estimated to be approximately 68 GHz.

[0169] For the ideal silicide-detector, assuming the same resistivity of about 40 $\mu\Omega$·cm, both R and C are reduced due to a reduction in L_{abs}, and the cutoff frequency, f_{max}, may be estimated to be approximately 228 GHz.

[0170] As illustrated by the above analysis, both the dark current, I_{dark}, and the speed, f_{max}, may be improved by reducing the Si_3N_4 and/or Si core widths, while maintaining the responsivity of the photodetector of various embodiments.

[0171] Therefore, various embodiments of a silicide Schottky-barrier detector may be designed to detect surface plasmon polariton (SPP) signal propagating along the horizontal metal/isolator/Si/isolator/metal nanoplasmonic slot waveguide, which may be fabricated using the standard complementary metal–oxide–semiconductor (CMOS) technology. In various embodiments, silicide layers or ultrathin silicide layers may be inserted or arranged between any one or both of the isolators and Si to effectively absorb power.

[0172] In various embodiments, the Schottky barrier height may be broadly tuned through the Schottky effect, owing to the metal-Si-metal structure with a narrow or very narrow Si core waveguide.

[0173] In various embodiments, the silicide may be tantalum silicide ($TaSi_2$) which has the lowest permittivity among other silicides. In various embodiments, the isolator may be silicon nitride (Si_3N_4) which has a large permittivity, as compared to silicon oxide (SiO_2).

[0174] Using $TaSi_2$ as an example, a $TaSi_2$-photodetector, e.g. with optimized dimensions, may exhibit a responsivity of about 0.07 A/W, a dark current of about 66 nA at room temperature, and a speed of about 60 GHz, under a bias voltage of about 1 V. The minimum detectable power may be about -29 dBm. In contrast, for a conventional Si-waveguide based silicide Schottky barrier detector under a bias voltage of about 1 V, the conventional detector exhibits a responsivity of about 19 mA/W, a dark current of about 30 nA, and a speed of about 7 GHz.

[0175] In various embodiments, the performance of the photodetector may be further improved by reducing the width of the Si core and/or the width of the isolator. In addition, the overall performance of the photodetector may also be improved where a silicide with a smaller permittivity is adopted or employed, for example some ternary or quaternary silicides.

[0176] It should be appreciated that the photodetector of various embodiments may be integrated with other plasmonic devices to form an integrated circuit.

[0177] While the invention has been particularly shown and described with reference to specific embodiments, it should be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention as defined by the appended claims. The scope of the invention is thus indicated by the appended claims and all changes which come within the meaning and range of equivalency of the claims are therefore intended to be embraced.

CLAIMS

1. A photodetector comprising:

    a substrate;

    a waveguide formed on a surface of the substrate;

    a first metal layer formed on a first side of the waveguide, wherein a first interface is defined between the waveguide and the first metal layer; and

    a silicide layer formed on a second side of the waveguide, wherein a second interface is defined between the waveguide and the silicide layer, and wherein the second side is opposite to the first side; and

    wherein at least one of the first interface or the second interface is at least substantially perpendicular to the surface of the substrate.
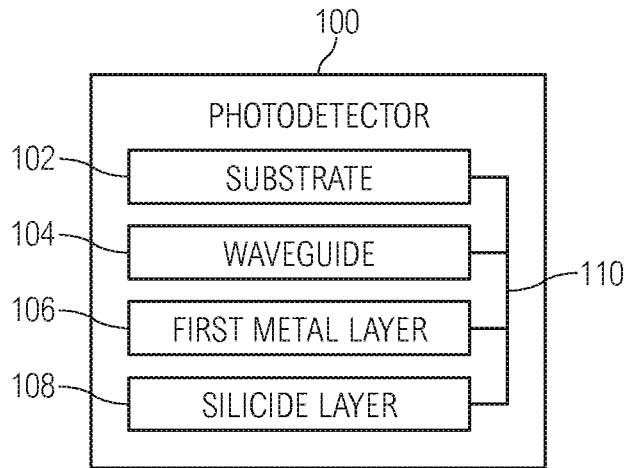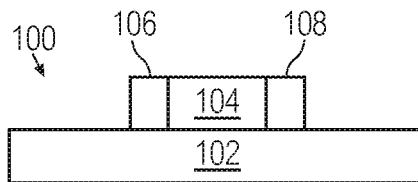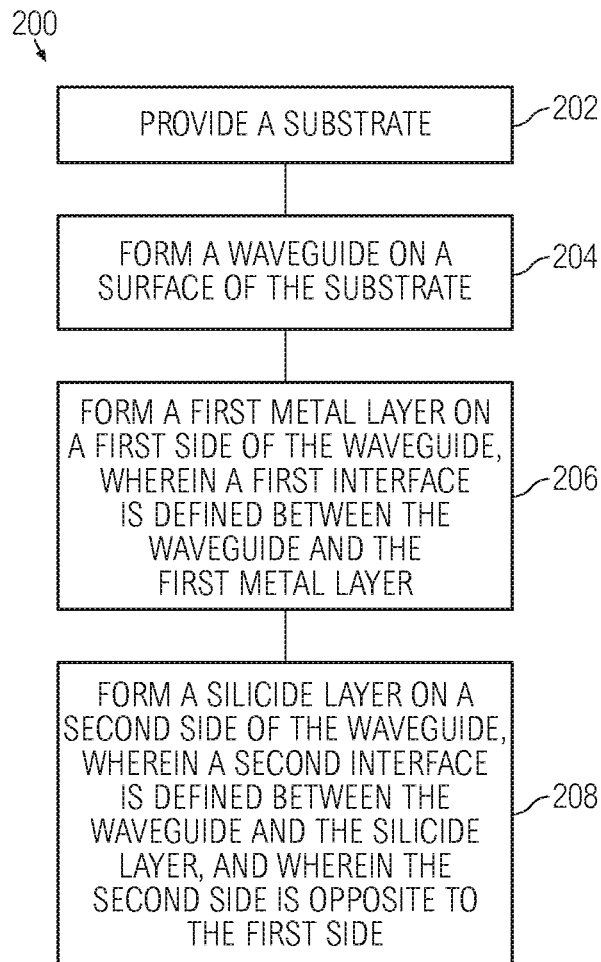
2. The photodetector as claimed in claim 1, wherein the first metal layer is another silicide layer.

3. The photodetector as claimed in claim 2, wherein the silicide layer and the other silicide layer comprise an at least substantially same material or different materials.

4. The photodetector as claimed in claim 2 or 3, wherein the silicide layer and the other silicide layer comprise a material having a complex refractive index, wherein the complex refractive index has a real index and an imaginary index, and wherein the real index is between about 1 and about 6 and the imaginary index is between about 0 and about 5.5.

5. The photodetector as claimed in any one of claims 2 to 4, wherein the silicide layer and the other silicide layer comprise a material selected from a group consisting of cobalt silicide, nickel silicide, titanium silicide, palladium silicide, hafnium silicide, niobium silicide, platinum silicide, vanadium silicide, tantalum silicide and any combinations thereof.

6.   The photodetector as claimed in any one of claims 1 to 5, wherein a first Schottky barrier is formed at the first interface, and wherein a second Schottky barrier is formed at the second interface.

7.   The photodetector as claimed in claim 6, wherein one of the first Schottky barrier or the second Schottky barrier is forward biased, and the other Schottky barrier is reverse biased when a voltage is applied between the first metal layer and the silicide layer.

8.   The photodetector as claimed in any one of claims 1 to 7, further comprising:
       a second metal layer formed adjacent to the first metal layer; and
       a third metal layer formed adjacent to the silicide layer.

9.   The photodetector as claimed in claim 8, wherein the second metal layer and the third metal layer are formed on the surface of the substrate.

10.   The photodetector as claimed in claim 8 or 9, further comprising:
       a first dielectric layer formed between the first metal layer and the second metal layer; and
       a second dielectric layer formed between the silicide layer and the third metal layer.

11.   The photodetector as claimed in claim 10, wherein the first dielectric layer is formed partially in a longitudinal direction of the waveguide, and wherein the second dielectric layer is formed partially in the longitudinal direction of the waveguide.

12.   The photodetector as claimed in claim 10 or 11, wherein the first metal layer has a first permittivity, the silicide layer has a second permittivity, the first dielectric layer has a third permittivity and the second dielectric layer has a fourth permittivity, and wherein the third permittivity and the fourth permittivity are lower than the first permittivity and the second permittivity.

13.   The photodetector as claimed in claim 12, wherein the first permittivity and the second permittivity are lower than a permittivity of a material of the waveguide.

14.   The photodetector as claimed in any one of claims 10 to 13, wherein the first dielectric layer and the second dielectric layer have a width of between about 1 nm and about 40 nm.

15.   The photodetector as claimed in any one of claims 1 to 14, wherein the first metal layer and the silicide layer have a width of between about 1 nm and about 10 nm.

16.   The photodetector as claimed in any one of claims 1 to 15, wherein the waveguide comprises a semiconductor.

17.   The photodetector as claimed in any one of claims 1 to 16, wherein the waveguide comprises silicon.

18.   The photodetector as claimed in claim 17, wherein the first side of the silicon waveguide and the second side of the silicon waveguide are silicon (110) crystal planes.

19.   The photodetector as claimed in any one of claims 1 to 18, wherein the waveguide has a width of between about 10 nm and about 100 nm.

20.   A method of forming a photodetector, the method comprising:
        providing a substrate;
        forming a waveguide on a surface of the substrate;
        forming a first metal layer on a first side of the waveguide, wherein a first interface is defined between the waveguide and the first metal layer; and
        forming a silicide layer on a second side of the waveguide, wherein a second interface is defined between the waveguide and the silicide layer, and wherein the second side is opposite to the first side; and

wherein at least one of the first interface and the second interface is at least substantially perpendicular to the surface of the substrate.

100

PHOTODETECTOR
102 — SUBSTRATE
104 — WAVEGUIDE
106 — FIRST METAL LAYER
108 — SILICIDE LAYER

110

FIG. 1A

100

106   108

104

102

FIG. 1B

200

PROVIDE A SUBSTRATE — 202

FORM A WAVEGUIDE ON A SURFACE OF THE SUBSTRATE — 204

FORM A FIRST METAL LAYER ON A FIRST SIDE OF THE WAVEGUIDE, WHEREIN A FIRST INTERFACE IS DEFINED BETWEEN THE WAVEGUIDE AND THE FIRST METAL LAYER — 206

FORM A SILICIDE LAYER ON A SECOND SIDE OF THE WAVEGUIDE, WHEREIN A SECOND INTERFACE IS DEFINED BETWEEN THE WAVEGUIDE AND THE SILICIDE LAYER, AND WHEREIN THE SECOND SIDE IS OPPOSITE TO THE FIRST SIDE — 208

FIG. 2
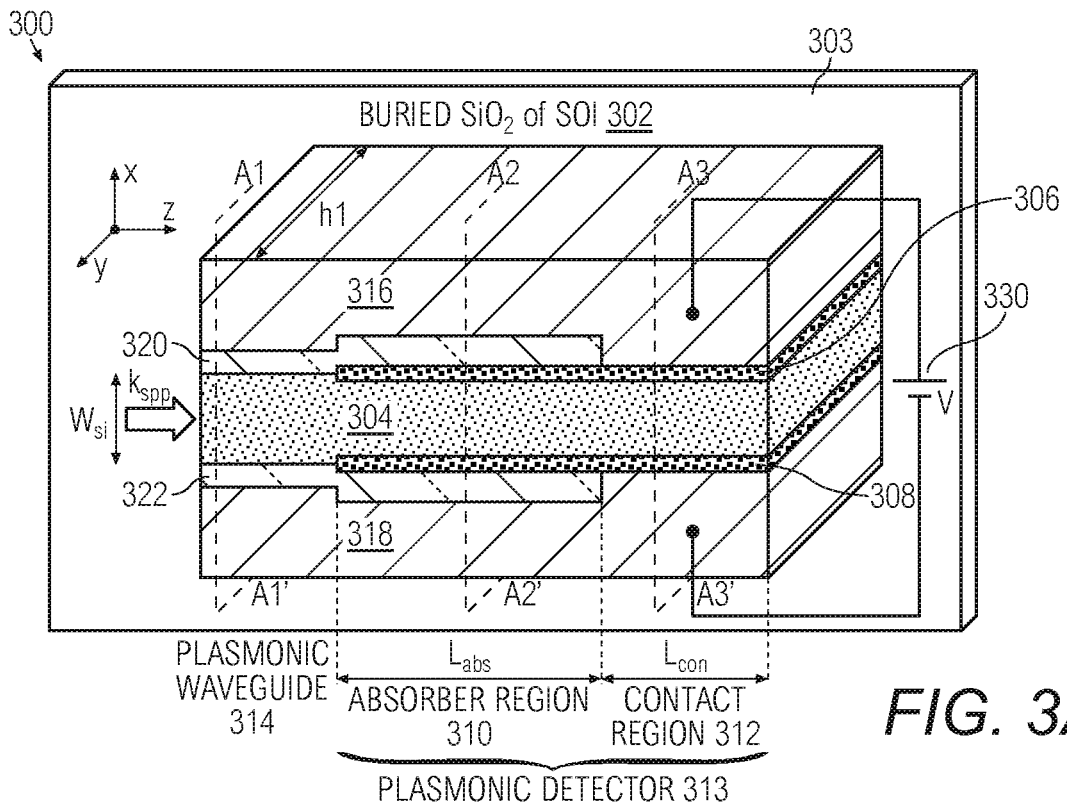
FIG. 3A
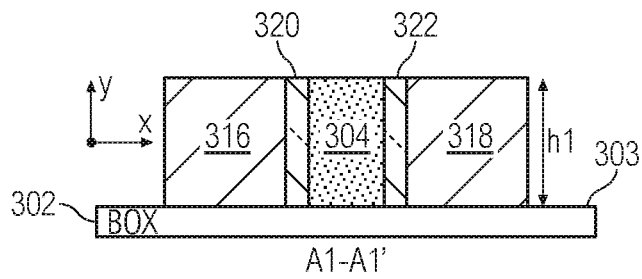
FIG. 3B
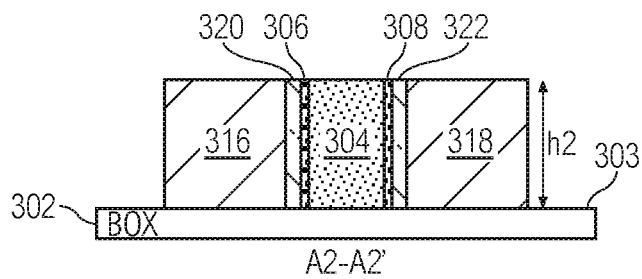
FIG. 3C
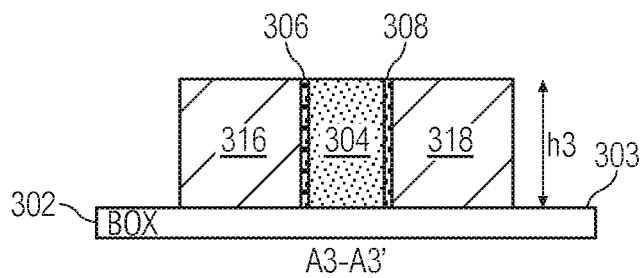
FIG. 3D
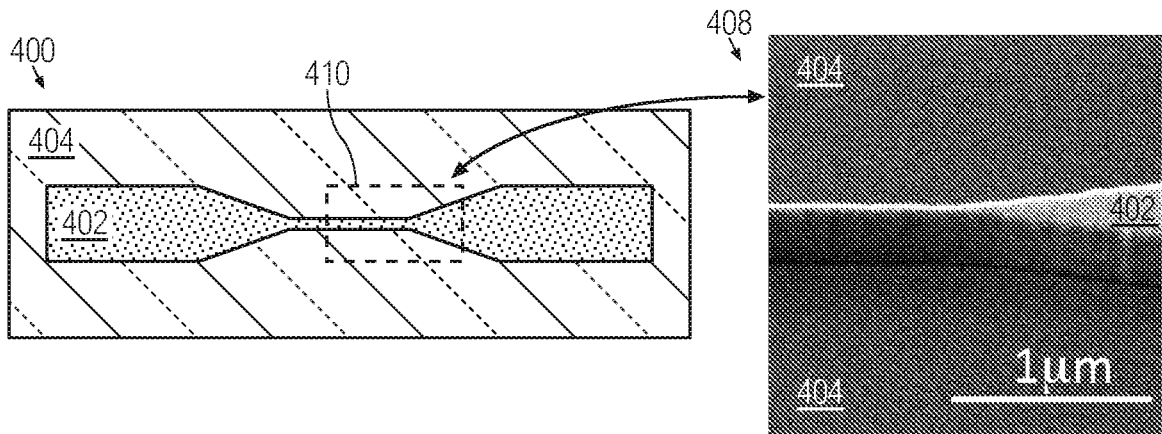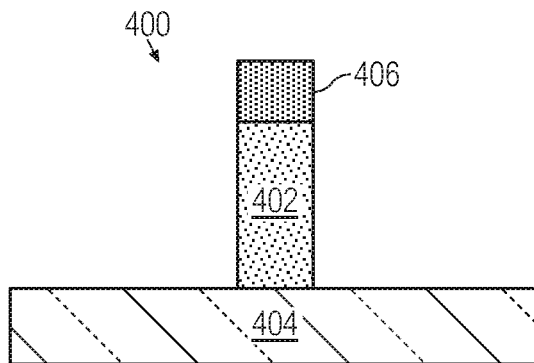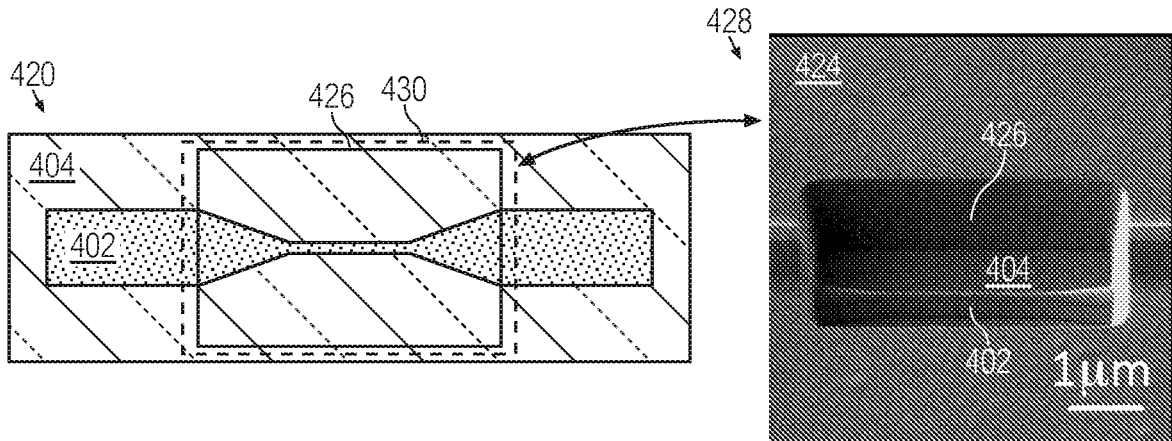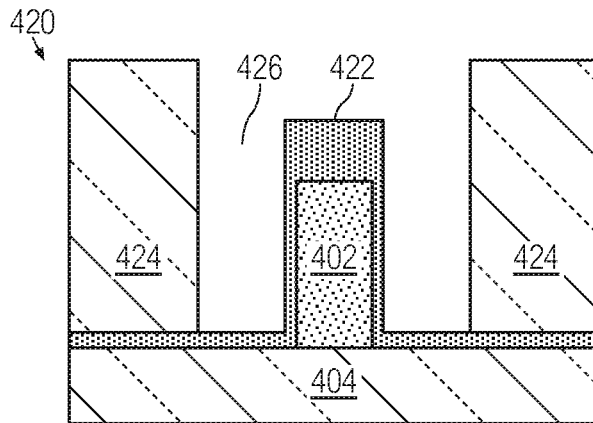
FIG. 4A

FIG. 4B

FIG. 4C

FIG. 4D
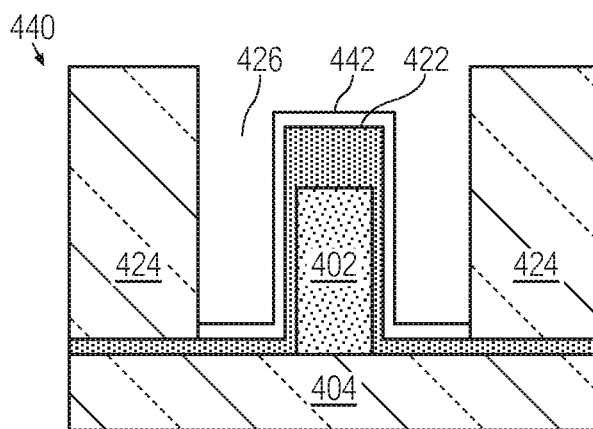
FIG. 4E
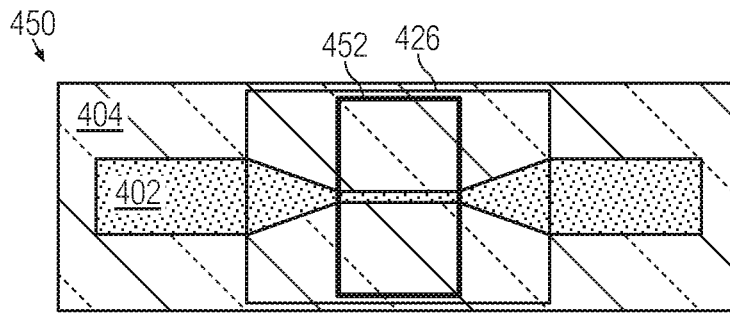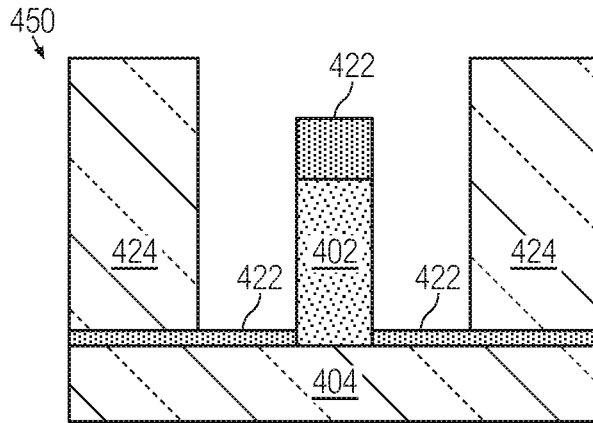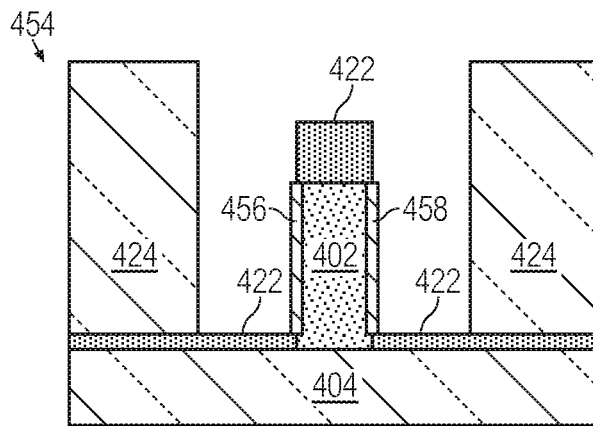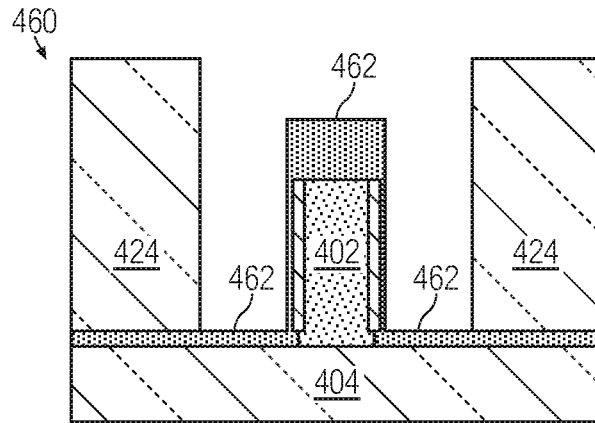
450

404

452   426

402

FIG. 4F

450

422

424   422   402   422   424

404

FIG. 4G

454

422

456   458

424   422   402   422   424

404

FIG. 4H

460

462

424   462   402   462   424

404

FIG. 4I

466

426   452   468

404

402

FIG. 4J

470

462

472   402   474

424   462   462   424

404

FIG. 4K

480

462 456 462 458 462

462 424 482 402 482 424 462

404

FIG. 4L

481

472 462 474

402

462 424 482 482 424 462

404

FIG. 4M

483

SiO₂ 487

SiN 485

Cu 484

SiO₂ 486

Si Core 496

0.2µm

FIG. 4N

488

50nm

Cu 484

SiO₂ 486

Si 492

SiO₂ 489

Cu 484

50 nm

FIG. 4O

490

Al 494

HfO₂ 493

Si 492

HfO₂ 493

Al 494

50 nm

FIG. 4P

FIG. 5

Z (μm)

FIG. 6A

PLASMONIC
WAVEGUIDE

FIG. 6B

Z (μm)

FIG. 6C

PLASMONIC
WAVEGUIDE
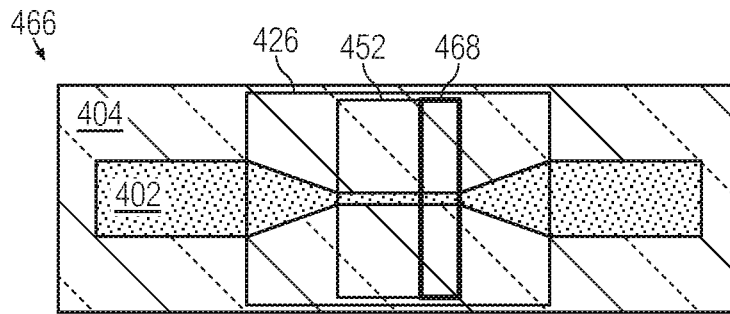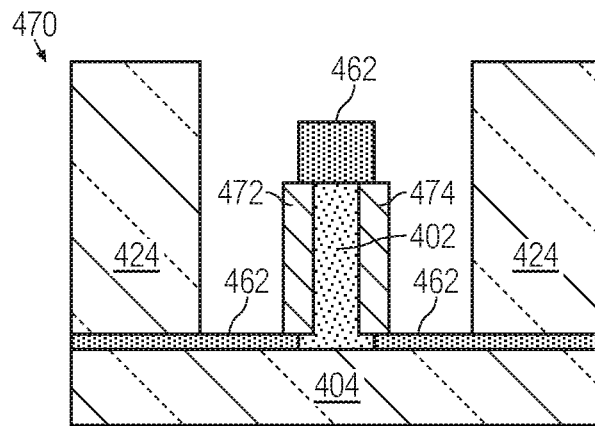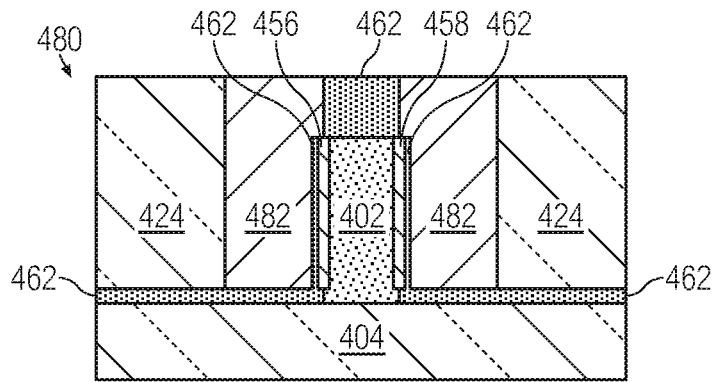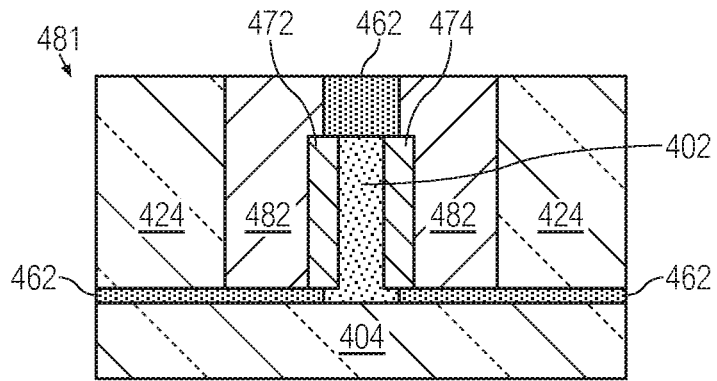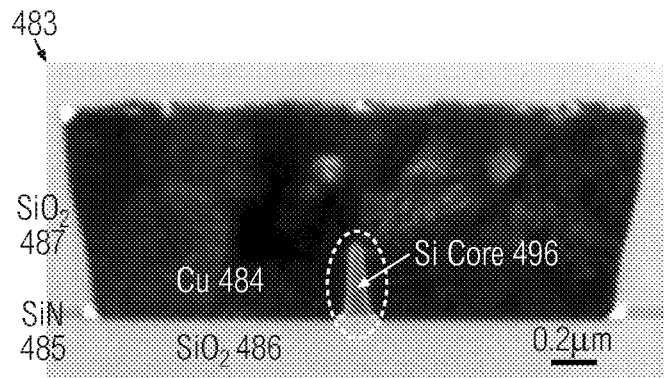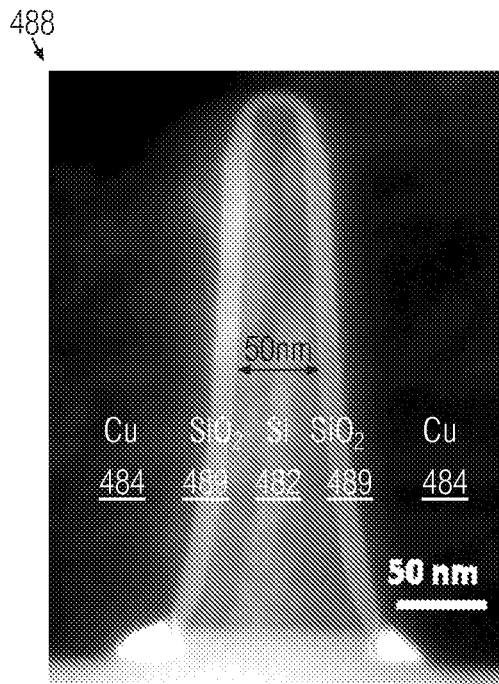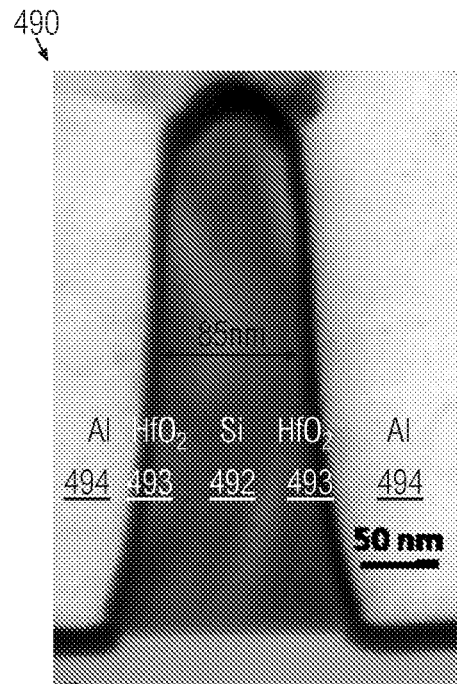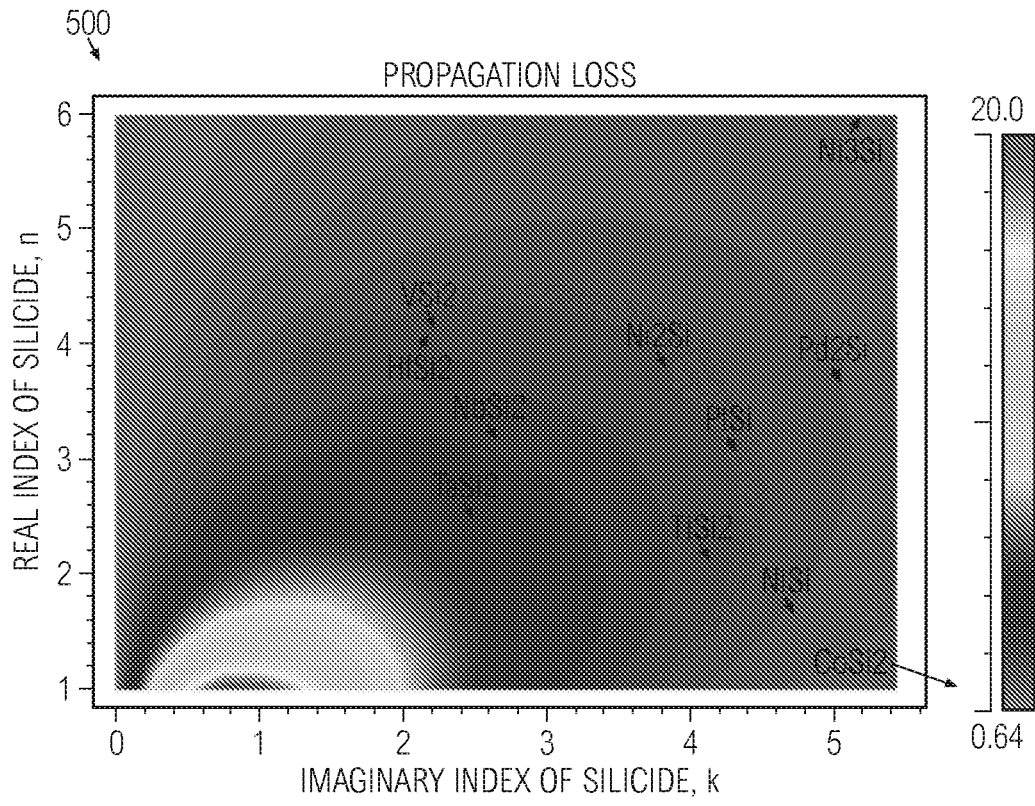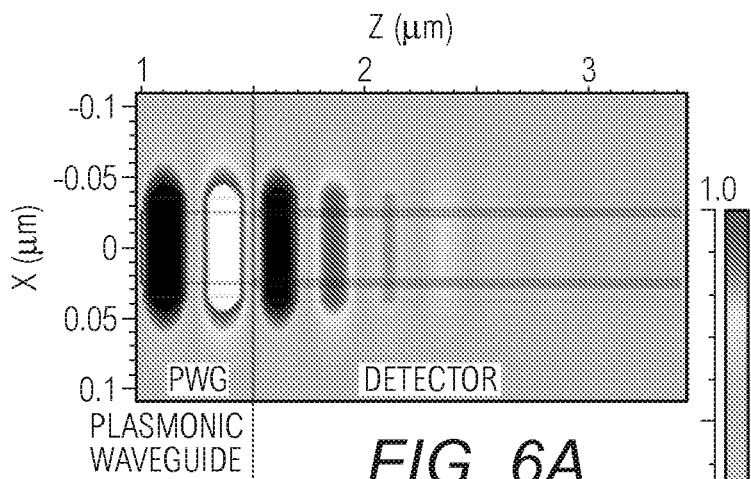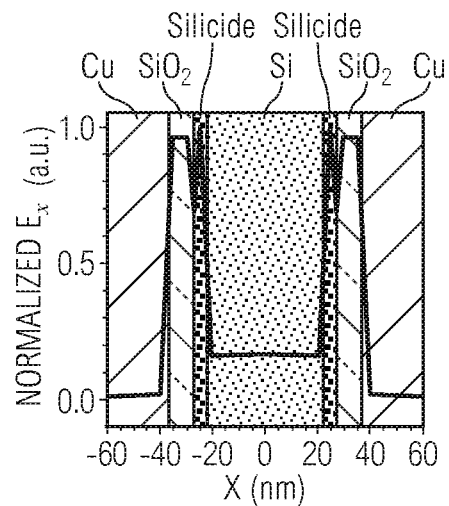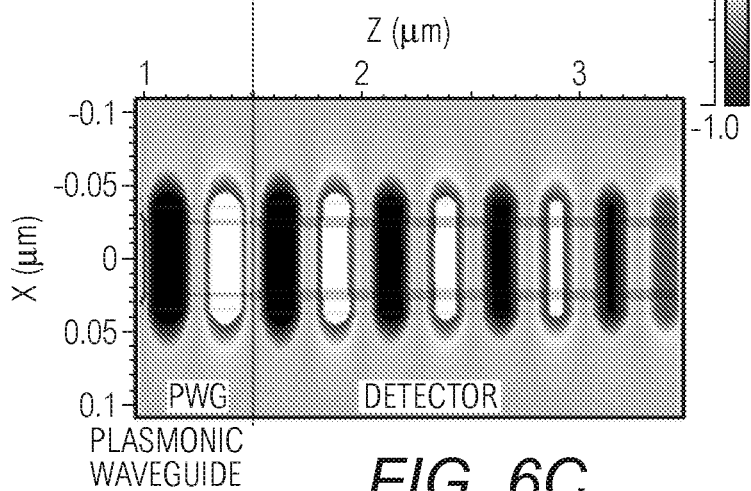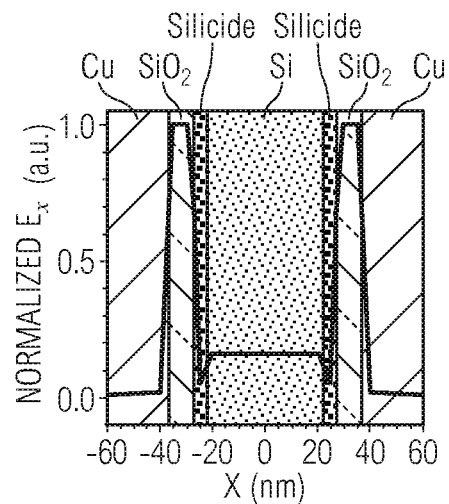
FIG. 6D
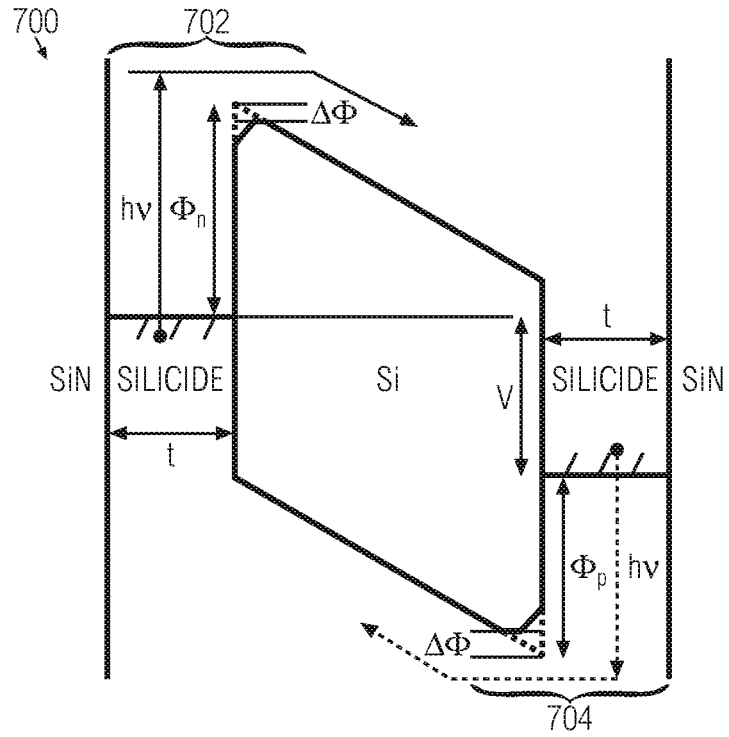
FIG. 7A
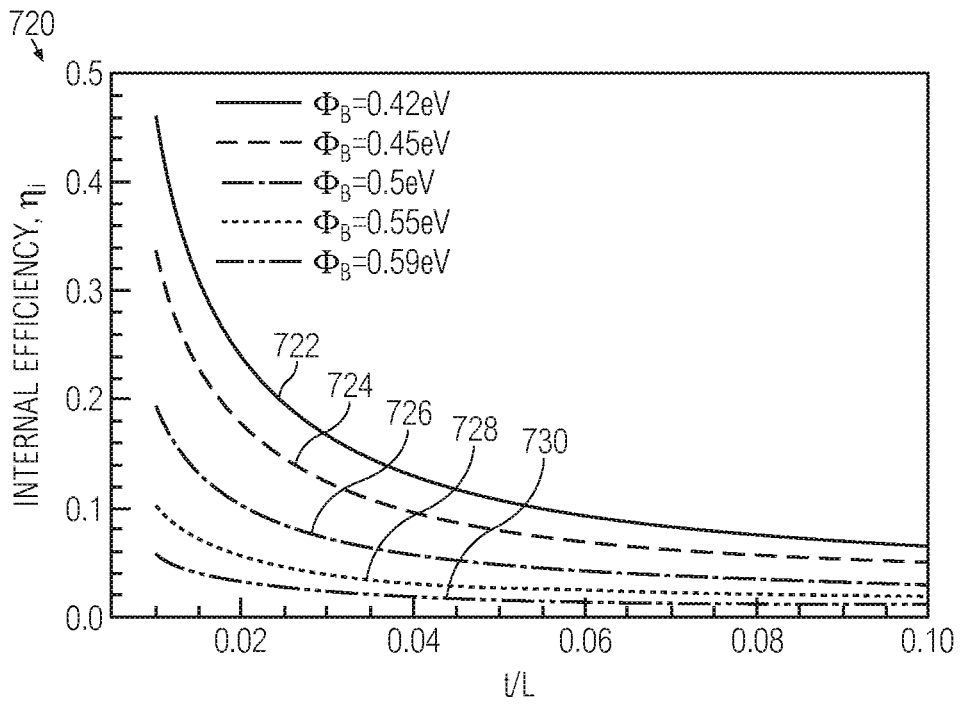
FIG. 7B

FIG. 8A

FIG. 8B

FIG. 9

FIG. 10