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GB 1597203 A GB 1291575 A US 4385838 A

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(54) **Optically aligned electron beam lithography**

(57) A wafer 16 on a stage 17 is aligned for a step and repeat electron beam lithography 11, 12, 14 process by first positioning the wafer 16 optionally 13, 15 and then aligning each exposure field with electron beam registration marks. This obviates large area global electron beam registration marks. The optical system may be included within, or be external to, the electron beam equipment.

FIG. 3

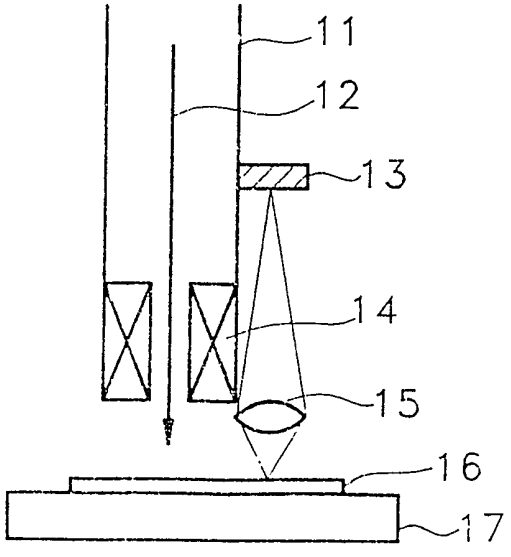

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FIG. 1
(PRIOR ART)

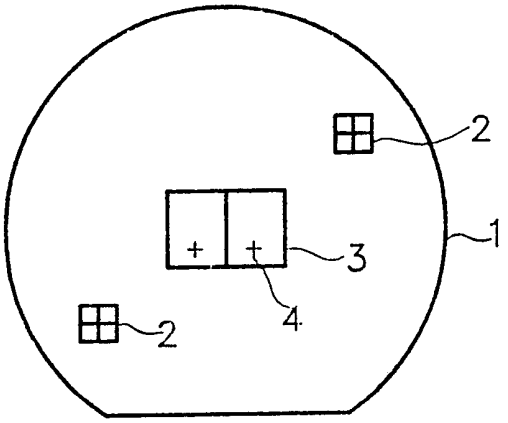


FIG. 2

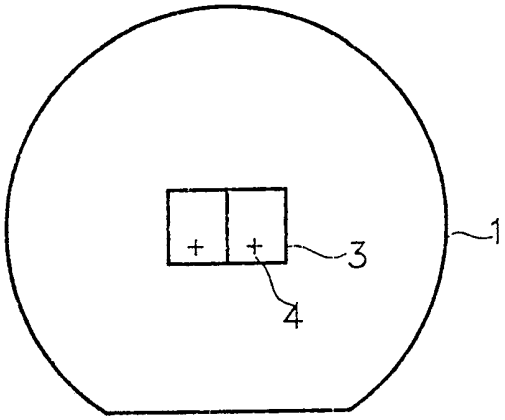
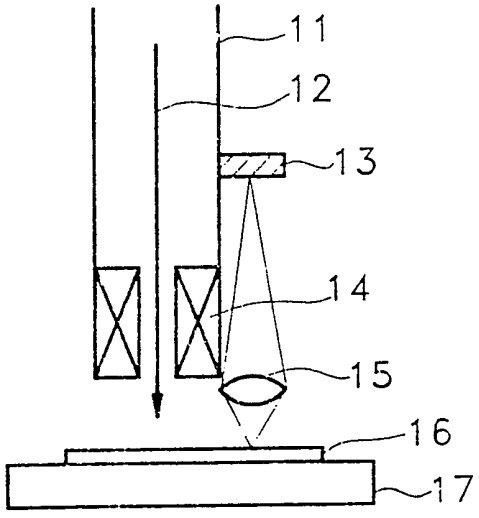


FIG. 3



ELECTRON BEAM LITHOGRAPHY AND A SYSTEM THEREFOR

The present invention relates to electron beam lithography and a system therefor, and more particularly, electron beam lithography for aligning a wafer globally using optical alignment marks and a electron beam lithography system comprising an optical alignment mark pattern detector.

In the fabrication of a semiconductor device, patterning a resist film is essential. A great many resist films are used as etching masks in various etching steps, for example, forming a window of an insulation layer on a semiconductor substrate in order to define a diffusion region selectively, and forming fine metal wiring of a semiconductor device.

The above patterns are formed by exposing a resist film to UV light or deep UV light through a photomask and subsequently developing it. This technology is referred to as photolithography.

However, when forming a pattern by using UV light or deep UV light as above, the resolution of optical lithography is limited to somewhat less than 1μm. Recently, with increasing the density of semiconductor device, alternatives to optical lithography,which may form submicron patterns,have been developed, including

electron beam lithography, x-ray lithography and ion beam lithography.

Electron beam lithography (hereinafter referred to as "EBL") is the process of forming circuit patterns by using a focused electron beam. Using an electron beam, fine patterns less than 1μm can be directly written on a resist film formed on a semiconductor wafer or a resist film formed on a photomask in a photolithography process.

A pattern formed in a lay-out stage is registered as an image pattern in a computer and electron beam is controlled by an electron deflecting plate according to a signal from the computer. Accordingly, EBL provides the ability to produce features less than 1μm directly on a wafer without the use of a mask. This technique can provide extremely accurate layer-to-layer registration and therefore, features as small as 0.1μm can be made with this technique. This is possible because, although electrons do possess wave-like properties, for the energies used in EBL systems, their wavelengths are on the order of 0.2-0.5Å. As a result, diffraction effects which can limit resolution in optical lithography are avoided. Therefore, the method for forming a pattern by EBL process draws a great deal of attention and great efforts for the practical utilization of the EBL process commercially are continuously being made.

In a general process for forming a semiconductor device, the lithography process for forming patterns is carried out in multi-steps. Each pattern formed during any particular step must be aligned and transferred very precisely with previously formed patterns. EBL is extremely slow when compared to conventional optical lithography. Therefore, in forming patterns generally, resist patterns are formed according to the faster conventional optical lithograph process and very fine patterns are formed by exposing resists using an electron beam, thereby reducing the manufacturing time of a semiconductor device. The electron beam system used in the above EBL process comprises an electron beam optical system and a mechanical stage.

When a pattern is formed according to EBL process on only one resist layer in a lithography process forming patterns in multi-steps as above, after optical lithography, a necessary resist layer is exposed by the EBL process. Then, another optical lithography process succeeds the EBL process.

In conventional EBL, it is known to form alignment marks on the wafer and to employ the marks for precisely registering the beam with respect to the wafer. In this way, the beam position is accurately initialized for a subsequent writing operation. During the registration step, the alignment marks are scanned by the beam in both

the X and Y directions. Electrons backscattered from the scanned marks are detected and utilized to generate electrical signals. These signals serve as the basis for precisely positioning the beam with respect to the wafer.

If the wafer is to be written by a machine capable of producing a very high speed integrated circuit, it would typically include a first alignment mark for aligning the wafer globally and a second alignment mark which allows alignment at each field or die unit of the area scanned by the electron beam. Alignment marks may be a pattern of either a high atomic number metal pedestal or a feature etched in the silicon or SiO_2. Alignment is achieved by detecting backscattered electrons from such marks.

At this time, the first alignment mark pattern in electron beam lithography has an area of about $1mm^2$, which is a hundred times or more as large as that of an alignment mark pattern in optical lithography, for preventing the resist of the active device region from being exposed when scanning the electron beam in order to detect the alignment mark pattern.

This makes it impossible to form the first alignment mark pattern on scribe corridor by which the chips are separated from each other. Therefore, the first alignment mark pattern is formed by an additional process. For example, there is described in U.S. Patent

No. 4,407,933 a method for exposing the resist with an electron beam which comprises forming tantalum disilicide alignment marks in spaced-apart regions of a wafer.

The above second alignment mark pattern is typically formed to have the shape of a cross in the separation regions for chips. FIG. 1 of the accompanying drawings illustrates a wafer which has the first and second alignment marks formed thereon and is to be exposed by using an electron beam, wherein reference numeral 1 represents a wafer, reference numeral 2 represents a first alignment mark pattern, reference numeral 3 represents a field, and reference numeral 4 represents a second alignment mark pattern.

When a resist coated on the wafer shown in FIG. 1 is exposed by an electron beam after conventional optical lithography, the first alignment mark pattern 2 is detected at first by scanning the wafer 1 with an electron beam. Then, the entire wafer 1 is rotationally and translationally aligned. Thereafter, for exposing the wafer with an electron beam by field or die units, the second alignment mark pattern 4 is detected to align the wafer again and expose the resist with electron beam by a field or die unit. After exposing a field or die unit of the resist, another second alignment mark pattern is detected in order to align the wafer again by the mechanical stage and to expose another field or die unit.

According to the above method, an electron beam is used in detecting the first alignment mark pattern for EBL. Therefore, an electron beam resist coated on the wafer may be exposed when scanning the wafer with the electron beam. Additionally, since the wafer is not positioned precisely, a spaced region without semiconductor devices should be formed along the wafer's edge, having a width of about 1mm.

Besides the above, the first alignment mark pattern should be formed by a separate process using an electron beam, and therefore, the throughput of the wafer is lowered.

Hence, an object of the present invention is to provide a method for electron beam exposure without forming a first alignment mark pattern or detecting it by means of an electron beam.

Another object of the present invention is to provide a system for electron beam exposure applicable to the above method.

Briefly, according to the present invention, there is provided a method for exposing an electron beam resist coated on a wafer which comprises firstly aligning the wafer by detecting an alignment mark pattern used in optical lithography, secondly aligning the wafer by detecting the alignment mark pattern for electron beam lithography formed on the wafer and then exposing the

resist with an electron beam forming patterns in multi-steps by means of optical lithography and electron beam lithography.

Additionally, according to the present invention, there is provided an electron beam lithography system comprising an electron beam system capable of scanning a wafer with an electron beam, a mechanical stage used to position the wafer under the electron beam, and an optical alignment mark pattern detector for aligning the wafer firstly and globally.

Further features and advantages of the present invention will be apparent to those skilled in the art from the following detailed description, given by way of example, of embodiments of the invention, with reference to the accompanying drawings, in which:

FIG. 1 illustrates a conventional wafer for electron beam lithography which has the first and second alignment marks formed thereon;

FIG. 2 illustrates a wafer for electron beam lithography according to an embodiment of the present invention;

FIG. 3 illustrates an EBL system provided with an optical alignment mark pattern detector according to an embodiment of the present invention.

In Fig. 2, the reference numerals have the same designations as in Fig. 1.

In conventional optical lithography, alignment mark patterns are previously formed on the wafer with a photoresist formed thereon to be exposed by an optical exposing means, and then detected to produce electrical signals. According to the signals, the relative position of the mask with respect to the wafer is determined.(S. Wolf and R.N. Tauber, Silicon Processing for the VLSI Era, Vol. 1, PP473-476, 1987)

Alignment in wafer steppers can be performed globally and locally. Global alignment performs rotational and translational alignment of the entire wafer. Local alignment provides alignment to a target that is a mark within the particular die which is in position for immediate exposure and is also referred to as die-by-die or field-by-field alignment. Global alignment is usually done at a remote alignment station before a wafer is sent under the projection lens for exposure. When the overlay tolerance is great (for example: 0.7μm or more), the wafer is exposed only after the global alignment without local alignment. When local alignment is used, global alignment always precedes the sequence of local alignments.

The method of the present invention is characterized in that the wafer is firstly aligned in an electron beam exposure step using the optical aligning method as above.

That is, firstly, the wafer is globally aligned by an optical aligning method using the means for detecting optical alignment mark patterns, and secondly, the wafer is locally aligned by scanning the wafer with an electron beam and detecting backscattered electrons from the alignment mark for EBL.

At first, the wafer 1 in FIG. 2 is globally aligned by detecting the optical alignment mark pattern (not shown) formed on the wafer. At this time, the overlay tolerance in the global alignment step is 5μm or less. After the above first alignment, local alignment is carried out by detecting the second alignment mark pattern 4 using an electron beam. In this local alignment, the overlay tolerance is 0.1μm or less.

FIG. 3 illustrates a system provided with an optical alignment mark pattern detector according to an embodiment of the present invention. Reference numeral 11 represents an electron beam system, reference numeral 12 represents an electron beam, reference numeral 13 represents a sensor for optical alignment mark patterns, reference numeral 14 represents an electron condenser lens, reference numeral 15 represents an optical lens, reference numeral 16 represents a wafer and reference numeral 17 represents a mechanical stage.

The above optical alignment mark pattern detector comprises a sensor 13 and an optical lens 15 . This

optical alignment mark pattern detector may be positioned to one side of or inside the electron beam system 11 .

When exposing the electron beam resist layer formed on a wafer as shown in FIG. 2, the sensor 13 detects through the optical lens 15 an optical alignment mark pattern formed on the semiconductor wafer 1 . Then, on the basis of the signals from the sensor 13 the semiconductor wafer 1 is aligned globally at first. Thereafter, the wafer 1 is scanned with an electron beam 12 and the backscattered electrons from the electron beam alignment mark pattern 4 is detected. On this basis, the wafer 1 is then aligned again (that is, locally aligned).

When a resist layer formed on a wafer is exposed with an electron beam, the alignment mark pattern need not be formed for global alignment of the entire wafer as in a conventional EBL process. Therefore, the unnecessary exposure of electron beam resist can be avoided, and throughput of the semiconductor wafer is enhanced.

Additionally, if an EBL process is performed by means of the EBL system provided with an optical alignment mark pattern detector , without additional steps (for example, the steps for forming a global alignment mark pattern for EBL and aligning globally the entire wafer using an electron beam), the EBL process

can be used in multi-steps for forming patterns, comprising optical lithography process. Therefore, the lithography process is simplified, and the EBL and optical lithography processes can be simultaneously employed without difficulty.

CLAIMS

1. A method for exposing an electron beam resist coated on a wafer for use in forming patterns in multi-steps by means of optical lithography and electron beam lithography, the method comprising the steps of;

firstly aligning the wafer by detecting an alignment mark pattern used in optical lithography;

secondly aligning the wafer by detecting the alignment mark pattern for electron beam lithography formed on the wafer;

and then exposing the resist with electron beam.

2. A method as claimed in claim 1, wherein the overlay tolerance in said step of firstly aligning the wafer is 5 μm or less.

3. A method as claimed in claim 1 or 2, wherein the overlay tolerance in said step of secondly aligning the wafer is 0.1 μm or less.

4. A method for exposing an electron beam resist coated on a wafer substantially as herein described with reference to Figures 2 and 3 of the accompanying drawings.

5. A method of forming patterns in multi-steps on a wafer by means of optical lithography and electron beam lithography comprising the method of any preceding claim.

6. An electron beam lithography system comprising:

an electron beam system capable of scanning a wafer with an electron beam;

means for positioning the wafer under the electron beam; and

detecting means for detecting optical alignment mark patterns for aligning the wafer globally.

7. A system as claimed in claim 6 wherein said means for positioning comprise a mechanical stage.

8. A system as claimed in claim 6 or 7, wherein said detecting means consists of an optical lens and a sensor for optical alignment mark patterns.

9. A system as claimed in claim 6, 7 or 8, wherein said detecting means is located to one side of said electron beam system.

10. A system as claimed in claims 6, 7 or 8 wherein said detecting means is located inside said electron beam system.

11. An electron beam lithography and a system therefor substantially as hereinbefore described with reference to Figure 3 with or without reference to Figure 2 of the accompanying drawings.

Examiner's report to the Comptroller under Section 17 (The Search Report)

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Relevant Technical fields

(i) UK Cl (Edition K) G1A(AMU), H1D(DAH1)

(ii) Int CL (Edition 5) G01B(11/00, 11/14,11/27)

Search Examiner

K SYLVAN

Databases (see over)

(i) UK Patent Office

(ii) ONLINE DATABASES: WPI

Date of Search

12 MAY 1992

Documents considered relevant following a search in respect of claims 1-11

Category (see over)	Identity of document and relevant passages		Relevant to claim(s)
X	GB 1597203 A	(SIEMENS) see page 1 lines 70-82, and page 6 lines 65-71	6
X	GB 1291575 A	(T.I) see page 1 line 56 to page 2 line 30, page 2 lines 100-106 and Figure 5	1,3, 6-9
X	US 4385838 A	(NIPPON KOGAKU) see column 5 line 15 to column 6 line 61 and column 13 line 28-35	6-8

Category	Identity of document and relevant passages	Relevant to claim(s)

Categories of documents

X: Document indicating lack of novelty or of inventive step.

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E: Patent document published on or after, but with priority date earlier than, the filing date of the present application.

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