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Hackett

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(54) **ENHANCED RAKE STRUCTURE**

(75) Inventor: **William C. Hackett**, Doylestown, PA (US)

(73) Assignee: **InterDigital Technology Corporation**, Wilmington, DE (US)

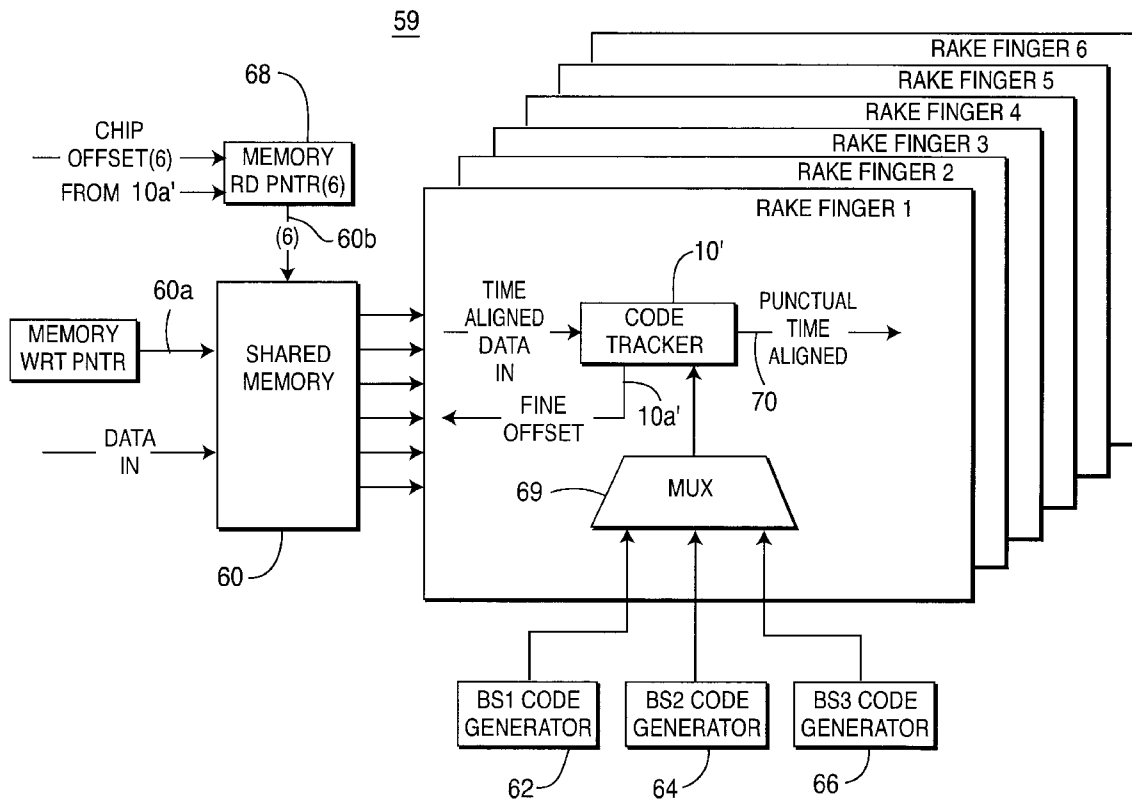(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 235 days.

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(52) **U.S. Cl.** **375/148**; 375/130; 375/133; 375/134; 375/136; 375/137
(58) **Field of Search** 375/148, 130, 375/133, 134, 136, 137, 147, 335, 342, 441

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Primary Examiner—Shuwang Liu
(74) Attorney, Agent, or Firm—Volpe and Koenig, P.C.

(57) **ABSTRACT**

A rake architecture for a frequency division duplex (FDD) and use also in TDD and TD-SCDMA type communications system, designed to significantly reduce the memory capacity required and thereby also reduce an area on the die of an application specific integrated circuit (ASIC) into which the memory is integrated. A single circular buffer, preferably of the shared memory type is shared by all of the rake fingers of a rake receiver to significantly reduce the hardware and software required to time align multipath signals received by a UE from a base station. This unique time alignment technique also reduces the number of code generators required to track a plurality (typically three) of base stations.

22 Claims, 4 Drawing Sheets

_59_

SLOT #0   SLOT #1   SLOT #14

PRIMARY
SYNC CODE ac_p ac_p ac_p

SECONDARY $ac_s^{1.0}$ $ac_s^{1.1}$ ● ● ● ● ● ● $ac_s^{1.14}$
SYNC CODES
            256 CHIPS

            2560 CHIPS

            ONE 10ms SCH RADIO FRAME
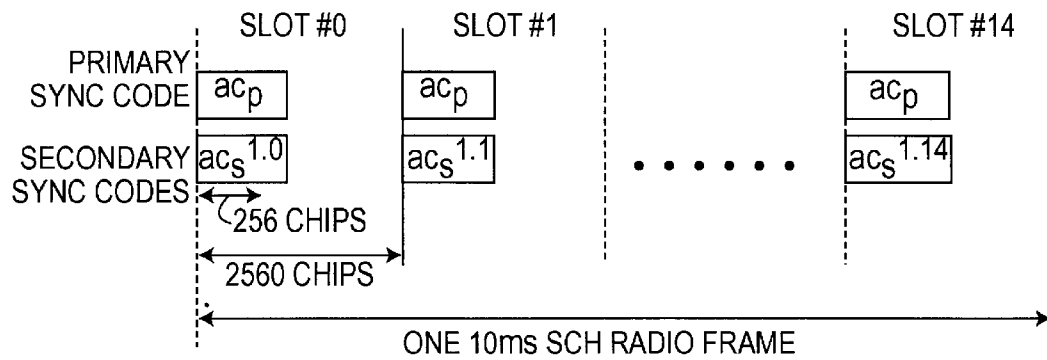
FIG. 1
PRIOR ART
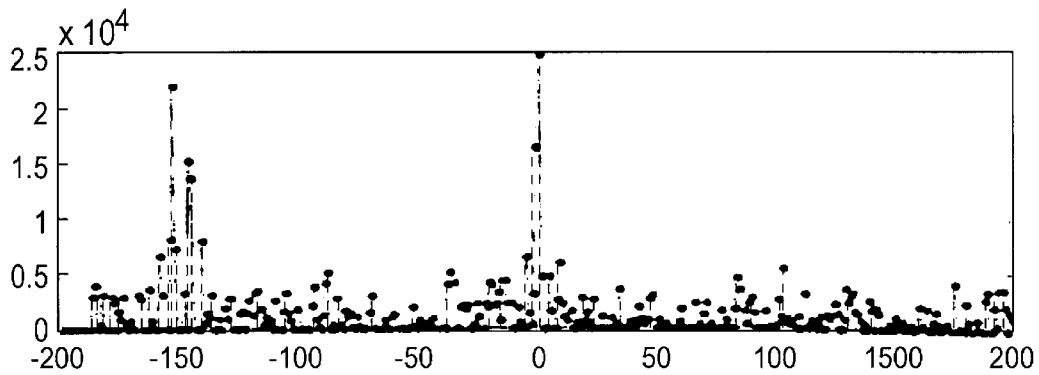
FIG. 2
PRIOR ART

FIG. 3
PRIOR ART

LOOP FILTER 40

NORMALIZATION 32

SQUARING DEVICE 26

SQUARING DEVICE 28

e(t)

+

30

-

INTEGRATE & DUMP 22

INTEGRATE & DUMP 24

SHIFT FROM RAKE LOCATOR AND CTL CONTROLLER

PILOT GENERATOR 12

HARDLIMITER 38

MOVING AVERAGE FILTER 36

INTEGRATE & DUMP 34

ACCUMULATOR 42

GAIN K 44

HARDLIMITER -Tc TO Tc 46

16

LATE

14a

EARLY

18

26

DELAY ESTIMATE PROCESSING 48

10

14b

PUNCTUAL OUTPUT

14c

INTERPOLATOR & DECIMATOR 14

x(t-T)

DELAY ESTIMATE
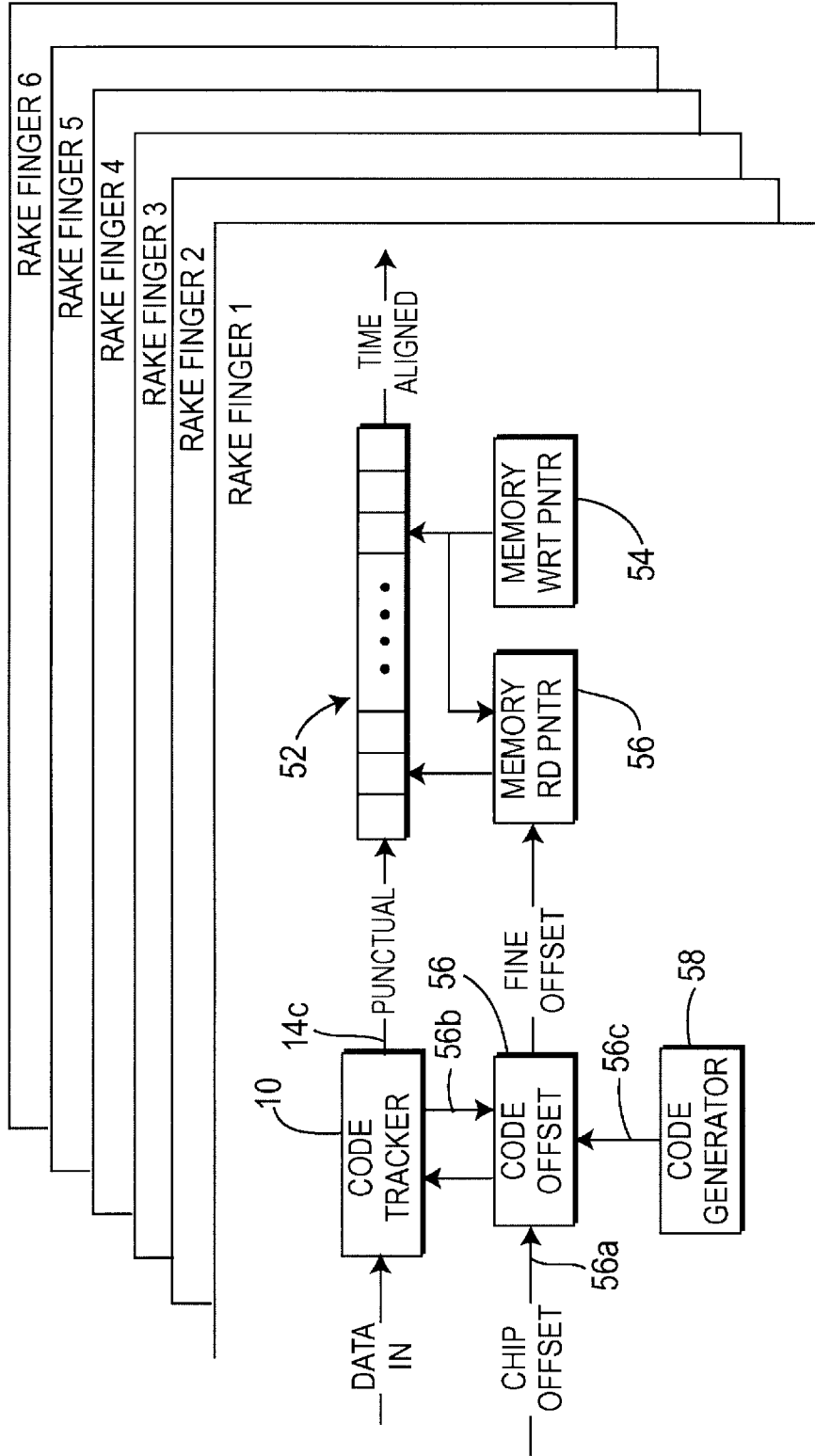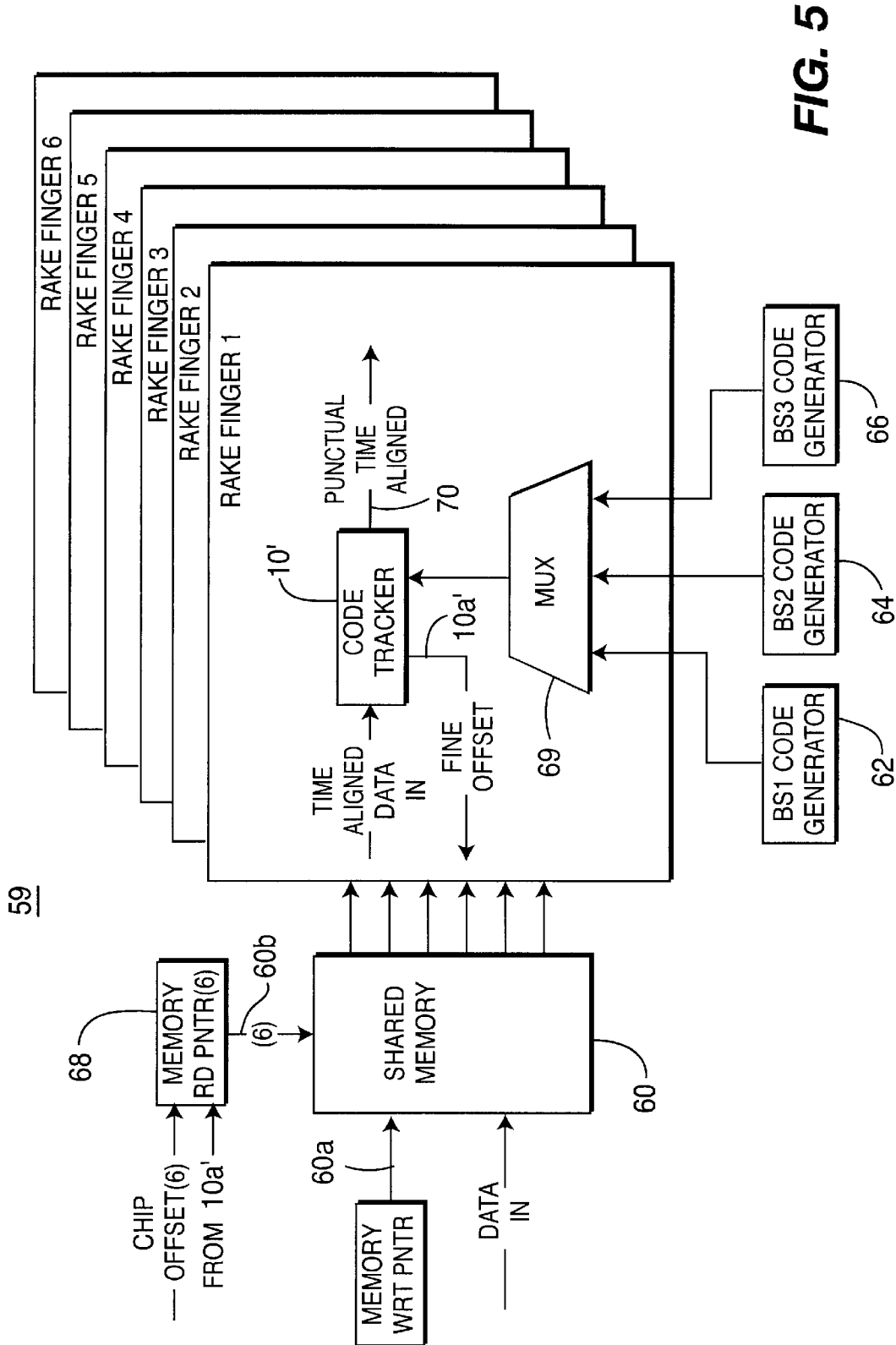
QUANTIZER 50

FIG. 4
PRIOR ART

FIG. 5

ENHANCED RAKE STRUCTURE

BACKGROUND

The present invention relates to a rake architecture employed in CDMA communication systems. More particularly the invention relates to a rake architecture employing a shared memory designed to significantly reduce the memory capacity required and thereby also reduce a die area of an application specific integrated circuit (ASIC) for the rake architecture without any reduction in system capabilities. The architecture may be employed in all types of communication systems employing a rake receiver including, but not limited to, frequency division duplex (FDD), time division duplex (TDD), and time division-synchronous code division multiple access (TD-SCDMA).

Rake receivers are utilized in many types of communications systems. In the wide band code division multiple access (W-CDMA) type of system, a base station transmits primary and secondary sync codes as well as a common pilot channel (CPICH), the pilot signal being unique to each base station. Wireless mobile units (UEs) then receive and synchronize to these codes in order to establish and support a communication.

In one example, a UE can track three or more base stations. A rake receiver is utilized to despread transmissions received from base stations through utilization of a cross correlator and a code generator, as is conventional. The UE receiver receives both direct (i.e., line of sight) RF waves as well as delayed (i.e. multipath) waves due to different transmission path lengths, reflections, etc. Since the direct wave is not necessarily the strongest signal or is not a strong enough signal for reception purposes, synthesizing (i.e. combining) the energy of the direct waves with the energy of delayed waves results in a better signal. Each finger of a rake receiver is provided with a cross-correlator and code-generator for performing despreading. Time offset is adjusted using a delay circuit whereupon all the signals are added together after imposing the appropriate delays to these signals.

The rake fingers work in conjunction with a cell search mechanism and the rake finger locator.

FIG. 1 shows the basic timing of a frame. One ten millisecond (10 m sec) synchronization channel (SCH) radio frame is divided into fifteen (15) slots labeled zero (0) through fourteen (14). Each base station transmits a primary sync code and a secondary sync code as well as a common pilot channel (CPICH). Unlike the primary and secondary sync codes that are present only during the first 256 chips of each slot, the CPICH is present during the entire frame and repeats every frame, in addition to being unique for each base station. The rake finger locator uses this uniqueness to perform a correlation against the CPICH from each of the possible base stations in the area of the UE. After the correlation is performed, the rake finger locator determines which peak to assign to which finger of the rake receiver. As was mentioned hereinabove, each UE is typically required to track up to three (3) or more base stations, which capability is due to handover requirements.

Referring to FIG. 3, a simplified block diagram of a conventional code tracker 10 is shown. Each rake finger is provided with a code tracker 10. A code generator 12 is provided with a code for a specific base station. The code timing must be offset to compensate for the current time offset from the start of the frame for the assigned peak. An interpolator and decimator filter 14 produces early, late and

punctual outputs at 14a, 14b and 14c respectively. The early and late outputs are utilized to keep the punctual output centered in the chip time.

The early, late and punctual outputs are despread with the code for the specific base station at 16, 18 and 20 respectively. The early and late despread signals undergo integration and dumping at integration and dumping devices 22 and 24, squaring at squaring devices 26 and 28 and are summed at 30 to produce an error signal e(t).

The punctual output also undergoes integration and dumping at integration and dumping device 34, the output of which passes through moving average filter 36 and hard limiter 38 for application to normalization circuit 32, together with the error sum e(t) outputted from summing circuit 30. The normalized output is then passed through a feedback path to the interpolator and decimator 14 through loop filter 40, accumulator 42, amplifier 44, hard limiter 46, delay estimate processor 48 and quantitizer 50, to provide a delay estimate to the interpolator and decimator 14, for purposes of keeping the punctual output centered in the chip time. If the error becomes too large for the code tracker to track, the code generator 12 will be adjusted. The interpolator and decimator filter 14 basically breaks the chip time into, for example, eight (8) segments. Based on the error signal, one of the eight (8) segments is selected. As time progresses and, if the error continues to increase, a different output is selected from the filter 14. Eventually, if the error is great enough that chip time runs out, at this point the pilot generator 12 is adjusted. The pilot generator 12 is usually a linear feedback shift register (LFSR), that is clocked (i.e., advanced) at the chip rate. If the pilot generator needs to be advanced at the next chip time, it will actually advance twice for that chip time. Conversely, if the pilot generator needs to be delayed, the pilot generator will hold its current value for a second chip time.

FIG. 2 shows a typical multipath. Each of the higher value points represents a multipath.

Each of the punctual outputs is fed into separate time delay elements (not shown) of the rake receiver. The purposes of time delay elements is to remove the time ambiguity, shown in FIG. 2, from the various multipaths. All of the energy remaining after code tracking is then summed in a data estimator (not shown) and is despread and descrambled into symbols.

Referring to FIG. 4, a conventional rake structure comprising of six (6) rake fingers is shown. Since all of the rake fingers are substantially identical in design and function, only one is shown in detail in FIG. 4, for purposes of simplicity. As was set forth hereinabove, the code tracker 10 shown in FIG. 3, and also shown in simplified block diagram form in FIG. 4, produces a punctual output 14c (see FIG. 3) which is fed into a delay element 52 which is preferably a circular buffer having a read port and a write port. A memory write pointer 54 increments the memory contents at a chip rate to locations where a punctual input is written and continually points to the next chip location within buffer 52. A read pointer 56 also increments at the chip rate, but is offset from the write pointer 54 based at the number of chips offset from the referenced slot timing. The fine offset is obtained from the code offset circuitry 56 which receives the chip offset at 56a, an output from the code tracker at 56b and the output from code generator 58 at 56c, providing a fine offset for further adjustments of the memory read pointer 56. The buffer 52 provides a time aligned output. It should be understood that the remaining rake fingers "2" through "6" operate in a similar fashion.

SUMMARY

The main advantage of the present invention resides in providing an apparatus and method to share the (possibly) many small memories needed to align the tracked multipaths and to move the shared memories ahead of the code tracker. Although the alignment of the multipaths and tracking of their movement is still performed by the code tracker, the code tracker now receives its data from a shared buffer of input symbols versus the more conventional method of sending the input stream to all code trackers and requiring that each code tracker buffers the results and then provides the required delay to obtain alignment.

The invention utilizes a circular buffer, preferably in the form of a shared memory, and has a memory read pointer for each rake finger to provide an offset from the location at which the memory write pointer writes the data, with the offset being associated with each rake finger receiving a multipath component. Each multipath component is sent to its assigned rake finger to undergo code tracking. Since the multipaths are all aligned, the codes are also time aligned, enabling a single code generator to be shared among the code trackers of all of the rake fingers. This novel apparatus and method enable a three-to-one savings in memory as well as reducing the number of code generators required for the rake receiver.

BRIEF DESCRIPTION OF THE DRAWING(S)

The method and apparatus of the present invention would be better understood upon a consideration of the drawings, in which:

FIG. 1 shows a typical 10 millisecond SCH radio frame.

FIG. 2 is a plot showing a typical multipath.

FIG. 3 is a simplified block diagram of a conventional code tracker employed in each rake finger of a rake receiver.

FIG. 4 is a simplified block diagram showing a conventional code tracker employed in each rake finger of a rake receiver.

FIG. 5 is a simplified block diagram showing apparatus for time aligning multipath signal for the rake fingers of a rake receiver and embodying the principles of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT(S)

The present invention will be described with reference to the drawing figures where like numbers represent like elements throughout.

FIG. 5 shows a rake receiver 59 embodying the principles of the present invention and which comprises six (6) rake fingers, only of one of which (i.e. "rake finger 1") is shown in detail for purposes of simplicity. It should be understood that the remaining rake fingers "2" through "6" are similar in design and function. It should be noted that the number of rake fingers is not a requirement of the invention, but is only used herein as a means to explain how the various components operate.

The rake receiver 59 utilizes a circular buffer 60, preferably of the shared memory type, operating at twice the chip rate and having a write pointer 60a and six read pointers 60b, (shown as a single lead for purposes of simplicity). The rake receiver 59 performs time alignment by initially moving the multipath pilot signals from the same base station into alignment prior to undergoing code tracking.

Making reference to FIG. 2, and assuming that the peaks from the higher Hierarchical Golay Correlation (HGC) are

all from the same base station and are all capable of being shifted in time to line up on top of each other, once the offset is accomplished each multipath component is sent to its assigned rake finger and code tracking is performed. Assuming receipt of two (2) signals that are five (5) chips apart, let it be assumed that each dot of the multipath plot is a chip time. Assuming that the read and write pointers in FIG. 5 operate at the chip rate, by advancing the read pointer 68 by a count of five (5), the two (2) signals can be read out of the memory at the same time. The code offsets provided to the read pointer 68 are each associated with one of the rake fingers (1 through 6). The locations of the peaks shown in FIG. 2 are known. The spacing and the number of multipaths are employed to determine the offset amount for the read pointers.

Since the multipath components have been lined up, the codes are also time aligned and the desired code generator (i.e. one of 62, 64 and 66) can be shared among the code trackers 10' of each of the six (6) rake fingers 1 through 6. Three code generators 62, 64 and 66 are provided for respectively generating pseudo-random noise (PN) codes for the three base stations BS1, BS2 and BS3, to be tracked by the UE having the rake receiver shown in FIG. 5. A multiplexer 69 selectively couples the desired code generator to the code trackers 10' by multiplexer 69.

When the code trackers 10' of the rake fingers request the code generator, 62 for example, to change to one of 64 or 66, the memory read pointer 68 for the rake fingers associated with that code generator are adjusted. The read point corresponding to that code tracker 10' is incremented, or decremented by 1. The unique memory sharing arrangement of the present invention enables the use of a single memory 60 shared by all six (6) rake fingers, resulting in three-to-one savings in memory based on the fact that, although there is only one shared memory for all six rake fingers, the shared memory (60) operates at twice the chip rate, since the code tracker 10' requires two samples per chip.

The code tracker 10' thus provides a punctual time aligned output 70 according to the base station code being decoded. The code tracker 10' which also includes the code offset circuit 56 shown in FIG. 4 provides the fine offset output 10a' to the memory read pointer 68 in a manner similar to that described hereinabove which regard to FIG. 4.

What is claimed is:

1. Apparatus for use in a rake receiver for time aligning multipath signals from a base station, comprising:

a plurality of rake fingers, each rake finger having a code tracker;

a plurality of code generators each generating codes associated with a given base station, said codes being different from one another;

said time aligning apparatus, comprising a shared memory for selectively providing time aligned multipath signals to code trackers of each rake finger;

a memory write pointer for writing multipath signals into the shared memory at a given location;

a memory read pointer for reading out multipath signals from a memory location of the shared memory offset from said given location;

one of said code generators providing a base station code to the code trackers of said rake fingers; and

each of said code trackers receiving one of the outputs read out by said read pointer.

2. The apparatus of claim 1 wherein each of said code trackers provide a fine offset to said memory read pointer for

adjusting an offset between said memory write pointer and memory read pointer for providing a time aligned output.

3. The apparatus of claim 1 further comprising a multiplexer for selectively coupling one of said base station code generators to the code trackers of each rake finger.

4. The apparatus of claim 1 wherein said shared memory is a circular buffer.

5. The apparatus of claim 3 wherein an offset between said memory read pointer and said memory write pointer is determined by chip offsets and said fine offsets.

6. The apparatus of claim 5 wherein each chip offset is associated with one of said rake fingers.

7. The apparatus of claim 1 further comprising means for changing the memory read pointer responsive to the code generator coupled to the code tracker of each rake finger.

8. The apparatus of claim 1 wherein three code generators are provided.

9. The apparatus of claim 8 wherein said code generators are selectively coupled to a code tracker by a multiplexer.

10. The apparatus of claim 1 wherein chip codes transmitted to said rake receiver from a base station operate at a predetermined chip rate, said read and write pointers operating at twice the chip rate.

11. The apparatus of claim 1 further comprising means for incrementing the write pointer to successive memory locations.

12. The apparatus of claim 11 wherein said incrementing means increments the write pointer to a start location in the memory means when the write pointer has been incremented to a end location in the memory means.

13. A method for time aligning multipath signals preparatory to applying the multipath signals to a plurality of code trackers provided in fingers of rake receiver comprising:

providing a shared memory for operation as a circular buffer;

receiving multipath signals from a base station;

writing multipath signals into the shared memory starting at a given memory location and incrementing locations at which the multipath signals are written into said shared memory;

reading multipath signals written into said shared memory at a location offset from locations at which signals were written into the memory responsive to chip offset data representing a number of chips offset from a referenced timing slot; and

selectively coupling the signals read out from the memory to a code tracker of each rake finger according to a chip offset associated with each rake finger.

14. The method of claim 13 further comprising;

providing a plurality of code generators each generating a different code;

selectively coupling one of the code generators to the code trackers of each rake finger for performing a correlation against a signal received from the base station to provide a punctual time aligned signal at each rake finger through the use of a single shared memory and a code generator which are shared by all of said rake fingers.

15. The method of claim 13 wherein said read and write operations of said memory are operated at twice a chip rate of a sync code received from a base station and being processed by the rake receiver.

16. The method of claim 13 further comprising;

coupling each signal fed from the shared memory to a code tracker of a given rake finger according to a chip offset associated with each rake finger.

17. The method of claim 16 further comprising coupling a single code generator to the code trackers selected from a group of code generators, the code generator selected generating a code which is the same as the code utilized by the base station transmitting to the rake receiver.

18. A method for providing time alignment of multipath signals received by a rake receiver from a given base station, said rake receiver having a plurality of rake fingers, comprising:

receiving encoded multipath signals from said base station;

writing said signals into a given location in a shared memory;

reading said signals from a location in the shared memory offset from the write-in location responsive to a given chip offset so that the signals are time aligned when read out of the shared memory; wherein said base station transmits signals to said rake receiver at a given chip rate, said shared memory operating at twice said chip rate when reading into and writing out of said shared memory.

19. The method of claim 16 wherein the chip offsets are each associated with a given rake finger.

20. The method of claim 16 wherein each code tracker converts data received from the base station by correlation against the code from the code generator.

21. The method of claim 16 wherein said chip offsets for adjusting the read out locations of the shared memory relative to the write-in location is determined according to rake finger associated with each chip offset.

22. The method of claim 16, wherein each tracker generates a fine offset responsive to correlation of a signal processed by the code tracker to provide a further adjustment of the offset between the memory read location and the memory write location.

* * * * *